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L6713A

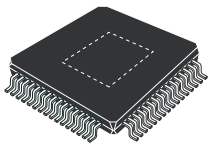
2/3 phase controller with embedded drivers for Intel VR10, VR11 and AMD 6 bit CPUs

Features

- Load transient boost LTB Technology™ to minimize the number of output capacitors (patent pending)
- Dual-edge asynchronous PWM
- Selectable 2 or 3 phase operation
- 0.5 % output voltage accuracy
- 7/8 bit programmable output up to 1.60000 V - Intel VR10.x, VR11 DAC
- 6 bit programmable output up to 1.5500 V - AMD 6 bit DAC
- High current integrated gate drivers
- Full differential current sensing across inductor
- Embedded VRD thermal monitor
- Differential remote voltage sensing
- Dynamic VID management
- Adjustable voltage offset
- Low-side-less startup
- Programmable soft-start
- Programmable over voltage protection
- Preliminary over voltage protection
- Programmable over current protection
- Adjustable switching frequency
- Output enable
- SS_END / PGOOD signal
- TQFP64 10x10 mm package with exposed pad

Applications

- High current VRD for desktop CPUs
- Workstation and server CPU power supply
- VRM modules



TQFP64 (Exposed pad)

Description

L6713A implements a two/three phase step-down controller with 180º/120º phase-shift between each phase with integrated high current drivers in a compact 10x10 mm body package with exposed pad.The 2 or 3 phase operation can be easily selected through PHASE_SEL pin.

Load transient boost LTB Technology™ (patent pending) reduces system cost by providing the fastest response to load transition therefore requiring less bulk and ceramic output capacitors to satisfy load transient requirements.

LTB Technology™ can be disabled and in this condition the device works as a dual-edge asynchronous PWM.

The device embeds selectable DACs: the output voltage ranges up to 1.60000 V (both Intel VR10.x and VR11 DAC) or up to 1.5500 V (AMD 6BIT DAC) managing D-VID with ± 0.5% output voltage accuracy over line and temperature variations.

The controller assures fast protection against load over current and under / over voltage (in this last case also before UVLO). In case of over-current the device turns off all MOSFET and latches the condition.

System thermal monitor is also provided allowing system protection from over-temperature conditions.

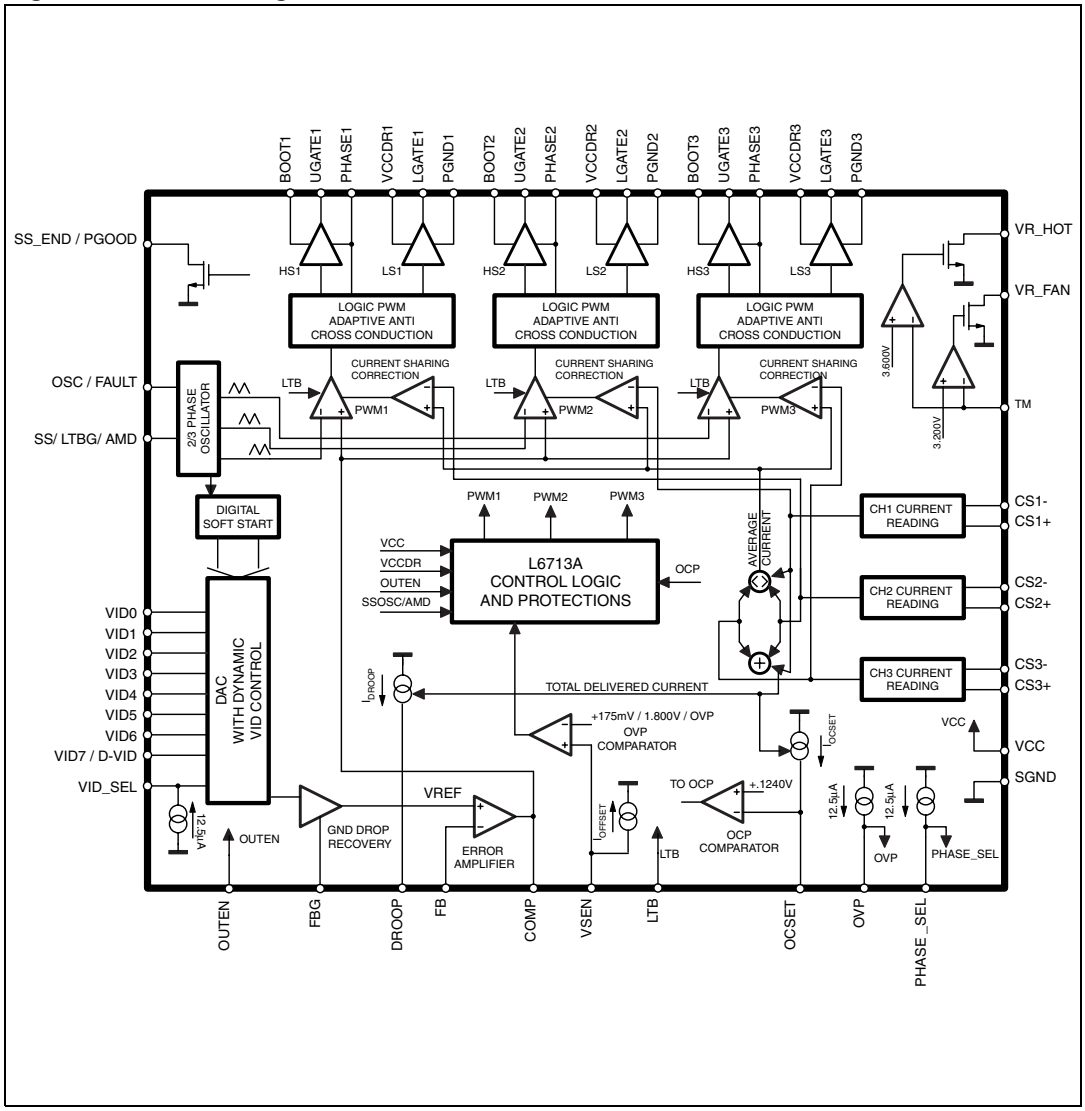
Table 1. Device summary

Order codes	Package	Packaging
L6713A	TQFP64 (Exposed pad)	Tube
L6713ATR		Tape and reel

Contents

1 Block diagram

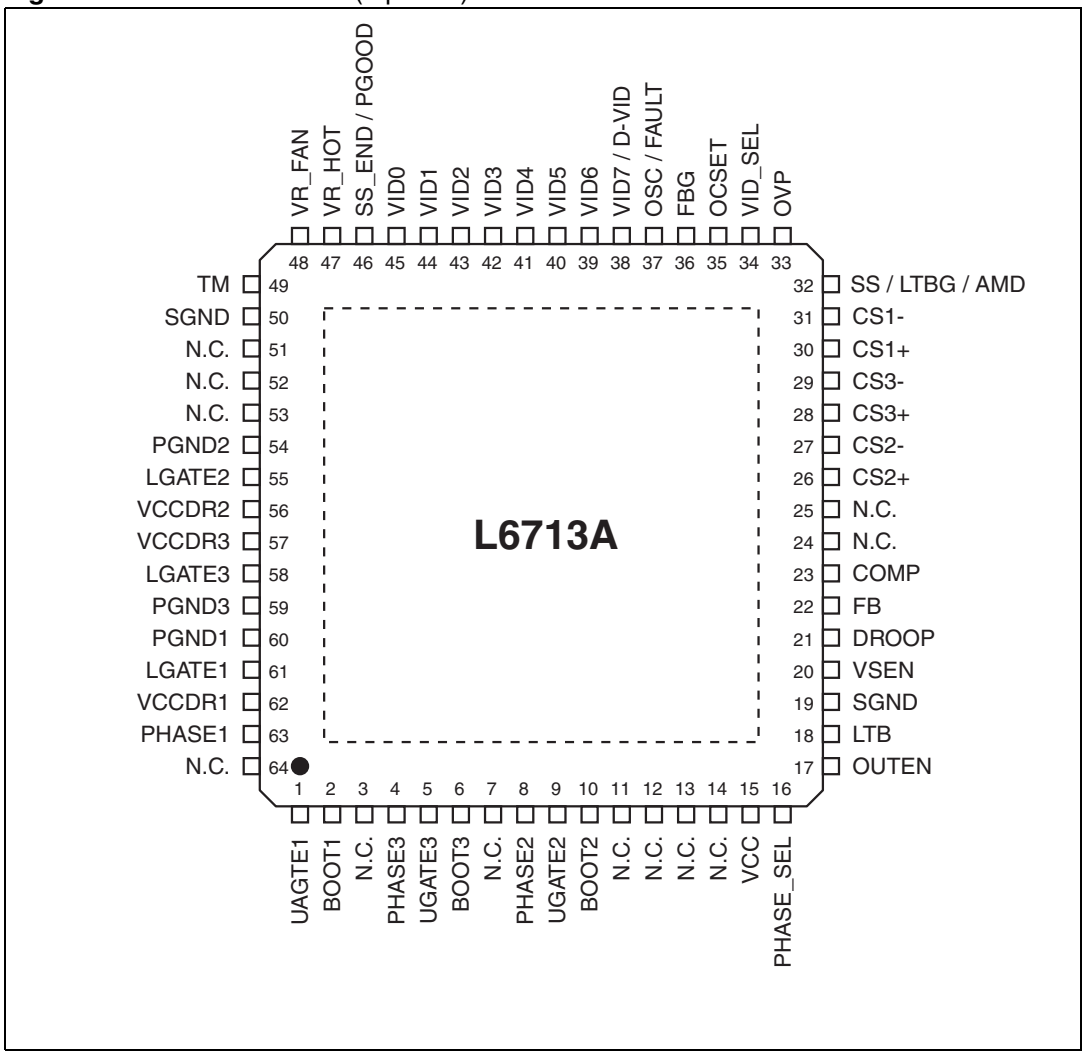
Figure 1. Block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

N°	Pin	Function
1	UGATE1	Channel 1 HS driver output. A small series resistors helps in reducing device-dissipated power.
2	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE1 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
3	N.C.	Not internally connected.
4	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 MOSFET source and provides return path for the HS driver of channel 3.
5	UGATE3	Channel 3 HS driver output. A small series resistors helps in reducing device-dissipated power.
6	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE3 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
7	N.C.	Not internally connected.
8	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 MOSFET source and provides return path for the HS driver of channel 2. Leave floating when using 2 phase operation.
9	UGATE2	Channel 2 HS driver output. A small series resistors helps in reducing device-dissipated power. Leave floating when using 2 phase operation.
10	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE2 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.Leave floating when using 2 phase operation.
11	N.C.	Not internally connected.
12	N.C.	Not internally connected.
13	N.C.	Not internally connected.
14	N.C.	Not internally connected.
15	VCC	Device supply voltage. The operative voltage is 12 V ±15 %. Filter with 1 µF (typ) MLCC vs. SGND.
16	PHASE_ SEL	Phase selection pin. Internally pulled up by 12.5 µA(typ) to 5 V. It allows selecting between 2 phase and 3 phase operation. See Table 11 for details.

Table 2. Pin description (continued)

N°	Pin	Function
17	OUTEN	Output enable pin. Internally pulled up by 12.5 µA(typ) to 5 V. Forced low, the device stops operations with all MOSFETs OFF: all the protections are disabled except for Preliminary over voltage. Leave floating, the device starts-up implementing soft-start up to the selected VID code. Cycle this pin to recover latch from protections; filter with 1 nF (typ) vs. SGND.
18	LTB	Load transient boost pin. Internally fixed at 1 V, connecting a R_{LTB} - C_{LTB} vs. VOUT allows to enable the Load transient boost technology™: as soon as the device detects a transient load it turns on all the PHASEs at the same time. Short to SGND to disable the function.
19	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
20	VSEN	It manages OVP and UVP protections and PGOOD (when applicable). See “Output voltage monitor and protections” Section. 100 µA constant current (I_{OFFSET}, See Table 5) is sunk by VSEN pin in order to generate a positive offset in according to the R_{OFFSET} resistor between VSEN pin and VOUT. See “Offset (Optional)” Section for details.
21	DROOP	A current proportional to the total current read is sourced from this pin according to the current reading gain. Short to FB to implement droop function or short to SGND to disable the function. Connecting to SGND through a resistor and filtering with a capacitor, the current info can be used for other purposes.
22	FB	Error amplifier inverting input. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F vs. COMP.
23	COMP	Error amplifier output. Connect with an R_F - C_F vs. FB. The device cannot be disabled by pulling down this pin.
24	N.C.	Not internally connected.
25	N.C.	Not internally connected.
26	CS2+	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. Short to SGND or to V_{OUT} when using 2 Phase operation. See “Layout guidelines” Section for proper layout of this connection.
27	CS2-	Channel 2 current sense negative input. Connect through a Rg resistor to the output-side of the channel 2 inductor. Leave floating when using 2 Phase operation. See “Layout guidelines” Section for proper layout of this connection.
28	CS3+	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. See “Layout guidelines” Section for proper layout of this connection.
29	CS3-	Channel 3 current sense negative input. Connect through a Rg resistor to the output-side of the channel 3 inductor. See “Layout guidelines” Section for proper layout of this connection.

Table 2. Pin description (continued)

N°	Pin	Function
30	CS1+	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor. See “Layout guidelines” Section for proper layout of this connection.
31	CS1-	Channel 1 current sense negative input. Connect through a Rg resistor to the output-side of the channel 1 inductor. See “Layout guidelines” Section for proper layout of this connection.
32	SS/ LTBG/ AMD	Soft-start oscillator, LTB gain and AMD selection pin. It allows selecting between INTEL DACs and AMD DAC. Short to SGND to select AMD DAC otherwise INTEL mode is selected. When INTEL mode is selected trough this pin it is possible to select the soft-start time and also the gain of LTB Technology™. See “Soft-start” Section” and See “Load transient boost technologyTM” Section for details.
33	OVP	Over voltage programming pin. Internally pulled up by 12.5 µA (typ) to 5 V. Leave floating to use built-in protection thresholds as reported into *Table 12*. Connect to SGND through a R_{OVP} resistor and filter with 100 pF (max) to set the OVP threshold to a fixed voltage according to the R_{OVP} resistor. See “Over voltage and programmable OVP” Section Section for details.
34	VID_SEL	Intel mode. Internally pulled up by 12.5 µA (typ) to 5 V. It allows selecting between VR10 (short to SGND, *Table 8*) or VR11 (floating, See Table 7) DACs. See “Configuring the device” Section for details. ***AMD mode.*** Not applicable. Needs to be shorted to SGND.
35	OCSET	Over current set pin. Connect to SGND through a R_{OCSET} resistor to set the OCP threshold. Connect also a C_{OCSET} capacitor to set a delay for the OCP intervention. See “Over current protection” Section for details.
36	FBG	Connect to the negative side of the load to perform remote sense. See “Layout guidelines” Section for proper layout of this connection.
37	OSC/ FAULT	Oscillator pin. It allows programming the switching frequency F_{SW} of each channel: the equivalent switching frequency at the load side results in being multiplied by the phase number N. Frequency is programmed according to the resistor connected from the pin vs. SGND or VCC with a gain of 8 kHz/µA (see relevant section for details). Leaving the pin floating programs a switching frequency of 200kHz per phase. The pin is forced high (5 V) to signal an OVP FAULT: to recover from this condition, cycle VCC or the OUTEN pin. See “Oscillator” Section for details.
38	VID7/DVID	***VID7 - Intel mode.*** See VID5 to VID0 section. ***DVID - AMD mode.*** DVID output. CMOS output pulled high when the controller is performing a D-VID transition (with 32 clock cycle delay after the transition has finished). See “Dynamic VID transitions” Section Section for details.
39	VID6	***Intel mode.*** See VID5 to VID0 section. ***AMD mode.*** Not applicable. Needs to be shorted to SGND.

Table 2. Pin description (continued)

N°	Pin	Function
40 to 45	VID5 to VID0	***Intel mode.*** Voltage identification pins (also applies to VID6, VID7). Internally pulled up by 25 µA to 5 V, connect to SGND to program a '0' or leave floating to program a '1'. They allow programming output voltage as specified in Table 7 and Table 8 according to VID_SEL status. OVP and UVP protection comes as a consequence of the programmed code (See Table 12). ***AMD mode.*** Voltage identification pins. Internally pulled down by 12.5 µA, leave floating to program a '0' while pull up to more than 1.4 V to program a '1'. They allow programming the output voltage as specified in Table 10 (VID7 doesn't care). OVP and UVP protection comes as a consequence of the programmed code (See Table 12). **Note.** VID6 not used, need to be shorted to SGND.
46	SS_END/ PGOOD	***SSEND - Intel mode.*** soft-start end signal. Open drain output sets free after SS has finished and pulled low when triggering any protection. Pull up to a voltage lower than 5 V (typ), if not used it can be left floating. PGOOD - AMD mode. Open drain output set free after SS has finished and pulled low when VSEN is lower than the relative threshold. Pull up to a voltage lower than 5 V (typ), if not used it can be left floating.
47	VR_HOT	Voltage regulator hot. Over temperature alarm signal. Open drain output, set free when TM overcomes the alarm threshold. Thermal monitoring output enabled if Vcc > $UVLO_{VCC}$. See "Thermal monitor" Section for details and typical connections.
48	VR_FAN	Voltage regulator fan. Over temperature warning signal. Open drain output, set free when TM overcomes the warning threshold. Thermal monitoring output enabled if Vcc > $UVLO_{VCC}$. See "Thermal monitor" Section for details and typical connections.
49	TM	Thermal monitor input. It senses the regulator temperature through apposite network and drives VR_FAN and VR_HOT accordingly. Short TM pin to SGND if not used. See "Thermal monitor" Section for details and typical connections.
50	SGND	All the internal references are referred to this pin. Connect to the PCB signal Ground.
51	N.C.	Not internally connected.
52	N.C.	Not internally connected.
53	N.C.	Not internally connected.
54	PGND2	Channel 2 LS driver return path. Connect to power ground plane. It must be connected to power ground plane also when using 2-phase operation.
55	LGATE2	Channel 2 LS driver output. A small series resistor helps in reducing device-dissipated power. Leave floating when using 2 phase operation.

Table 2. Pin description (continued)

N°	Pin	Function
56	VCCDR2	Channel 2 LS driver supply. It must be connected to others VCCDRx pins also when using 2-phase operation. LS driver supply can range from 5 Vbus up to 12 Vbus, filter with 1 µF MLCC cap vs. PGND2.
57	VCCDR3	Channel 3 LS driver supply. It must be connected to others VCCDRx pins. LS driver supply can range from 5 Vbus up to 12 Vbus, filter with 1 µF MLCC cap vs. PGND3.
58	LGATE3	Channel 3 LS driver output. A small series resistor helps in reducing device-dissipated power.
59	PGND3	Channel 3 LS driver return path. Connect to power ground plane.
60	PGND1	Channel 1 LS driver return path. Connect to power ground plane.
61	LGATE1	Channel 1 LS driver output. A small series resistor helps in reducing device-dissipated power.
62	VCCDR1	Channel 1 LS driver supply. It must be connected to others VCCDRx pins. LS driver supply can range from 5 Vbus up to 12 Vbus, filter with 1 µF MLCC cap vs. PGND1.
63	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.
64	N.C.	Not internally connected.
PAD	Thermal pad	Thermal pad connects the silicon substrate and makes good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect to the PGND plane with several VIAs to improve thermal conductivity.

3 Electrical data

3.1 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDRx}	to PGNDx	15	V
V_{BOOTx} - V_{PHASEx}	Boot voltage	15	V
V_{UGATEx} - V_{PHASEx}		15	V
V_{CC} - V_{BOOTx}		7.5	V
	LGATEx, PHASEx, to PGNDx	-0.3 to V_{CC} + 0.3	V
	VID0 to VID7, VID_SEL	-0.3 to 5	V
	All other pins to PGNDx	-0.3 to 7	V
V_{PHASEx}	Static condition to PGNDx, VCC = 14 V, BOOTx = 7 V, PHASEx = -7.5 V	-7.5	V
	Positive peak voltage to PGNDx; T < 20 ns @ 600 kHz	26	V

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	40	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25 °C	2.5	W

4 Electrical characteristics

V_{CC} = 12 V ± 15 %, T_J = 0 °C to 70 °C, unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply current						
I_{CC}	VCC supply current	HGATEx and LGATEx = OPEN VCCDRx = BOOTx = 12 V		17		mA
I_{CCDRx}	VCCDRx supply current	LGATEx = OPEN; VCCDRx = 12 V		1		mA
I_{BOOTx}	BOOTx supply current	HGATEx = OPEN; PHASEx to PGNDx VCC = BOOTx = 12 V		0.75		mA
Power-ON						
$UVLO_{VCC}$	VCC turn-ON	VCC Rising; VCCDRx = 5 V		8.9	9.3	V
	VCC turn-OFF	VCC Falling; VCCDRx = 5 V	7.3	7.7		V
$UVLO_{VCCDR}$	VCCDR turn-ON	VCCDRx Rising; VCC = 12 V		4.5	4.8	V
	VCCDR turn-OFF	VCCDRx Falling; VCC = 12 V	3.9	4.3		V
$UVLO_{OVP}$	Pre-OVP turn-ON	VCC Rising; VCCDRx = 5 V		3.6	4.2	V
	Pre-OVP turn-OFF	VCC Falling; VCCDRx = 5 V	3.05	3.3		V
Oscillator and inhibit						
F_{OSC}	Main oscillator accuracy	OSC = OPEN OSC = OPEN; T_J = 0 °C to 125 °C	180 175	200	220 225	kHz
T_1	SS delay time	Intel mode	1			ms
T_2	SS time T_2	Intel mode; R_{SSOSC} = 25 kΩ		500		µs
T_3	SS time T_3	Intel mode	50			µs
OUTEN	Output enable intel mode	Rising thresholds voltage	0.80	0.85	0.90	V
		Hysteresis		100		mV
	Output enable AMD mode	Input low			0.80	V
		Input high	1.40			V
	OUTEN pull-up current	OUTEN to SGND		12.5		µA
ΔV_{OSC}	PWMx ramp amplitude			3		V
FAULT	Voltage at pin OSC	OVP active		5		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Reference and DAC						
k_{VID}	Output voltage accuracy	Intel mode VID = 1.000 V to VID = 1.600 V FB = VOUT; FBG = GNDOUT	-0.5	-	0.5	%
		AMD mode VID = 1.000 V to VID = 1.550 V FB = VOUT; FBG = GNDOUT	-0.6	-	0.6	%
V_{BOOT}	Boot voltage	Intel mode		1.081		V
I_{VID}	VID pull-up current	Intel mode; VIDx to SGND		25		µA
	VID pull-down current	AMD mode; VIDx to 5.4 V		12.5		µA
VID_{IL}	VID thresholds	Intel mode; Input low AMD mode; Input low			0.3 0.8	V
VID_{IH}		Intel mode; Input high AMD mode; Input high	0.8 1.35			V
VID_SEL	VID_SEL threshold (Intel mode)	Input low Input high	 0.8		0.3	V
	VID_SEL pull-up current	VIDSEL to SGND		12.5		µA
Error amplifier						
A_0	EA DC gain			80		dB
SR	EA slew rate	COMP = 10 pF to SGND		20		V/µs
Differential current sensing and offset						
I_{CSx+}	Bias current	Inductor sense		0		µA
$\frac{I_{INFOx}-I_{AVG}}{I_{AVG}}$	Current sense mismatch	Rg = 1 kΩ; I_{INFOx} = 25 µA	-3	-	3	%
V_{OCTH}	Over current threshold	V_{OCSET} (OCP)	1.215	1.240	1.265	V
K_{IOCSET}	OCSET current accuracy	Rg = 1 kΩ 2-PHASE, I_{OCSET} = 60 µA; 3-PHASE, I_{OCSET} = 90 µA;	-5	-	5	%
k_{IDROOP}	Droop current deviation from nominal value	Rg = 1kΩ 2-PHASE, I_{DROOP} = 0 to 40 µA; 3-PHASE, I_{DROOP} = 0 to 60 µA;	-1	-	1	µA
I_{OFFSET}	Offset current	VSEN = 0.500 V to 1.600 V	90	100	110	µA
Gate driver						
t_{RISE_UGATEx}	HS rise time	BOOTx - PHASEx = 10 V; C_{UGATEx} to PHASEx = 3.3 nF		15	30	ns
I_{UGATEx}	HS source current	BOOTx - PHASEx = 10 V		2		A
R_{UGATEx}	HS sink resistance	BOOTx - PHASEx = 12 V	1.5	2	2.5	Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RISE_LGATEx}	LS rise time	VCCDRx = 10 V; C_{LGATEx} to PGNDx = 5.6 nF		30	55	ns
I_{LGATEx}	LS source current	VCCDRx = 10 V		1.8		A
R_{LGATEx}	LS sink resistance	VCCDRx = 12 V	0.7	1.1	1.5	Ω
Protections						
OVP	Over voltage protection (VSEN rising)	Intel mode; Before V_{BOOT}			1.300	V
		Intel mode; Above VID	150	175	200	mV
		AMD mode	1.700	1.740	1.780	V
Program-mable OVP	I_{OVP} current	OVP = SGND	11.5	12.5	13.5	µA
	Comparator offset voltage	OVP = 1.8 V	-20	0	20	mV
Pre-OVP	Preliminary over voltage protection	$UVLO_{OVP}$ < VCC < $UVLO_{VCC}$ VCC > $UVLO_{VCC}$ & OUTEN = SGND		1.800		V
		Hysteresis		350		mV
UVP	Under voltage protection	VSEN falling; Below VID		-750		mV
PGOOD	PGOOD threshold	AMD mode; VSEN falling; Below VID		-300		mV
$V_{SSEND/PGOOD}$	SSEND / PGOOD voltage low	I = -4 mA			0.4	V
Thermal monitor						
V_{TM}	TM warning (VR_FAN)	V_{TM} rising		3.2		V
	TM alarm (VR_HOT)	V_{TM} rising	3.420	3.6	3.770	V
	TM hysteresis			100		mV
V_{VR_HOT}; V_{VR_FAN}	VR_HOT voltage low; VR_FAN voltage low	I = -4 mA			0.4 0.4	V V

5 VID Tables

5.1 Mapping for the Intel VR11 mode

Table 6. Voltage identification (VID) mapping for Intel VR11 mode

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
800 mV	400 mV	200 mV	100 mV	50 mV	25 mV	12.5 mV	6.25 mV

5.2 Voltage identification (VID) for Intel VR11 mode

Table 7. Voltage identification (VID) for Intel VR11 mode (See Note)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
0	0	OFF	4	0	1.21250	8	0	0.81250	C	0	0.41250
0	1	OFF	4	1	1.20625	8	1	0.80625	C	1	0.40625
0	2	1.60000	4	2	1.20000	8	2	0.80000	C	2	0.40000
0	3	1.59375	4	3	1.19375	8	3	0.79375	C	3	0.39375
0	4	1.58750	4	4	1.18750	8	4	0.78750	C	4	0.38750
0	5	1.58125	4	5	1.18125	8	5	0.78125	C	5	0.38125
0	6	1.57500	4	6	1.17500	8	6	0.77500	C	6	0.37500
0	7	1.56875	4	7	1.16875	8	7	0.76875	C	7	0.36875
0	8	1.56250	4	8	1.16250	8	8	0.76250	C	8	0.36250
0	9	1.55625	4	9	1.15625	8	9	0.75625	C	9	0.35625
0	A	1.55000	4	A	1.15000	8	A	0.75000	C	A	0.35000
0	B	1.54375	4	B	1.14375	8	B	0.74375	C	B	0.34375
0	C	1.53750	4	C	1.13750	8	C	0.73750	C	C	0.33750
0	D	1.53125	4	D	1.13125	8	D	0.73125	C	D	0.33125
0	E	1.52500	4	E	1.12500	8	E	0.72500	C	E	0.32500
0	F	1.51875	4	F	1.11875	8	F	0.71875	C	F	0.31875
1	0	1.51250	5	0	1.11250	9	0	0.71250	D	0	0.31250
1	1	1.50625	5	1	1.10625	9	1	0.70625	D	1	0.30625
1	2	1.50000	5	2	1.10000	9	2	0.70000	D	2	0.30000
1	3	1.49375	5	3	1.09375	9	3	0.69375	D	3	0.29375
1	4	1.48750	5	4	1.08750	9	4	0.68750	D	4	0.28750
1	5	1.48125	5	5	1.08125	9	5	0.68125	D	5	0.28125
1	6	1.47500	5	6	1.07500	9	6	0.67500	D	6	0.27500

Table 7. Voltage identification (VID) for Intel VR11 mode (See Note) (continued)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
1	7	1.46875	5	7	1.06875	9	7	0.66875	D	7	0.26875
1	8	1.46250	5	8	1.06250	9	8	0.66250	D	8	0.26250
1	9	1.45625	5	9	1.05625	9	9	0.65625	D	9	0.25625
1	A	1.45000	5	A	1.05000	9	A	0.65000	D	A	0.25000
1	B	1.44375	5	B	1.04375	9	B	0.64375	D	B	0.24375
1	C	1.43750	5	C	1.03750	9	C	0.63750	D	C	0.23750
1	D	1.43125	5	D	1.03125	9	D	0.63125	D	D	0.23125
1	E	1.42500	5	E	1.02500	9	E	0.62500	D	E	0.22500
1	F	1.41875	5	F	1.01875	9	F	0.61875	D	F	0.21875
2	0	1.41250	6	0	1.01250	A	0	0.61250	E	0	0.21250
2	1	1.40625	6	1	1.00625	A	1	0.60625	E	1	0.20625
2	2	1.40000	6	2	1.00000	A	2	0.60000	E	2	0.20000
2	3	1.39375	6	3	0.99375	A	3	0.59375	E	3	0.19375
2	4	1.38750	6	4	0.98750	A	4	0.58750	E	4	0.18750
2	5	1.38125	6	5	0.98125	A	5	0.58125	E	5	0.18125
2	6	1.37500	6	6	0.97500	A	6	0.57500	E	6	0.17500
2	7	1.36875	6	7	0.96875	A	7	0.56875	E	7	0.16875
2	8	1.36250	6	8	0.96250	A	8	0.56250	E	8	0.16250
2	9	1.35625	6	9	0.95625	A	9	0.55625	E	9	0.15625
2	A	1.35000	6	A	0.95000	A	A	0.55000	E	A	0.15000
2	B	1.34375	6	B	0.94375	A	B	0.54375	E	B	0.14375
2	C	1.33750	6	C	0.93750	A	C	0.53750	E	C	0.13750
2	D	1.33125	6	D	0.93125	A	D	0.53125	E	D	0.13125
2	E	1.32500	6	E	0.92500	A	E	0.52500	E	E	0.12500
2	F	1.31875	6	F	0.91875	A	F	0.51875	E	F	0.11875
3	0	1.31250	7	0	0.91250	B	0	0.51250	F	0	0.11250
3	1	1.30625	7	1	0.90625	B	1	0.50625	F	1	0.10625
3	2	1.30000	7	2	0.90000	B	2	0.50000	F	2	0.10000
3	3	1.29375	7	3	0.89375	B	3	0.49375	F	3	0.09375
3	4	1.28750	7	4	0.88750	B	4	0.48750	F	4	0.08750
3	5	1.28125	7	5	0.88125	B	5	0.48125	F	5	0.08125
3	6	1.27500	7	6	0.87500	B	6	0.47500	F	6	0.07500
3	7	1.26875	7	7	0.86875	B	7	0.46875	F	7	0.06875

Table 7. Voltage identification (VID) for Intel VR11 mode (See Note) (continued)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
3	8	1.26250	7	8	0.86250	B	8	0.46250	F	8	0.06250
3	9	1.25625	7	9	0.85625	B	9	0.45625	F	9	0.05625
3	A	1.25000	7	A	0.85000	B	A	0.45000	F	A	0.05000
3	B	1.24375	7	B	0.84375	B	B	0.44375	F	B	0.04375
3	C	1.23750	7	C	0.83750	B	C	0.43750	F	C	0.03750
3	D	1.23125	7	D	0.83125	B	D	0.43125	F	D	0.03125
3	E	1.22500	7	E	0.82500	B	E	0.42500	F	E	OFF
3	F	1.21875	7	F	0.81875	B	F	0.41875	F	F	OFF

1. According to VR11 specs, the device automatically regulates output voltage 19 mV lower to avoid any external offset to modify the built-in 0.5 % accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19 mV built-in offset.

5.3 Voltage identifications (VID) for Intel VR10 mode + 6.25 mV

(VID7 does not care)

Table 8. Voltage identifications (VID) for Intel VR10 mode + 6.25 mV (See Note)

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
0	1	0	1	0	1	1	1.60000	1	1	0	1	0	1	1	1.20000
0	1	0	1	0	1	0	1.59375	1	1	0	1	0	1	0	1.19375
0	1	0	1	1	0	1	1.58750	1	1	0	1	1	0	1	1.18750
0	1	0	1	1	0	0	1.58125	1	1	0	1	1	0	0	1.18125
0	1	0	1	1	1	1	1.57500	1	1	0	1	1	1	1	1.17500
0	1	0	1	1	1	0	1.56875	1	1	0	1	1	1	0	1.16875
0	1	1	0	0	0	1	1.56250	1	1	1	0	0	0	1	1.16250
0	1	1	0	0	0	0	1.55625	1	1	1	0	0	0	0	1.15625
0	1	1	0	0	1	1	1.55000	1	1	1	0	0	1	1	1.15000
0	1	1	0	0	1	0	1.54375	1	1	1	0	0	1	0	1.14375
0	1	1	0	1	0	1	1.53750	1	1	1	0	1	0	1	1.13750
0	1	1	0	1	0	0	1.53125	1	1	1	0	1	0	0	1.13125
0	1	1	0	1	1	1	1.52500	1	1	1	0	1	1	1	1.12500
0	1	1	0	1	1	0	1.51875	1	1	1	0	1	1	0	1.11875
0	1	1	1	0	0	1	1.51250	1	1	1	1	0	0	1	1.11250
0	1	1	1	0	0	0	1.50625	1	1	1	1	0	0	0	1.10625

Table 8. Voltage identifications (VID) for Intel VR10 mode + 6.25 mV (See Note)

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
0	1	1	1	0	1	1	1.50000	1	1	1	1	0	1	1	1.10000
0	1	1	1	0	1	0	1.49375	1	1	1	1	0	1	0	1.09375
0	1	1	1	1	0	1	1.48750	1	1	1	1	1	0	1	OFF
0	1	1	1	1	0	0	1.48125	1	1	1	1	1	0	0	OFF
0	1	1	1	1	1	1	1.47500	1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	0	1.46875	1	1	1	1	1	1	0	OFF
1	0	0	0	0	0	1	1.46250	0	0	0	0	0	0	1	1.08750
1	0	0	0	0	0	0	1.45625	0	0	0	0	0	0	0	1.08125
1	0	0	0	0	1	1	1.45000	0	0	0	0	0	1	1	1.07500
1	0	0	0	0	1	0	1.44375	0	0	0	0	0	1	0	1.06875
1	0	0	0	1	0	1	1.43750	0	0	0	0	1	0	1	1.06250
1	0	0	0	1	0	0	1.43125	0	0	0	0	1	0	0	1.05625
1	0	0	0	1	1	1	1.42500	0	0	0	0	1	1	1	1.05000
1	0	0	0	1	1	0	1.41875	0	0	0	0	1	1	0	1.04375
1	0	0	1	0	0	1	1.41250	0	0	0	1	0	0	1	1.03750
1	0	0	1	0	0	0	1.40625	0	0	0	1	0	0	0	1.03125
1	0	0	1	0	1	1	1.40000	0	0	0	1	0	1	1	1.02500
1	0	0	1	0	1	0	1.39375	0	0	0	1	0	1	0	1.01875
1	0	0	1	1	0	1	1.38750	0	0	0	1	1	0	1	1.01250
1	0	0	1	1	0	0	1.38125	0	0	0	1	1	0	0	1.00625
1	0	0	1	1	1	1	1.37500	0	0	0	1	1	1	1	1.00000
1	0	0	1	1	1	0	1.36875	0	0	0	1	1	1	0	0.99375
1	0	1	0	0	0	1	1.36250	0	0	1	0	0	0	1	0.98750
1	0	1	0	0	0	0	1.35625	0	0	1	0	0	0	0	0.98125
1	0	1	0	0	1	1	1.35000	0	0	1	0	0	1	1	0.97500
1	0	1	0	0	1	0	1.34375	0	0	1	0	0	1	0	0.96875
1	0	1	0	1	0	1	1.33750	0	0	1	0	1	0	1	0.96250
1	0	1	0	1	0	0	1.33125	0	0	1	0	1	0	0	0.95625
1	0	1	0	1	1	1	1.32500	0	0	1	0	1	1	1	0.95000
1	0	1	0	1	1	0	1.31875	0	0	1	0	1	1	0	0.94375
1	0	1	1	0	0	1	1.31250	0	0	1	1	0	0	1	0.93750
1	0	1	1	0	0	0	1.30625	0	0	1	1	0	0	0	0.93125
1	0	1	1	0	1	1	1.30000	0	0	1	1	0	1	1	0.92500

Table 8. Voltage identifications (VID) for Intel VR10 mode + 6.25 mV (See Note)

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
1	0	1	1	0	1	0	1.29375	0	0	1	1	0	1	0	0.91875
1	0	1	1	1	0	1	1.28750	0	0	1	1	1	0	1	0.91250
1	0	1	1	1	0	0	1.28125	0	0	1	1	1	0	0	0.90625
1	0	1	1	1	1	1	1.27500	0	0	1	1	1	1	1	0.90000
1	0	1	1	1	1	0	1.26875	0	0	1	1	1	1	0	0.89375
1	1	0	0	0	0	1	1.26250	0	1	0	0	0	0	1	0.88750
1	1	0	0	0	0	0	1.25625	0	1	0	0	0	0	0	0.88125
1	1	0	0	0	1	1	1.25000	0	1	0	0	0	1	1	0.87500
1	1	0	0	0	1	0	1.24375	0	1	0	0	0	1	0	0.86875
1	1	0	0	1	0	1	1.23750	0	1	0	0	1	0	1	0.86250
1	1	0	0	1	0	0	1.23125	0	1	0	0	1	0	0	0.85625
1	1	0	0	1	1	1	1.22500	0	1	0	0	1	1	1	0.85000
1	1	0	0	1	1	0	1.21875	0	1	0	0	1	1	0	0.84375
1	1	0	1	0	0	1	1.21250	0	1	0	1	0	0	1	0.83750
1	1	0	1	0	0	0	1.20625	0	1	0	1	0	0	0	0.83125

1. According to VR10.x specs, the device automatically regulates output voltage 19 mV lower to avoid any external offset to modify the built-in 0.5 % accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19mVbuilt-in offset. VID7 doesn't care.

5.4 Mapping for the AMD 6 bit mode

Table 9. Voltage identifications (VID) mapping for AMD 6 bit mode

VID4	VID3	VID2	VID1	VID0
400 mV	200 mV	100 mV	50 mV	25 mV

5.5 Voltage identifications (VID) codes for AMD 6 bit mode

Table 10. Voltage identifications (VID) codes for AMD 6 bit mode (See Note)

VID5	VID4	VID3	VID2	VID1	VID0	Output voltage (1)	VID5	VID4	VID3	VID2	VID1	VID0	Output voltage (1)
0	0	0	0	0	0	1.5500	1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250	1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000	1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750	1	0	0	0	1	1	0.7250

Table 10. Voltage identifications (VID) codes for AMD 6 bit mode (See Note) (continued)

VID5	VID4	VID3	VID2	VID1	VID0	Output voltage (1)	VID5	VID4	VID3	VID2	VID1	VID0	Output voltage (1)
0	0	0	1	0	0	1.4500	1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250	1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000	1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750	1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500	1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250	1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000	1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750	1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500	1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250	1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000	1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750	1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500	1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250	1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000	1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750	1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500	1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250	1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000	1	1	0	1	1	0	0.4875
0	1	0	1	1	1	0.9750	1	1	0	1	1	1	0.4750
0	1	1	0	0	0	0.9500	1	1	1	0	0	0	0.4625
0	1	1	0	0	1	0.9250	1	1	1	0	0	1	0.4500
0	1	1	0	1	0	0.9000	1	1	1	0	1	0	0.4375
0	1	1	0	1	1	0.8750	1	1	1	0	1	1	0.4250
0	1	1	1	0	0	0.8500	1	1	1	1	0	0	0.4125
0	1	1	1	0	1	0.8250	1	1	1	1	0	1	0.4000
0	1	1	1	1	0	0.8000	1	1	1	1	1	0	0.3875
0	1	1	1	1	1	0.7750	1	1	1	1	1	1	0.3750

1. VID6 not applicable, need to be left unconnected.

6 Reference schematic

Figure 3. Reference schematic - Intel VR10.x, VR11 - 3-phase operation

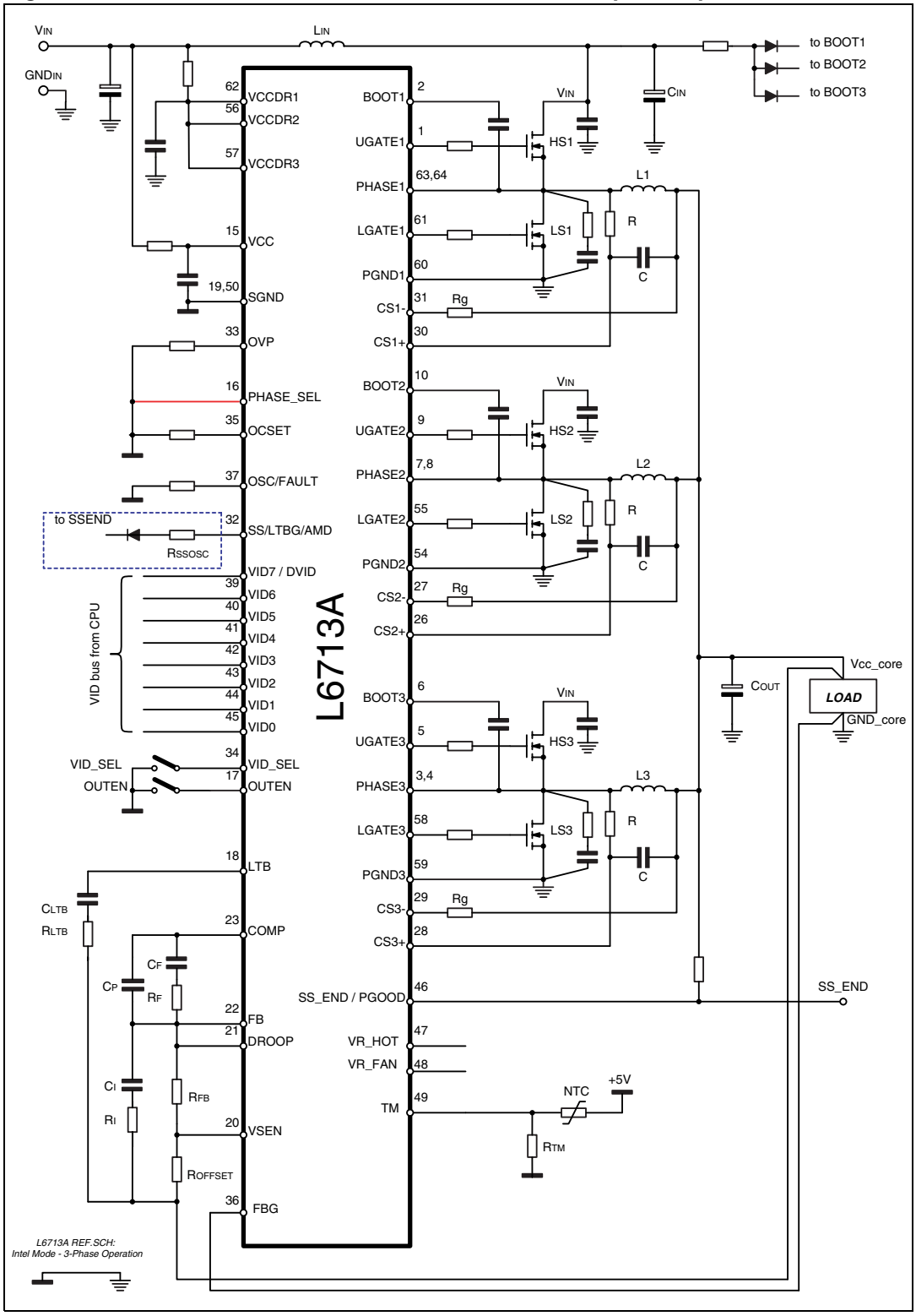


Figure 4. Reference schematic - Intel VR10.x, VR11 - 2-phase operation

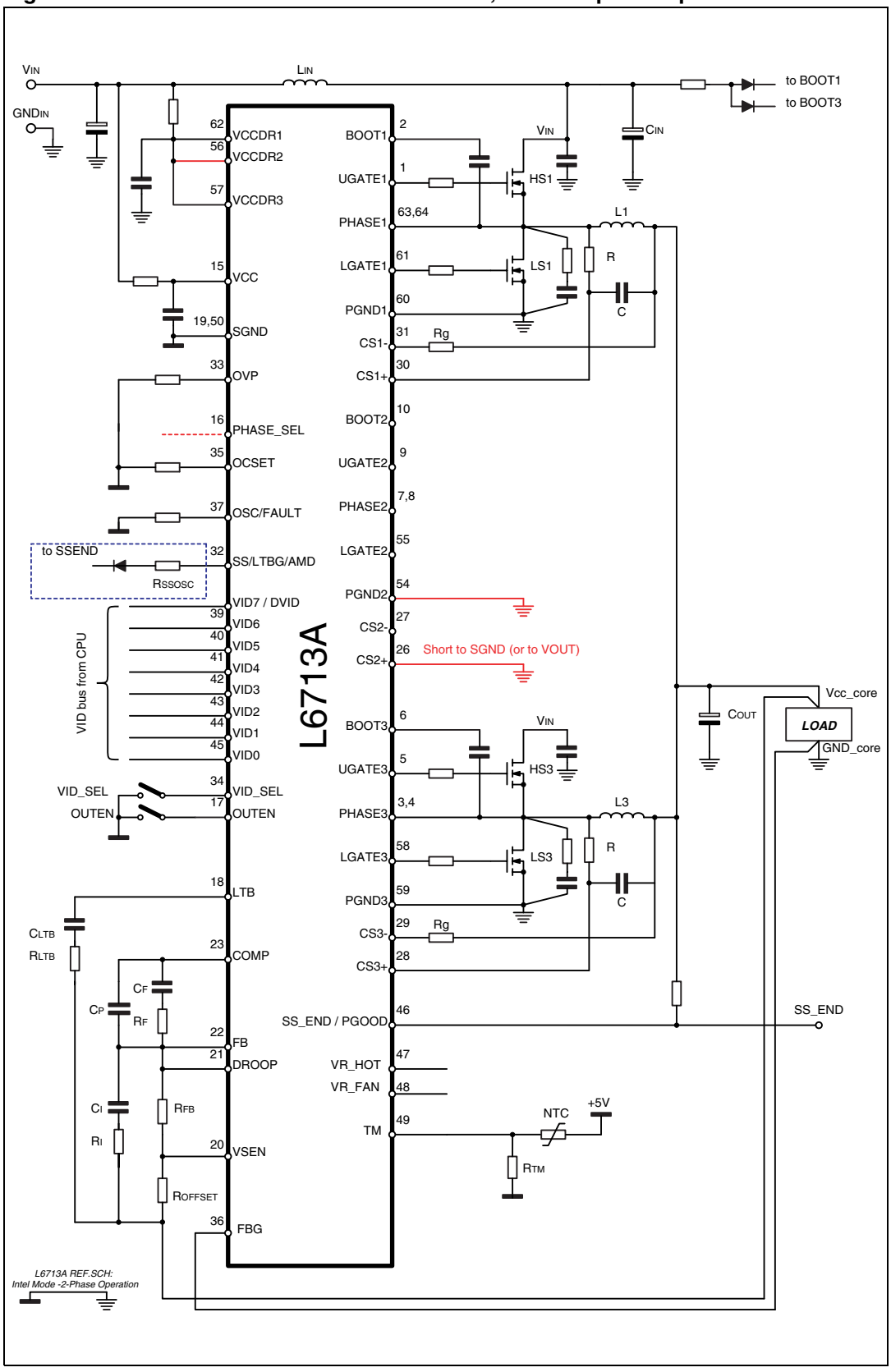


Figure 5. Reference schematic - AMD 6 bit - 3-phase operation

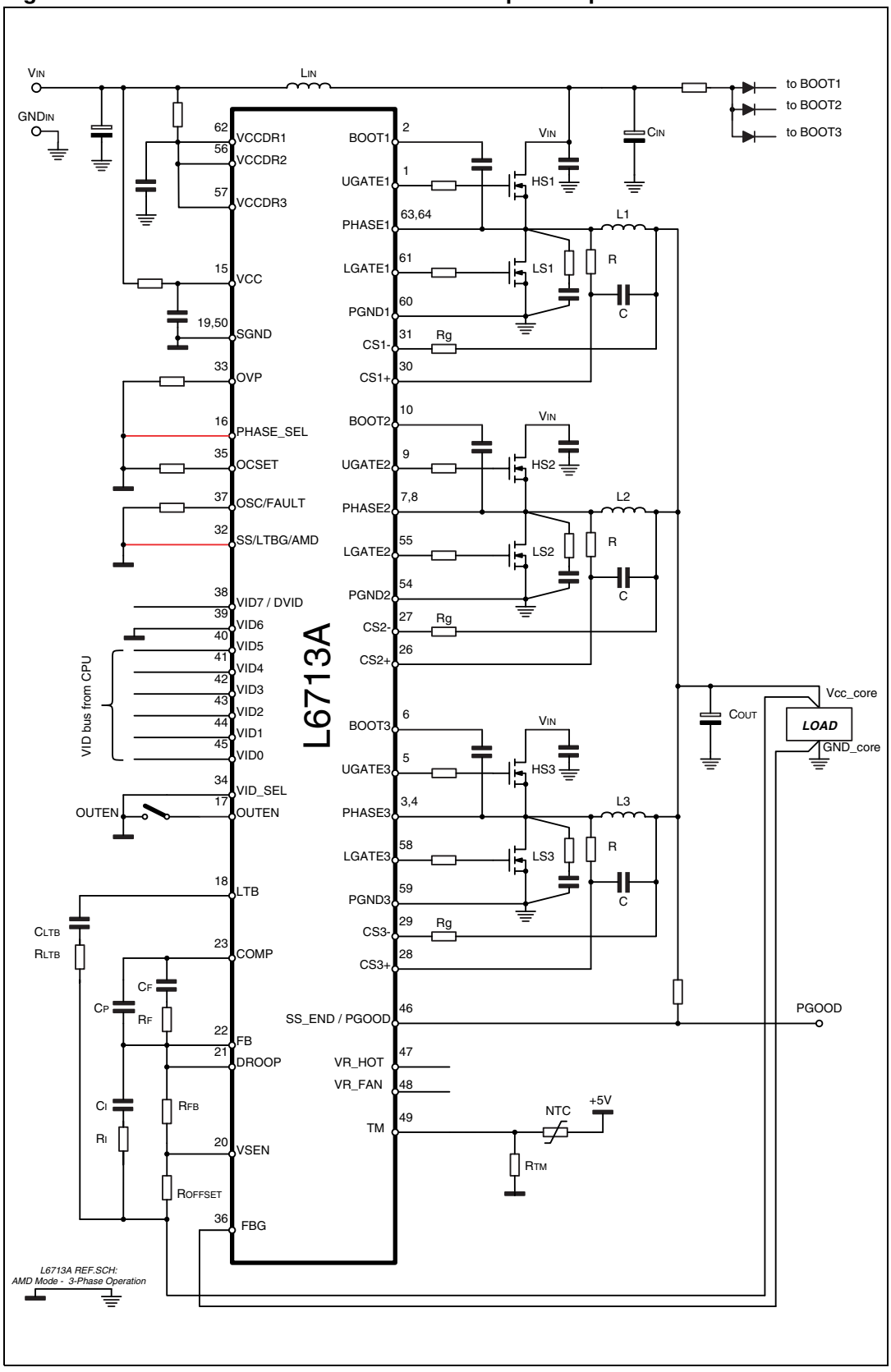


Figure 6. Reference schematic - AMD 6 bit - 2-phase operation