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L6714

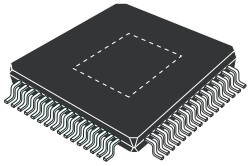
4 phase controller with embedded drivers for Intel VR10, VR11 and AMD 6Bit CPUs

Features

- 0.5% output voltage accuracy
- 7/8 bit programmable output up to 1.60000V - Intel VR10.x, VR11 DAC
- 6 bit programmable output up to 1.5500V - AMD 6Bit DAC
- High current integrated gate drivers
- Full differential current sensing across inductor or low side MOSFET
- Embedded VRD thermal monitor
- Integrated remote sense buffer
- Dynamic VID management
- Adjustable reference voltage offset
- Programmable Soft-Start
- Low-Side-Less startup
- Programmable over voltage protection
- Preliminary over voltage
- Constant over current protection
- Oscillator internally fixed at 150kHz externally adjustable
- Output enable
- SS_END / PGOOD signal
- TQFP64 10mm x 10mm package with Exposed Pad

Application

- High current VRD for desktop CPUs
- Workstation and server CPU power supply
- VRM modules



TQFP64 (Exposed Pad)

Description

L6714 implements a four phase step-down controller with 90º phase-shift between each phase with integrated high current drivers in a compact 10mm x 10mm body package with exposed pad.

The device embeds selectable DACs: the output voltage ranges up to 1.60000V (both Intel VR10.x and VR11 DAC) or up to 1.5500V (AMD 6Bit DAC) managing D-VID with ±0.5% output voltage accuracy over line and temperature variations. Additional programmable offset can be added to the reference voltage with a single external resistor.

The controller assures fast protection against load over current and under / over voltage (in this last case also before UVLO). In case of over-current the system works in Constant Current mode until UVP.

Selectable current reading adds flexibility to the design allowing current sense across inductor or LS MOSFET.

System Thermal Monitor is also provided allowing system protection from over-temperature conditions.

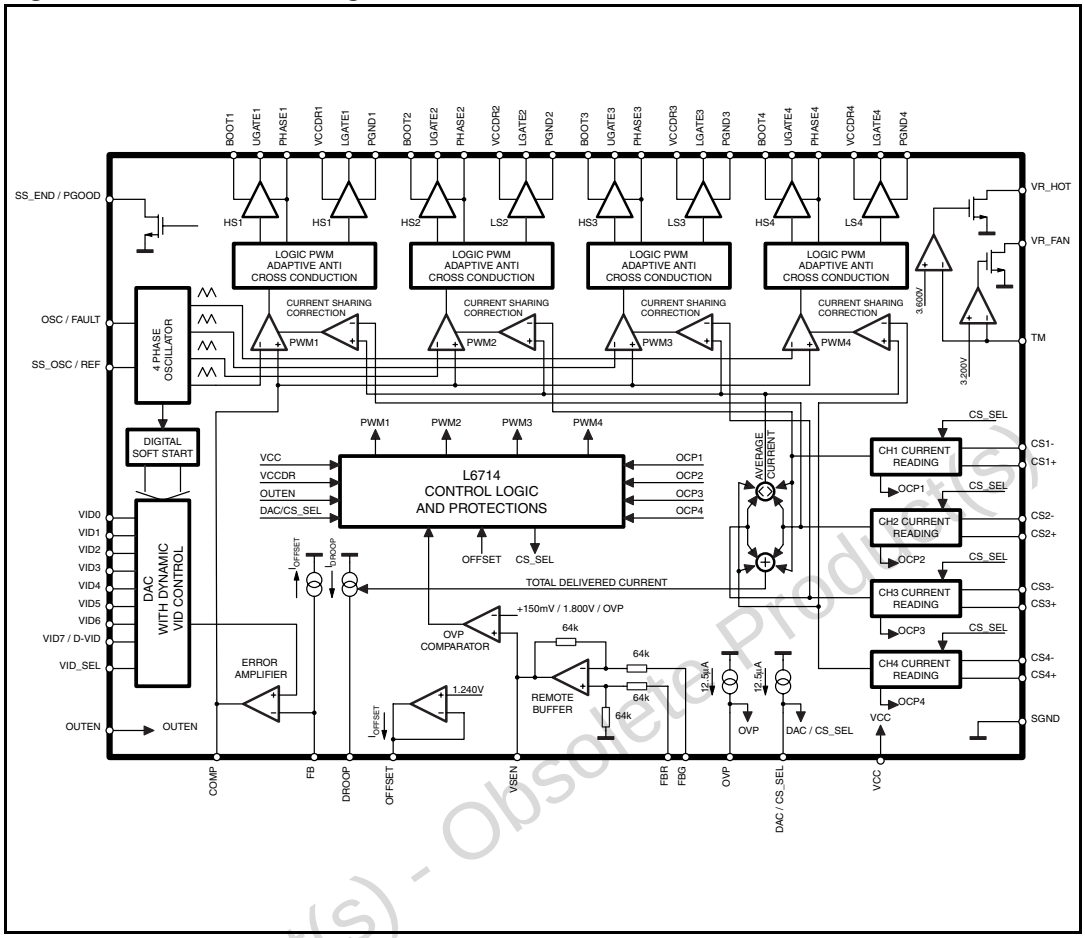
Order codes

Part number	Package	Packaging
L6714	TQFP64	Tube
L6714TR	TQFP64	Tape and reel

Contents

1 Block diagram

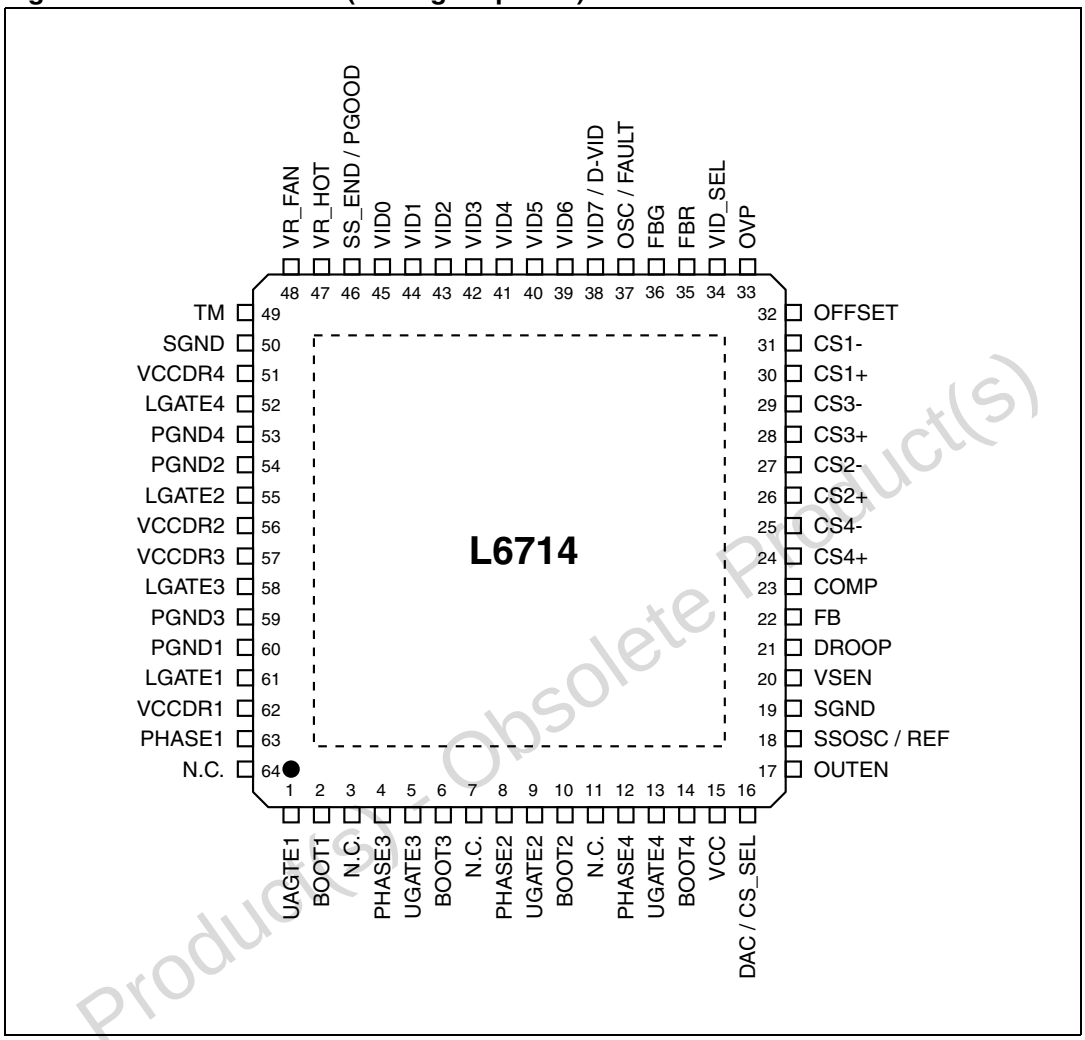
Figure 1. L6714 block diagram



2 Pin settings

2.1 Connections

Figure 2. Pin connection (Through top view)



2.2 Functions

Table 1. Pin functions

N°	Pin	Function
1	UGATE1	Channel 1 HS driver output. A small series resistors helps in reducing device-dissipated power.
2	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE1 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
3	N.C.	Not internally connected.
4	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 mosfet source and provides return path for the HS driver of channel 3.
5	UGATE3	Channel 3 HS driver output. A small series resistors helps in reducing device-dissipated power.
6	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE3 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
7	N.C.	Not internally connected.
8	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 mosfet source and provides return path for the HS driver of channel 2.
9	UGATE2	Channel 2 HS driver output. A small series resistors helps in reducing device-dissipated power.
10	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE2 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.
11	N.C.	Not internally connected.
12	PHASE4	Channel 4 HS driver return path. It must be connected to the HS4 mosfet source and provides return path for the HS driver of channel 4.
13	UGATE4	Channel 4 HS driver output. A small series resistors helps in reducing device-dissipated power.
14	BOOT4	Channel 4 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE4 and provide necessary Bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge.

Table 1. Pin functions

N°	Pin	Function
15	VCC	Device supply voltage. The operative voltage is 12V ±15%. Filter with 1µF (typ) MLCC vs. SGND.
16	DAC/ CS_SEL	DAC and Current Sense SELection Pin. This pin sources a constant 12.5µA current. By connecting a resistor vs. SGND it is possible to select between Intel and AMD integrated DACs and Current Sense methods. Filter with 100pF(max) vs. SGND. DACs and Current Sense methods cannot be changed dynamically. See “DAC selection” Section and See Table 10 for details.
17	OUTEN	OUTput ENable Pin. Forced low, the device stops operations with all MOSFET OFF: all the protections are disabled except for *Section 16.2: Preliminary over voltage on page 47*. Set free, the device starts-up implementing soft-start up to the selected VID code. Cycle this pin to recover latch from protections; filter with 1nF (typ) vs. SGND.
18	SSOSC/ REF	***Intel Mode.*** Soft Start OSCillator Pin. By connecting a resistor R_{SSOSC} vs. SGND, it allows programming the frequency F_{SS} of an internal additional oscillator that drives the reference during Soft-Start. Setting this frequency allows programming the Soft-Start time T_{SS} proportionally to the R_{SSOSC} connected with a gain of 20.1612 [µs / kΩ]. The same slope implemented to reach V_{BOOT} has to be considered also when the reference moves from V_{BOOT} to the programmed VID code. See “Soft start” Section for details. ***AMD Mode.*** REFerence Output. Filter with 47Ω - 4.7nF vs. SGND.
19	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
20	VSEN	Remote Buffer Output, it manages OVP and UVP protections and PGOOD (when applicable). See “Output voltage monitor and protections” Section and See Table 10 for details.
21	DROOP	A current proportional to the total current read is sourced from this pin according to the Current Reading Gain. Short to FB to implement Droop Function or Short to SGND to disable the function.Connecting to SGND through a resistor and filtering with a capacitor, the current info can be used for other purposes. See “Droop function (Optional)” Section
22	FB	Error Amplifier Inverting Input. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F vs. COMP.
23	COMP	Error Amplifier Output. Connect with an R_F - C_F vs. FB. The device cannot be disabled by pulling down this pin.
24	CS4+	Channel 4 Current Sense Positive Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Source. Inductor DCR Sense: connect through an R-C filter to the phase-side of the channel 4 inductor. See “Layout guidelines” Section for proper layout of this connection.

Table 1. Pin functions

N°	Pin	Function
25	CS4-	Channel 4 Current Sense Negative Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Drain. Inductor DCR Sense: connect through a Rg resistor to the output-side of the channel 4 inductor. See “Layout guidelines” Section for proper layout of this connection.
26	CS2+	Channel 2 Current Sense Positive Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Source. Inductor DCR Sense: connect through an R-C filter to the phase-side of the channel 2 inductor. See “Layout guidelines” Section for proper layout of this connection.
27	CS2-	Channel 2 Current Sense Negative Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Drain. Inductor DCR Sense: connect through a Rg resistor to the output-side of the channel 2 inductor. See “Layout guidelines” Section for proper layout of this connection.
28	CS3+	Channel 3 Current Sense Positive Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Source. Inductor DCR Sense: connect through an R-C filter to the phase-side of the channel 3 inductor. See “Layout guidelines” Section for proper layout of this connection.
29	CS3-	Channel 3 Current Sense Negative Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Drain. Inductor DCR Sense: connect through a Rg resistor to the output-side of the channel 3 inductor. See “Layout guidelines” Section for proper layout of this connection.
30	CS1+	Channel 1 Current Sense Positive Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Source. Inductor DCR Sense: connect through an R-C filter to the phase-side of the channel 1 inductor. See “Layout guidelines” Section for proper layout of this connection.
31	CS1-	Channel 1 Current Sense Negative Input. LS Mosfet Sense: connect through a resistor Rg to the LS mosfet Drain. Inductor DCR Sense: connect through a Rg resistor to the output-side of the channel 1 inductor. See “Layout guidelines” Section for proper layout of this connection.
32	OFFSET	Offset Programming Pin. Internally fixed at 1.240V, connecting a R_{OFFSET} resistor vs. SGND allows setting a current that is mirrored into FB pin in order to program a positive offset according to the selected R_{FB}. Short to SGND to disable the function. See “Offset (Optional)” Section for details.

Table 1. Pin functions

N°	Pin	Function
33	OVP	Over Voltage Programming Pin. Internally pulled up by 12.5µA(typ) to 5V. Set free to use built-in protection thresholds as reported into *Table 10*. Connect to SGND through a R_{OVP} resistor and filter with 100pF (max) to set the OVP threshold to a fixed voltage according to the R_{OVP} resistor. See "Over voltage and programmable OVP" Section Section for details.
34	VID_SEL	***Intel Mode.*** It allows selecting between VR10 (short to SGND, *Table 7*) or VR11 (floating,*Table 6*) DACs ,internally pulled up by 12.5µA (typ.).. See "Configuring the device" Section for details. ***AMD Mode.*** Not Applicable. Needs to be shorted to SGND.
35	FBR	Remote Buffer Non Inverting Input. Connect to the positive side of the load to perform remote sense. See "Layout guidelines" Section for proper layout of this connection.
36	FBG	Remote Buffer Inverting Input. Connect to the negative side of the load to perform remote sense. See "Layout guidelines" Section for proper layout of this connection.
37	OSC/ FAULT	Oscillator Pin. It allows programming the switching frequency F_{SW} of each channel: the equivalent switching frequency at the load side results in being multiplied by the phase number N. Frequency is programmed according to the resistor connected from the pin vs. SGND or VCC with a gain of 6kHz/µA (see relevant section for details). Leaving the pin floating programs a switching frequency of 150kHz per phase. The pin is forced high (5V) to signal an OVP FAULT: to recover from this condition, cycle VCC or the OUTEN pin. See "Oscillator" Section for details.
38	VID7/ DVID	***VID7 - Intel Mode.*** See VID5 to VID0 Section. ***DVID - AMD Mode.*** DVID Output. CMOS output pulled high when the controller is performing a D-VID transition (with 32 clock cycle delay after the transition has finished). See "Dynamic VID transitions" Section Section for details.
39	VID6	***Intel Mode.*** See VID5 to VID0 Section. ***AMD Mode.*** Not Applicable. Need to be shorted to SGND.
40 to 45	VID5 to VID0	***Intel Mode.*** Voltage IDentification Pins (also applies to VID6, VID7). Internally pulled up by 25µA to 5V, connect to SGND to program a '0' or leave floating to program a '1'. They allow programming output voltage as specified in *Table 6* and *Table 7* according to VID_SEL status. OVP and UVP protection comes as a consequence of the programmed code (See Table 10). ***AMD Mode.*** Voltage IDentification Pins. Internally pulled down by 12.5µA, leave floating to program a '0' while pull up to more than 1.4V to program a '1'. They allow programming the output voltage as specified in *Table 9 on page 21* (VID7 doesn't care). OVP and UVP protection comes as a consequence of the programmed code (See Table 10). **Note.** VID6 not used, need to be shorted to SGND.

Table 1. Pin functions

N°	Pin	Function
46	SS_END/ PGOOD	***SSEND - Intel Mode.*** Soft Start END Signal. Open Drain Output set free after SS has finished and pulled low when triggering any protection. Pull up to a voltage lower than 5V (typ), if not used it can be left floating. PGOOD - AMD Mode. Open Drain Output set free after SS has finished and pulled low when VSEN is lower than the relative threshold. Pull up to a voltage lower than 5V (typ), if not used it can be left floating.
47	VR_HOT	Voltage Regulator HOT. Over Temperature Alarm Signal. Open Drain Output, set free when TM overcomes the Alarm Threshold. Thermal Monitoring Output enabled if Vcc > $UVLO_{VCC}$. See “Thermal monitor” Section for details and typical connections.
48	VR_FAN	Voltage Regulator FAN. Over Temperature Warning Signal. Open Drain Output, set free when TM overcomes the Warning Threshold. Thermal Monitoring Output enabled if Vcc > $UVLO_{VCC}$. See “Thermal monitor” Section for details and typical connections.
49	TM	Thermal Monitor Input. It senses the regulator temperature through apposite network and drives VR_FAN and VR_HOT accordingly.Short TM pin to SGND if not used. See “Thermal monitor” Section for details and typical connections.
50	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
51	VCCDR4	Channel 4 LS Driver Supply. It must be connected to others VCCDRx pins. LS Driver supply can range from 5Vbus up to 12Vbus, filter with 1µF MLCC cap vs. PGND4.
52	LGATE4	Channel 4 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
53	PGND4	Channel 4 LS Driver return path. Connect to Power ground Plane.
54	PGND2	Channel 2 LS Driver return path. Connect to Power ground Plane.
55	LGATE2	Channel 2 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
56	VCCDR2	Channel 2 LS Driver Supply. It must be connected to others VCCDRx pins. LS Driver supply can range from 5Vbus up to 12Vbus, filter with 1µF MLCC cap vs. PGND2.
57	VCCDR3	Channel 3 LS Driver Supply. It must be connected to others VCCDRx pins. LS Driver supply can range from 5Vbus up to 12Vbus, filter with 1µF MLCC cap vs. PGND3.
58	LGATE3	Channel 3 LS Driver Output.A small series resistor helps in reducing device-dissipated power.
59	PGND3	Channel 3 LS Driver return path. Connect to Power ground Plane.

Table 1. Pin functions

N°	Pin	Function
60	PGND1	Channel 1 LS Driver return path. Connect to Power ground Plane.
61	LGATE1	Channel 1 LS Driver Output.A small series resistor helps in reducing device-dissipated power.
62	VCCDR1	Channel 1 LS Driver Supply. It must be connected to others VCCDRx pins. LS Driver supply can range from 5Vbus up to 12Vbus, filter with 1µF MLCC cap vs. PGND1.
63	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 mosfet source and provides return path for the HS driver of channel 1.
64	N.C.	Not internally connected.
PAD	THERMAL PAD	Thermal pad connects the Silicon substrate and makes good thermal contact with the PCB to dissipate the power necessary to drive the external mosfets. Connect to the PGND plane with several VIAs to improve thermal conductivity.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDRx}	to PGNDx	15	V
V_{BOOTx} - V_{PHASEx}	Boot voltage	15	V
V_{UGATEx} - V_{PHASEx}		15	V
V_{CC} - V_{BOOTx}		7.5	V
	LGATEx, PHASEx, to PGNDx	-0.3 to V_{CC} + 0.3	V
	VID0 to VID7, VID_SEL	-0.3 to 5	V
	All other Pins to PGNDx	-0.3 to 7	V
V_{PHASEx}	Static condition To PGNDx, VCC=14V, BOOTx=7V, PHASEx=-7.5V	-7.5	V
	Positive peak voltage to PGNDx; T < 20ns @ 600kHz	26	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC Board)	40	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C
P_{TOT}	Maximum power dissipation at T_A = 25°C	2.5	W

4 Electrical characteristics

V_{CC} = 12V ± 15%, T_J = 0°C to 70°C, unless otherwise specified

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply Current						
I_{CC}	VCC supply current	HGATEx and LGATEx = OPEN VCCDRx = BOOTx = 12V		17		mA
I_{CCDRx}	VCCDRx supply current	LGATEx = OPEN; VCCDRx = 12V		1		mA
I_{BOOTx}	BOOTx supply current	HGATEx = OPEN; PHASEx to PGNDx; VCC = BOOTx = 12V		0.75		mA
Power-ON						
$UVLO_{VCC}$	VCC turn-ON	VCC Rising; VCCDRx = 5V		8.9	9.3	V
	VCC turn-OFF	VCC Falling; VCCDRx = 5V	7.3	7.7		V
$UVLO_{VCCDR}$	VCCDR turn-ON	VCCDRx Rising; VCC = 12V		4.5	4.8	V
	VCCDR turn-OFF	VCCDRx Falling; VCC = 12V	3.9	4.3		V
$UVLO_{OVP}$	Pre-OVP turn-ON	VCC Rising; VCCDRx = 5V		3.6	3.85	V
	Pre-OVP turn-OFF	VCC Falling; VCCDRx = 5V	3.05	3.3		V
Oscillator and Inhibit						
F_{OSC}	Main Oscillator Accuracy	OSC = OPEN OSC = OPEN; T_J = 0°C to 125°C	135 130	150	165 170	kHz
T_1	SS Delay Time	Intel mode	1			ms
T_2	SS Time T_2	Intel mode; R_{SSOSC} = 25kΩ		500		µs
T_3	SS Time T_3	Intel mode	50			µs
OUTEN	Output enable intel mode	Rising thresholds voltage	0.80	0.85	0.90	V
		Hysteresis		100		mV
	Output enable AMD mode	Input low			0.80	V
		Input high	1.40			V
	Pull-up current			12.5		µA
d_{MAX}	Maximum duty cycle	OSC = OPEN; I_{DROOP} = 0µA		80		%
		OSC = OPEN; I_{DROOP} = 140µA		40		%
ΔV_{OSC}	PWMx ramp amplitude			4		V
FAULT	Voltage at Pin OSC	OVP Active		5		V

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Reference and DAC						
k_{VID}	Output voltage accuracy	Intel mode VID = 1.000V to VID = 1.600V FBR = VOUT; FBG = GNDOUT	-0.5	-	0.5	%
		AMD mode VID=1.000V to VID = 1.550V FBR = VOUT; FBG = GNDOUT	-0.6	-	0.6	%
REF	Reference accuracy	AMD mode; respect VID	-10	-	10	mV
V_{BOOT}	Boot voltage	Intel mode		1.081		V
I_{VID}	VID Pull-up current	Intel mode; VIDx to SGND		25		µA
	VID Pull-down current	AMD mode; VIDx to 5.4V		12.5		µA
VID_{IL}	VID thresholds	Intel mode; Input Low AMD mode; Input Low			0.3 0.8	V
VID_{IH}		Intel mode; Input High AMD mode; Input High	0.8 1.35			V
VID_SEL	VID_SEL threshold (Intel mode)	Input low Input high	 0.8		0.3	V
Error amplifier and remote buffer						
A_0	EA DC gain			80		dB
SR	EA slew rate	COMP = 10pF to SGND		20		V/µs
	RB DC gain			1		V/V
CMRR	Remote buffer common mode rejection ratio			40		dB
Differential current sensing and offset						
I_{CSx+}	Bias current	LS sense Inductor sense		25 0		µA
$\frac{I_{INFOx}-I_{AVG}}{I_{AVG}}$	Current sense mismatch	Rg = 1kΩ; I_{INFOx} = 25µA	-3	-	3	%
I_{OCTH}	Over current threshold	I_{CSx-}(OCP) - I_{CSx-}(0)	30	35	40	µA
k_{IDROOP}	Droop current deviation from nominal value	OFFSET = SGND; Rg = 1kΩ I_{DROOP} = 0 to 80µA;	-2	-	2	µA
$K_{IOFFSET}$	Offset current accuracy	I_{OFFSET} = 50µA to 250µA	-8	-	8	%
I_{OFFSET}	OFFSET current range		0		250	µA
V_{OFFSET}	OFFSET pin bias	I_{OFFSET} = 0 to 250µA		1.240		V

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Gate drivers						
t_{RISE_UGATEx}	HS rise time	BOOTx - PHASEx = 10V; C_{UGATEx} to PHASEx = 3.3nF		15	30	ns
I_{UGATEx}	HS source current	BOOTx - PHASEx = 10V		2		A
R_{UGATEx}	HS sink resistance	BOOTx - PHASEx = 12V	1.5	2	2.5	Ω
t_{RISE_LGATEx}	LS rise time	VCCDRx = 10V; C_{LGATEx} to PGNDx = 5.6nF		30	55	ns
I_{LGATEx}	LS source current	VCCDRx = 10V		1.8		A
R_{LGATEx}	LS sink resistance	VCCDRx = 12V	0.7	1.1	1.5	Ω
Protections						
OVP	Over voltage protection (VSEN Rising)	Intel mode; before V_{BOOT}			1.300	V
		Intel mode; above VID	100	150	200	mV
		AMD mode	1.700	1.740	1.780	V
Program-mable OVP	I_{OVP} current	OVP = SGND	11.5	12.5	13.5	µA
	Comparator offset voltage	OVP = 1.8V	-50	0	50	mV
Pre-OVP	Preliminary over voltage protection	$UVLO_{OVP}$ < VCC < $UVLO_{VCC}$ VCC > $UVLO_{VCC}$ & OUTEN = SGND		1.800		V
		Hysteresis		350		mV
UVP	Under voltage protection	VSEN falling; below VID		-750		mV
PGOOD	PGOOD threshold	AMD mode; VSEN falling; below VID		-300		mV
$V_{SSEND/PGOOD}$	SSEND / PGOOD Voltage low	I = -4mA			0.4	V
Thermal Monitor						
V_{TM}	TM Warning (VR_FAN)	V_{TM} rising		3.2		V
	TM Alarm (VR_HOT)	V_{TM} rising		3.6		V
	TM Hysteresis			100		mV
V_{VR_HOT}; V_{VR_FAN}	VR_HOT voltage low; VR_FAN voltage low	I = -4mA			0.4 0.4	V V

5 VID Tables

5.1 Mapping for the Intel VR11 mode

Table 5. Voltage Identification (VID) Mapping for Intel VR11 Mode

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
800mV	400mV	200mV	100mV	50mV	25mV	12.5mV	6.25mV

5.2 Voltage Identification (VID) for Intel VR11 mode

Table 6. Voltage Identification (VID) for Intel VR11 mode (See Note).

HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)
0	0	OFF	4	0	1.21250	8	0	0.81250	C	0	0.41250
0	1	OFF	4	1	1.20625	8	1	0.80625	C	1	0.40625
0	2	1.60000	4	2	1.20000	8	2	0.80000	C	2	0.40000
0	3	1.59375	4	3	1.19375	8	3	0.79375	C	3	0.39375
0	4	1.58750	4	4	1.18750	8	4	0.78750	C	4	0.38750
0	5	1.58125	4	5	1.18125	8	5	0.78125	C	5	0.38125
0	6	1.57500	4	6	1.17500	8	6	0.77500	C	6	0.37500
0	7	1.56875	4	7	1.16875	8	7	0.76875	C	7	0.36875
0	8	1.56250	4	8	1.16250	8	8	0.76250	C	8	0.36250
0	9	1.55625	4	9	1.15625	8	9	0.75625	C	9	0.35625
0	A	1.55000	4	A	1.15000	8	A	0.75000	C	A	0.35000
0	B	1.54375	4	B	1.14375	8	B	0.74375	C	B	0.34375
0	C	1.53750	4	C	1.13750	8	C	0.73750	C	C	0.33750
0	D	1.53125	4	D	1.13125	8	D	0.73125	C	D	0.33125
0	E	1.52500	4	E	1.12500	8	E	0.72500	C	E	0.32500
0	F	1.51875	4	F	1.11875	8	F	0.71875	C	F	0.31875
1	0	1.51250	5	0	1.11250	9	0	0.71250	D	0	0.31250
1	1	1.50625	5	1	1.10625	9	1	0.70625	D	1	0.30625
1	2	1.50000	5	2	1.10000	9	2	0.70000	D	2	0.30000
1	3	1.49375	5	3	1.09375	9	3	0.69375	D	3	0.29375
1	4	1.48750	5	4	1.08750	9	4	0.68750	D	4	0.28750
1	5	1.48125	5	5	1.08125	9	5	0.68125	D	5	0.28125
1	6	1.47500	5	6	1.07500	9	6	0.67500	D	6	0.27500

Table 6. Voltage Identification (VID) for Intel VR11 mode (See Note).

HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)
1	7	1.46875	5	7	1.06875	9	7	0.66875	D	7	0.26875
1	8	1.46250	5	8	1.06250	9	8	0.66250	D	8	0.26250
1	9	1.45625	5	9	1.05625	9	9	0.65625	D	9	0.25625
1	A	1.45000	5	A	1.05000	9	A	0.65000	D	A	0.25000
1	B	1.44375	5	B	1.04375	9	B	0.64375	D	B	0.24375
1	C	1.43750	5	C	1.03750	9	C	0.63750	D	C	0.23750
1	D	1.43125	5	D	1.03125	9	D	0.63125	D	D	0.23125
1	E	1.42500	5	E	1.02500	9	E	0.62500	D	E	0.22500
1	F	1.41875	5	F	1.01875	9	F	0.61875	D	F	0.21875
2	0	1.41250	6	0	1.01250	A	0	0.61250	E	0	0.21250
2	1	1.40625	6	1	1.00625	A	1	0.60625	E	1	0.20625
2	2	1.40000	6	2	1.00000	A	2	0.60000	E	2	0.20000
2	3	1.39375	6	3	0.99375	A	3	0.59375	E	3	0.19375
2	4	1.38750	6	4	0.98750	A	4	0.58750	E	4	0.18750
2	5	1.38125	6	5	0.98125	A	5	0.58125	E	5	0.18125
2	6	1.37500	6	6	0.97500	A	6	0.57500	E	6	0.17500
2	7	1.36875	6	7	0.96875	A	7	0.56875	E	7	0.16875
2	8	1.36250	6	8	0.96250	A	8	0.56250	E	8	0.16250
2	9	1.35625	6	9	0.95625	A	9	0.55625	E	9	0.15625
2	A	1.35000	6	A	0.95000	A	A	0.55000	E	A	0.15000
2	B	1.34375	6	B	0.94375	A	B	0.54375	E	B	0.14375
2	C	1.33750	6	C	0.93750	A	C	0.53750	E	C	0.13750
2	D	1.33125	6	D	0.93125	A	D	0.53125	E	D	0.13125
2	E	1.32500	6	E	0.92500	A	E	0.52500	E	E	0.12500
2	F	1.31875	6	F	0.91875	A	F	0.51875	E	F	0.11875
3	0	1.31250	7	0	0.91250	B	0	0.51250	F	0	0.11250
3	1	1.30625	7	1	0.90625	B	1	0.50625	F	1	0.10625
3	2	1.30000	7	2	0.90000	B	2	0.50000	F	2	0.10000
3	3	1.29375	7	3	0.89375	B	3	0.49375	F	3	0.09375
3	4	1.28750	7	4	0.88750	B	4	0.48750	F	4	0.08750
3	5	1.28125	7	5	0.88125	B	5	0.48125	F	5	0.08125
3	6	1.27500	7	6	0.87500	B	6	0.47500	F	6	0.07500
3	7	1.26875	7	7	0.86875	B	7	0.46875	F	7	0.06875

Table 6. Voltage Identification (VID) for Intel VR11 mode (See Note).

HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)	HEX Code		Output voltage (1)
3	8	1.26250	7	8	0.86250	B	8	0.46250	F	8	0.06250
3	9	1.25625	7	9	0.85625	B	9	0.45625	F	9	0.05625
3	A	1.25000	7	A	0.85000	B	A	0.45000	F	A	0.05000
3	B	1.24375	7	B	0.84375	B	B	0.44375	F	B	0.04375
3	C	1.23750	7	C	0.83750	B	C	0.43750	F	C	0.03750
3	D	1.23125	7	D	0.83125	B	D	0.43125	F	D	0.03125
3	E	1.22500	7	E	0.82500	B	E	0.42500	F	E	OFF
3	F	1.21875	7	F	0.81875	B	F	0.41875	F	F	OFF

1. According to VR11 specs, the device automatically regulates output voltage 19mV lower to avoid any external offset to modify the built-in 0.5% accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19mV built-in offset.

5.3 Voltage Identifications (VID) for Intel VR10 mode + 6.25mV

(VID7 does not care)

Table 7. Voltage identifications (VID) for Intel VR10 mode + 6.25mV (See Note).

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
0	1	0	1	0	1	1	1.60000	1	1	0	1	0	1	1	1.20000
0	1	0	1	0	1	0	1.59375	1	1	0	1	0	1	0	1.19375
0	1	0	1	1	0	1	1.58750	1	1	0	1	1	0	1	1.18750
0	1	0	1	1	0	0	1.58125	1	1	0	1	1	0	0	1.18125
0	1	0	1	1	1	1	1.57500	1	1	0	1	1	1	1	1.17500
0	1	0	1	1	1	0	1.56875	1	1	0	1	1	1	0	1.16875
0	1	1	0	0	0	1	1.56250	1	1	1	0	0	0	1	1.16250
0	1	1	0	0	0	0	1.55625	1	1	1	0	0	0	0	1.15625
0	1	1	0	0	1	1	1.55000	1	1	1	0	0	1	1	1.15000
0	1	1	0	0	1	0	1.54375	1	1	1	0	0	1	0	1.14375
0	1	1	0	1	0	1	1.53750	1	1	1	0	1	0	1	1.13750
0	1	1	0	1	0	0	1.53125	1	1	1	0	1	0	0	1.13125
0	1	1	0	1	1	1	1.52500	1	1	1	0	1	1	1	1.12500
0	1	1	0	1	1	0	1.51875	1	1	1	0	1	1	0	1.11875
0	1	1	1	0	0	1	1.51250	1	1	1	1	0	0	1	1.11250
0	1	1	1	0	0	0	1.50625	1	1	1	1	0	0	0	1.10625

Table 7. Voltage identifications (VID) for Intel VR10 mode + 6.25mV (See Note).

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
0	1	1	1	0	1	1	1.50000	1	1	1	1	0	1	1	1.10000
0	1	1	1	0	1	0	1.49375	1	1	1	1	0	1	0	1.09375
0	1	1	1	1	0	1	1.48750	1	1	1	1	1	0	1	OFF
0	1	1	1	1	0	0	1.48125	1	1	1	1	1	0	0	OFF
0	1	1	1	1	1	1	1.47500	1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	0	1.46875	1	1	1	1	1	1	0	OFF
1	0	0	0	0	0	1	1.46250	0	0	0	0	0	0	1	1.08750
1	0	0	0	0	0	0	1.45625	0	0	0	0	0	0	0	1.08125
1	0	0	0	0	1	1	1.45000	0	0	0	0	0	1	1	1.07500
1	0	0	0	0	1	0	1.44375	0	0	0	0	0	1	0	1.06875
1	0	0	0	1	0	1	1.43750	0	0	0	0	1	0	1	1.06250
1	0	0	0	1	0	0	1.43125	0	0	0	0	1	0	0	1.05625
1	0	0	0	1	1	1	1.42500	0	0	0	0	1	1	1	1.05000
1	0	0	0	1	1	0	1.41875	0	0	0	0	1	1	0	1.04375
1	0	0	1	0	0	1	1.41250	0	0	0	1	0	0	1	1.03750
1	0	0	1	0	0	0	1.40625	0	0	0	1	0	0	0	1.03125
1	0	0	1	0	1	1	1.40000	0	0	0	1	0	1	1	1.02500
1	0	0	1	0	1	0	1.39375	0	0	0	1	0	1	0	1.01875
1	0	0	1	1	0	1	1.38750	0	0	0	1	1	0	1	1.01250
1	0	0	1	1	0	0	1.38125	0	0	0	1	1	0	0	1.00625
1	0	0	1	1	1	1	1.37500	0	0	0	1	1	1	1	1.00000
1	0	0	1	1	1	0	1.36875	0	0	0	1	1	1	0	0.99375
1	0	1	0	0	0	1	1.36250	0	0	1	0	0	0	1	0.98750
1	0	1	0	0	0	0	1.35625	0	0	1	0	0	0	0	0.98125
1	0	1	0	0	1	1	1.35000	0	0	1	0	0	1	1	0.97500
1	0	1	0	0	1	0	1.34375	0	0	1	0	0	1	0	0.96875
1	0	1	0	1	0	1	1.33750	0	0	1	0	1	0	1	0.96250
1	0	1	0	1	0	0	1.33125	0	0	1	0	1	0	0	0.95625
1	0	1	0	1	1	1	1.32500	0	0	1	0	1	1	1	0.95000
1	0	1	0	1	1	0	1.31875	0	0	1	0	1	1	0	0.94375
1	0	1	1	0	0	1	1.31250	0	0	1	1	0	0	1	0.93750
1	0	1	1	0	0	0	1.30625	0	0	1	1	0	0	0	0.93125
1	0	1	1	0	1	1	1.30000	0	0	1	1	0	1	1	0.92500

Table 7. Voltage identifications (VID) for Intel VR10 mode + 6.25mV (See Note).

VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)	VID 4	VID 3	VID 2	VID 1	VID 0	VID 5	VID 6	Output voltage (1)
1	0	1	1	0	1	0	1.29375	0	0	1	1	0	1	0	0.91875
1	0	1	1	1	0	1	1.28750	0	0	1	1	1	0	1	0.91250
1	0	1	1	1	0	0	1.28125	0	0	1	1	1	0	0	0.90625
1	0	1	1	1	1	1	1.27500	0	0	1	1	1	1	1	0.90000
1	0	1	1	1	1	0	1.26875	0	0	1	1	1	1	0	0.89375
1	1	0	0	0	0	1	1.26250	0	1	0	0	0	0	1	0.88750
1	1	0	0	0	0	0	1.25625	0	1	0	0	0	0	0	0.88125
1	1	0	0	0	1	1	1.25000	0	1	0	0	0	1	1	0.87500
1	1	0	0	0	1	0	1.24375	0	1	0	0	0	1	0	0.86875
1	1	0	0	1	0	1	1.23750	0	1	0	0	1	0	1	0.86250
1	1	0	0	1	0	0	1.23125	0	1	0	0	1	0	0	0.85625
1	1	0	0	1	1	1	1.22500	0	1	0	0	1	1	1	0.85000
1	1	0	0	1	1	0	1.21875	0	1	0	0	1	1	0	0.84375
1	1	0	1	0	0	1	1.21250	0	1	0	1	0	0	1	0.83750
1	1	0	1	0	0	0	1.20625	0	1	0	1	0	0	0	0.83125

1. According to VR10.x specs, the device automatically regulates output voltage 19mV lower to avoid any external offset to modify the built-in 0.5% accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19mVbuilt-in offset. VID7 doesn't care.

5.4 Mapping for the AMD 6BIT mode

Table 8. Voltage identifications (VID) mapping for AMD 6BIT mode

VID4	VID3	VID2	VID1	VID0
400mV	200mV	100mV	50mV	25mV

5.5 Voltage identifications (VID) codes for AMD 6BIT mode

Table 9. Voltage identifications (VID) codes for AMD 6BIT mode (See Note).

VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Output Voltage (1)	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Output Voltage (1)
0	0	0	0	0	0	1.5500	1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250	1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000	1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750	1	0	0	0	1	1	0.7250

Table 9. Voltage identifications (VID) codes for AMD 6BIT mode (See Note).

VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Output Voltage (1)	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Output Voltage (1)
0	0	0	1	0	0	1.4500	1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250	1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000	1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750	1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500	1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250	1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000	1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750	1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500	1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250	1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000	1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750	1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500	1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250	1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000	1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750	1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500	1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250	1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000	1	1	0	1	1	0	0.4875
0	1	0	1	1	1	0.9750	1	1	0	1	1	1	0.4750
0	1	1	0	0	0	0.9500	1	1	1	0	0	0	0.4625
0	1	1	0	0	1	0.9250	1	1	1	0	0	1	0.4500
0	1	1	0	1	0	0.9000	1	1	1	0	1	0	0.4375
0	1	1	0	1	1	0.8750	1	1	1	0	1	1	0.4250
0	1	1	1	0	0	0.8500	1	1	1	1	0	0	0.4125
0	1	1	1	0	1	0.8250	1	1	1	1	0	1	0.4000
0	1	1	1	1	0	0.8000	1	1	1	1	1	0	0.3875
0	1	1	1	1	1	0.7750	1	1	1	1	1	1	0.3750

1. VID6 Not Applicable, need to be left unconnected.

6 Reference schematic

Figure 3. Reference schematic - Intel VR10.x, VR11 inductor sense

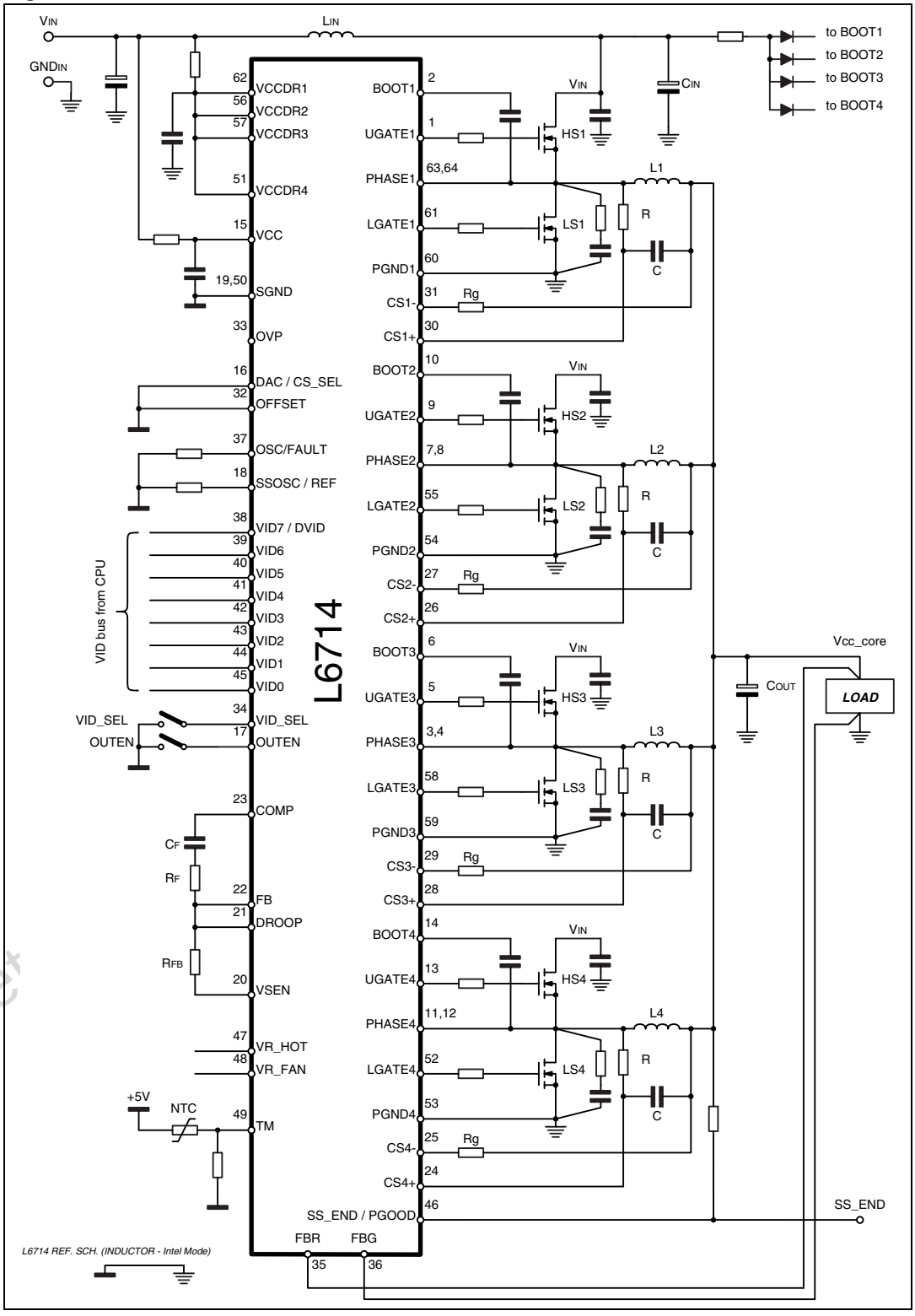


Figure 4. Reference schematic - Intel VR10.x, VR11 LS MOSFET sense

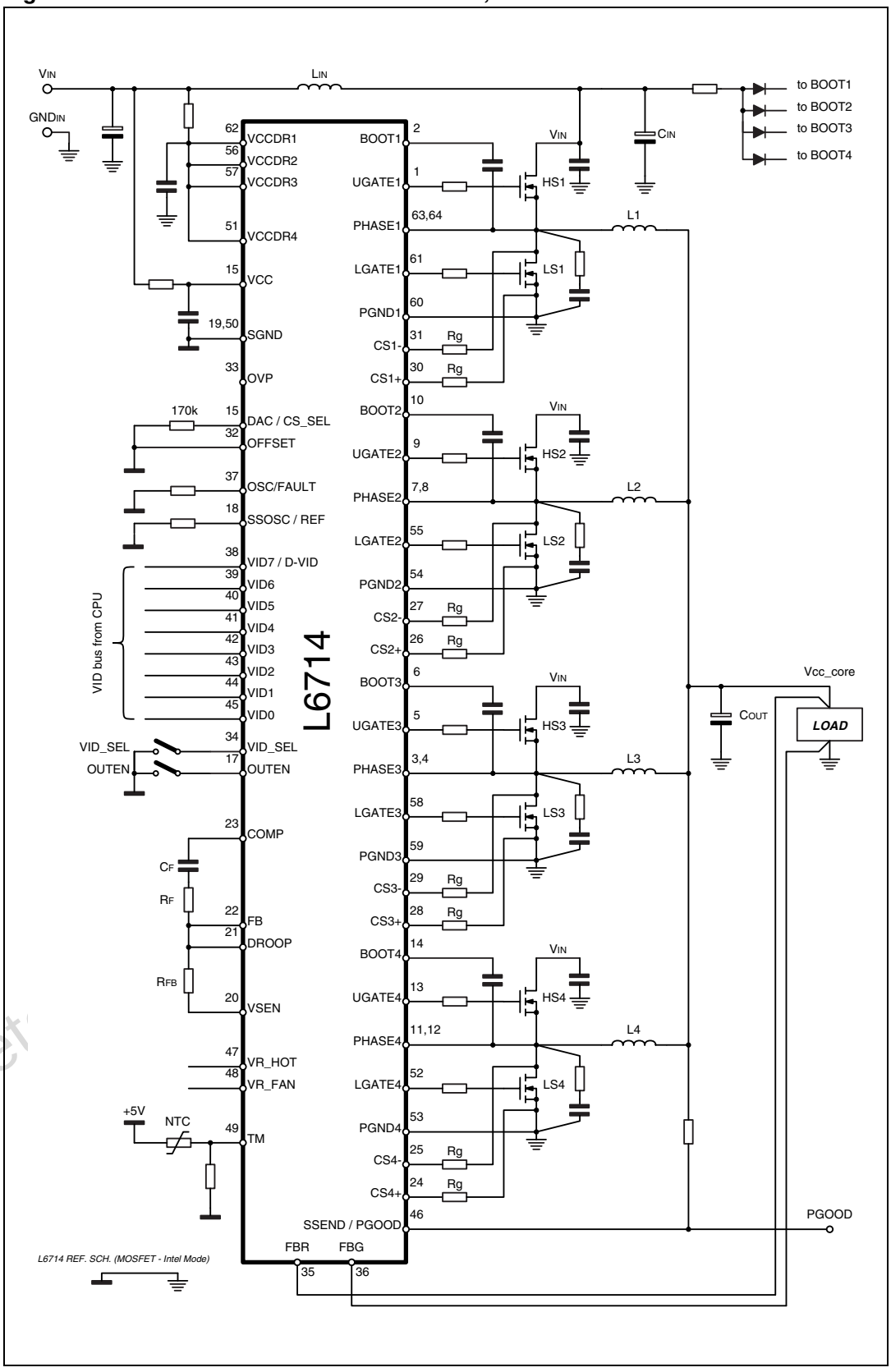


Figure 5. Reference schematic - AMD 6BIT inductor sense