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L6716

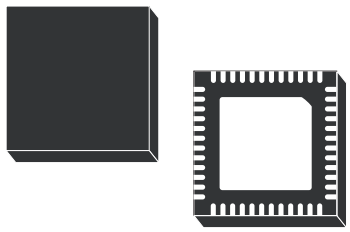
2/3/4 phase controller with embedded drivers for Intel® VR11.1

Features

- Load transient boost LTB Technology™ to minimize the number of output capacitors
- 2 or 3-phase operation with internal driver
- 4-phase operation with external PWM driver signal
- PSI input with programmable strategy
- Imon output
- 0.5% output voltage accuracy
- 8-bit programmable output up to 1.60000 V - Intel VR11.1 DAC - backward compatible with VR10/VR11
- Full differential current sense across inductor
- Differential remote voltage sensing
- Adjustable voltage offset
- LSLess startup to manage pre-biased output
- Feedback disconnection protection
- Preliminary overvoltage protection
- Programmable overcurrent protection
- Programmable overvoltage protection
- Adjustable switching frequency
- SS_END and OUTEN signal
- VFQFPN-48 7x7 mm package with exposed pad

Applications

- High current VRM/VRD for desktop / server / workstation CPUs
- High density DC/DC converters



VFQFPN-48 - 7 x 7 mm

Description

The device implements a two-to-four phases step-down controller with three integrated high current drivers in a compact 7x7 mm body package with exposed pad.

Load transient boost LTB Technology™ reduces system cost by providing the fastest response to load transition therefore requiring less bulk and ceramic output capacitors to satisfy load transient requirements.

The device embeds VR11.x DACs: the output voltage ranges up to 1.60000 V managing D-VID with ±0.5% output voltage accuracy over line and temperature variations.

The controller assures fast protection against load overcurrent and under / overvoltage (in this last case also before UVLO). Feedback disconnection prevents from damaging the load in case of disconnections in the system board.

In case of overcurrent, the system works in constant current mode until UVP.

Table 1. Device summary

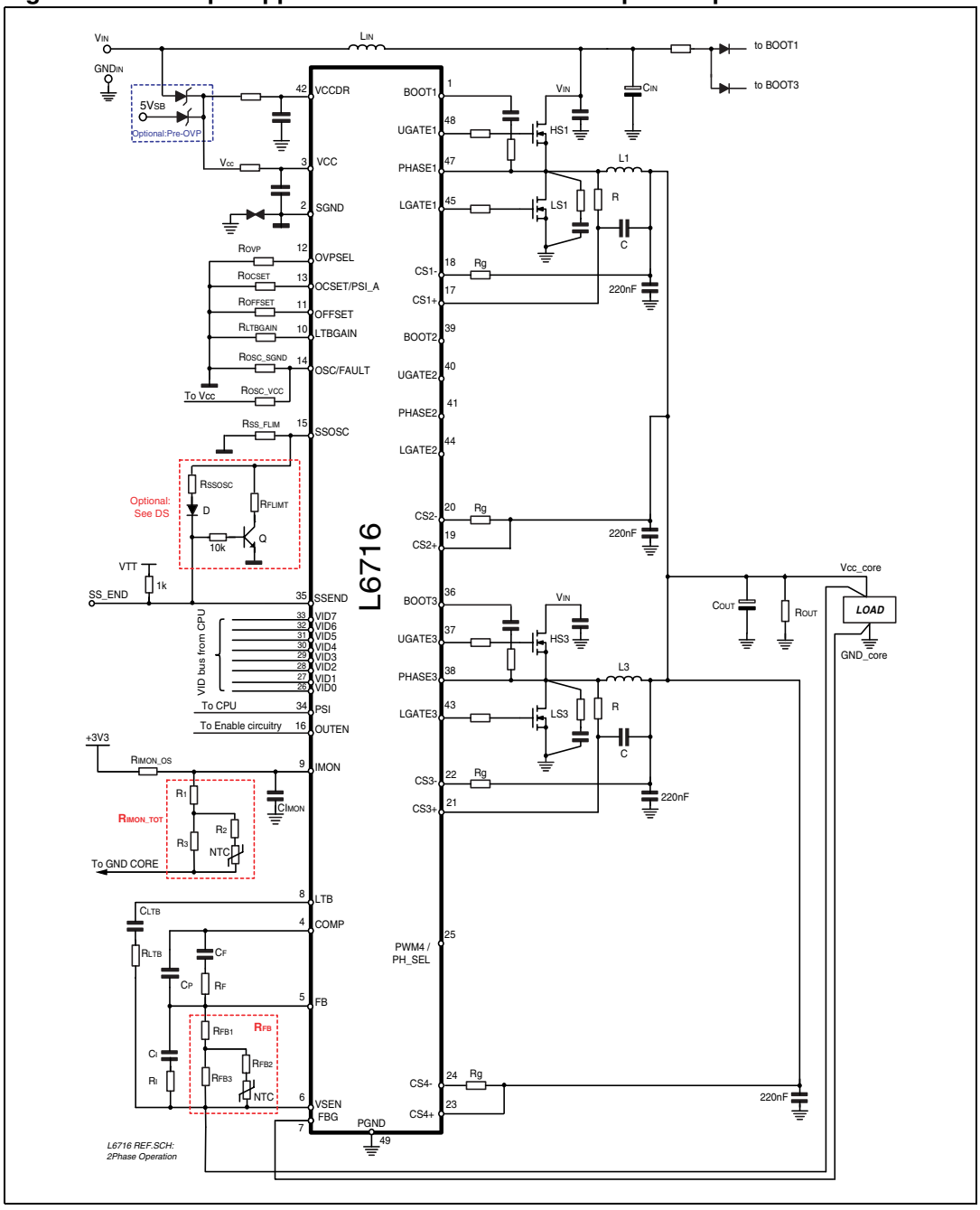
Order codes	Package	Packing
L6716	VFQFPN-48	Tray
L6716TR		Tape and reel

Contents

1 Principle application circuit and block diagram

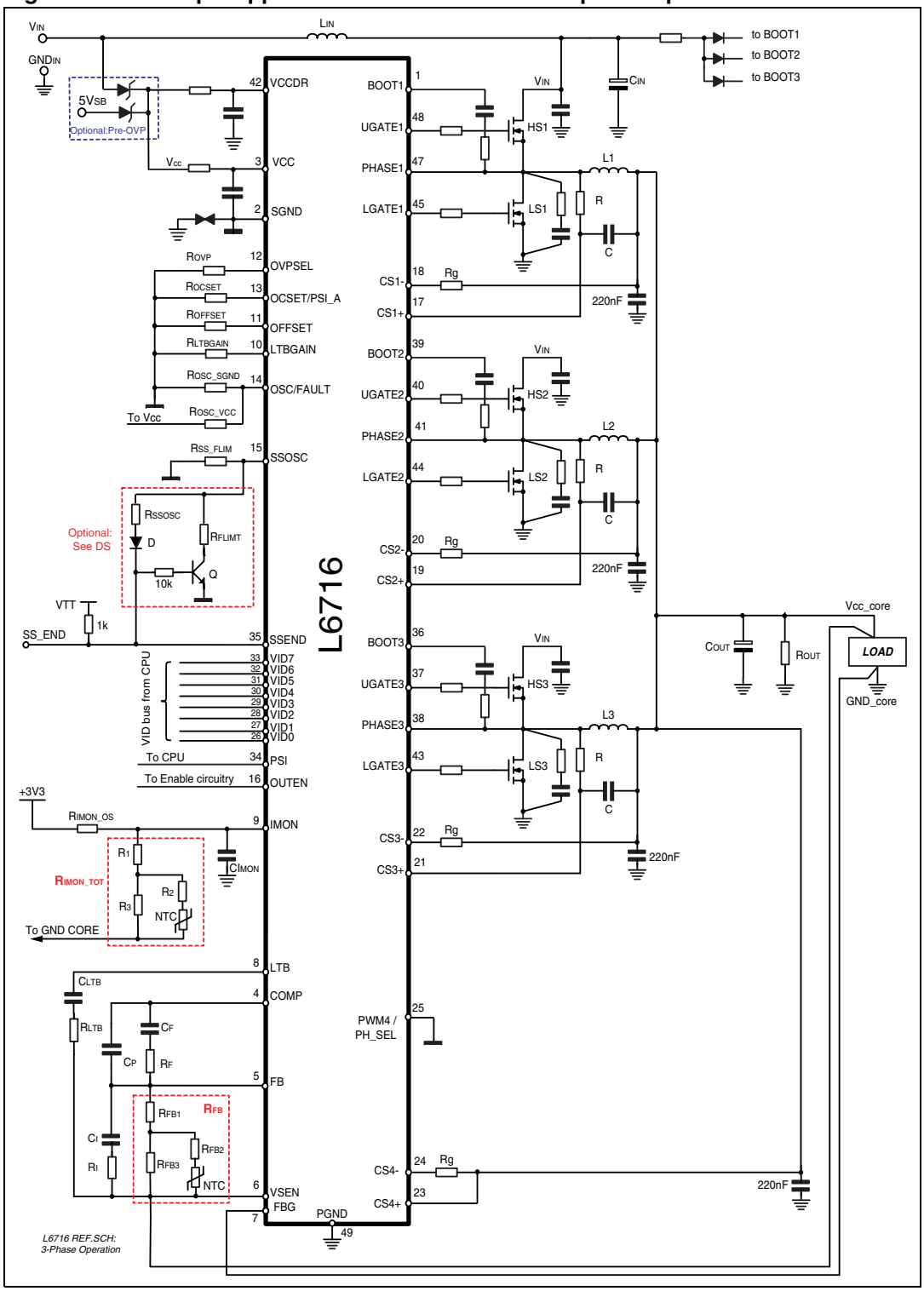
1.1 Principle application circuit

Figure 1. Principle application circuit for VR11.1 - 2 phase operation (a)



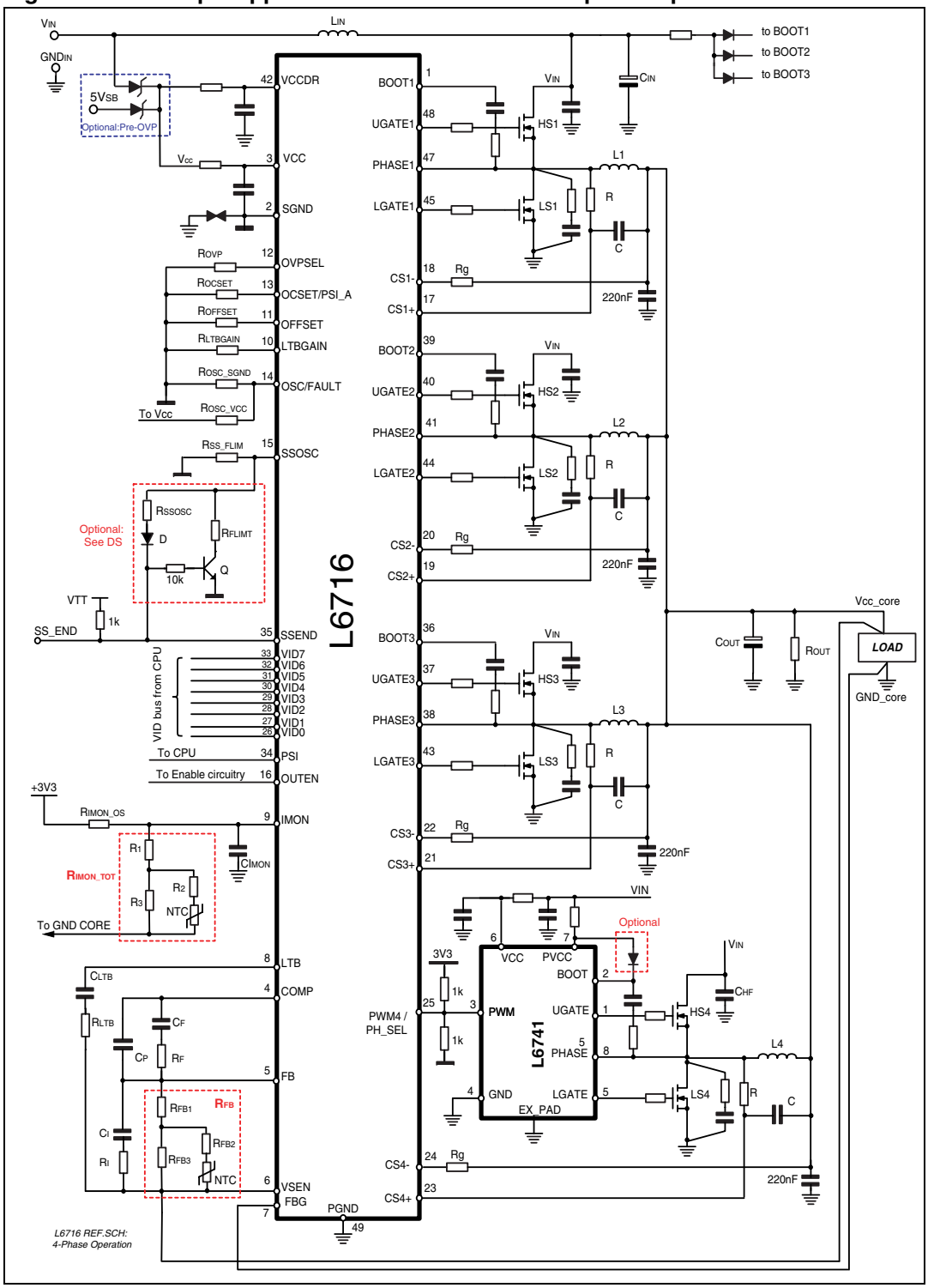
a. Refer to the application note for the reference schematic.

Figure 2. Principle application circuit for VR11.1- 3 phase operation (b)



b. Refer to the application note for the reference schematic.

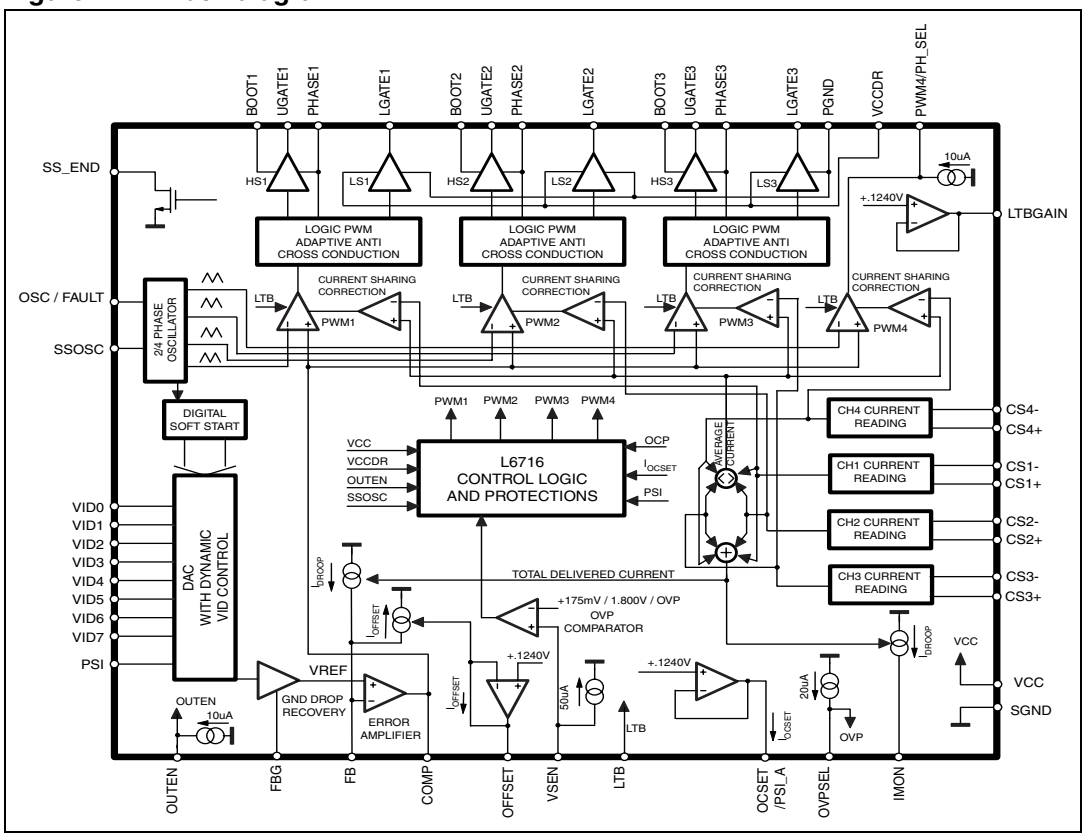
Figure 3. Principle application circuit for VR11.1- 4 phase operation (c)



c. Refer to the application note for the reference schematic.

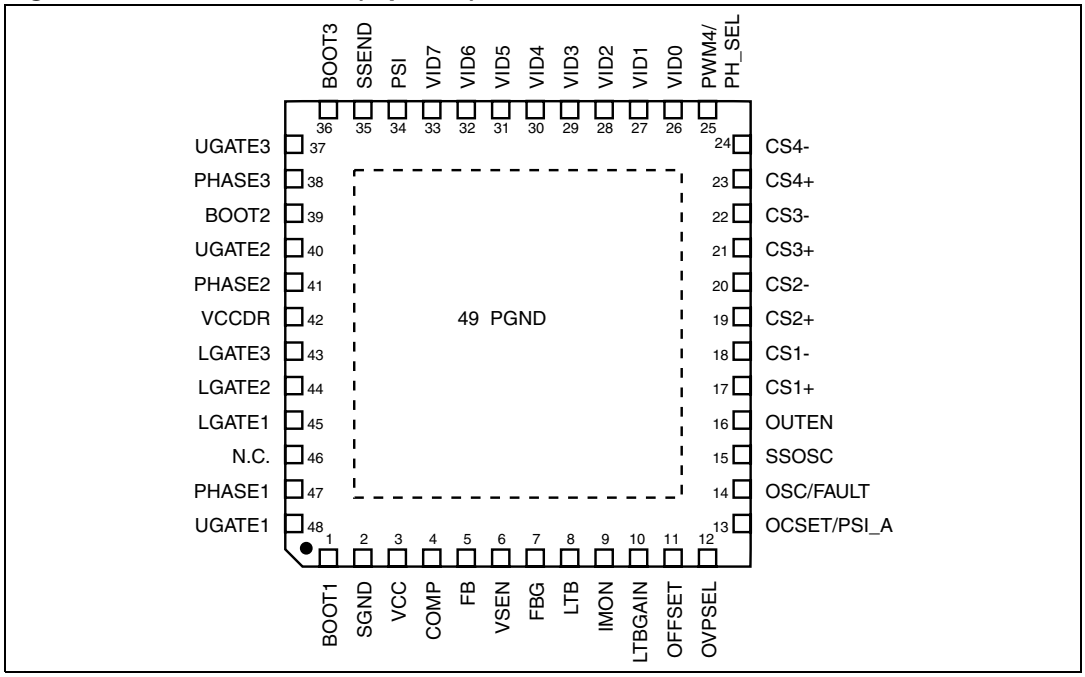
1.2 Block diagram

Figure 4. Block diagram



2 Pin description and connection diagram

Figure 5. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

N°	Name	Description
1	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE1 and provide necessary bootstrap diode. A small resistor in series to the boot diode helps in reducing boot capacitor overcharge.
2	SGND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
3	VCC	Device supply voltage pin. The operative supply voltage is 12 V ±15%. Filter with at least 1 µF capacitor vs. SGND.
4	COMP	Error amplifier output. Connect with an R_F - C_F//C_P vs. FB pin. The device cannot be disabled by pulling down this pin.
5	FB	Error amplifier inverting input pin. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F//C_P vs. COMP pin. A current proportional to the load current is sourced from this pin in order to implement the Droop effect. *See "Droop function" Section* for details.
6	VSEN	Output voltage monitor, manages OVP/UVP protections and FB disconnection. Connect to the positive side of the load to perform remote sense. *See "Layout guidelines" Section* for proper layout of this connection.
7	FBG	Connect to the negative side of the load to perform remote sense. *See "Layout guidelines" Section* for proper layout of this connection.

Table 2. Pin description (continued)

N°	Name	Description
8	LTB	Load transient boost pin. Internally fixed at 2 V, connecting a R_{LTB} - C_{LTB} vs. V_{OUT} allows to enable the load transient boost technology™: as soon as the device detects a transient load it turns on all the PHASEs at the same time. Short to SGND to disable the function. *See "Load transient boost technology" Section* for details.
9	IMON	Current monitor output pin. A current proportional to the load current is sourced from this pin. Connect through a resistor R_{MON} to FBG to implement a load indicator. Connect the load indicator directly to VR11.1 CPUs.The pin voltage is clamped to 1.1 V max to preserve the CPU from excessive voltages.
10	LTBGAIN	Load transient boost technology™ gain pin. Internally fixed at 1.24 V, connecting a $R_{LTBGAIN}$ resistor vs SGND allows setting the gain of the LTB action. See *See "Load transient boost technology" Section* for details.
11	OFFSET	Offset programming pin. Internally fixed at 1.240 V, connecting a R_{OFFSET} resistor vs. SGND allows setting a current that is mirrored into FB pin in order to program a positive offset according to the selected R_{FB}. Short to SGND to disable the function. *See "Offset (optional)" Section* for details.
12	OVPSEL	Overvoltage programming pin. Internally pulled up by 20 µA (typ) to 3.3 V. Leave floating to use built-in protection thresholds (OVP_{TH} = VID + 175 mV typ). Connect to SGND through a R_{OVP} resistor and filter with 100 pF (max) to set the OVP threshold to a fixed voltage according to the R_{OVP} resistor. *See "Overvoltage and programmable OVP" Section* for details. Connect to SGND to select VR10/VR11 table. In this case the OVP threshold becomes 1.800 V (typ).
13	OCSET/ PSI_A	Overcurrent setting, PSI action pin. Connect to SGND through a R_{OCSET} resistor to set the OCP threshold for each phase. It also allows to select the number of phase when PSI mode is selected. *See "Overcurrent protection" Section* for details.
14	OSC/ FAULT	Oscillator, FAULT pin. It allows programming the switching frequency F_{SW} of each channel: the equivalent switching frequency at the load side results in being multiplied by the phase number N. Frequency is programmed according to the resistor connected from the pin vs. SGND or VCC with a gain of 9.1 kHz/µA (see relevant section for details). Leaving the pin floating programs a switching frequency of 200 kHz per phase. The pin is forced high (3.3 V typ) to signal an OVP/UVP fault: to recover from this condition, cycle VCC or the OUTEN pin. *See "Oscillator" Section* for details.
15	SSOSC	Soft-start oscillator pin. By connecting a resistor R_{SS} to GND, it allows programming the soft-start time. Soft-Start time T_{SS} will proportionally change with a gain of 25 [µs / kΩ]. The same slope implemented to reach V_{BOOT} has to be considered also when the reference moves from V_{BOOT} to the programmed VID code. The pin is kept to a fixed 1.240 V. *See "Soft-start" Section* for details.

Table 2. Pin description (continued)

N°	Name	Description
16	OUTEN	Output enable pin. Internally pulled up by 10 µA (typ) to 3 V. Forced low, the device stops operations with all MOSFETs OFF: all the protections are disabled except for preliminary overvoltage. Leave floating, the device starts-up implementing soft-start up to the selected VID code. Cycle this pin to recover latch from protections; filter with 1 nF (typ) vs. SGND.
17	CS1+	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor. *See "Layout guidelines" Section* for proper layout of this connection.
18	CS1-	Channel 1 current sense negative input. Connect through a Rg resistor to the output-side of the channel 1 inductor. *See "Layout guidelines" Section* for proper layout of this connection.
19	CS2+	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. Short to V_{OUT} when using 2-phase operation. *See "Layout guidelines" Section* for proper layout of this connection.
20	CS2-	Channel 2 current sense negative input. Connect through a Rg resistor to the output-side of the channel 2 inductor. Still connect to V_{OUT} through Rg resistor when using 2-phase operation. *See "Layout guidelines" Section* for proper layout of this connection.
21	CS3+	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. *See "Layout guidelines" Section* for proper layout of this connection.
22	CS3-	Channel 3 current sense negative input. Connect through a Rg resistor to the output-side of the channel 3 inductor. *See "Layout guidelines" Section* for proper layout of this connection.
23	CS4+	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. Short to V_{OUT} when using 2-phase or 3-phase operation. *See "Layout guidelines" Section* for proper layout of this connection.
24	CS4-	Channel 4 current sense negative input. Connect through a Rg resistor to the output-side of the channel 4 inductor. Still connect to V_{OUT} through Rg resistor when using 2-phase or 3-phase operation. *See "Layout guidelines" Section* for proper layout of this connection.
25	PWM4/ PH_SEL	PWM outputs, phase selection pin. Internally pulled up by 10 µA to 3.3 V (until the soft-start has not finished), connect to external driver PWM input when 4-phase operation is used. The device is able to manage HiZ status by setting the pis floating. Short to SGND to select 3-phase operation and leave floating to select 2-phase operation.
26 to 33	VID0 to VID7	Voltage identification pins. (not internally pulled up). Connect to SGND to program a '0' or connect to the external pull-up resistor to program a '1'. They allow programming output voltage as specified in *Table 7.*

Table 2. Pin description (continued)

N°	Name	Description
34	PSI	Power saving indicator pin. Connect to the PSI pin of the CPU to manage low-power state. When asserted (pulled low), the controller will act as programmed on the OCSET/PSI_A.
35	SSEND	Soft-start END signal. Open drain output sets free after ss has finished and pulled low when triggering any protection. Pull up to a voltage lower than 3.3 V, if not used it can be left floating.
36	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE3 and provide necessary bootstrap diode.A small resistor in series to the boot diode helps in reducing boot capacitor overcharge.
37	UGATE3	Channel 3HS driver output. It must be connected to the HS3 MOSFET gate. A small series resistors helps in reducing device-dissipated power.
38	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 MOSFET source and provides return path for the HS driver of channel 3.
39	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE2 and provide necessary bootstrap diode. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge. Leave floating when using 2-Phase operation.
40	UGATE2	Channel 2HS driver output. It must be connected to the HS2 MOSFET gate. A small series resistors helps in reducing device-dissipated power. Leave floating when using 2-Phase operation.
41	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 MOSFET source and provides return path for the HS driver of channel 2. Leave floating when using 2-phase operation.
42	VCCDR	LS Driver Supply. VCDDR pin voltage has to be the same of VCC pin. Filter with 2 x 1 µF MLCC capacitor vs. PGND.
43	LGATE3	Channel 3LS driver output. A small series resistor helps in reducing device-dissipated power.
44	LGATE2	Channel 2LS driver output. A small series resistor helps in reducing device-dissipated power. Leave floating when using 2-phase operation.
45	LGATE1	Channel 1LS driver output. A small series resistor helps in reducing device-dissipated power.
46	N.C.	Not internally connected.
47	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.

Table 2. Pin description (continued)

N°	Name	Description
48	UGATE1	Channel 1HS driver output. It must be connected to the HS1 MOSFET gate. A small series resistors helps in reducing device-dissipated power.
49	PGND	Power ground pin (LS drivers return path). Connect to power ground plane. Exposed pad connects also the silicon substrate. As a consequence it makes a good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect it to the power ground plane using 5.2 x 5.2 mm square area on the PCB and with sixteen vias (uniformly distributed), to improve electrical and thermal conductivity.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDR}	To PGND	15	V
V_{BOOTx}- V_{PHASEx}	Boot voltage	15	V
V_{UGATEx}- V_{PHASEx}		15	V
	LGATEx to PGND	-0.3 to Vcc+0.3	V
	All other pins to PGND	-0.3 to 3.6	V
V_{PHASE}	Negative peak voltage to PGND; T < 400 ns VCC = VCCDR = 12 V	-8	V
	Positive voltage to PGND VCC = VCCDR = 12 V	26	V
	Positive peak voltage to PGND; T < 200 ns VCC = VCCDR = 12 V	30	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	+/- 1750	V

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	40	°C / W
T_{MAX}	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-10 to 125	°C
P_{tot}	Max power dissipation at T_A = 25 °C	2.5	W

4 Electrical characteristics

4.1 Electrical characteristics

V_{CC} = 12 V ± 15%, T_J = 0 °C to 70 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	UGATEx and LGATEx open; VCC = VBOOTx = 12 V		22	25	mA
I_{CCDR}	VCCDR supply current	LGATEx = OPEN; VCCDR = 12 V		5	7	mA
I_{BOOTx}	BOOTx supply current	UGATEx = OPEN; PHASEx to PGND; VCC = BOOTx = 12V		1.8	2.7	mA
Power-on						
$UVLO_{VCC}$	VCC turn-ON	VCC rising; VCCDR = VCC		3.7	4.0	V
	VCC turn-OFF	VCC falling; VCCDR = VCC	3.3	3.5		V
$UVLO_{Pre-OVP}$	Pre-OVP turn-ON	VCC rising; VCCDR = VCC		3.7	4.0	V
	Pre-OVP turn-OFF	VCC falling; VCCDR = VCC	3.3	3.5		V
Oscillator and inhibit						
F_{OSC}	Initial accuracy	OSC=OPEN; T_J = 0 to 125 °C	180	200	220	kHz
TD_1	SS delay time		1	1.5		ms
TD_2	SS TD_2 time	R_{SSOSC} = 20 kΩ		500		µs
TD_3	SS TD_3 time		150	250		µs
OUTEN	Output enable	Rising thresholds voltage	0.80	0.85	0.90	V
		Hysteresis		100		mV
	Output pull-up current	OUTEN to SGND		10		µA
ΔVosc	Ramp amplitude			1.5		V
FAULT	Voltage at pin OSC/FAULT	OVP and UVP Active		3.3		V
Reference and DAC						
K_{VID}	Output voltage accuracy	VID = 1.000 V to VID = 1.600 V FB = VOUT; FBG = GNDOUT	-0.5	-	0.5	%
		VID = 0.800 V to VID = 1.000 V FB = VOUT; FBG = GNDOUT	-5	-	+5	mV
		VID = 0.500 V to VID = 0.800 V FB = VOUT; FBG = GNDOUT	-8	-	+8	mV
V_{BOOT}	Boot voltage			1.081		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{VID}	VID pull-up current	VIDx to SGND		0		µA
VID_{IH}	VID thresholds	Input low			0.35	V
VID_{IL}		Input high	0.8			V
PSI	PSI thresholds	Input low			0.4	V
		Input high	0.8			
	PSI pull-up current	PSI to SGND		0		µA
Error amplifier						
A_0	EA DC gain			130		dB
SR	EA slew-rate	COMP = 10 pF to SGND		25		V/µs
Differential current sensing and offset						
I_{CSx+}	Bias current			0		µA
V_{OCSET}	OCSET pin voltage		1.105	1.245	1.385	mV
K_{IDROOP}	Droop current deviation from nominal value	Rg = 1 kΩ; 1-PHASE, I_{DROOP} = 25 µA; 2-PHASE, I_{DROOP} = 50 µA; 3-PHASE, I_{DROOP} = 75 µA; 4-PHASE, I_{DROOP} = 100 µA;	-3	-	+3	µA
$K_{IOFFSET}$	Offset current accuracy	I_{OFFSET} = 50 µA to 250 µA	-5	-	5	%
I_{OFFSET}	OFFSET current range		0		250	µA
V_{OFFSET}	OFFSET pin bias	I_{OFFSET} = 0 to 250 µA		1.240		V
Gate drivers						
$t_{RISE\ UGATE}$	High side rise time	BOOTx-PHASEx = 12 V; C_{UGATEx} to PHASEx = 3.3 nF		20		ns
I_{UGATEx}	High side source current	BOOTx-PHASEx = 12 V		1.5		A
R_{UGATEx}	High side sink resistance	BOOTx-PHASEx = 12 V		2		Ω
$t_{RISE\ LGATE}$	Low side rise time	VCCDR = 12 V; C_{LGATEx} to PGNDx = 5.6 nF		25		ns
I_{LGATEx}	Low side source current	VCCDR = 12 V		2		A
R_{LGATEx}	Low side sink resistance	VCCDR = 12 V		1		Ω
PWM output						
PWM4	Output high	I = 1 mA	3			V
	Output low	I = -1 mA			0.2	V
I_{PWM4}	PWM4 pull-up current	Before SSEND = 1; PWM4 to SGND		10		µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Protections						
OVP	Overvoltage protection (VSEN rising)	Before V_{BOOT}		1.24	1.300	V
		Above VID-19 mV (after TD_3)	150	175	200	mV
Programmable OVP	I_{OVP} current	OVP = SGND	20	22	24	µA
	Comparator offset voltage	OVP = 1.800 V	-20	0	20	mV
Pre- OVP	Preliminary overvoltage protection	$UVLO_{OVP}$ < VCC < $UVLO_{VCC}$ VCC> $UVLO_{VCC}$ and OUTEN = SGND VSEN rising	1.750	1.800	1.850	V
		Hysteresis		350		mV
UVP	Under voltage threshold	VSEN falling; below VID-19 mV	550	600	650	mV
V_{SSEND}	SS_END voltage low	I = -4 mA			0.4	V

5 Voltage identifications

Table 6. Voltage identification (VID) mapping for intel VR11.1 mode

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
800 mV	400 mV	200 mV	100 mV	50 mV	25 mV	12.5 mV	6.25 mV

Table 7. Voltage identification (VID) for Intel VR11.1 mode

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
0	0	OFF	4	0	1.21250	8	0	0.81250	C	0	0.41250
0	1	OFF	4	1	1.20625	8	1	0.80625	C	1	0.40625
0	2	1.60000	4	2	1.20000	8	2	0.80000	C	2	0.40000
0	3	1.59375	4	3	1.19375	8	3	0.79375	C	3	0.39375
0	4	1.58750	4	4	1.18750	8	4	0.78750	C	4	0.38750
0	5	1.58125	4	5	1.18125	8	5	0.78125	C	5	0.38125
0	6	1.57500	4	6	1.17500	8	6	0.77500	C	6	0.37500
0	7	1.56875	4	7	1.16875	8	7	0.76875	C	7	0.36875
0	8	1.56250	4	8	1.16250	8	8	0.76250	C	8	0.36250
0	9	1.55625	4	9	1.15625	8	9	0.75625	C	9	0.35625
0	A	1.55000	4	A	1.15000	8	A	0.75000	C	A	0.35000
0	B	1.54375	4	B	1.14375	8	B	0.74375	C	B	0.34375
0	C	1.53750	4	C	1.13750	8	C	0.73750	C	C	0.33750
0	D	1.53125	4	D	1.13125	8	D	0.73125	C	D	0.33125
0	E	1.52500	4	E	1.12500	8	E	0.72500	C	E	0.32500
0	F	1.51875	4	F	1.11875	8	F	0.71875	C	F	0.31875
1	0	1.51250	5	0	1.11250	9	0	0.71250	D	0	0.31250
1	1	1.50625	5	1	1.10625	9	1	0.70625	D	1	0.30625
1	2	1.50000	5	2	1.10000	9	2	0.70000	D	2	0.30000
1	3	1.49375	5	3	1.09375	9	3	0.69375	D	3	0.29375
1	4	1.48750	5	4	1.08750	9	4	0.68750	D	4	0.28750
1	5	1.48125	5	5	1.08125	9	5	0.68125	D	5	0.28125
1	6	1.47500	5	6	1.07500	9	6	0.67500	D	6	0.27500
1	7	1.46875	5	7	1.06875	9	7	0.66875	D	7	0.26875
1	8	1.46250	5	8	1.06250	9	8	0.66250	D	8	0.26250
1	9	1.45625	5	9	1.05625	9	9	0.65625	D	9	0.25625

Table 7. Voltage identification (VID) for Intel VR11.1 mode (continued)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
1	A	1.45000	5	A	1.05000	9	A	0.65000	D	A	0.25000
1	B	1.44375	5	B	1.04375	9	B	0.64375	D	B	0.24375
1	C	1.43750	5	C	1.03750	9	C	0.63750	D	C	0.23750
1	D	1.43125	5	D	1.03125	9	D	0.63125	D	D	0.23125
1	E	1.42500	5	E	1.02500	9	E	0.62500	D	E	0.22500
1	F	1.41875	5	F	1.01875	9	F	0.61875	D	F	0.21875
2	0	1.41250	6	0	1.01250	A	0	0.61250	E	0	0.21250
2	1	1.40625	6	1	1.00625	A	1	0.60625	E	1	0.20625
2	2	1.40000	6	2	1.00000	A	2	0.60000	E	2	0.20000
2	3	1.39375	6	3	0.99375	A	3	0.59375	E	3	0.19375
2	4	1.38750	6	4	0.98750	A	4	0.58750	E	4	0.18750
2	5	1.38125	6	5	0.98125	A	5	0.58125	E	5	0.18125
2	6	1.37500	6	6	0.97500	A	6	0.57500	E	6	0.17500
2	7	1.36875	6	7	0.96875	A	7	0.56875	E	7	0.16875
2	8	1.36250	6	8	0.96250	A	8	0.56250	E	8	0.16250
2	9	1.35625	6	9	0.95625	A	9	0.55625	E	9	0.15625
2	A	1.35000	6	A	0.95000	A	A	0.55000	E	A	0.15000
2	B	1.34375	6	B	0.94375	A	B	0.54375	E	B	0.14375
2	C	1.33750	6	C	0.93750	A	C	0.53750	E	C	0.13750
2	D	1.33125	6	D	0.93125	A	D	0.53125	E	D	0.13125
2	E	1.32500	6	E	0.92500	A	E	0.52500	E	E	0.12500
2	F	1.31875	6	F	0.91875	A	F	0.51875	E	F	0.11875
3	0	1.31250	7	0	0.91250	B	0	0.51250	F	0	0.11250
3	1	1.30625	7	1	0.90625	B	1	0.50625	F	1	0.10625
3	2	1.30000	7	2	0.90000	B	2	0.50000	F	2	0.10000
3	3	1.29375	7	3	0.89375	B	3	0.49375	F	3	0.09375
3	4	1.28750	7	4	0.88750	B	4	0.48750	F	4	0.08750
3	5	1.28125	7	5	0.88125	B	5	0.48125	F	5	0.08125
3	6	1.27500	7	6	0.87500	B	6	0.47500	F	6	0.07500
3	7	1.26875	7	7	0.86875	B	7	0.46875	F	7	0.06875
3	8	1.26250	7	8	0.86250	B	8	0.46250	F	8	0.06250
3	9	1.25625	7	9	0.85625	B	9	0.45625	F	9	0.05625
3	A	1.25000	7	A	0.85000	B	A	0.45000	F	A	0.05000
3	B	1.24375	7	B	0.84375	B	B	0.44375	F	B	0.04375

Table 7. Voltage identification (VID) for Intel VR11.1 mode (continued)

HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)	HEX code		Output voltage (1)
3	C	1.23750	7	C	0.83750	B	C	0.43750	F	C	0.03750
3	D	1.23125	7	D	0.83125	B	D	0.43125	F	D	0.03125
3	E	1.22500	7	E	0.82500	B	E	0.42500	F	E	OFF
3	F	1.21875	7	F	0.81875	B	F	0.41875	F	F	OFF

1. According to INTEL specs, the device automatically regulates output voltage 19 mV lower to avoid any external offset to modify the built-in 0.5% accuracy improving TOB performances. Output regulated voltage is than what extracted from the table lowered by 19 mV.

6 Device description

L6716 is two-to-four phase PWM controller with three embedded high current drivers providing complete control logic and protections for a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor power supply. Multi phase buck is the simplest and most cost-effective topology employable to satisfy the increasing current demand of newer microprocessors and modern high current VRM modules. It allows distributing equally load and power between the phases using smaller, cheaper and most common external power MOSFETs and inductors. Moreover, thanks to the equal phase shift between each phase, the input and output capacitor count results in being reduced. Phase interleaving causes in fact input rms current and output ripple voltage reduction.

L6716 is a dual-edge asynchronous PWM controller featuring load transient boost LTB Technology™: the device turns on simultaneously all the phases as soon as a load transient is detected allowing to minimize system cost by providing the fastest response to load transition. Load transition is detected (through LTB pin) measuring the derivate dV/dt of the output voltage and the dV/dt can be easily programmed extending the system design flexibility. Moreover, load transient boost (LTB) Technology™ gain can be easily modified in order to keep under control the output voltage ring back.

LTB Technology™ can be disabled and in this condition the device works as a dual-edge asynchronous PWM.

The controller allows to implement a scalable design: a three phase design can be easily downgraded to two phase and upgraded to four phase (using an external driver).The same design can be used for more than one project saving development and debug time.

L6716 permits easy system design by allowing current reading across inductor in fully differential mode. Also a sense resistor in series to the inductor can be considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase limiting the error in the static and dynamic conditions.

The controller allows compatibility with both Intel VR11.0 and VR11.1 processors specifications, also performing D-VID transitions accordingly.

The device is VR11.1 compatible implementing IMON signal and managing the PSI# signal to enhance the system performances at low current in low-power states.

Low-side-less start-up allows soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side.

L6716 provides a programmable overvoltage protection to protect the load from dangerous over stress, latching immediately by turning ON the lower driver and driving high the OSC/FAULT pin. Furthermore, preliminary OVP protection also allows the device to protect load from dangerous OVP when VCC is not above the UVLO threshold or OUTEN is low. The overcurrent protection is for each phase and externally adjustable through a single resistor. The device keeps constant the peak of the inductor current ripple working in constant current mode until the latched UVP.

A compact 7x7 mm body VFQFPN-48 package with exposed thermal pad allows dissipating the power to drive the external MOSFET through the system board.

7 DAC and Phase number selection

L6716 embeds VRD11.x DAC *(see Table 7)* that allows to regulate the output voltage with a tolerance of ±0.5% recovering from offsets and manufacturing variations.

The device automatically introduces a -19 mV (both VRD11.x and VR10) offset to the regulated voltage in order to avoid any external offset circuitry to worsen the guaranteed accuracy and, as a consequence, the calculated system TOB.

Output voltage is programmed through the VID pins: they are inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the voltage reference (i.e. the set-point of the error amplifier, V_{REF}).

L6716 implements a flexible 2 to 4 interleaved-phase converter. The device allows to select the phase number operation simply using the PWM4/PHASE_SEL pin, as shown in the following table.

Table 8. Number of phases setting

PWM4 / PH_SEL pin	Number of phases	Phases used
Floating	2-PHASE	Phase1, Phase3
Short to SGND	3-PHASE	Phase1, Phase2, Phase3
Connect to PWM driver input	4-PHASE	Phase1, Phase2, Phase3, Phase4

Note: PWM4 pin is internally pulled up by 10 µA to 3.3 V, until soft-start is not finished.

For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSx+ needs to be connected to the regulated output voltage while CSX- needs to be connected to V_{OUT} trough the same R_G resistor used for the other phases.

Note: To select VR10/VR11 table, short to SGND the OVP pin. In this case the PSI pin becomes the VIDSEL pin (to select VR10 and VR11 table, in according to the VR11 specification).

8 Power dissipation

L6716 embeds three high current MOSFET drivers for both high side and low side MOSFETs: it is then important to consider the power the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Exposed pad (PGND pin) needs to be soldered to the PCB power ground plane through several VIAs in order to facilitate the heat dissipation.

Two main terms contribute in the device power dissipation: bias power and drivers' power. The first one (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{CCDR} + N_D \cdot I_{BOOTx})$$

where N_D is the number of internal drivers used.

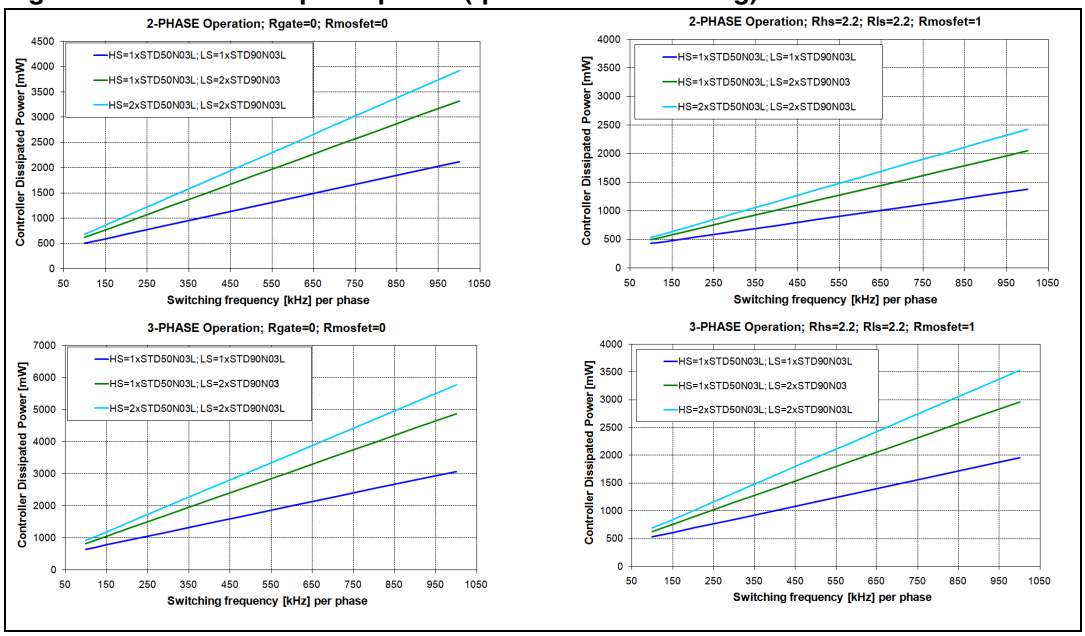
Drivers' power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation.

The total power dissipated to switch the MOSFETs results:

$$P_{SW} = N_D \cdot F_{SW} \cdot (Q_{GHS} \cdot V_{BOOT} + Q_{GLS} \cdot V_{CCDR})$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device. When driving multiple MOSFETs in parallel, it is suggested to use one gate resistor for each MOSFET.

Figure 6. L6716 dissipated power (quiescent + switching)



9 Current reading and current sharing loop

L6716 embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy.

Reading current across the inductor DCR, the current flowing trough each phase is read using the voltage drop across the output inductor or across a sense resistor in its series and internally converted into a current. The trans-conductance ratio is issued by the external resistor Rg placed outside the chip between CSx- pin toward the reading points.

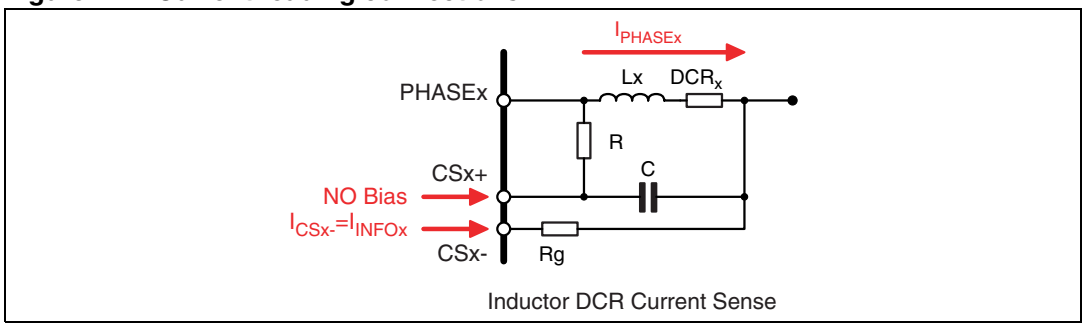
The current sense circuit always tracks the current information, no bias current is sourced from the CSx+ pin: this pin is used as a reference keeping the CSx- pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element.

The current that flows from the CSx- pin is then given by the following equation (see *Figure 7*):

$$I_{CSx-} = \frac{DCR}{Rg} \cdot \frac{1 + s \cdot L/(DCR)}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Where I_{PHASEx} is the current carried by the relative phase.

Figure 7. Current reading connections



Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance), it results:

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSx-} = \frac{DCR}{Rg} \cdot I_{PHASEx} = I_{INFOx} \Rightarrow \quad I_{INFOX} = \frac{DCR}{Rg} \cdot I_{PHASEx}$$

Where I_{INFOx} is the current information reproduced internally.

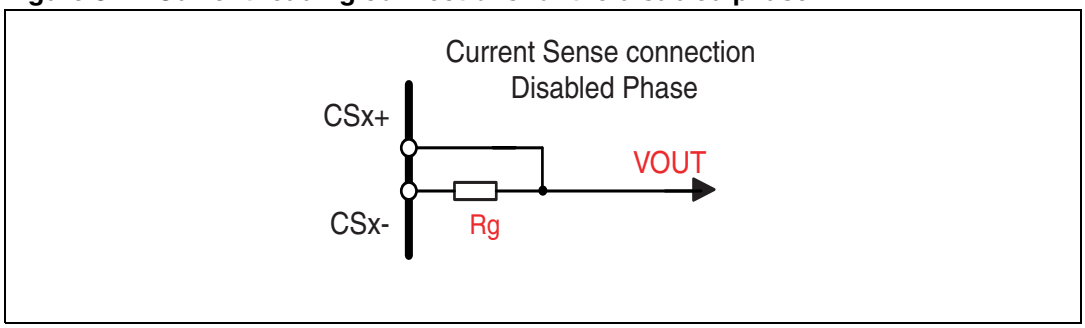
The Rg trans-conductance resistor has to be selected using the following formula, in order to guarantee the correct functionality of internal current reading circuitry:

$$Rg = \frac{DCR^{MAX}}{20\mu A} \cdot \frac{I_{OUT}MAX}{N}$$

Where I_{OUT}^{MAX} is the maximum output current, DCR^{MAX} the maximum inductor DCR and N number of phases.

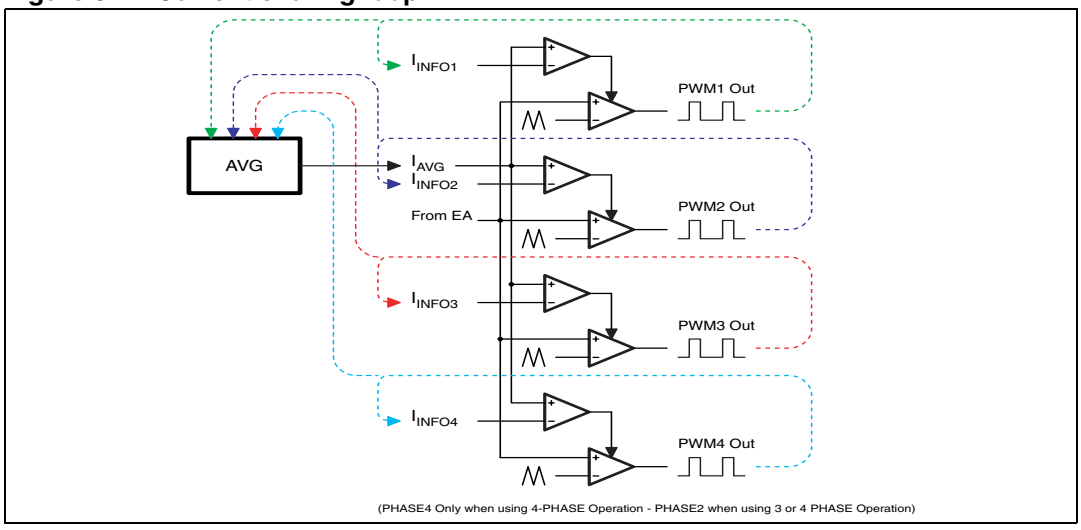
For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSx+ needs to be connected to the regulated output voltage while CSX- needs to be connected to V_{OUT} trough the same R_G resistor used for the other phases, as shown in figure *Figure 9.*

Figure 8. Current reading connections for the disabled phase



Current sharing control loop reported in *Figure 9*: it considers a current I_{INFOx} proportional to the current delivered by each phase and the average current $I_{AVG} = \Sigma I_{INFOx}/N$. The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase. Details about connections are shown in *Figure 9*.

Figure 9. Current sharing loop



10 Differential remote voltage sensing

The output voltage is sensed in fully-differential mode between the FB and FBG pin.

The FB pin has to be connected through a resistor to the regulation point while the FBG pin has to be connected directly to the remote sense ground point.

In this way, the output voltage programmed is regulated between the remote sense point compensating motherboard or connector losses.

Keeping the FB and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 10. Differential remote voltage sensing connections