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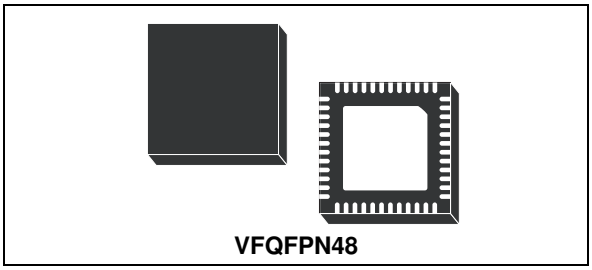
L6717A

High-efficiency hybrid controller with I^{2}C interface and embedded drivers

Datasheet - production data



VFQFPN48

Features

- Hybrid controller for both PVI and SVI CPUs G34 compliant
- Dual controller with embedded high current drivers: 2 phases for CPU CORE + 2 PWM for ext drivers, 1 phase for NB
- Dynamic phase management (DPM)
- I^{2}C interface to control offset, switching frequency and PSI_L
- Dual-edge asynchronous architecture with LTB Technology®
- PSI management to increase efficiency in light-load conditions
- Dual overcurrent protection: total and per-phase compatible with Itdc and IddSpike
- Voltage positioning
- Dual remote sense
- Feedback disconnection protection
- Programmable OV protection
- Oscillator internally fixed at 200 kHz externally adjustable
- LSLess startup to manage pre-biased output
- VFQFPN48 package

Applications

- Hybrid high-current VRM / VRD for desktop / server / workstation / IPC CPUs supporting PVI and SVI interface
- High-density DC-DC converters

Description

L6717A is a hybrid CPU power supply controller embedding 2 high-current drivers for the CORE section and 1 driver for the NB section - requiring up to 2 external drivers when the CORE section works at 4 phase to optimize the application over-all cost.

I^{2}C interface is provided to manage offset for CORE section, switching frequency and dynamic phase management saving in component count and space consumption.

Dynamic phase management automatically adjusts phase-count according to CPU load optimizing the system efficiency under all load conditions.

The dual-edge asynchronous architecture is optimized by LTB technology® allowing fast load-transient response minimizing the output capacitor and reducing the total BOM cost.

Fast protection against load overcurrent is provided for both the sections. Feedback disconnection protection prevents from damaging the load in case of misconnections in the system board. L6717A is available in VFQFPN48 package.

Table 1. Device summary

Order codes	Package	Packing
L6717A	VFQFPN48	Tray
L6717ATR		Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical 4+1 application circuit

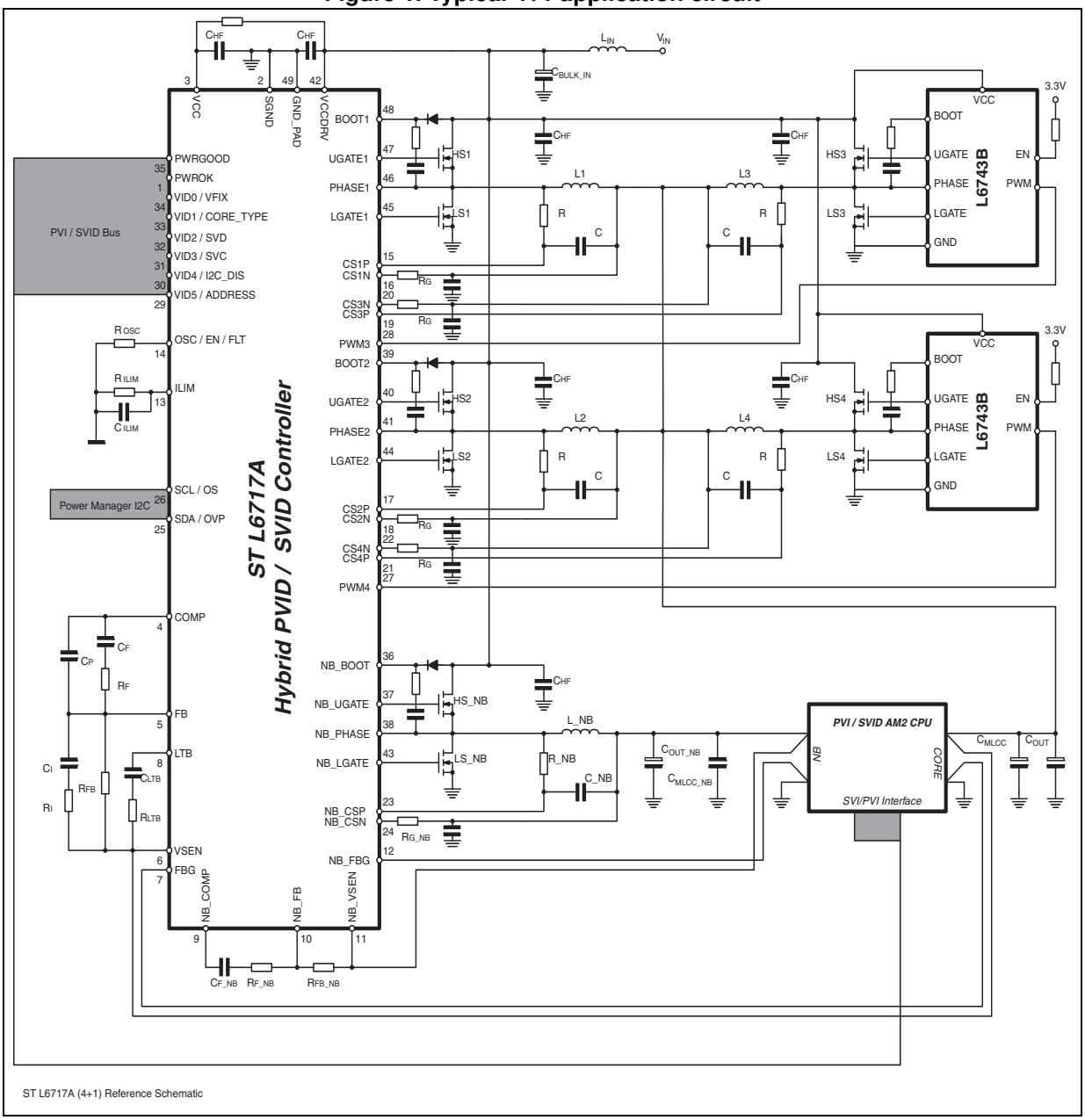


Figure 2. Typical 3+1 application circuit

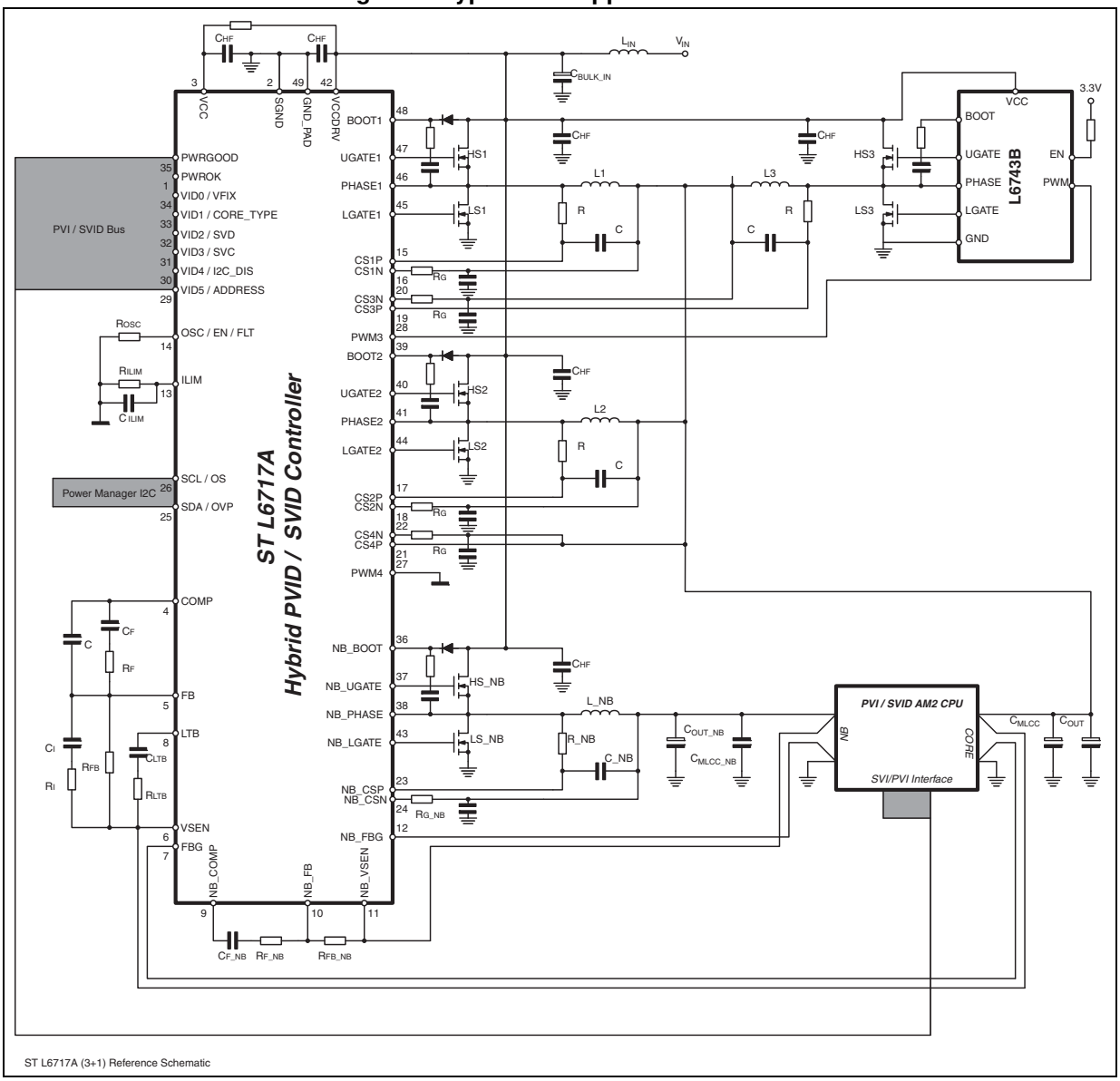
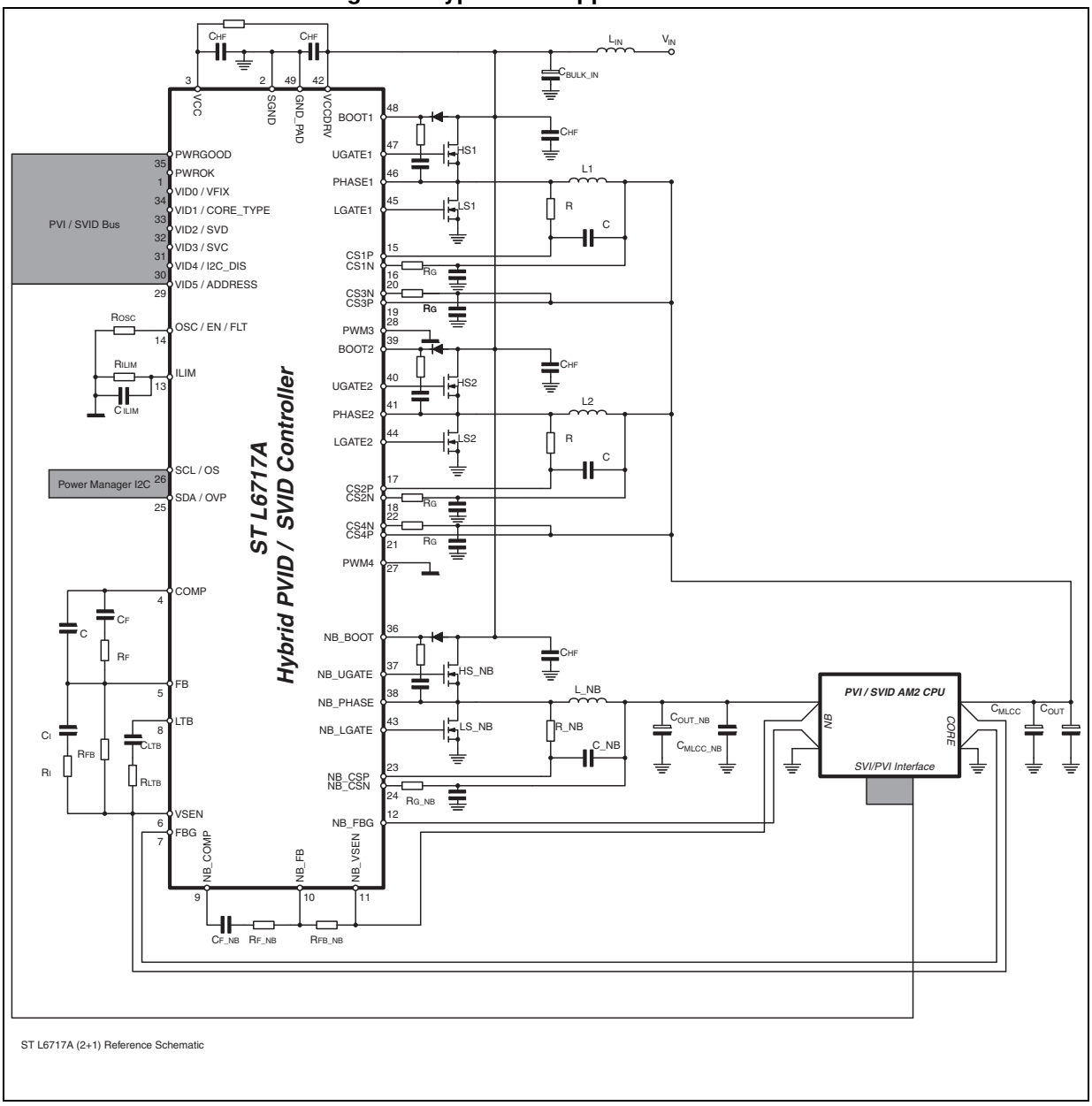


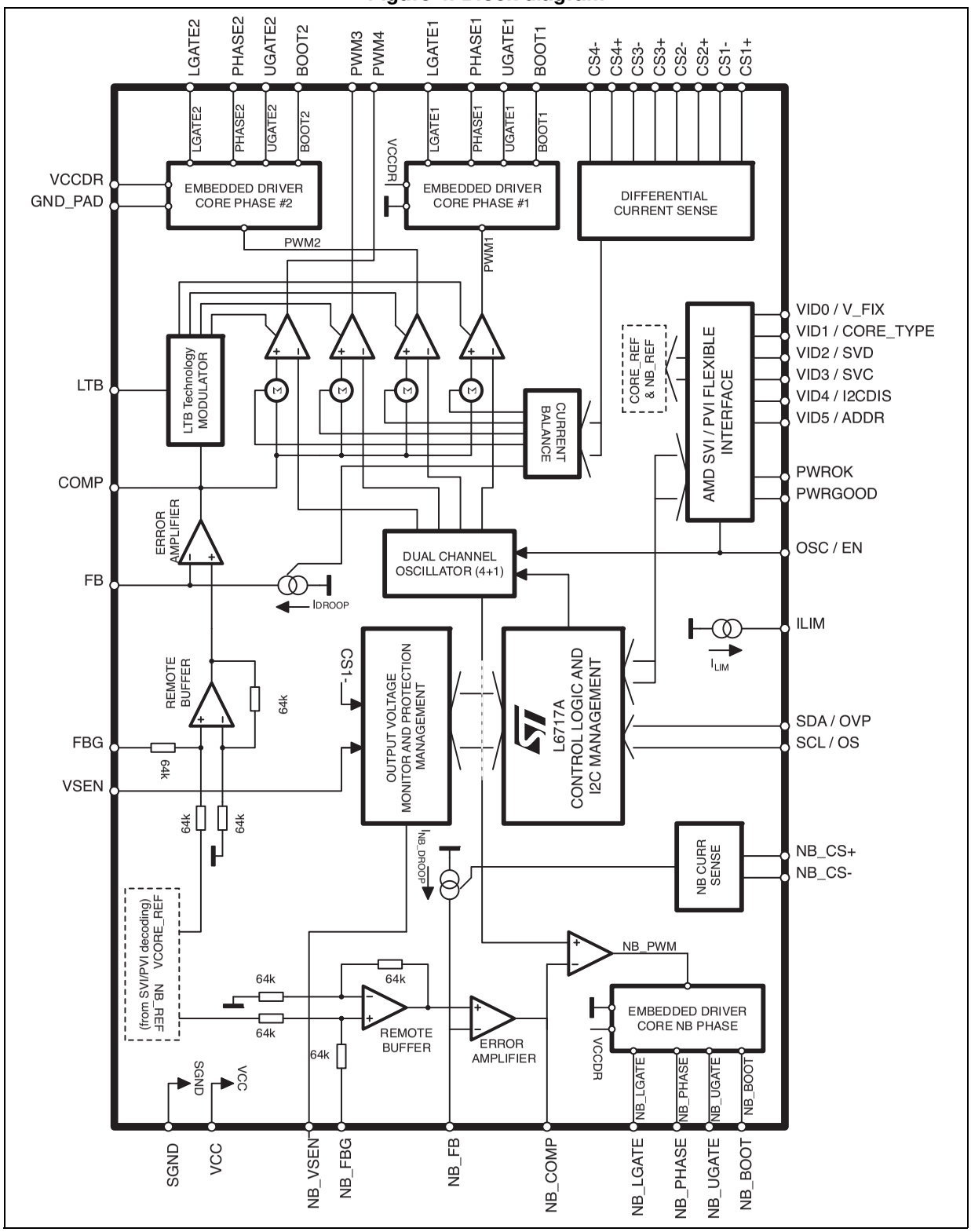
Figure 3. Typical 2+1 application circuit



ST L6717A (2+1) Reference Schematic

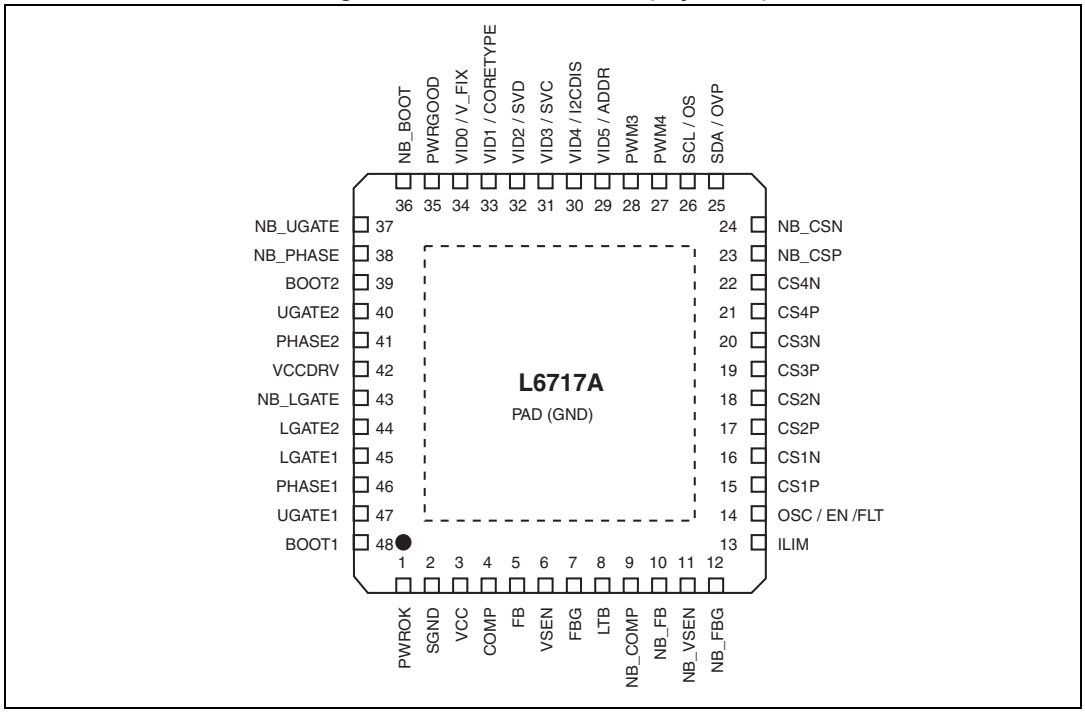
1.2 Block diagram

Figure 4. Block diagram



2 Pins description and connection diagrams

Figure 5. Pins connection (top view)



2.1 Pin descriptions

Table 2. Pin description

Pin#		Name	Function
1		PWROK	System-wide power good input (Ignored in PVI mode). Internally pulled-low by 10µA. When low, the device will decode the two SVI bits SVC and SVD to determine the *Pre-PWROK Metal VID*. When high, the device will actively run the SVI protocol. *Pre-PWROK Metal VID* are latched after EN is asserted and re-used in case of PWROK de-assertion. Latch is reset by VCC or EN cycle.
2		SGND	Device signal ground. All the internal references are referred to this pin. Connect to the PCB signal ground.
3		VCC	Device power supply. Operative voltage is 12 ±15%. Filter with 1µF MLCC to SGND.
4	CORE section	COMP	CORE error amplifier output. Connect with an R_F - C_F to FB. The CORE section and/or the device cannot be disabled by grounding this pin.

Table 2. Pin description (continued)

Pin#		Name	Function
5	CORE section	FB	CORE error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F to COMP. Droop current for voltage positioning is sourced from this pin.
6		VSEN	CORE output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the load for remote sensing. See *Section 8* for details.
7		FBG	CORE remote ground sense. Connect to the negative side of the load for remote sensing. See *Section 11* for proper layout of this connection.
8		LTB	LTB Technology® input pin. Connect through an R_{LTB} - C_{LTB} network to the regulated voltage (CORE section) to detect load transient. See *Section 12* for details.
9	NB section	NB_COMP	NB error amplifier output. Connect with an R_{F_NB} - C_{F_NB} to NB_FB. The NB section and/or the device cannot be disabled by grounding this pin.
10		NB_FB	NB error amplifier inverting input. Connect with a resistor R_{FB_NB} to NB_VSEN and with an R_{F_NB} - C_{F_NB} to NB_COMP. Droop current for Voltage Positioning is sourced from this pin.
11		NB_VSEN	NB output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the NB load to perform remote sensing. See *Section 11* for proper layout of this connection.
12		NB_FBG	NB remote ground sense. Connect to the negative side of the load to perform remote sense. See *Section 11* for proper layout of this connection.
13	CORE section	ILIM	CORE overcurrent pin. A current I_{LIM}=DCR/R_G*I_{OUT} proportional to the current delivered by the CORE section is sourced from this pin. The OC threshold is programmed by connecting a resistor R_{ILIM} to SGND. When the generated voltage crosses the OC_TOT threshold (V_{OC_TOT} = 2.5V Typ) the device latches with all MOSFETs OFF (to recover, cycle VCC or the EN pin). This pin is monitored for dynamic phase management. Filter with proper capacitor to provide OC masking time (0.5mSec typ time constant). See *Section 8.4.1* for details.
14		OSC / EN / FLT	*OSC*: It allows programming the switching frequency F_{SW} of both Sections. Switching frequency can be increased according to the resistor R_{OSC} connected to SGND with a gain of 10kHz/μA (see *Section 9* for details). If floating, the switching frequency is 200kHz per phase. *EN*: Pull-low to disable the device. When set free, the device immediately checks for the VID1 status to determine the SVI / PVI protocol to be adopted and configures itself accordingly. *FLT*: The pin is forced high (3.3V) in case of an OV / UV fault. To recover from this condition, cycle VCC or the EN pin. Drive with open drain circuit. See *Section 8* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
5	CORE section	FB	CORE error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F to COMP. Droop current for voltage positioning is sourced from this pin.
6		VSEN	CORE output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the load for remote sensing. See *Section 8* for details.
7		FBG	CORE remote ground sense. Connect to the negative side of the load for remote sensing. See *Section 11* for proper layout of this connection.
8		LTB	LTB Technology® input pin. Connect through an R_{LTB} - C_{LTB} network to the regulated voltage (CORE section) to detect load transient. See *Section 12* for details.
9	NB section	NB_COMP	NB error amplifier output. Connect with an R_{F_NB} - C_{F_NB} to NB_FB. The NB section and/or the device cannot be disabled by grounding this pin.
10		NB_FB	NB error amplifier inverting input. Connect with a resistor R_{FB_NB} to NB_VSEN and with an R_{F_NB} - C_{F_NB} to NB_COMP. Droop current for Voltage Positioning is sourced from this pin.
11		NB_VSEN	NB output voltage monitor. It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the NB load to perform remote sensing. See *Section 11* for proper layout of this connection.
12		NB_FBG	NB remote ground sense. Connect to the negative side of the load to perform remote sense. See *Section 11* for proper layout of this connection.
13	CORE section	ILIM	CORE overcurrent pin. A current I_{LIM}=DCR/R_G*I_{OUT} proportional to the current delivered by the CORE section is sourced from this pin. The OC threshold is programmed by connecting a resistor R_{ILIM} to SGND. When the generated voltage crosses the OC_TOT threshold (V_{OC_TOT} = 2.5V Typ) the device latches with all MOSFETs OFF (to recover, cycle VCC or the EN pin). This pin is monitored for dynamic phase management. Filter with proper capacitor to provide OC masking time (0.5mSec typ time constant). See *Section 8.4.1* for details.
14		OSC / EN / FLT	*OSC*: It allows programming the switching frequency F_{SW} of both Sections. Switching frequency can be increased according to the resistor R_{OSC} connected to SGND with a gain of 10kHz/μA (see *Section 9* for details). If floating, the switching frequency is 200kHz per phase. *EN*: Pull-low to disable the device. When set free, the device immediately checks for the VID1 status to determine the SVI / PVI protocol to be adopted and configures itself accordingly. *FLT*: The pin is forced high (3.3V) in case of an OV / UV fault. To recover from this condition, cycle VCC or the EN pin. Drive with open drain circuit. See *Section 8* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
15	CORE section	CS1P	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor. See *Section 11* for proper layout of this connection.
16		CS1N	Channel 1 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
17		CS2P	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. See *Section 11* for proper layout of this connection.
18		CS2N	Channel 2 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
19		CS3P	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2 phase, directly connect to V_{out_CORE}. See *Section 11* for proper layout of this connection.
20		CS3N	Channel 3 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. When working at 2 phase, connect through R_G to CS3+. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
21		CS4P	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at 2 or 3 phase, directly connect to V_{out_CORE}. See *Section 11* for proper layout of this connection.
22		CS4N	Channel 4 current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. When working at 2 or 3 phase, connect through R_G to CS4+.Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.
23	NB section	NB_CSP	NB channel current sense positive input. Connect through an R-C filter to the phase-side of the NB channel inductor. See *Section 11* for proper layout of this connection.
24		NB_CSN	NB channel current sense negative input. Connect through a R_G resistor to the output-side of the channel inductor. Filter the Vout-side of R_G resistor with 100nF to GND. See *Section 11* for proper layout of this connection.

Table 2. Pin description (continued)

Pin#		Name	Function
25	Power manager I^2C	SDA / OVP	*SDA - power manager I^2C data.* When power manager I^2C is enabled, this is the data connection. See *Section 6* for details. *OVP - over voltage setting.* When power manager I^2C is disabled (VID4 / I2CDIS to 3.3V) this pin sources a constant 10µA current. By connecting a resistor R_{OVP} to GND, the OV threshold for both Sections is defined. See *Section 8.1* for details.
26		SCL / OS	*SCL - power manager I^2C clock.* When power manager I^2C is enabled, this is the clock connection. See *Section 6* for details. *OS - CORE section offset.* When power manager I^2C is disabled (VID4 / I2CDIS to 3.3V) this pin is internally set to 1.24V(2.0V): connecting a R_{OS} resistor to GND (3.3V) allows setting a current that is mirrored into FB pin in order to program a positive (negative) offset according to the selected R_{FB}. Short to GND to disable the function. See *Section 7.4* for details.
27, 28		PWM4, PWM3	PWM output for external drivers. Connect to external drivers PWM inputs. The device is able to manage HiZ status by setting the pins floating. By shorting to GND PWM4 or PWM3 and PWM4, it is possible to program the CORE section to work at 3 or 2 phase respectively. See *Section 5.4.4* for details about HiZ management.
29	SVI / PVI interface	VID5 / ADDR	Voltage identification pin - I^2C address pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. In SVI mode, the pin is monitored on the EN pin rising-edge to modify the I^2C address. See *Section 5* for details.
30		VID4 / I2CDIS	Voltage identification pin - I^2C disable pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. In SVI mode, the pin is monitored on the EN pin rising-edge to enable/disable the I^2C. See *Section 5* for details.
31		VID3 / SVC	Voltage IDentification Pin - SVI Clock Pin. Internally pulled-low by 10µA, it programs the output voltage in both SVI and PVI modes. In SVI mode, the 10µA pull down is disabled. See *Section 5* for details.
32		VID2 / SVD	Voltage identification pins - SVI data pin. Internally pulled-low by 10µA, it programs the output voltage in both SVI and PVI modes. In SVI mode, the 10µA pull down is disabled. See *Section 5* for details.
33	SVI / PVI interface	VID1 / CORETYPE	Voltage identification pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. The pin is monitored on the EN pin rising-edge to define the operative mode of the controller (SVI or PVI). See *Section 5* for details.
34		VID0 / VFIX	Voltage identification pin. Internally pulled-low by 10µA, it programs the output voltage in PVI mode. If the pin is pulled to 3.3V, the device enters V_FIX mode and SVI commands are ignored. See *Section 5* for details.

Table 2. Pin description (continued)

Pin#		Name	Function
35		PWRGOOD	VCORE and NB power good. It is an open-drain output set free after SS as long as both the voltage planes are within specifications. Pull-up to 3.3V (typ) or lower, if not used it can be left floating. When in PVI mode, it monitors the CORE section only.
36	Embedded drivers	NB_BOOT	NB section high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the NB_PHASE pin. See *Section 10* for guidance in designing the capacitor value.
37		NB_UGATE	NB Section High-Side Driver Output. Connect to NB Section High-Side MOSFET gate. A small series resistor may help in reducing NB_PHASE pin negative spike as well as cooling the device.
38		NB_PHASE	NB section high-side driver return path. Connect to the NB section high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
39		BOOT2	CORE section, phase 2 high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the PHASE2 pin. See *Section 10* for guidance in designing the capacitor value.
40		UGATE2	High-Side Driver Output. Connect to Phase2 High-Side MOSFET gate. A small series resistor may help in reducing PHASE2 pin negative spike as well as cooling the device.
41		PHASE2	CORE section, phase 2 high-side driver return path. Connect to the phase2 high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
42		VCCDRV	Supply voltage for low-side embedded drivers. Operative voltage is flexible from 5V ±5% to 12 ±15%. Filter with 1µF MLCC to GND.
43 to 45	Embedded drivers	NB_LGATE, LGATE2, LGATE1	Low-side driver output. Connect directly to the low-side MOSFET gate of the related section. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
46		PHASE1	CORe section, phase 1 high-side driver return path. Connect to the phase1 high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
47		UGATE1	High-side driver output. Connect to phase1 high-side MOSFET gate. A small series resistor may help in reducing PHASE1 pin negative spike as well as cooling the device.
48		BOOT1	CORE section, phase 1 high-side driver supply. This pin supplies the high-side floating driver. Connect through C_{BOOT} capacitor to the PHASE1 pin. See *Section 10* for guidance in designing the capacitor value.
Thermal PAD		GND	All internal references, logic, and the silicon substrate are referenced to this pin. Connect to the PCB GND ground plane by multiple vias to improve heat dissipation.

2.2 Thermal data

Table 3.Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	40	°C/W
R_{THJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}, V_{CCDRV}	to GND	-0.3 to 15	V
V_{BOOTx}, V_{UGATEx}	to GND to PHASEx	41 15	V
V_{PHASEx}	(VCC=VCCDR=12V) To GND Negative spike to GND, t < 400ns Positive spike to GND, t < 200 ns	-0.3 to 26 -8 30	V
V_{LGATEx}	to GND to GND, t < 100nsec.	-0.3 to VCCDRV + 0.3 -3	V
	All other pins to GND	-0.3 to 3.6	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance “Normal Performance”	±1750	V

3.2 Electrical characteristics

V_{CC}=12V±15%, T_J = 0°C to 70°C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	OSC = GND		15		mA
I_{CCDR}	VCCDR supply current			4		mA
I_{BOOTx}	BOOTx supply current			1.5		mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising			4.5	V
	VCC turn-OFF	VCC falling	4			V
Oscillator						
F_{SW}	Main oscillator accuracy		180	200	220	kHz
	Oscillator adjustability	R_{OSC} = 36kΩ	425	500	575	kHz
ΔV_{OSC}	PWM ramp amplitude	CORE and NB section		1.5		V
FAULT	Voltage at Pin OSC	OVP, UVP latch active	3		3.6	V
EN	Turn-OFF threshold	OSC/EN falling	0.3			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PVI / SVI interface						
PWROK	Input high		1.3			V
	Input low				0.80	V
VID2,/SVD VID3/SVC	Input high	(SVI mode)	0.95			V
	Input low	(SVI mode)			0.65	V
SVD	Voltage low (ACK)	I_{SINK} = -5mA			250	mV
VID0 to VID5	Input high	(PVI mode)	1.3			V
	Input low	(PVI mode)			0.80	V
V_FIX	Entering V_FIX mode	VID0/V_FIX rising	3			V
Power manager I^2C						
SDA, SCL	Input high		1.3			V
	Input low				0.8	V
SDA	Voltage low (ACK)	I_{SINK} = -5mA			250	mV
Voltage positioning (CORE and NB section)						
CORE	Output voltage accuracy	VSEN to V_{CORE}; FBG to GND_{CORE}	-8		8	mV
NB		NBVSEN to V_{NB}; NBFBG to GND_{FB}	-10		10	mV
OS	OFFSET bias voltage	I2DIS=3.3V, I_{OS} = 0 to 250µA	1.190	1.24	1.290	V
	OFFSET current range	I2DIS=3.3V	0		250	µA
	OFFSET - I_{FB} accuracy	I2DIS=3.3V, I_{OS} = 0µA	-2.25		2.25	µA
		I2DIS=3.3V, I_{OS} = 250µA	-9		9	µA
DROOP	DROOP accuracy	I_{DROOP} = 0 to 25µA, k_{DRP} = 1/4	-3		3	µA
		I_{NB_DROOP} = 0 to 6µA, k_{NBDRP} = 1/4	-1		1	µA
A_0	EA DC gain			100		dB
SR	Slew rate	COMP, NB_COMP to SGND = 10pF		20		V/µs
PWM outputs (CORE only) and embedded drivers						
PWM3, PWM4	Output high	I = 1mA	3		3.6	V
	Output low	I = -1mA			0.2	V
I_{PWMx}	Test current			10		µA
High current embedded drivers						
R_{HIHS}	HS source resistance	BOOT - PHASE = 12V; 100mA		2.3	2.8	Ω
I_{UGATE}	HS source current	BOOT - PHASE = 12V; (1) C_{UGATE} to PHASE = 3.3nF		2		A
R_{LOHS}	HS sink resistance	BOOT - PHASE = 12V; 100mA		2	2.5	Ω
R_{HILS}	LS source resistance	100mA		1.3	1.8	Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LGATE}	LS source current	C_{LGATE} to GND = 5.6nF; (1)		3		A
R_{LOLS}	LS sink resistance	100mA		1	1.5	Ω
Protections						
OVP	Overvoltage protection	I^2C enabled, no commands issued, wrt VID, CORE & NB section	+200	+250	+300	mV
		I^2C enabled, V_FIX mode; VSEN, NB_VSEN rising		1.800		V
	SDA/OVP bias current	I2CDIS = 3.3V	9	11	13	µA
UVP	Undervoltage protection	VSEN, NB_VSEN falling; wrt Ref.	-450	-400	-350	mV
PWRGOOD	PGOOD threshold	VSEN, NB_VSEN falling; wrt Ref	-285	-250	-215	mV
	Voltage low	$I_{PWRGOOD}$ = -4mA			0.4	V
$V_{FB-DISC}$	FB disconnection	V_{CSN} rising, above VSEN CORE and NB sections		600		mV
$V_{FBG\ DISC}$	FBG disconnection	EA NI input wrt VID		500		mV
V_{OC_TOT}	CORE OC		2.425	2.500	2.575	V
kI_{ILIM}		I_{LIM} = 0µA	0		4	µA
		I_{LIM} = 100µA		100		µA

1. Parameter(s) guaranteed by designed, not fully tested in production

4 Device description and operation

L6717A is a hybrid CPU power supply controller compatible with both parallel (PVI) and serial (SVI) protocols for AMD processors. The device provides complete control logic and protections for a high-performance step-down DC-DC voltage regulator, optimized for advanced microprocessor power supply supporting both PVI and SVI communication. It embeds two independent controllers for CPU CORE and the integrated NB, each one with its own set of protections. NB phase (when enabled) is automatically phase-shifted with respect to the CORE phases in order to reduce the total input rms current amount.

The device features an additional power manager I^2C interface to easy the system design for enthusiastic application where the main parameters of the voltage regulator have to be modified. L6717A is able to adjust the regulated voltage, the switching frequency and also the OV protection threshold through the power manager I^2C bus while the application is running assuring fast and reliable transitions.

Dynamic phase management (DPM) allows the device to automatically adjust the phase count according to the current delivered to the load. This feature allow the system to keep alive only the phases really necessary to sustain the load saving in power dissipation so optimizing the efficiency over the whole current range of the application. DPM can be enabled through the power manager I^2C bus.

L6717A is able to detect which kind of CPU is connected in order to configure itself to work as a single-plane PVI controller or dual-plane SVI controller.

The controller performs a single-phase control for the NB section and a programmable 2-to-4 phase control for the CORE section featuring dual-edge non-latched architecture: this allows fast load-transient response optimizing the output filter consequently reducing the total BOM cost. Further reduction in output filter can be achieved by enabling LTB Technology®.

PSI_L Flag is sent to the VR through the SVI bus. The controller monitors this flag and selectively modifies the phase number in order to optimize the system efficiency when the CPU enters low-power states. This causes the over-all efficiency to be maximized at light loads so reducing losses and system power consumption.

Both sections feature programmable overvoltage protection and adjustable constant overcurrent protection. Voltage positioning (LL) is possible thanks to an accurate fully-differential current-sense across the main inductors for both sections.

L6717A features dual remote sensing for the regulated outputs (CORE and NB) in order to recover from PCB voltage drops also protecting the load from possible feedback network disconnections.

LSLess start-up function allows the controller to manage pre-biased start-up avoiding dangerous current return through the main inductors as well as negative undershoot on the output voltage if the output filter is still charged before start-up.

L6717A supports V_FIX mode for system debugging: in this particular configuration the SVI bus is used as a static bus configuring 4 operative voltages for both the sections and ignoring any serial-VID command.

When working in PVI mode, the device features On-the-Fly VID management: VID code is continuously sampled and the reference update according to the variation detected,

L6717A is available in VFQFPN48 package.

5 Hybrid CPU support and CPU_TYPE detection

L6717A is able to detect the type of the CPU-core connected and to configure itself accordingly. At system Start-up, on the rising-edge of the EN signal, the device monitors the status of VID1 and configures the PVI mode (VID1 = 1) or SVI mode (VID1 = 0).

When in PVI mode, L6717A uses the information available on the VID[0: 5] bus to address the CORE section output voltage according to *Table 6*. NB section is kept in HiZ mode, both MOSFETs are kept OFF.

When in SVI mode, L6717A DAC ignores the information available on VID0, VID4 and VID5 and uses VID2 and VID3 as a SVI bus addressing the CORE and NB sections according to the SVI protocol. The device supports 3.4MHz bus rate frequency.

Caution: To avoid any risk of errors in CPU type detection (i.e. detecting SVI CPU when PVI CPU is installed on the socket and vice versa), it is recommended to carefully control the start-up sequencing of the system hosting L6717A in order to ensure than on the EN rising-edge, VID1 is in valid and correct state. Typical connections consider VID1 connected to CPU CORE_TYPE through a resistor to correctly address the CPU detection.

5.1 PVI - parallel interface

PVI is a 6-bit-wide parallel interface used to address the CORE section reference. According to the selected code, the device sets the CORE section reference and regulates its output voltage as reported into *Table 6*.

NB section is always kept in HiZ; no activity is performed on this section and both the high-side and low-side of this section are kept OFF. Furthermore, PWROK information is ignored as well since the signal only applies to the SVI protocol.

5.2 PVI start-up

Once the PVI mode has been detected, the device uses the whole code available on the VID[0:5] lines to define the reference for the CORE section. NB section is kept in HiZ. Soft-start to the programmed reference is performed regardless of the state of PWROK.

See *Section 7.8* for details about soft-start.

Figure 6. System start-up: SVI (to Metal-VID; left) and PVI (right)

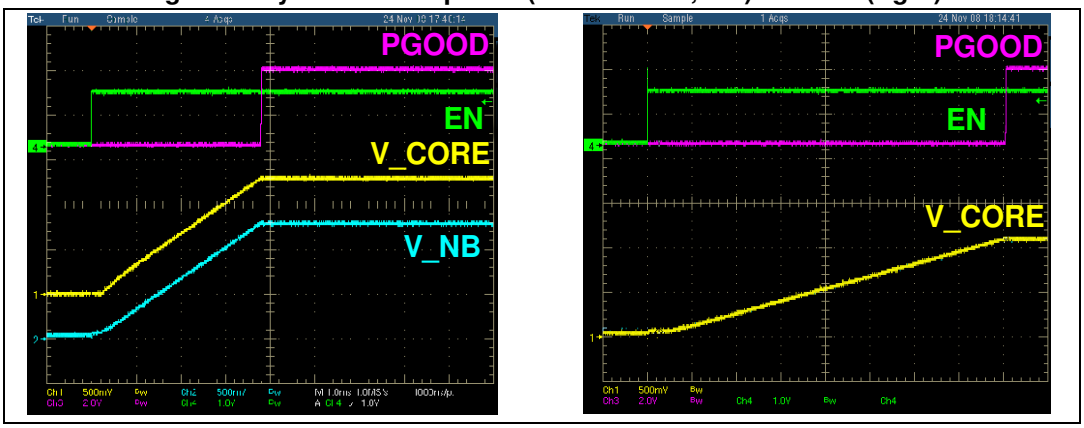


Table 6. Voltage identifications (VID) codes for PVI mode

VID5	VID4	VID3	VID2	VID1	VID0	Output voltage	VID5	VID4	VID3	VID2	VID1	VID0	Output voltage
0	0	0	0	0	0	1.5500	1	0	0	0	0	0	0.7625
0	0	0	0	0	1	1.5250	1	0	0	0	0	1	0.7500
0	0	0	0	1	0	1.5000	1	0	0	0	1	0	0.7375
0	0	0	0	1	1	1.4750	1	0	0	0	1	1	0.7250
0	0	0	1	0	0	1.4500	1	0	0	1	0	0	0.7125
0	0	0	1	0	1	1.4250	1	0	0	1	0	1	0.7000
0	0	0	1	1	0	1.4000	1	0	0	1	1	0	0.6875
0	0	0	1	1	1	1.3750	1	0	0	1	1	1	0.6750
0	0	1	0	0	0	1.3500	1	0	1	0	0	0	0.6625
0	0	1	0	0	1	1.3250	1	0	1	0	0	1	0.6500
0	0	1	0	1	0	1.3000	1	0	1	0	1	0	0.6375
0	0	1	0	1	1	1.2750	1	0	1	0	1	1	0.6250
0	0	1	1	0	0	1.2500	1	0	1	1	0	0	0.6125
0	0	1	1	0	1	1.2250	1	0	1	1	0	1	0.6000
0	0	1	1	1	0	1.2000	1	0	1	1	1	0	0.5875
0	0	1	1	1	1	1.1750	1	0	1	1	1	1	0.5750
0	1	0	0	0	0	1.1500	1	1	0	0	0	0	0.5625
0	1	0	0	0	1	1.1250	1	1	0	0	0	1	0.5500
0	1	0	0	1	0	1.1000	1	1	0	0	1	0	0.5375
0	1	0	0	1	1	1.0750	1	1	0	0	1	1	0.5250
0	1	0	1	0	0	1.0500	1	1	0	1	0	0	0.5125
0	1	0	1	0	1	1.0250	1	1	0	1	0	1	0.5000
0	1	0	1	1	0	1.0000	1	1	0	1	1	0	0.4875
0	1	0	1	1	1	0.9750	1	1	0	1	1	1	0.4750
0	1	1	0	0	0	0.9500	1	1	1	0	0	0	0.4625
0	1	1	0	0	1	0.9250	1	1	1	0	0	1	0.4500
0	1	1	0	1	0	0.9000	1	1	1	0	1	0	0.4375
0	1	1	0	1	1	0.8750	1	1	1	0	1	1	0.4250
0	1	1	1	0	0	0.8500	1	1	1	1	0	0	0.4125
0	1	1	1	0	1	0.8250	1	1	1	1	0	1	0.4000
0	1	1	1	1	0	0.8000	1	1	1	1	1	0	0.3875
0	1	1	1	1	1	0.7750	1	1	1	1	1	1	0.3750

5.3 SVI - serial interface

SVI is a two wire, clock and data, bus that connects a single master (CPU) to one slave (L6717A). The master initiates and terminates SVI transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave receives the SVI transactions and acts accordingly. SVI wire protocol is based on fast-mode I^2C.

SVI interface also considers two additional signal needed to manage the system start-up. These signals are EN and PWROK. The device return a PWRGOOD signal if the output voltages are in regulation.

5.4 SVI start-up

Once the SVI mode has been detected on the EN rising-edge, L6717A checks for the status of the two serial VID pins, SVC and SVD, and stores this value as the *Pre-PWROK Metal VID*. The controller initiate a soft-start phase regulating both CORE and NB voltage planes to the voltage level prescribed by the *Pre-PWROK Metal VID*. See *Table 7* for details about *Pre-PWROK Metal VID* codifications. The stored *Pre-PWROK Metal VID* value are re-used in any case of PWROK de-assertion.

After bringing the output rails into regulation, the controller asserts the PWRGOOD signal and waits for PWROK to be asserted. Until PWROK is asserted, the controller regulates to the *Pre-PWROK Metal VID* ignoring any commands coming from the SVI interface.

After PWROK is asserted, the processor has initialized the serial VID interface and L6717A waits for commands from the CPU to move the voltage planes from the *Pre-PWROK Metal VID* values to the operative VID values. As long as PWROK remains asserted, the controller will react to any command issued through the SVI interface according to SVI protocol.

See *Section 7.8* for details about soft-start.

Table 7. V_FIX mode and *Pre-PWROK MetalVID*

SVC	SVD	Output voltage [V]	
		Pre-PWROK Metal VID	V_FIX mode
0	0	1.1V	1.4V
0	1	1.0V	1.2V
1	0	0.9V	1.0V
1	1	0.8V	0.8V

5.4.1 Set VID command

The *set VID command* is defined as the command sequence that the CPU issues on the SVI bus to modify the voltage level of the CORE Section and/or the NB section.

During a *set VID Command*, the processor sends the start (START) sequence followed by the address of the Section which the *set VID command* applies. The processor then sends the write (WRITE) bit. After the write bit, the voltage regulator (VR) sends the acknowledge (ACK) bit. The processor then sends the VID bits code during the *data phase*. The VR sends the acknowledge (ACK) bit after the data phase. Finally, the processor sends the stop (STOP) sequence. After the VR has detected the stop, it performs an On-the-Fly VID

transition for the addressed section(s) or, more in general, react to the sent command accordingly. Refer to *Figure 7*, *Table 8* and *Table 9* for details about the *set VID command.*

L6717A is able to manage individual power OFF for both the sections. The CPU may issue a serial VID command to power OFF or power ON one section while the other one remains powered. In this case, the PWRGOOD signal remains asserted.

Figure 7. SVI communications - send byte

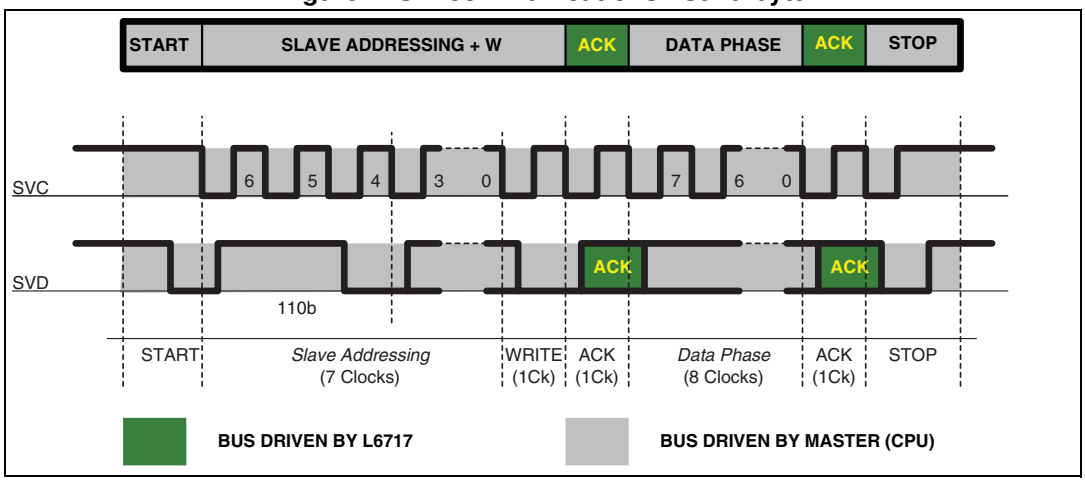


Table 8. SVI send byte - address and data phase description

bits	Description
Address phase	
6:4	Always 110b.
3	Not applicable, ignored.
2	Not applicable, ignored.
1	CORE section(1). If set then the following data byte contains the VID code for CORE section.
0	NB section(1). If set then the following data byte contains the VID code for NB section.
Data phase	
7	PSI_L flag (Active low).When asserted, the VR is allowed to enter power-saving mode. See *Section 5.4.3*.
6:0	VID code. See *Table 9*.

1. Assertion in both bit 1 and 0 will address the VID code to both CORE and NB simultaneously.

Table 9. Data phase - serial VID codes

SVI [6:0]	Output voltage	SVI [6:0]	Output voltage	SVI [6:0]	Output voltage	SVI [6:0]	Output voltage
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500	110_0000	0.3500
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375	110_0001	0.3375
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250	110_0010	0.3250
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125	110_0011	0.3125
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000	110_0100	0.3000
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875	110_0101	0.2875
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750	110_0110	0.2750
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625	110_0111	0.2625
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500	110_1000	0.2500
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375	110_1001	0.2375
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250	110_1010	0.2250
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125	110_1011	0.2125
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000	110_1100	0.2000
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875	110_1101	0.1875
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750	110_1110	0.1750
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625	110_1111	0.1625
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500	111_0000	0.1500
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375	111_0001	0.1375
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250	111_0010	0.1250
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125	111_0011	0.1125
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000	111_0100	0.1000
001_0101	1.2875	011_0101	0.8875	101_0101	0.4875	111_0101	0.0875
001_0110	1.2750	011_0110	0.8750	101_0110	0.4750	111_0110	0.0750
001_0111	1.2625	011_0111	0.8625	101_0111	0.4625	111_0111	0.0625
001_1000	1.2500	011_1000	0.8500	101_1000	0.4500	111_1000	0.0500
001_1001	1.2375	011_1001	0.8375	101_1001	0.4375	111_1001	0.0375
001_1010	1.2250	011_1010	0.8250	101_1010	0.4250	111_1010	0.0250
001_1011	1.2125	011_1011	0.8125	101_1011	0.4125	111_1011	0.0125
001_1100	1.2000	011_1100	0.8000	101_1100	0.4000	111_1100	OFF
001_1101	1.1875	011_1101	0.7875	101_1101	0.3875	111_1101	OFF
001_1110	1.1750	011_1110	0.7750	101_1110	0.3750	111_1110	OFF
001_1111	1.1625	011_1111	0.7625	101_1111	0.3625	111_1111	OFF

5.4.2 PWROK de-assertion

Anytime PWROK de-asserts while EN is asserted, the controller uses the previously stored *Pre-PWROK Metal VID* and regulates all the planes to that level performing an on-the-fly transition to that level.

PWRGOOD is treated appropriately being de-asserted in case the *Pre-PWROK Metal VID* voltage is out of the initial voltage specifications.

5.4.3 PSI_L and efficiency optimization at light-load

PSI_L is an active-low flag (i.e. low logic level when asserted) that can be set by the CPU to allow the VR to enter power-saving mode to maximize the system efficiency when in light-load conditions. The status of the flag is communicated to the controller through the SVI bus.

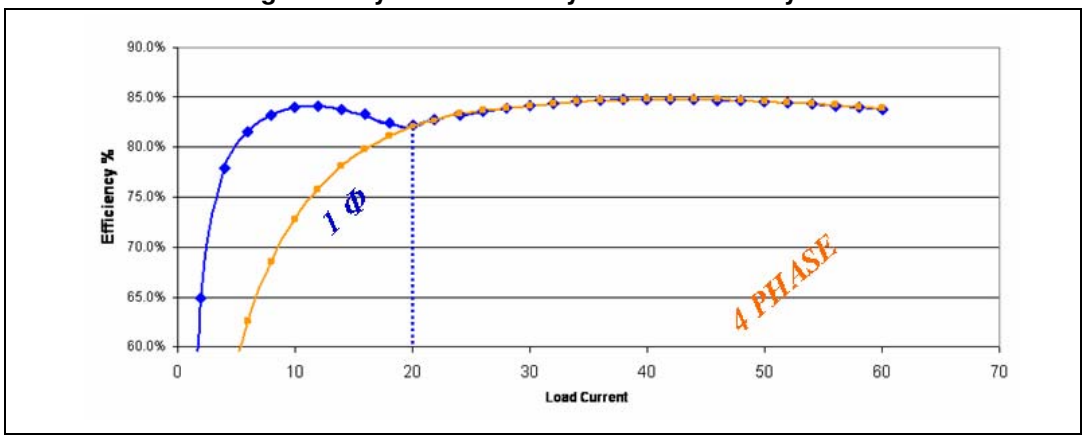
When the PSI_L flag is asserted by the CPU through the SVI bus, the device adjusts the phase number and interleaving according to the strategy programmed. Default strategy, when enabled, consists in working in single phase. PSI strategy can be disabled as well as re-configured through specific power manager I^2C commands. See *Section 6* for details.

In case the phase number is changed, the device will set HiZ on the related phase and re-configure internal phase-shift to maintain the interleaving. Furthermore, the internal current-sharing will be adjusted to consider the phase number reduction.

When PSI_L is de-asserted, the device will return to the original configuration. Start-up is performed with all the configured phases enabled. In case of on-the-fly VID transitions, the device will maintain the phase configuration set before.

NB section is not impacted by PSI_L status change. *Figure 8* shows an example of the efficiency improvement that can be achieved by enabling the PSI management.

Figure 8. System efficiency enhancement by PSI



5.4.4 HiZ management

L6717A is able to manage HiZ for internal drivers and for the external drivers through the PWMx signals. When the controller wants to set in high impedance the output of one section, it sets the relative PWM floating and, at the same time, turn OFF the embedded drivers of the related section.