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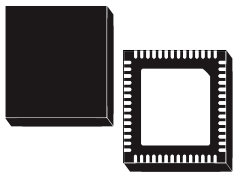
L6718

Digitally controlled dual PWM with embedded drivers for VR12 processors

Datasheet - production data



VFQFPN56 -7x7 mm

Features

- VR12 compliant with 25 MHz SVID bus rev. 1.5
- Second generation LTB Technology™
- Very compact dual controller:
  - Up to 4 phases for core section with 2 internal drivers
  - 1 phase for GFX section with internal driver
- Input voltage up to 12 V
- SMBus interface for power management
- SWAP, Jmode, multi-rail only support
- Programmable offset voltage
- Single NTC design for TM, LL and IMON thermal compensation (for each section)
- VFDE for efficiency optimization
- DPM - dynamic phase management
- Dual differential remote sense
- 0.5% output voltage accuracy
- Full-differential current sense across DCR
- AVP - adaptive voltage positioning
- Programmable switching frequency
- Dual current monitor
- Pre-biased output management
- High-current embedded drivers optimized for 7 V operation
- OC, OV, UV and FB disconnection protection
- Dual VR_READY
- VFQFPN56 7x7 mm package with exposed pad

Applications

- High-current VRM / VRD for desktop / server / new generation workstation CPUs
- DDR3 DDR4 memory supply for VR12

Description

The L6718 is a very compact, digitally controlled and cost effective dual controller designed to power Intel® VR12 processors. Dedicated pinstrapping is used to program the main parameters.

The device features from 2 to 4-phase programmable operation for the core section providing 2 embedded drivers. A single-phase with embedded driver and with independent control loop is used for GFX.

The L6718 supports power state transitions featuring VFDE and a programmable DPM, maintaining the best efficiency over all loading conditions without compromising transient response.

Second generation LTB Technology™ allows a minimal cost output filter providing fast load transient response. The controller assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in VFQFPN56, 7x7 mm compact package with exposed pad.

Table 1. Device summary

Order code	Package	Packaging
L6718	VFQFPN56 7x7 mm	Tray
L6718TR	VFQFPN56 7x7 mm	Tape and reel

This is information on a product in full production. www.st.com

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1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical 4-phase application circuit

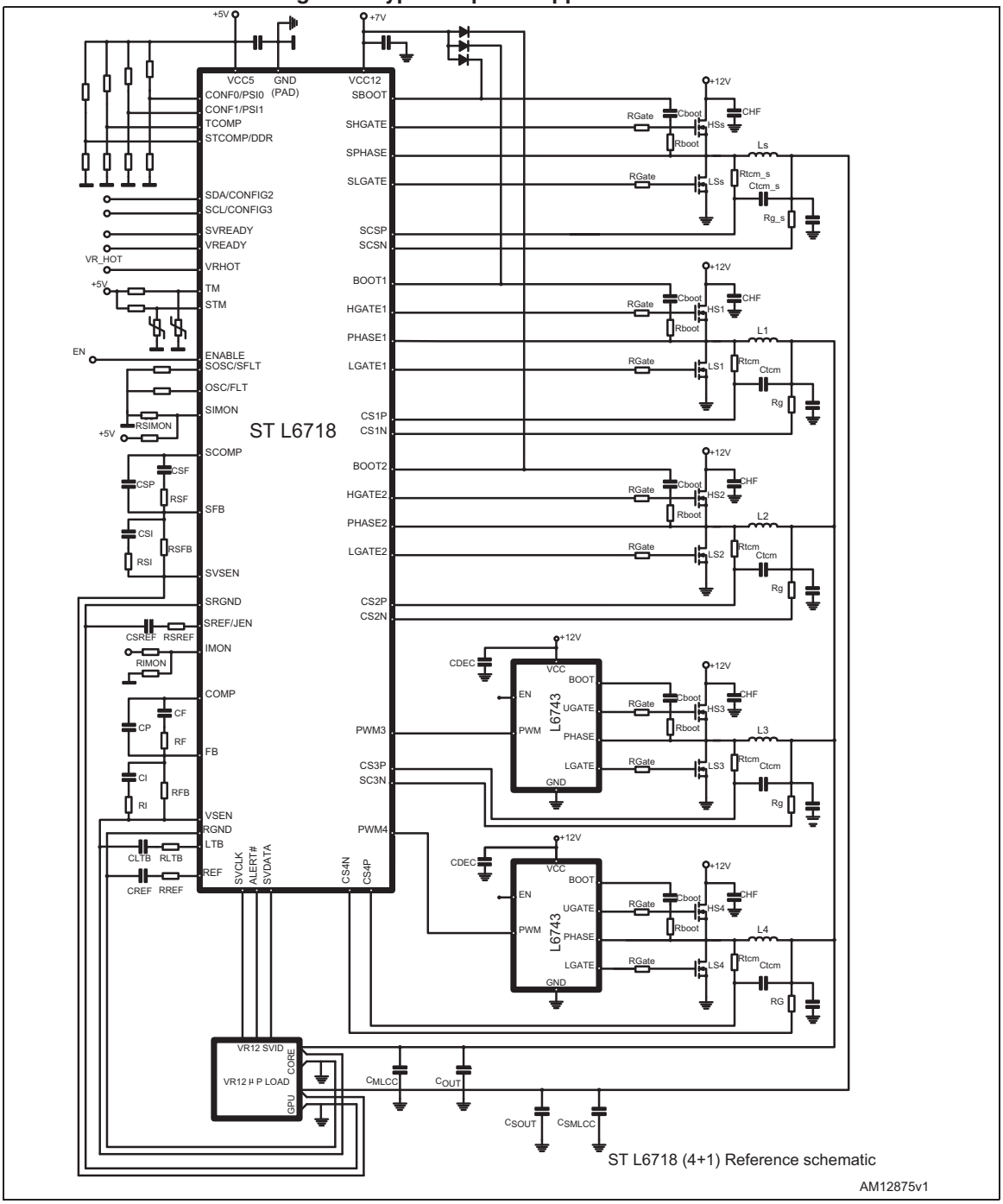


Figure 2. Typical 3-phase application circuit

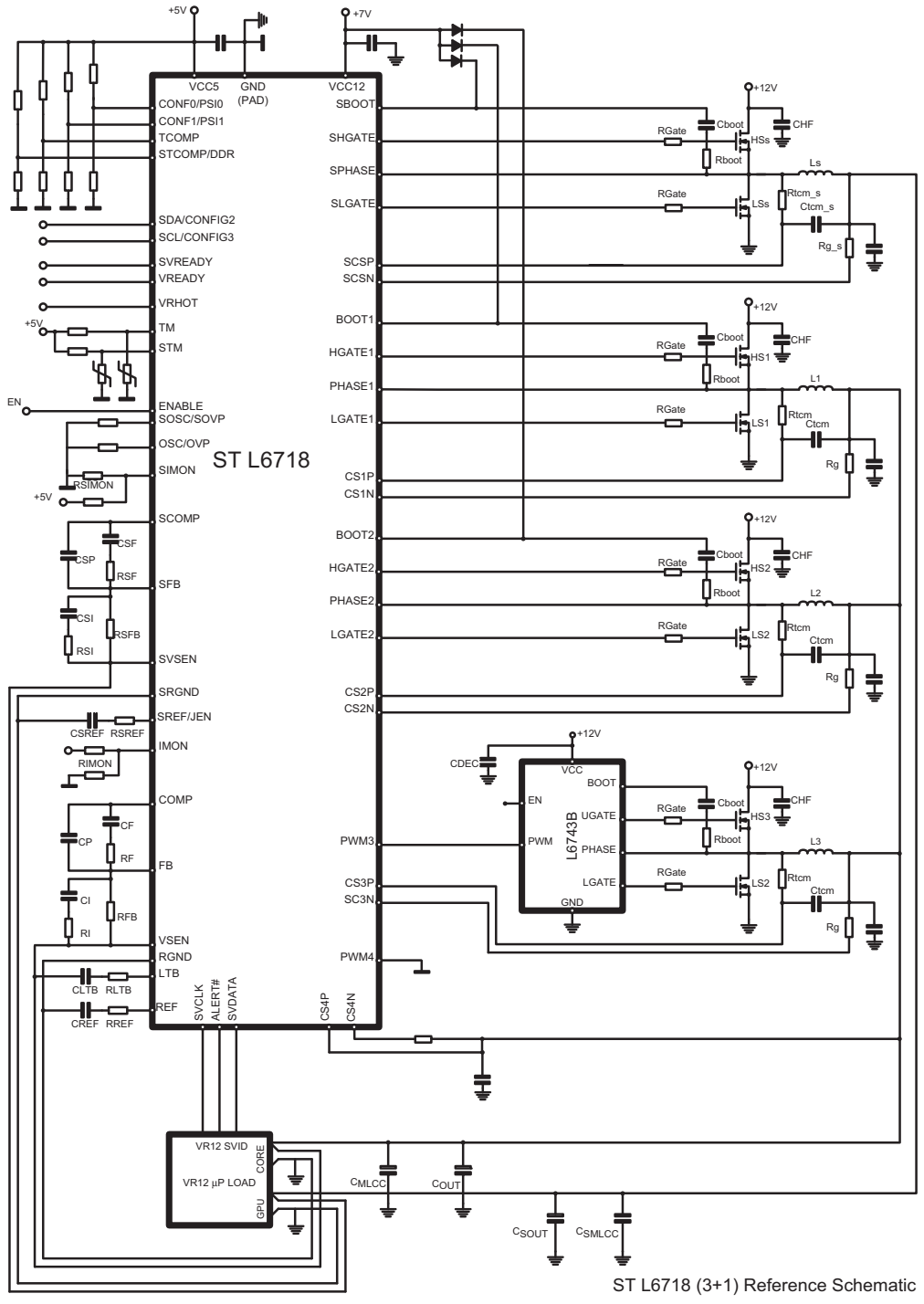
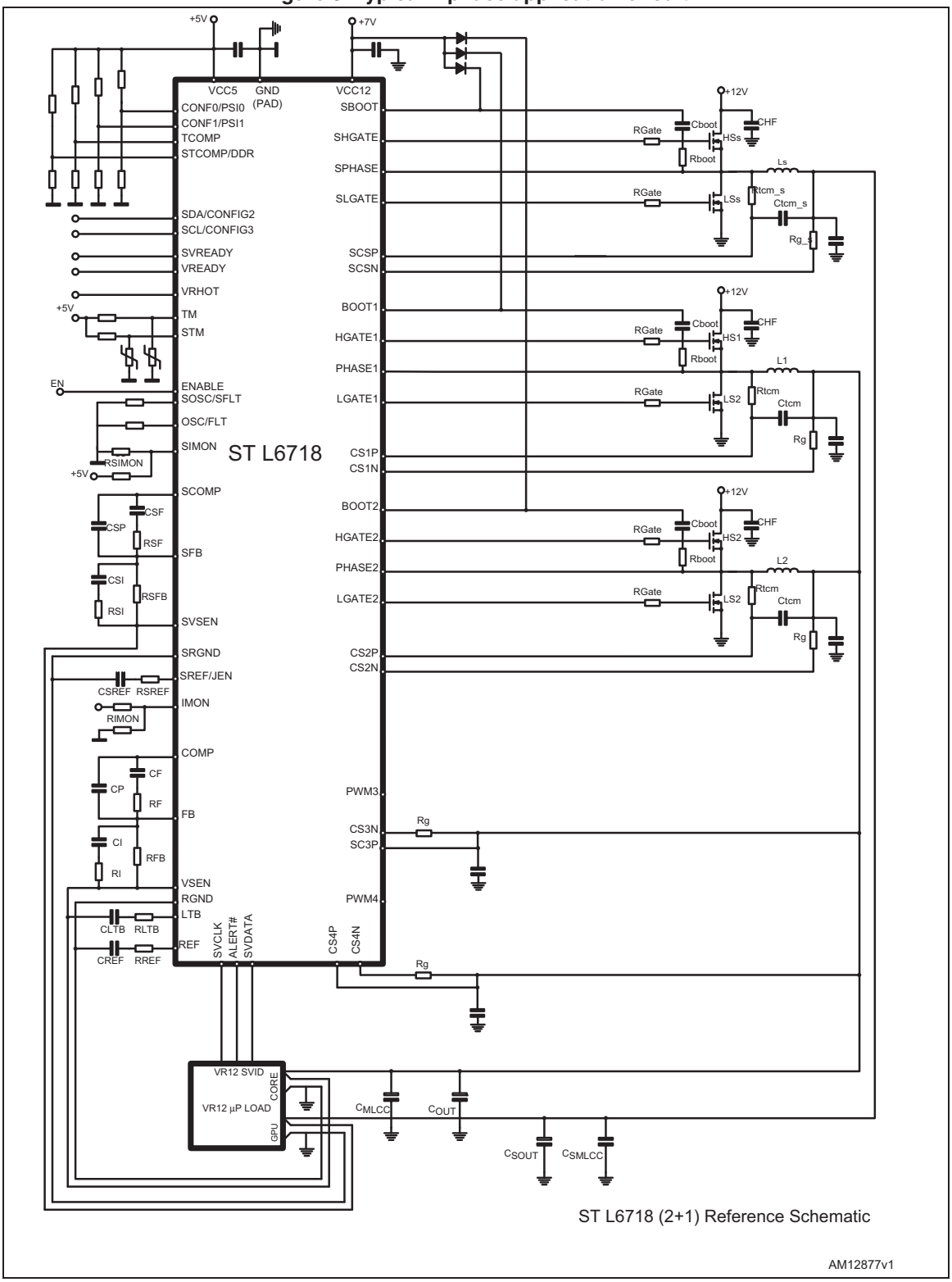
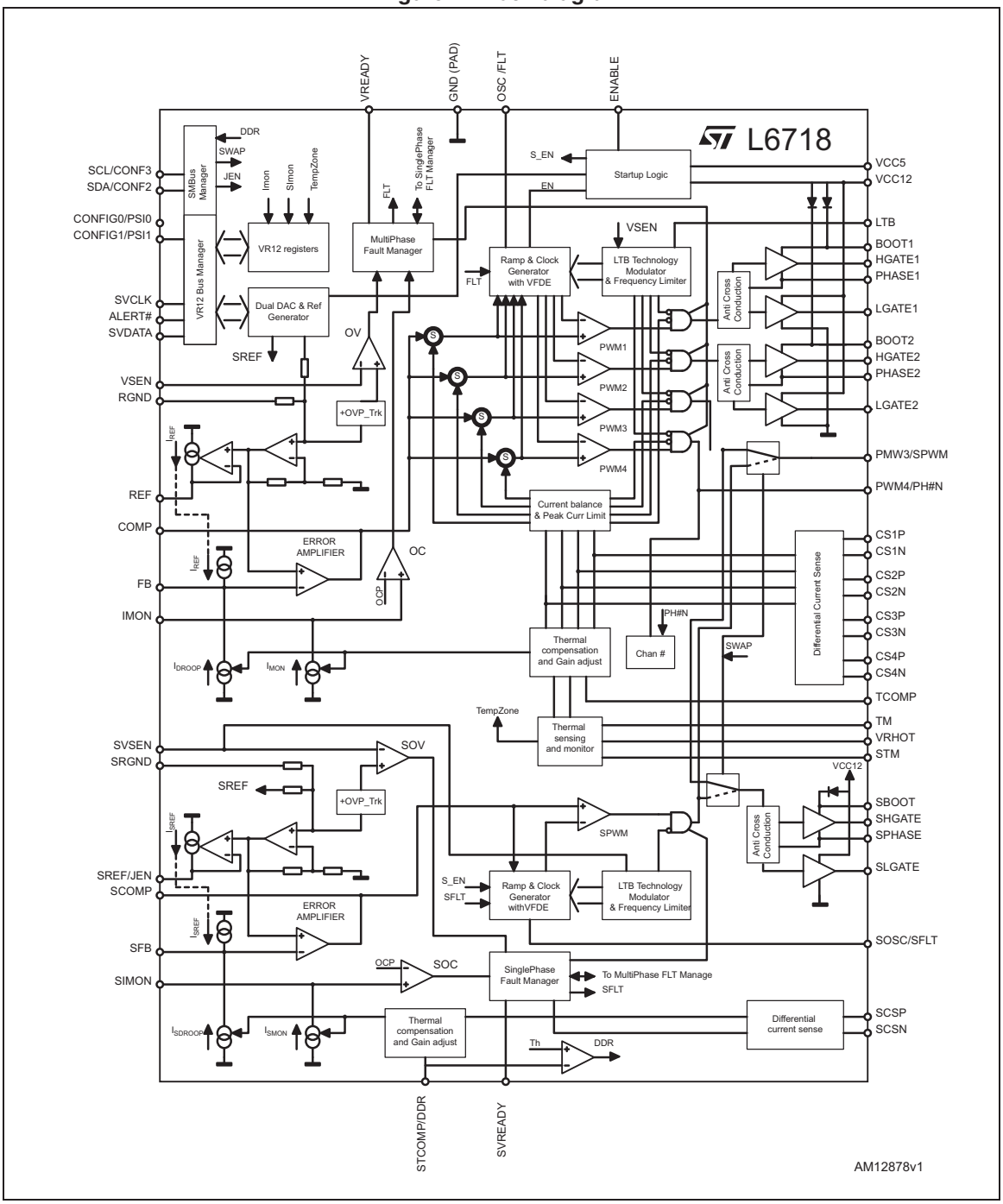


Figure 3. Typical 2-phase application circuit



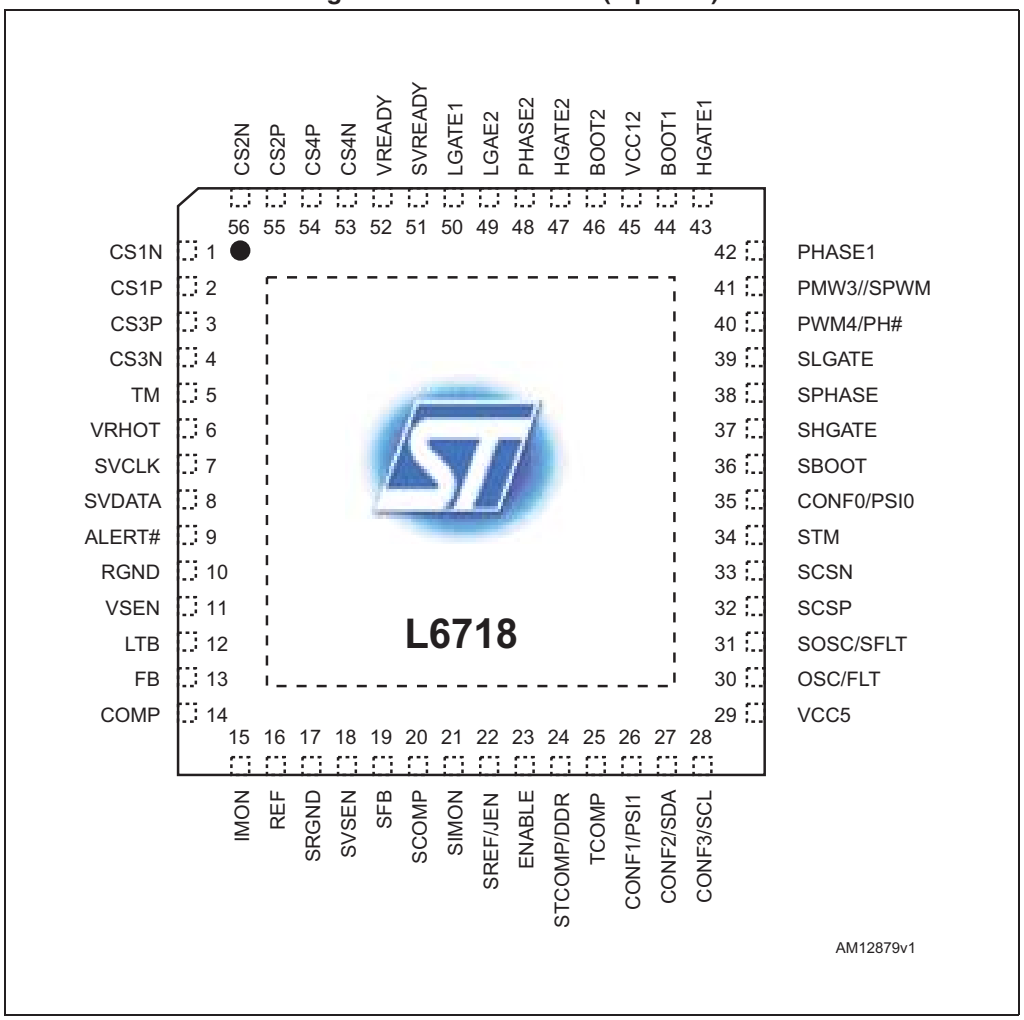
1.2 Block diagram

Figure 4. Block diagram



2 Pin description and connection diagrams

Figure 5. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin#	Name		Function
1	CS1N	MULTI-RAIL SECTION	Channel 1 current sense negative input. Connect through an R_G resistor to the output-side of channel 1 inductor. Filter the output-side of R_G with 100 nF (typ.) to GND. This pin is compared with VSEN for the feedback disconnection. See *Section 14* for proper layout of this connection.
2	CS1P		Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of channel 1 inductor. See *Section 14* for proper layout of this connection.
3	CS3P		Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of channel 3 inductor. Short to V_{OUT} when not using channel 3. See *Section 14* for proper layout of this connection.
4	CS3N		Channel 3 current sense negative input. Connect through an R_G resistor to the output-side of channel 3 inductor. Filter the output-side of R_G with 100 nF (typ.) to GND. Connect to V_{OUT} through an R_G resistor when not using channel 3. See *Section 14* for proper layout of this connection.
5	TM		Thermal monitor sensor. Connect with proper network embedding NTC to the multi-phase rail power section. The IC senses the power section temperature and uses the information to define the VRHOT signal and temperature zone register. By programming proper TCOMP gain, the IC also implements load-line thermal compensation for the multi-phase rail section. See *Section 10* for details.
6	VRHOT		Voltage regulator HOT. Open drain output, set free by controller when the temperature sensed through the TM pin exceeds TMAX (active low). See *Section 10.1* for details.
7	SVCLK	SVID BUS	Serial clock
8	SVDATA		Serial data
9	ALERT#		Alert

Table 2. Pin description (continued)

Pin#	Name		Function
10	RGND	MULTI-RAIL SECTION	Remote ground sense pin. Connect to the negative side of the load to perform remote sense. See *Section 14* for proper layout of this connection.
11	VSEN		Output voltage monitor pin. Manages OVP/UVP protection and feedback disconnection. Connect to the positive side of the load to perform remote sense. A fixed 50 uA current is sourced from this pin. See *Section 14* for proper layout of this connection.
12	LTB		Load transient boost technology input pin. Internally fixed at 1.67 V, connecting R_{LTB} - C_{LTB} vs. V_{OUT} allows the load transient boost technology to be enabled, as soon as the device detects a transient load it turns on all the phases at the same time. Short to SGND to disable the function. See *Section 12.2* for details.
13	FB		Error amplifier inverting input. Connect with an R_{FB} to VSEN and (R_F - C_F)// C_P to COMP. A current proportional to the load current is sourced from this pin in order to implement the droop effect. See *Section 8.2* for details.
14	COMP		Error amplifier output. Connect with (R_F - C_F)// C_P to FB. The device cannot be disabled by pulling down this pin.
15	IMON		Current monitor output. A current proportional to the multi-phase rail output current is sourced from this pin. Connect through a resistor R_{IMON} to GND to show a voltage proportional to the current load. Based on pin voltage level, DPM and overcurrent protection can be triggered. Filtering through C_{IMON} to GND allows control of the delay. See *Section 9.2* for R_{IMON} definition.
16	REF		The reference used for the regulation of the multi-phase rail section is available on this pin with -100 mV + offset. Connect through an R_{REF}-C_{REF} to RGND to optimize DVID transitions. See *Section 8.6* for details.

Table 2. Pin description (continued)

Pin#	Name		Function
17	SRGND	SINGLE-RAIL SECTION	Single-phase rail remote ground sense. Connect to the negative side of the single-phase rail load to perform remote sense. See *Section 14* for proper layout of this connection.
18	SVSEN		Single-rail output voltage monitor. Manages OVP/UVP protection and feedback disconnection. Connect to the positive side of the load to perform remote sense. It is also the sense for the single-phase rail LTB. Connect to the positive side of the single-phase rail load to perform remote sense. See *Section 14* for proper layout of this connection.
19	SFB		Error amplifier inverting input. Connect with a resistor R_{SFB} to SVSEN and with (R_{SF} - C_{SF})// C_{SP} to SCOMP. A current proportional to the load current is supplied from this pin in order to implement the droop effect. See *Section 8.4* for details.
20	SCOMP		Error amplifier output. Connect with an (R_{SF} - C_{SF})// C_{SP} to SFB. The device cannot be disabled by pulling this pin low.
21	SIMON		Current monitor output. A current proportional to the output current is sourced from this pin. Connect through a resistor R_{SIMON} to local GND. Based on pin voltage, overcurrent protection can be triggered. Filtering through C_{SIMON} to GND allows control of the delay for OC intervention. See *Section 9.2* for R_{SIMON} definition.
22	SREF/JEN		The reference used for the regulation of the single-rail section is available on this pin with -100 mV + offset. Connect through an R_{SREF}-C_{SREF} to SRGND to optimize DVID transitions. See *Section 8.6* for details. If Jmode is selected by Config1 pinstrapping, this pin is used as a logic input for the single-phase rail enable. Pulling this pin up above 0.8 V, the single-phase rail turns on.
23	ENABLE		Enable pin. External pull-up is needed on this pin. Forced low to disable the device with all MOSFETs OFF: all protection is disabled except for preliminary overvoltage. Over 0.65 V the device turns up. Cycle this pin to recover latch from protection, filter with 1 nF (typ.) to GND.
24	STCOMP/ DDR	SINGLE-RAIL SECTION	Thermal monitor sensor gain and DDR selected. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by ST to implement thermal compensation for the single-phase rail. See *Section 10* for details. Short to GND to disable thermal compensation and set the device to DDR mode.

Table 2. Pin description (continued)

Pin#	Name	Function	
25	TCOMP	MULTI-RAIL SECTION	Thermal monitor sensor gain. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by TM to implement thermal compensation for the multi-phase rail. Short to GND to disable the single NTC thermal compensation for multi-phase section. See *Section 10* for details.
26	CONFIG1/ PSI1	PINSTRAPPING	Connect a resistor divider to GND and VCC5 to define power management configuration. See *Section 6.6* for details. At the end of the soft-start, this pin is internally pulled up or pulled down to indicate the power status. See *Table 17* for details.
27	SDA / CONFIG2	SMBus / PINSTRAPPING	If SMBus power management is enabled through Config0 pinstrapping, connect to data signal of SMBus communicator. If SMBus power management is disabled through Config0 pinstrapping, connect a resistor divider to GND and VCC5 to define power management characteristics. See *Section 6.6.5* for details.
28	SCL / CONFIG3		If SMBus power management is enabled through Config0 pinstrapping, connect to clock signal of SMBus communicator. If SMBus power management is disabled through Config0 pinstrapping, connect a resistor divider to GND and VCC5 to define power management characteristics. See *Section 6.6.5* for details.
29	VCC5		Main IC power supply. Operative voltage is connected to 5 V filtered with 1 µF MLCC to GND.
30	OSC/FLT	MULTI-RAIL SECTION	Oscillator pin for multi-phase rail. Allows the programming of the switching frequency F_{SW} for multi-phase section. The equivalent switching frequency at the load side results in being multiplied by the number of phases active. The pin is internally set to 1.8 V, frequency is programmed according to a resistor connected to GND or VCC with a gain of 10 kHz/µA. Free running is set to 200 kHz. The pin is forced high (3.3 V) if a fault is detected on a multi-rail section. To recover from this condition, it is necessary to cycle VCC or enable. See *Section 11* for details.
31	SOSC / SFLT	SINGLE-RAIL SECTION	Oscillator pin for single-phase. Allows the programming of the switching frequency F_{SW} for the single-phase section. The pin is internally set to 1.8 V, frequency is programmed according to the resistor connected to GND or VCC with a gain of 10 kHz/µA. Free running is set to 200 kHz. The pin is forced high (3.3 V) if a fault is detected on a single-phase rail section. To recover from this condition, it is necessary to cycle VCC or enable. See *Section 11* for details.

Table 2. Pin description (continued)

Pin#	Name		Function
32	SCSP	SINGLE-RAIL SECTION	Single-phase rail current sense positive input. Connect through an R-C filter to the phase-side of single-phase rail inductor. See *Section 14* for proper layout of this connection.
33	SCSN		Single-phase rail current sense negative input. Connect through an R_G resistor to the output-side of single-phase rail inductor. Filter the output-side of R_G with 100 nF (typ.) to GND. See *Section 14* for proper layout of this connection.
34	STM		Thermal monitor sensor. Connect with proper network embedding NTC to the single-phase power section. The IC senses the hot spot temperature and uses the information to define the VRHOT signal and temperature zone register. By programming proper STCOMP gain, the IC also implements load-line thermal compensation for the single-phase section. Short to GND if not used. See *Section 10* for details.
35	CONFIG0 /PSI0	PINSTRAPPING	Connect a resistor divider to GND and VCC5 to define power management characteristics. See *Section 6.6* for details. At the end of the soft-start, this pin is internally pulled up or pulled down to indicate the power status. See *Table 17* for details.
36	SBOOT	SINGLE-RAIL SECTION	Single-phase rail high-side driver supply. Connect through a capacitor (220 nF typ.) and a resistor (2.2 Ohm) to SPHASE and provide a Schottky bootstrap diode. A small resistor in series to the boot diode helps to reduce boot capacitor overcharge.
37	SHGATE		Single-phase rail high-side driver output. It must be connected to the HS MOSFET gate. A small series resistor helps to reduce the device-dissipated power and the negative phase spike.
38	SPHASE		Single-phase rail high-side driver return path. It must be connected to the HS MOSFET source and provides return path for the HS driver.
39	SLGATE		Single-phase rail low-side driver output. It must be connected to the low-side MOSFET gate. A small series resistor helps to reduce device-dissipated power.
40	PWM4 / PH#		Fourth phase PWM output of the multi-phase rail and phase number selection pin. Internally pulled up to 3.3 V, connect to external driver PWM4 when channel 4 is used. The device is able to manage the HiZ by setting the pin floating. Short to GND or leave floating to 3/2 phase operation, see *Table 7* for details.

Table 2. Pin description (continued)

Pin#	Name	Function	
41	PWM3 / SPWM		Third phase PWM output of multi-phase rail or PWM output for single-phase rail. Connect to external driver PWM input if this channel is used. Internally pull up to 3.3 V, connect to external driver PWM3 when channel 3 is used (see *Table 7* for details). The device is able to manage HiZ status by setting the pin floating. If SWAP mode is selected by pinstrapping Config0, it must be connected to single-phase external driver SPWM, see *Section 6.3* for details.
42	PHASE1	MULTI-RAIL SECTION	Channel 1 HS driver return path. It must be connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.
43	HGATE1		Channel 1 HS driver output. It must be connected to the HS1 MOSFET gate. A small series resistor helps to reduce the device-dissipated power and the negative phase spike.
44	BOOT1		Channel 1 HS driver supply. Connect through a capacitor (220 nF typ.) and a resistor (2.2 Ohm typ.) to PHASE1 and provide a Schottky bootstrap diode. A small resistor in series to the boot diode helps to reduce boot capacitor overcharge.
45	VCC12		7 V supply. It is the low-side driver supply. It must be connected to the 7 V bus and filtered with 2 x 1 µf MLCC caps vs. GND.
46	BOOT2	MULTI-RAIL SECTION	Channel 2 high-side driver supply. Connect through a capacitor (220 nF typ.) and a resistor (2.2 Ohm typ.) to PHASE2 and provide a Schottky bootstrap diode. A small resistor in series to the boot diode helps to reduce boot capacitor overcharge.
47	HGATE2		Channel 2 high-side driver output. It must be connected to the HS2 MOSFET gate. A small series resistor helps to reduce the device-dissipated power and the negative phase spike
48	PHASE2		Channel 2 HS driver return path. It must be connected to the HS2 MOSFET source and provides a return path for the HS driver of channel 2.
49	LGATE2		Channel 2 low-side driver output. It must be connected to the LS2 MOSFET gate. A small series resistor helps to reduce device-dissipated power.
50	LGATE1		Channel 1 low-side driver output. It must be connected to the LS1 MOSFET gate. A small series resistor helps to reduce device-dissipated power.
51	SVREADY		Single-phase rail VREADY Open drain output set free after SS has finished and pulled low when triggering any protection on the single-phase rail. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.

Table 2. Pin description (continued)

Pin#	Name	Function	
52	VREADY	MULTI-RAIL SECTION	Multi-phase rail VREADY Open drain output set free after SS has finished and pulled low when triggering any protection on multi-phase rail. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating
53	CS4N		Channel 4 current sense negative input. Connect through an R_G resistor to the output-side of channel 4 inductor. Filter the output-side of R_G with 100 nF (typ.) to GND. Connect to V_{OUT} through an R_G resistor when not using channel 4. See *Section 14* for proper layout of this connection.
54	CS4P		Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of channel 3 inductor. Short to V_{OUT} when not using channel 4. See *Section 14* for proper layout of this connection.
55	CS2P		Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of channel 2 inductor. See *Section 14* for proper layout of this connection.
56	CS2N		Channel 2 current sense negative input. Connect through an R_G resistor to the output-side of channel 2 inductor. Filter the output-side of R_G with 100 nF (typ.) to GND. See *Section 14* for proper layout of this connection.
PAD	GND		GND connection. Exposed pad connects also the silicon substrate. It makes a good thermal contact with the PCB to dissipate the internal power. All internal references and logic are referenced to this pin. Connect to power GND plane using 5.3 x 5.3 mm square area on the PCB and with 9 vias (uniformly distributed) to improve electrical and thermal conductivity.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient (device soldered on 2s2p PC board)	27	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-25 to 125	°C
P_{tot}	Maximum power dissipation at T_{amb} = 25 °C	2.5	W

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC12	To GND	-0.3 to 7.5	V
V_{BOOTX}-V_{PHASEx}		-0.3 to VCC12 + 0.3	V
	Positive peak voltage t<400 ns	15	V
V_{UGATEx}-V_{PHASEx}		-0.3 to VCC12 + 0.3	V
LGATEx to GND		-0.3 to VCC12 + 0.3	V
V_{PHASEX}	Negative peak voltage to GND t< 400 ns. BOOT>3.5 V	-8	V
	Positive peak voltage to GND t< 200 ns	35	V
VCC5, STM, TM, PWM3, PWM4, SIMAX,IMAX, CONFIGX,	To GND	-0.3 to 7	V
All other pins	To GND	-0.3 to 3.6	V
Maximum withstanding voltage range test condition: JEDEC/JS001- “human body model” acceptance criteria: “normal performance”	BOOTx	± 500	V
	Other pins	± 1000	V

3.2 Electrical characteristics

(V_{CC} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified).

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CC5}	VCC5 supply current	ENABLE = High		20		mA
		ENABLE = Low		15		mA
I_{CC12}	VCC12 supply current	ENABLE = High; Lgate open Phase to GND; BOOT=7 V		12		mA
		ENABLE = Low		1		mA
I_{BOOTX}	BOOTX supply current	ENABLE = High; Ugate open Phase to GND; BOOT=7 V		0.9		mA
Power-on						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$UVLO_{VCC5}$	VCC5 turn-on	VCC5 rising			4.1	V
	VCC5 turn-off	VCC5 falling	3			V
$UVLO_{VCC12}$	VCC12 turn-on	VCC12 rising			4.75	V
	VCC12 turn-off	VCC12 falling	4			V
Oscillator, soft-start and enable						
MP F_{SW}	Initial oscillator accuracy	OSC = open	180	200	220	kHz
MP F_{SW}	Initial oscillator accuracy	OSC = 62 K	429	475	521	kHz
SP F_{SW}	Initial oscillator accuracy	OSC = open	180	200	220	kHz
SP F_{SW}	Initial oscillator accuracy	OSC = 62 K	450	500	550	kHz
V_{OSC}	PWM ramp amplitude			1.5		V
FAULT	Voltage at pin SOSC	After latch	3			V
	Voltage at pin OSC	After latch	3			V
SOFT START	SS time	Vboot > 0, from pinstrapping; multi-phase section	2.5	2.8	3.1	mV/µs
		Vboot > 0, from pinstrapping; single-phase section	2.5	2.8	3.1	mV/µs
ENABLE	Turn-on	V_{ENABLE} rising			0.65	V
	Turn-off	V_{ENABLE} falling	0.4			V
SVI Serial Bus						
SVCLCK, SVDATA	Input high		0.6			V
	Input low				0.4	V
SVDATA, ALERT#	Voltage low (ACK)	I_{SINK} = -5 mA			50	mV
Reference and current reading						
K_{VID}	V_{OUT} accuracy (MPhase)	I_{OUT}=0 A; N=4; R_G= 810 Ω; R_{FB}=2.125 kΩ	-0.5		0.5	%
K_{SVID}	V_{OUT} accuracy (SPhase)	I_{OUT}=0 A R_G=1.1 kΩ; R_{FB} = 6.662 kΩ	-0.5		0.5	%
DROOP	LL accuracy (MPhase) 0 to full load	I_{INFOx}=0; N=4; VID>1 V R_G=810 Ω; R_{FB}=2.125 kΩ	-2.5		2	µA
DROOP	LL accuracy (MPhase) 0 to full load	I_{INFOx}=20 µA; N=4; VID>1 V R_G=810 Ω; R_{FB}=2.125 kΩ	-3.5		4	µA
SDROOP	LL accuracy (SPhase) 0 to full load	I_{SCSN}=0; VID>1 V R_G=1.1 kΩ; R_{FB}=6.662 kΩ	-0.75		0.75	µA
SDROOP	LL accuracy (SPhase) 0 to full load	I_{SCSN}=20 µA;VID>1 V R_G=1.1 kΩ; R_{FB}=6.662 kΩ	-1.5		1.5	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
k_{IMON}	IMON accuracy (MPhase)	I_{INFOx}=0 µA; N=4; R_G=810 Ω; R_{FB}=2.125 kΩ	-1.5		1.5	µA
		I_{INFOx}=20 µA; N=4; R_G=810 Ω; R_{FB}=2.125 kΩ	-2		2	µA
k_{SIMON}	SIMON accuracy (SPhase)	I_{SCSN}=0 µA; R_G=1.1 kΩ; R_{FB}=6.662 kΩkΩ	-0.75		0.75	µA
		I_{SCSN}=20 µA; R_G=1.1 kΩ; R_{FB}=6.662	-1		1	µA
A_0	EA DC gain			100		dB
SR	Slew rate	COMP, SCOMP to GND = 10 pF		20		V/µs
DVID	Slew rate fast	Multi-phase section	10			mV/µs
	Slew rate slow		2.5			mV/µs
DVID	Slew rate fast	Single-phase section	10			mV/µs
	Slew rate slow		2.5			mV/µs
IMON ADC	GetReg(15h)	V_{IMON} = 0.992 V		CC		Hex
	Accuracy		C0		CF	Hex
PWM OUTPUTS						
PWM3 / SPWM	Output high	I = 1 mA		5		V
	Output low	I = -1 mA			0.2	V
I_{PWM3},I_{PWM4}	Pull-up current			10		µA
Protection (both sections)						
OVP	Overvoltage protection	VSEN rising; wrt Ref.		+175		mV
		VSEN rising; wrt Ref.		+500		mV
UVP	Undervoltage protection	VSEN falling; wrt Ref; Ref > 500 mV		-500		mV
FBR DISC	FB disconnection	Vcs - rising above VSEN/SVSEN		+700		
FBG DISC	FBG disconnection	EA NI input wrt VID		+500		
VREADY, SVREADY, VRHOT	Voltage low	I = - 4 mA			0.4	V
V_{OC_TOT}	Overcurrent threshold	V_{IMON}, V_{SIMON} rising		1.70		V
				1.55		V
I_{OC_TH}	Constant current			35		µA
VRHOT	Voltage low	I_{SINK} = -5 mA			13	mΩ
Gate drives control						
t_{RISE_UGATE}	High-side rise time	BOOTx - PHASEx =7 V C_{UGATE} to GND=3.3 nF		20		ns

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{UGATEx}	High-side source current	BOOTx - PHASEx =7 V		TBD		A
R_{UGATEx}	High-side sink resistance	BOOTx - PHASEx =7 V; 100 mA		2.1		Ω
t_{RISE_LGATE}	Low-side rise time	VCC12 =7 V C_{LGATE} to GND=5.6 nF		20		ns
I_{LGATEx}	Low-side source current	VCC12 = 7 V		TBD		A
R_{LGATEx}	Low-side sink resistance	VCC12 = 7 V; 100 mA		2		Ω

4 VID tables

Table 6. VID table, both sections, commanded through serial bus

HEX code		VOUT [V]	HEX code		VOUT [V]	HEX code		VOUT [V]	HEX code		VOUT [V]
0	0	0.000	4	0	0.565	8	0	0.885	C	0	1.205
0	1	0.250	4	1	0.570	8	1	0.890	C	1	1.210
0	2	0.255	4	2	0.575	8	2	0.895	C	2	1.215
0	3	0.260	4	3	0.580	8	3	0.900	C	3	1.220
0	4	0.265	4	4	0.585	8	4	0.905	C	4	1.225
0	5	0.270	4	5	0.590	8	5	0.910	C	5	1.230
0	6	0.275	4	6	0.595	8	6	0.915	C	6	1.235
0	7	0.280	4	7	0.600	8	7	0.920	C	7	1.240
0	8	0.285	4	8	0.605	8	8	0.925	C	8	1.245
0	9	0.290	4	9	0.610	8	9	0.930	C	9	1.250
0	A	0.295	4	A	0.615	8	A	0.935	C	A	1.255
0	B	0.300	4	B	0.620	8	B	0.940	C	B	1.260
0	C	0.305	4	C	0.625	8	C	0.945	C	C	1.265
0	D	0.310	4	D	0.630	8	D	0.950	C	D	1.270
0	E	0.315	4	E	0.635	8	E	0.955	C	E	1.275
0	F	0.320	4	F	0.640	8	F	0.960	C	F	1.280
1	0	0.325	5	0	0.645	9	0	0.965	D	0	1.285
1	1	0.330	5	1	0.650	9	1	0.970	D	1	1.290
1	2	0.335	5	2	0.655	9	2	0.975	D	2	1.295
1	3	0.340	5	3	0.660	9	3	0.980	D	3	1.300
1	4	0.345	5	4	0.665	9	4	0.985	D	4	1.305
1	5	0.350	5	5	0.670	9	5	0.990	D	5	1.310
1	6	0.355	5	6	0.675	9	6	0.995	D	6	1.315
1	7	0.360	5	7	0.680	9	7	1.000	D	7	1.320
1	8	0.365	5	8	0.685	9	8	1.005	D	8	1.325
1	9	0.370	5	9	0.700	9	9	1.010	D	9	1.330
1	A	0.375	5	A	0.705	9	A	1.015	D	A	1.335
1	B	0.380	5	B	0.710	9	B	1.020	D	B	1.340
1	C	0.385	5	C	0.715	9	C	1.025	D	C	1.345
1	D	0.390	5	D	0.720	9	D	1.030	D	D	1.350
1	E	0.395	5	E	0.725	9	E	1.035	D	E	1.355

Table 6. VID table, both sections, commanded through serial bus (continued)

HEX code		VOUT [V]	HEX code		VOUT [V]	HEX code		VOUT [V]	HEX code		VOUT [V]
1	F	0.400	5	F	0.730	9	F	1.040	D	F	1.360
2	0	0.405	6	0	0.735	A	0	1.045	E	0	1.365
2	1	0.410	6	1	0.740	A	1	1.050	E	1	1.370
2	2	0.415	6	2	0.745	A	2	1.055	E	2	1.375
2	3	0.420	6	3	0.750	A	3	1.060	E	3	1.380
2	4	0.425	6	4	0.755	A	4	1.065	E	4	1.385
2	5	0.430	6	5	0.760	A	5	1.070	E	5	1.390
2	6	0.435	6	6	0.765	A	6	1.075	E	6	1.395
2	7	0.440	6	7	0.770	A	7	1.080	E	7	1.400
2	8	0.445	6	8	0.775	A	8	1.085	E	8	1.405
2	9	0.450	6	9	0.780	A	9	1.090	E	9	1.410
2	A	0.455	6	A	0.785	A	A	1.095	E	A	1.415
2	B	0.460	6	B	0.790	A	B	1.100	E	B	1.420
2	C	0.465	6	C	0.795	A	C	1.105	E	C	1.425
2	D	0.470	6	D	0.800	A	D	1.110	E	D	1.430
2	E	0.475	6	E	0.805	A	E	1.115	E	E	1.435
2	F	0.480	6	F	0.810	A	F	1.120	E	F	1.440
3	0	0.485	7	0	0.815	B	0	1.125	F	0	1.445
3	1	0.490	7	1	0.820	B	1	1.130	F	1	1.450
3	2	0.495	7	2	0.825	B	2	1.135	F	2	1.455
3	3	0.500	7	3	0.830	B	3	1.140	F	3	1.460
3	4	0.505	7	4	0.835	B	4	1.145	F	4	1.465
3	5	0.510	7	5	0.840	B	5	1.150	F	5	1.470
3	6	0.515	7	6	0.845	B	6	1.155	F	6	1.475
3	7	0.520	7	7	0.850	B	7	1.160	F	7	1.480
3	8	0.525	7	8	0.855	B	8	1.165	F	8	1.485
3	9	0.530	7	9	0.860	B	9	1.170	F	9	1.490
3	A	0.535	7	A	0.865	B	A	1.175	F	A	1.495
3	B	0.540	7	B	0.870	B	B	1.180	F	B	1.500
3	C	0.545	7	C	0.875	B	C	1.185	F	C	1.505
3	D	0.550	7	D	0.880	B	D	1.190	F	D	1.510
3	E	0.555	7	E	0.905	B	E	1.195	F	E	1.515
3	F	0.560	7	F	0.880	B	F	1.200	F	F	1.520