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# L6740L

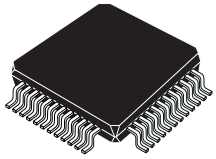
## Hybrid controller (4+1) for AMD SVID and PVID processors

## Features

- Hybrid controller: compatible with PVI and SVI CPUs
- Dual controller: 2 to 4 scalable phases for CPU CORE, 1 phase for NB
- Dual-edge asynchronous architecture with LTB Technology$^{tm}$
- PSI management to increase efficiency in light-load conditions
- Dual over-current protection: Average and per-phase
- Load indicator (CORE section)
- Logic level support for LVDDRIII
- Voltage positioning
- Dual remote sense
- Adjustable independent reference offset
- Feedback disconnection protection
- Programmable OV protection
- Oscillator internally fixed at 150 kHz externally adjustable
- LSLess startup to manage pre-biased output
- Flexible driver support
- HTQFP48 package

## Applications

- Hybrid high-current VRM, VRD for desktop, server, workstation, IPC CPUs supporting PVI and SVI interface
- High-density DC / DC converters



**HTQFP48**

## Description

L6740L is a hybrid CPU power supply controller compatible with both parallel (PVI) and serial (SVI) protocols for AMD processors.

The device embeds two independent control loops for the CPU core and the integrated NB, each one with its own set of protections. L6740L is able to work in single-plane mode, addressing only the CORE section, according to the parallel DAC codification. When in dual-plane mode, it is compatible with the AMD SVI specification addressing the CPU and NB voltages according to the SVI bus commands.

The dual-edge asynchronous architecture is optimized by LTB Technology$^{tm}$ allowing fast load-transient response minimizing the output capacitor and reducing the total BOM cost.

PSI management allows the device to selectively turn-off phases when the CPU is in low-power states increasing the over-all efficiency.

Fast protection against load over current is provided for both the sections. Furthermore, feedback disconnection protection prevents from damaging the load in case of disconnections in the system board.

**Table 1. Device summary**

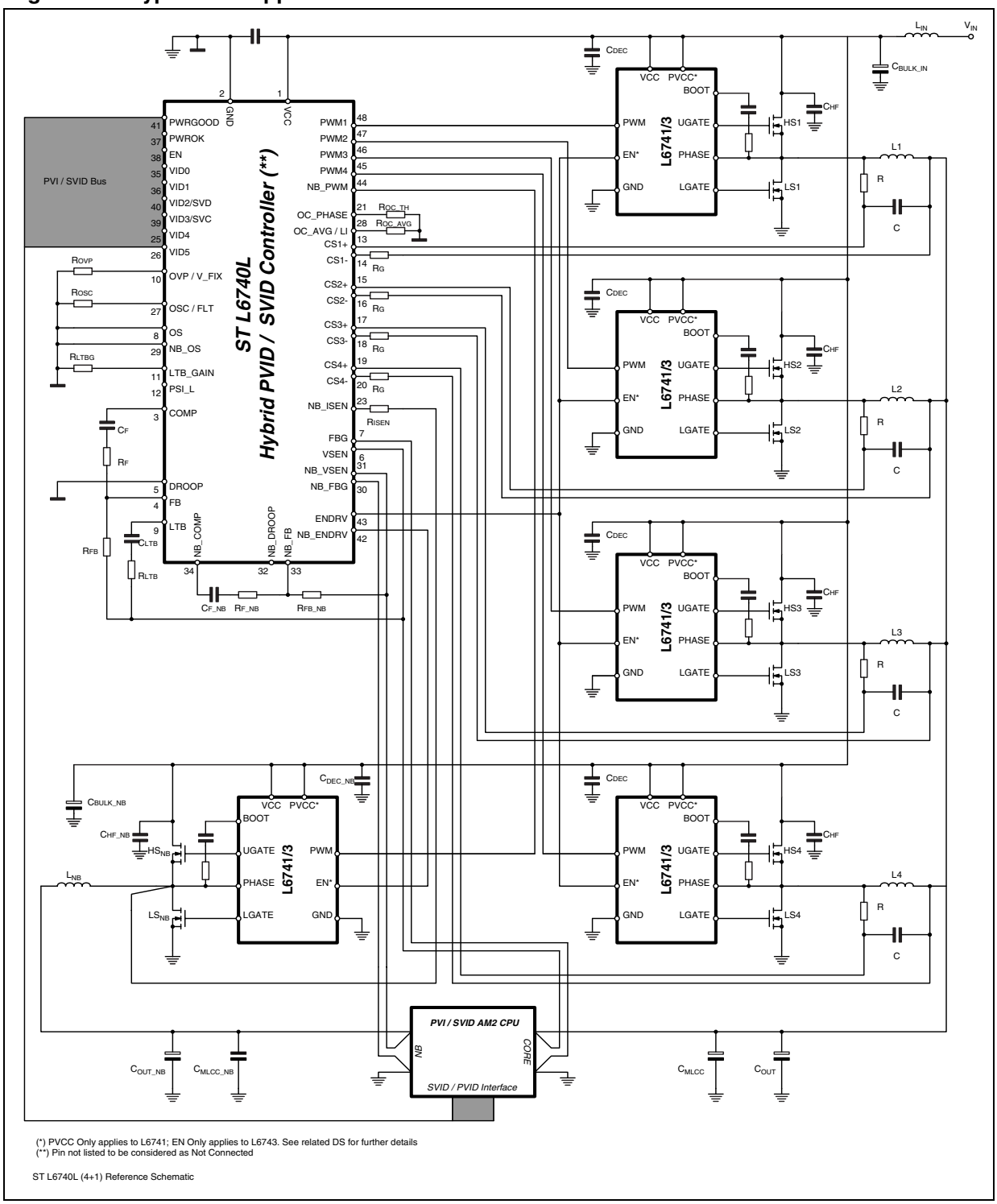
| Order codes | Package | Packaging |
|---|---|---|
| L6740L | HTQFP48 | Tube |
| L6740LTR | HTQFP48 | Tape and reel |

# Contents

# 1 Typical application circuit and block diagram

## 1.1 Application circuit

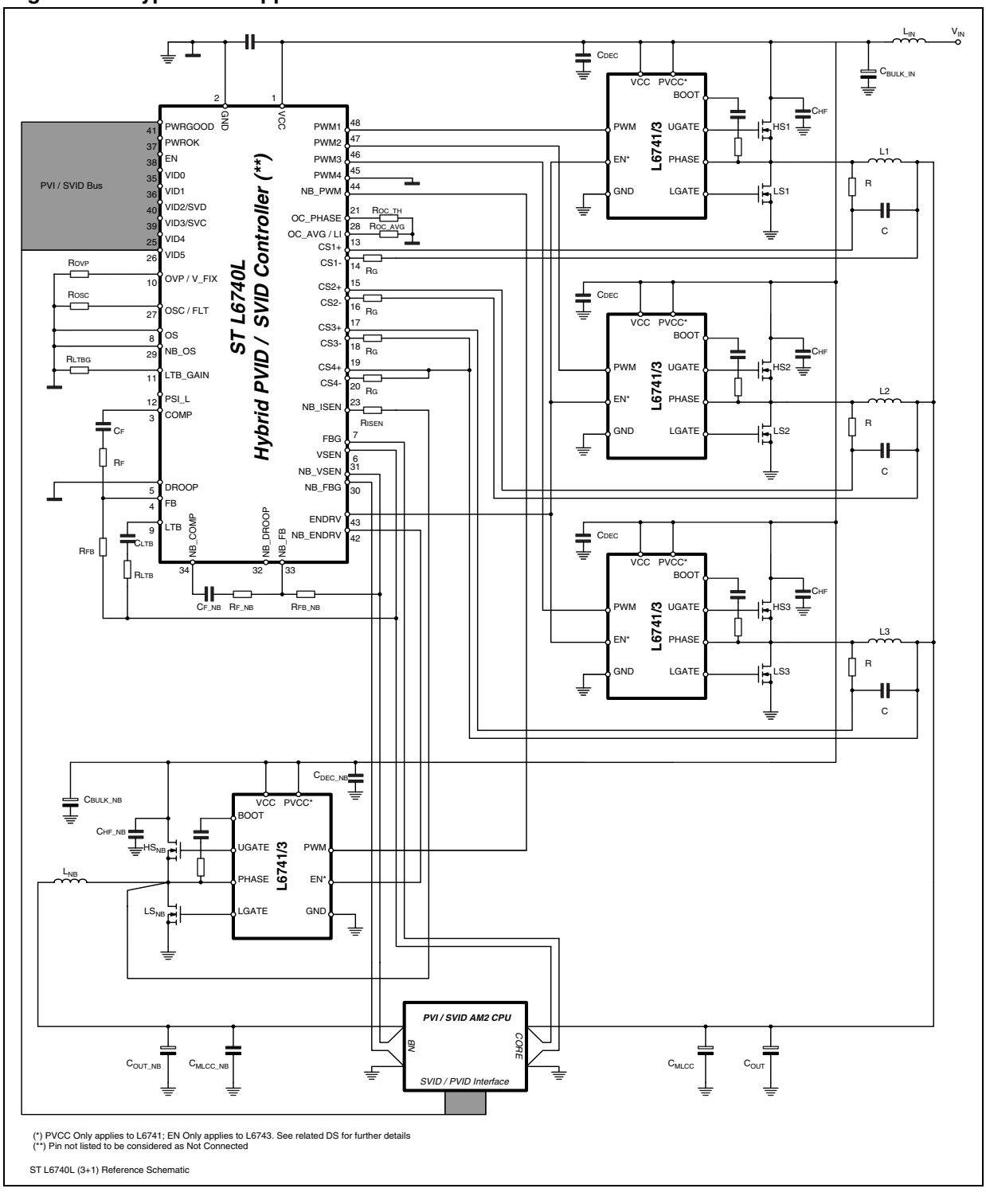
**Figure 1. Typical 4+1 application circuit**




(*) PVCC Only applies to L6741; EN Only applies to L6743. See related DS for further details
(**) Pin not listed to be considered as Not Connected

ST L6740L (4+1) Reference Schematic

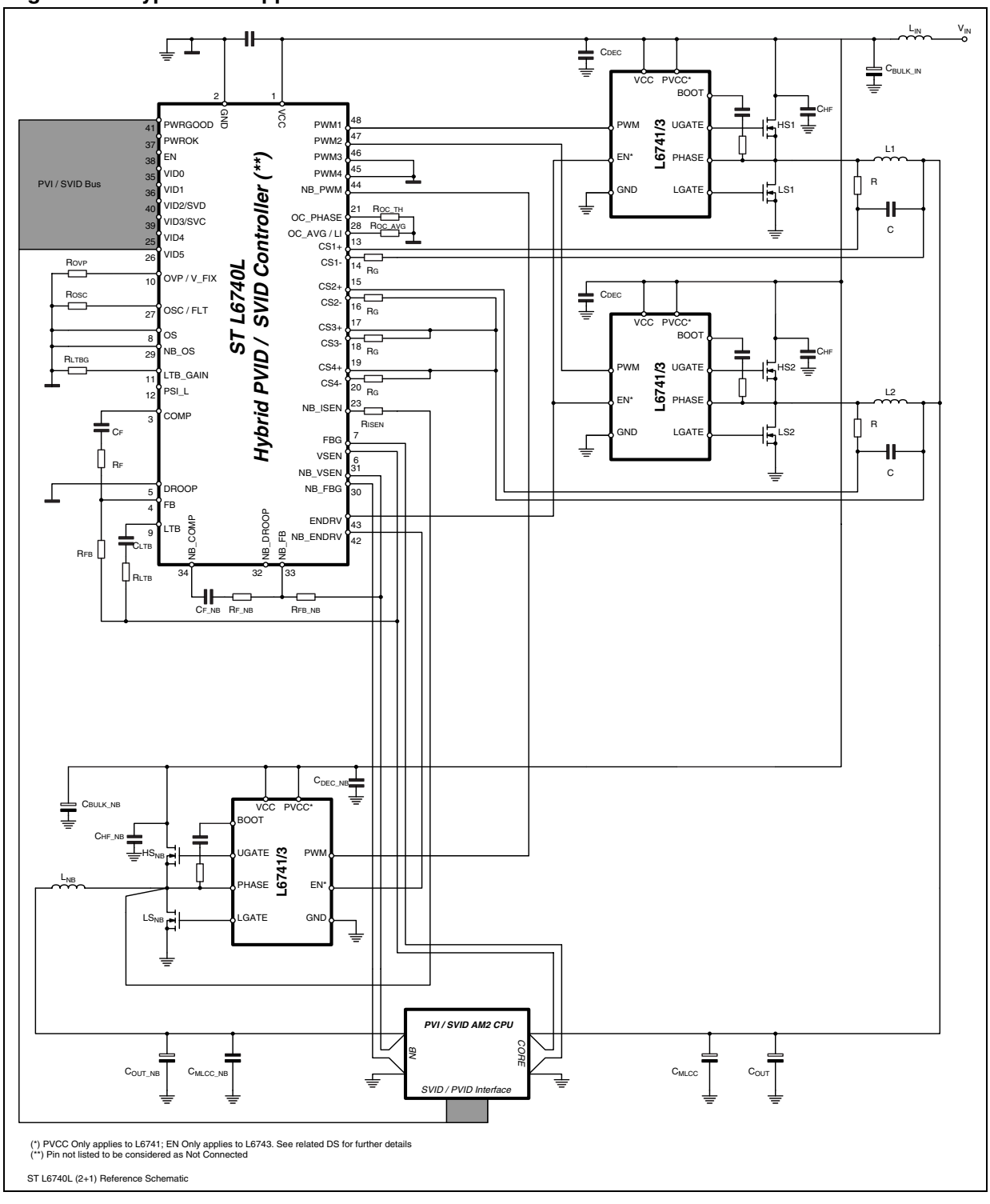
**Figure 2. Typical 3+1 application circuit**




(*) PVCC Only applies to L6741; EN Only applies to L6743. See related DS for further details
(**) Pin not listed to be considered as Not Connected

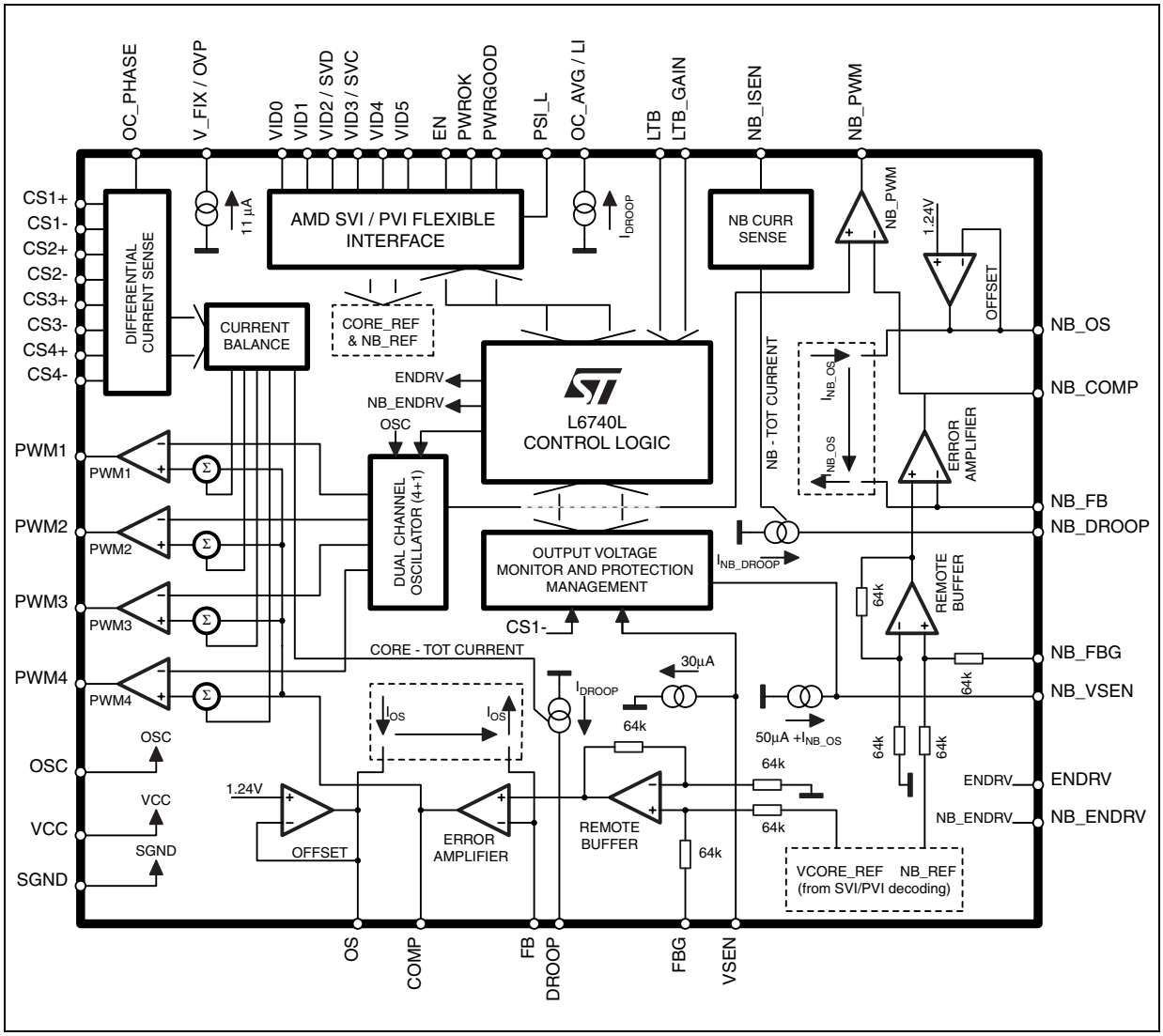
ST L6740L (3+1) Reference Schematic

**Figure 3. Typical 2+1 application circuit**



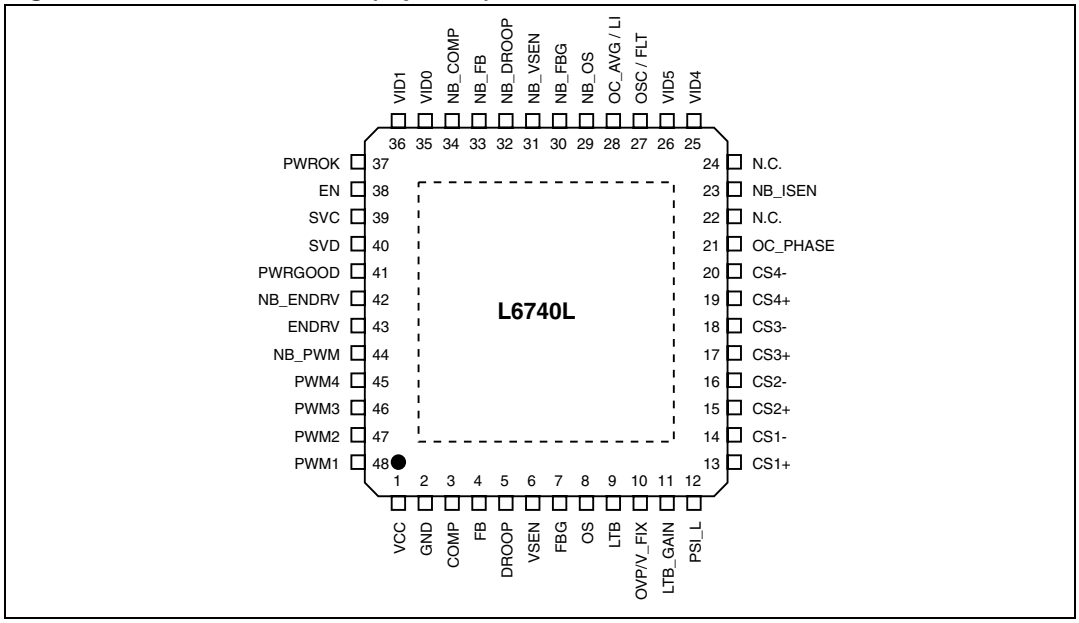
## 1.2 Block diagram

**Figure 4. Block diagram**



# 2 Pins description and connection diagrams

**Figure 5. Pins connection (top view)**




## 2.1 Pin descriptions

**Table 2. Pin description**

| Pin# | | Name | Function |
|---|---|---|---|
| 1 | | VCC | Device power supply.<br>Operative voltage is 12V ±15%. Filter with 1µF MLCC to SGND. |
| 2 | | SGND | All the internal references are referred to this pin. Connect to the PCB signal ground. |
| 3 | Core section | COMP | Error amplifier output.<br>Connect with an $R_F$ - $C_F$ to FB. The CORE section or the device cannot be disabled by grounding this pin. |
| 4 | | FB | Error amplifier inverting input.<br>Connect with a resistor $R_{FB}$ to VSEN and with an $R_F$ - $C_F$ to COMP. Offset current programmed by OS is sunk through this pin. |
| 5 | | DROOP | A current proportional to the total current read is sourced from this pin according to the current reading gain.<br>Short to FB to implement droop function, if not used, short to SGND. |
| 6 | | VSEN | Output voltage monitor.<br>It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the load for remote sensing. See *Section 7* for details. |

**Table 2. Pin description (continued)**

| Pin# | | Name | Function |
|---|---|---|---|
| 7 | Core section | FBG | Remote ground sense.<br>Connect to the negative side of the load for remote sensing. See *Section 9* for proper layout of this connection. |
| 8 | | OS | Offset programming pin.<br>Internally set to 1.24 V. Connecting a $R_{OS}$ resistor to SGND allows to set a current that is mirrored into FB pin in order to program a positive offset according to the selected $R_{FB}$.<br>Short to SGND to disable the function. See *Section 6.4* for details. |
| 9 | | LTB | LTB Technology™ input pin.<br>Connect through an $R_{LTB}$ - $C_{LTB}$ network to the regulated voltage (CORE section) to detect load transient. See *Section 10* for details. |
| 10 | | OVP / V_FIX | *OVP.* Overvoltage programming pin. Internally pulled-up to 3.3 V by 11 µA. Connect to SGND through a $R_{OVP}$ resistor and filter with 10 nF (typ) to set a fixed voltage according to the $R_{OVP}$ resistor. If floating it will program 3.3 V threshold. See *Section 7* for details.<br>*V_FIX - Hardware override.* Short to SGND to enter VFIX mode (WARNING: this condition overrides any code programmed on the VIDx lines). In this case, the device will use SVI inputs as static VIDs and OVP threshold will be set to 1.8 V. See *Section 5.4.5* for details. |
| 11 | Core section | LTB_GAIN | LTB Technology™ gain pin.<br>Connect to SGND through a resistor $R_{LTBGAIN}$ to program the LTB Gain. See *Section 10* for details. |
| 12 | | PSI_L | Power saving indicator (SVI mode).<br>Open-drain input/output pin. See *Section 5.4.3* for details. |
| 13 | Core section | CS1+ | Channel 1 current sense positive Input. Connect through an R-C filter to the phase-side of the channel 1 inductor.<br>See *Section 9* for proper layout of this connection. |
| 14 | | CS1- | Channel 1 current sense negative input. Connect through a $R_G$ resistor to the output-side of the channel inductor.<br>See *Section 9* for proper layout of this connection. |
| 15 | | CS2+ | Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.<br>See *Section 9* for proper layout of this connection. |
| 16 | | CS2- | Channel 2 current sense negative input. Connect through a $R_G$ resistor to the output-side of the channel inductor.<br>See *Section 9* for proper layout of this connection. |
| 17 | | CS3+ | Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2 phase, directly connect to $V_{out\_CORE}$.<br>See *Section 9* for proper layout of this connection. |
| 18 | | CS3- | Channel 3 current sense negative input. Connect through a $R_G$ resistor to the output-side of the channel inductor. When working at 2 phase, connect through $R_G$ to CS3+.<br>See *Section 9* for proper layout of this connection. |

**Table 2. Pin description (continued)**

| Pin# | | Name | Function |
|---|---|---|---|
| 19 | Core section | CS4+ | Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at 2 or 3 phase, directly connect to $V_{out\_CORE}$.<br>See *Section 9* for proper layout of this connection. |
| 20 | | CS4- | Channel 4 current sense negative input. Connect through a $R_G$ resistor to the output-side of the channel inductor. When working at 2 or 3 phase, connect through $R_G$ to CS4+.<br>See *Section 9* for proper layout of this connection. |
| 21 | | OC_PHASE | Per-phase over-current (CORE section).<br>Internally set to 1.24 V, connecting to SGND with a resistor $R_{OC\_TH}$ it programs the OC threshold per-phase. See *Section 7.4.1* for details. |
| 22 | | NC | Not internally connected. |
| 23 | NB section | NB_ISEN | NB current sense pin.<br>Used for NB voltage positioning and NB_OCP. Connect through a resistor $R_{ISEN}$ to the relative LS Drain. See *Section 7.4* for details. |
| 24 | | NC | Not internally connected. |
| 25, 26 | PVI interface | VID4, VID5 | Voltage IDentification pins.<br>Internally pulled-low by 10 µA, they are used to program the output voltage. Used only in PVI-mode, ignored when in SVI-mode.<br>See *Section 5* for details. |
| 27 | | OSC / FLT | *OSC*: It allows programming the switching frequency $F_{SW}$ of both sections. Switching frequency can be increased according to the resistor $R_{OSC}$ connected from the pin to. SGND with a gain of 6.8 kHz/µA (see *Section 8* for details). If floating, the switching frequency is 150 kHz per phase.<br>*FLT*: The pin is forced high (3.3 V) in case of an OV / UV fault. To recover from this condition, cycle VCC or the EN pin. See *Section 7* for details. |
| 28 | Core section | OC_AVG / LI | Average over-current and load indicator pin.<br>A current proportional to the current delivered by the CORE section (a copy of the DROOP current) is sourced through this pin.<br>The average-OC threshold is programmed by connecting a resistor $R_{OC\_AVG}$ to SGND. When the generated voltage crosses the OC_AVG threshold ($V_{OC\_AVGTH}$ = 2.5 V Typ) the device latches with all mosfets OFF (to recover, cycle VCC or the EN pin).<br>A load indicator with 2.5 V end-of-scale is then implemented.<br>See *Section 7.4.1* for details. |
| 29 | NB section | NB_OS | Offset programming pin.<br>Internally set to 1.24 V, connecting a $R_{OS\_NB}$ resistor to SGND allows setting a current that is mirrored into NB_FB pin in order to program a positive offset according to the selected $R_{FB\_NB}$. Short to SGND to disable the function. See *Section 6.7* for details. |
| 30 | | NB_FBG | Remote ground sense.<br>Connect to the negative side of the load to perform remote sense. See *Section 9* for proper layout of this connection. |

**Table 2. Pin description (continued)**

| Pin# | | Name | Function |
|---|---|---|---|
| 31 | NB section | NB_VSEN | NB output voltage monitor.<br>It manages OVP and UVP protections and PWRGOOD. Connect to the positive side of the NB load to perform remote sensing. See *Section 9* for proper layout of this connection. |
| 32 | | NB_DROOP | A current proportional to the total current read by the NB section is sourced through this pin according to the current reading gain ($R_{ISEN}$). Short to NB_FB to implement Droop Function or connect to SGND through a resistor and filter with 1nF capacitor to implement NB LOAD Indicator. If not used, short to SGND. |
| 33 | | NB_FB | NB error amplifier inverting input.<br>Connect with a resistor $R_{FB\_NB}$ to NB_VSEN and with an $R_{F\_NB}$ - $C_{F\_NB}$ to NB_COMP. Offset current programmed by NB_OS is sunk through this pin. |
| 34 | | NB_COMP | Error amplifier output.<br>Connect with an $R_{F\_NB}$ - $C_{F\_NB}$ to NB_FB. The NB section or the device cannot be disabled by grounding this pin. |
| 35, 36 | SVI / PVI interface | VID0, VID1 | Voltage IDentification pins.<br>Internally pulled-low by 10 µA, they are used to program the output voltage. VID1 is monitored on the EN pin rising-edge to define the operative mode of the controller (SVI or PVI). When in SVI mode, VID0 is ignored. See *Section 5* for details. |
| 37 | | PWROK | System-wide Power Good input (SVI mode).<br>Internally pulled-low by 10 µA. When low, the device will decode the two SVI bits (SVC, SVD) to determine the *Pre-PWROK Metal VID* (default condition when pin is floating).<br>When high, the device will actively run the SVI protocol.<br>*Pre-PWROK Metal VID* are latched after EN is asserted and re-used in case of PWROK de-assertion. Latch is reset by VCC or EN cycle. |
| 38 | | EN | VR Enable. Internally pulled-up to 3.3 V by 10 µA.<br>Pull-low to disable the device. When set free, the device immediately checks for the VID1 status to determine the SVI / PVI protocol to be adopted and configures itself accordingly. See *Section 5* for details. |
| 39 | SVI / PVI interface | SVC / VID3 | Voltage IDentification pin - SVI clock pin.<br>Internally pulled-low by 10 µA, it is used to program the output voltage. When in SVI-mode, it is considered as Serial-VID-data (input / open drain output). See *Section 5* for details. |
| 40 | | SVD / VID2 | Voltage IDentification pins - SVI data pin.<br>Internally pulled-low by 10 µA, it is used to program the output voltage. When in SVI-mode, it is considered as Serial-VID-data (input / open drain output). See *Section 5* for details. |
| 41 | | PWRGOOD | VCORE and NB Power Good.<br>It is an open-drain output set free after SS as long as both the voltage planes are within specifications. Pull-up to 3.3V (typ) or lower, if not used it can be left floating.<br>When in PVI mode, it monitors the CORE section only. |

Table 2. Pin description (continued)

| Pin# | | Name | Function |
|---|---|---|---|
| 42 | NB section | NB_ENDRV | External driver enable.<br>Open drain output used to control NB section external driver status: pulled-low to manage HiZ conditions or pulled-high to enable the driver. Pull up to 3.3 V (typ) or lower.<br>When in PVI mode, NB section is always kept in HiZ. |
| 43 | CORE section | ENDRV | External driver enable.<br>Open drain output used to control CORE section external driver status: pulled-low to manage HiZ conditions or pulled-high to enable the driver. Pull up to 3.3 V (typ) or lower. |
| 44 | NB section | NB_PWM | PWM output.<br>Connect to external driver PWM input. The device is able to manage HiZ status by setting the pin floating. When in PVI mode, NB section is kept in HiZ. See *Section 5.4.4* for details about HiZ management. |
| 45 to 48 | CORE section | PWM1 to PWM4 | PWM outputs.<br>Connect to external drivers PWM inputs. The device is able to manage HiZ status by setting the pins floating.<br>By shorting to SGND PWM4 or PWM3 and PWM4, it is possible to program the CORE section to work at 3 or 2 phase respectively.<br>See *Section 5.4.4* for details about HiZ management. |
| | | Thermal pad | Thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PGND plane. |

## 2.2 Thermal data

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction to ambient (device soldered on 2s2p PC board) | 40 | °C/W |
| $R_{thJC}$ | Thermal resistance junction to case | 1 | °C/W |
| $T_{MAX}$ | Maximum junction temperature | 150 | °C |
| $T_{STG}$ | Storage temperature range | -40 to 150 | °C |
| $T_J$ | Junction temperature range | 0 to 125 | °C |

# 3 Electrical specifications

## 3.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | to PGND | 15 | V |
| | All other pins to PGNDx | -0.3 to 3.6 | V |

## 3.2 Electrical characteristics

**Table 5. Electrical characteristics**
**($V_{CC}$ = 12 V ± 15%, $T_J$ = 0 °C to 70 °C unless otherwise specified).**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply current and power-ON** | | | | | | |
| $I_{CC}$ | VCC supply current | | | 20 | | mA |
| $UVLO_{VCC}$ | VCC turn-ON | VCC rising | | | 9 | V |
| | VCC turn-OFF | VCC falling | 7 | | | V |
| **Oscillator** | | | | | | |
| $F_{SW}$ | Main oscillator accuracy | | 135 | 150 | 165 | kHz |
| | Oscillator adjustability | $R_{OSC}$ = 27 kΩ | 380 | 465 | 550 | kHz |
| $\Delta V_{OSC}$ | PWM ramp amplitude | CORE and NB section | | 2 | | V |
| FAULT | Voltage at pin OSC | OVP, UVP latch active | 3 | | 3.6 | V |
| $d_{MAX\_NB}$ | NB duty-cycle limit | $I_{NB\_DROOP}$ = 0 µA | | 80 | | % |
| | | $I_{NB\_DROOP}$ = 35 µA | | 40 | | % |
| **PVI / SVI interface** | | | | | | |
| EN, PWROK | Input high | | 2 | | | V |
| | Input low | | | | 0.80 | V |
| | Pull-up current | EN pin | | 10 | | µA |
| | Pull-down current | PWORK pin | | 10 | | µA |
| VID2,/SVD VID3/SVC | Input high | (SVI mode) | 0.95 | | | V |
| | Input low | (SVI mode) | | | 0.65 | V |
| SVD | Voltage low (ACK) | $I_{SINK}$ = -5 mA | | | 250 | mV |
| VID0 to VID5 | Input high | (PVI mode) | 1.3 | | | V |
| | Input low | (PVI mode) | | | 0.80 | V |
| | Pull-down current | | | 10 | | µA |
| V_FIX | Entering V_FIX mode | | | | 0.90 | V |

**Table 5. Electrical characteristics** (continued)
**($V_{CC}$ = 12 V ± 15%, $T_J$ = 0 °C to 70 °C unless otherwise specified).**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PSI_L | Voltage low | $I_{SINK}$ = -5 mA | | | 250 | mV |
| **Voltage positioning (CORE and NB section)** | | | | | | |
| CORE | Output voltage accuracy | VSEN to $V_{CORE}$; FBG to $GND_{CORE}$ | -8 | | 8 | mV |
| NB | | NBVSEN to $V_{NB}$; NBFBG to $GND_{FB}$ | -10 | | 10 | mV |
| OS, NB_OS | OFFSET bias voltage | $I_{OS}$ = 0 to 250 µA | 1.190 | 1.24 | 1.290 | V |
| | OFFSET current range | | 0 | | 250 | µA |
| | OFFSET - $I_{FB}$ accuracy | $I_{OS}$ = 0 to 250 µA | -15 | | 15 | % |
| DROOP | DROOP accuracy | $I_{DROOP}$ = 0 to 140 µA; OS = OFF | -9 | | 9 | µA |
| NB_DROOP | | $I_{NB\_DROOP}$ = 0 to 35 µA; OS = OFF | -4 | | 4 | µA |
| $A_0$ | EA DC gain | | | 100 | | dB |
| SR | Slew rate | COMP, NB_COMP to SGND = 10pF | | 20 | | V/µs |
| **PWM outputs (CORE and NB section)** | | | | | | |
| PWMx, NB_PWM | Output high | I = 1 mA | 3 | | 3.6 | V |
| | Output low | I = -1 mA | | | 0.2 | V |
| $I_{PWMx}$ | Test current | | | 10 | | µA |
| ENDRV, NB_ENDRV | Output low | I = -5 mA | | | 0.4 | V |
| **Protections** | | | | | | |
| OVP | Overvoltage protection | V_FIX mode (V_FIX = SGND); VSEN, NB_VSEN rising | 1.720 | 1.800 | 1.880 | V |
| | Bias current | | 7 | 11 | 15 | µA |
| | OV programmability | $R_{OVP}$ = 180 kΩ | 1.730 | 1.800 | 1.870 | V |
| UVP | Under voltage protection | VSEN, NB_VSEN falling; wrt Ref. | -470 | -400 | -330 | mV |
| PWRGOOD | PGOOD threshold | VSEN, NB_VSEN falling; wrt Ref | -300 | -250 | -200 | mV |
| | Voltage low | $I_{PWRGOOD}$ = -4 mA | | | 0.4 | V |
| $I_{VSEN-DISC}$ | VSEN disconnection | Sourced from NB_VSEN; OS = OFF | | 50 | | µA |
| | | Sunk from VSEN; OS = OFF | | 30 | | µA |
| $V_{FB-DISC}$ | FB disconnection | CORE - $V_{CS-}$ rising, above VSEN | 500 | 600 | 700 | mV |
| FBG DISC | FBG disconnection | EA NI input wrt VID | 350 | 450 | 550 | mV |
| OC_PHASE | Per-phase OC | CORE section; bias voltage | 1.200 | 1.240 | 1.280 | V |
| $kV_{OC\_AVGTH}$ | Average OC | CORE section | 2.430 | 2.500 | 2.570 | V |
| $kI_{OC\_AVGTH}$ | | $I_{DROOP}$ = 0 to 140 µA; OS = OFF | -11 | | 11 | µA |
| $I_{OCTH\_NB}$ | OC threshold | NB section | 32 | 37.5 | 43 | µA |

# 4 Device description and operation

L6740L is a hybrid CPU power supply controller compatible with both parallel (PVI) and Serial (SVI) protocols for AMD K8 - second generation processors. The device provides complete control logic and protections for a high-performance step-down DC-DC voltage regulator, optimized for advanced microprocessor power supply supporting both PVI and SVI communication. It embeds two independent controllers for CPU CORE and the integrated NB, each one with its own set of protections.

L6740L is able to detect which kind of CPU is connected in order to configure itself to work as a single-plane PVI controller or dual-plane SVI controller.

The controller performs a single-phase control for the NB section and a programmable 2-to-4 phase control for the CORE section featuring dual-edge non-latched architecture: this allows fast load-transient response optimizing the output filter consequently reducing the total BOM cost. Further reduction can be achieved by enabling LTB Technology$^{(TM)}$. NB phase (when enabled) will be automatically phase-shifted with respect to the CORE phases in order to reduce the total input RMS current amount.

PSI_L Flag is sent to the VR through the SVI bus. The controller monitors this flag and selectively modifies the phase number in order to optimize the system efficiency when the CPU enters low-power states. This causes the over-all efficiency to be maximized at light loads so reducing losses and system power consumption.

Both sections feature programmable over-voltage protection and adjustable constant over-current protection. Voltage positioning (LL) is possible thanks to an accurate fully-differential current-sense across the main inductors for the CORE section and thanks to the loss-less current sense across low-side MOSFET $R_{DS(on)}$ for the NB section. In both cases, LL may be disabled and the generated current information may be used to implement a Load Indicator function.

L6740L features dual remote sensing for the regulated outputs (CORE and NB) in order to recover from PCB voltage drops also protecting the load from possible feedback network disconnections.

LSLess start-up function allows the controller to manage pre-biased start-up avoiding dangerous current return through the main inductors as well as negative undershoot on the output voltage if the output filter is still charged before start-up.

L6740L also supports V_FIX mode for system debugging: in this particular configuration the SVI bus is used as a static bus configuring 4 operative voltages for both the sections and ignoring any serial-VID command.

When working in PVI mode, the device features on-the-fly VID management: VID code is continuously sampled and the reference update according to the variation detected,

L6740L is available in TQFP48 package.

# 5 Hybrid CPU support and CPU_TYPE detection

L6740L is able to detect the type of the CPU-core connected and to configure itself accordingly. At system start-up, on the rising-edge of the EN signal, the device monitors the status of VID1 and configures the PVI mode (VID1 = 1) or SVI mode (VID1 = 0).

When in PVI mode, L6740L uses the information available on the VID[0: 5] bus to address the CORE section output voltage according to *Table 6*. NB section is kept in HiZ mode.

When in SVI mode, L6740L ignores the information available on VID0, VID4 and VID5 and uses VID2 and VID3 as a SVI bus addressing the CORE and NB sections according to the SVI protocol.

**Caution:** To avoid any risk of errors in CPU type detection (i.e. detecting SVI CPU when PVI CPU is installed on the socket and vice versa), it is recommended to carefully control the start-up sequencing of the system hosting L6740L in order to ensure than on the EN rising-edge, VID1 is in valid and correct state.

## 5.1 PVI - parallel interface

PVI is a 6-bit-wide parallel interface used to address the CORE section reference. According to the selected code, the device sets the CORE section reference and regulates its output voltage as reported into *Table 6*.

NB section is always kept in HiZ; no activity is performed on this section. Furthermore, PWROK information is ignored as well since the signal only applies to the SVI protocol.

## 5.2 PVI start-up

Once the PVI mode has been detected, the device uses the whole code available on the VID[0:5] lines to define the reference for the CORE section. NB section is kept in HiZ. Soft-start to the programmed reference is performed regardless of the state of PWROK.

See *Section 6.10* for details about soft-start.

**Figure 6. System start-up: SVI (to metal-VID; left) and PVI (right)**

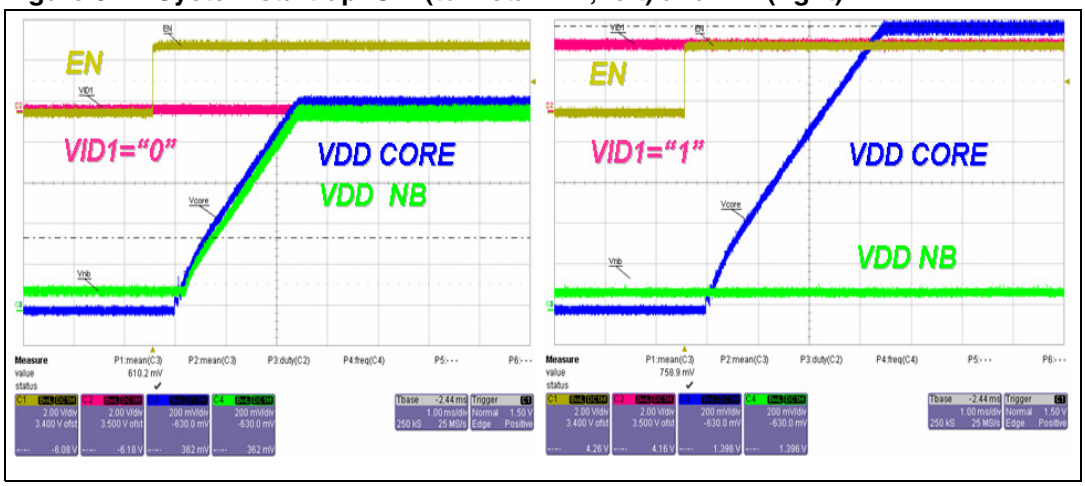


Table 6. Voltage identifications (VID) codes for PVI mode

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output voltage | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Output voltage |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1.5500 | 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.5250 | 1 | 0 | 0 | 0 | 0 | 1 | 0.7500 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.5000 | 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.4750 | 1 | 0 | 0 | 0 | 1 | 1 | 0.7250 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.4500 | 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.4250 | 1 | 0 | 0 | 1 | 0 | 1 | 0.7000 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.4000 | 1 | 0 | 0 | 1 | 1 | 0 | 0.6875 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.3750 | 1 | 0 | 0 | 1 | 1 | 1 | 0.6750 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.3500 | 1 | 0 | 1 | 0 | 0 | 0 | 0.6625 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.3250 | 1 | 0 | 1 | 0 | 0 | 1 | 0.6500 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.3000 | 1 | 0 | 1 | 0 | 1 | 0 | 0.6375 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.2750 | 1 | 0 | 1 | 0 | 1 | 1 | 0.6250 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.2500 | 1 | 0 | 1 | 1 | 0 | 0 | 0.6125 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.2250 | 1 | 0 | 1 | 1 | 0 | 1 | 0.6000 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.2000 | 1 | 0 | 1 | 1 | 1 | 0 | 0.5875 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.1750 | 1 | 0 | 1 | 1 | 1 | 1 | 0.5750 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.1500 | 1 | 1 | 0 | 0 | 0 | 0 | 0.5625 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.1250 | 1 | 1 | 0 | 0 | 0 | 1 | 0.5500 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.1000 | 1 | 1 | 0 | 0 | 1 | 0 | 0.5375 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.0750 | 1 | 1 | 0 | 0 | 1 | 1 | 0.5250 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.0500 | 1 | 1 | 0 | 1 | 0 | 0 | 0.5125 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.0250 | 1 | 1 | 0 | 1 | 0 | 1 | 0.5000 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.0000 | 1 | 1 | 0 | 1 | 1 | 0 | 0.4875 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.9750 | 1 | 1 | 0 | 1 | 1 | 1 | 0.4750 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.9500 | 1 | 1 | 1 | 0 | 0 | 0 | 0.4625 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.9250 | 1 | 1 | 1 | 0 | 0 | 1 | 0.4500 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.9000 | 1 | 1 | 1 | 0 | 1 | 0 | 0.4375 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.8750 | 1 | 1 | 1 | 0 | 1 | 1 | 0.4250 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.8500 | 1 | 1 | 1 | 1 | 0 | 0 | 0.4125 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.8250 | 1 | 1 | 1 | 1 | 0 | 1 | 0.4000 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.8000 | 1 | 1 | 1 | 1 | 1 | 0 | 0.3875 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.7750 | 1 | 1 | 1 | 1 | 1 | 1 | 0.3750 |

## 5.3 SVI - serial interface

SVI is a two wire, clock and data, bus that connects a single master (CPU) to one slave (L6740L). The master initiates and terminates SVI transactions and drives the clock, SVC, and the data, SVD, during a transaction. The slave receives the SVI transactions and acts accordingly. SVI wire protocol is based on fast-mode $I^2C$.

SVI interface also considers two additional signal needed to manage the system start-up. These signals are EN and PWROK. The device return a PWRGOOD signal if the output voltages are in regulation.

## 5.4 SVI start-up

Once the SVI mode has been detected on the EN rising-edge, L6740L checks for the status of the two serial VID pins, SVC and SVD, and stores this value as the *Pre-PWROK Metal VID*. The controller initiate a soft-start phase regulating both CORE and NB voltage planes to the voltage level prescribed by the *Pre-PWROK Metal VID*. See *Table 7* for details about *Pre-PWROK Metal VID* codifications. The stored *Pre-PWROK Metal VID* value are re-used in any case of PWROK de-assertion.

After bringing the output rails into regulation, the controller asserts the PWRGOOD signal and waits for PWROK to be asserted. Until PWROK is asserted, the Controller regulates to the *Pre-PWROK Metal VID* ignoring any commands coming from the SVI interface.

After PWROK is asserted, the processor has initialized the serial VID interface and L6740L waits for commands from the CPU to move the voltage planes from the *Pre-PWROK Metal VID* values to the operative VID values. As long as PWROK remains asserted, the controller will react to any command issued through the SVI interface according to SVI Protocol.

See *Section 6.10* for details about soft-start.

**Table 7. V_FIX mode and metalVID**

| SVC | SVD | Output voltage [V] | |
|---|---|---|---|
| | | ***Pre-PWROK metal VID*** | ***V_FIX mode*** |
| 0 | 0 | 1.1V | 1.4V |
| 0 | 1 | 1.0V | 1.2V |
| 1 | 0 | 0.9V | 1.0V |
| 1 | 1 | 0.8V | 0.8V |

### 5.4.1 Set VID command

The *Set VID Command* is defined as the command sequence that the CPU issues on the SVI bus to modify the voltage level of the CORE section and/or the NB section.

During a *Set VID Command*, the processor sends the start (START) sequence followed by the address of the section which the *Set VID Command* applies. The processor then sends the write (WRITE) bit. After the write bit, the Voltage Regulator (VR) sends the acknowledge (ACK) bit. The processor then sends the VID bits code during the *data phase*. The VR sends the acknowledge (ACK) bit after the data phase. Finally, the processor sends the stop (STOP) sequence. After the VR has detected the stop, it performs an On-the-Fly VID

transition for the addressed section(s) or, more in general, react to the sent command accordingly. Refer to *Figure 7*, *Table 8* and *Table 9* for details about the *Set VID command.*

L6740L is able to manage individual power OFF for both the sections. The CPU may issue a serial VID command to power OFF or power ON one section while the other one remains powered. In this case, the PWRGOOD signal remains asserted.

**Figure 7. SVI communications - send byte**

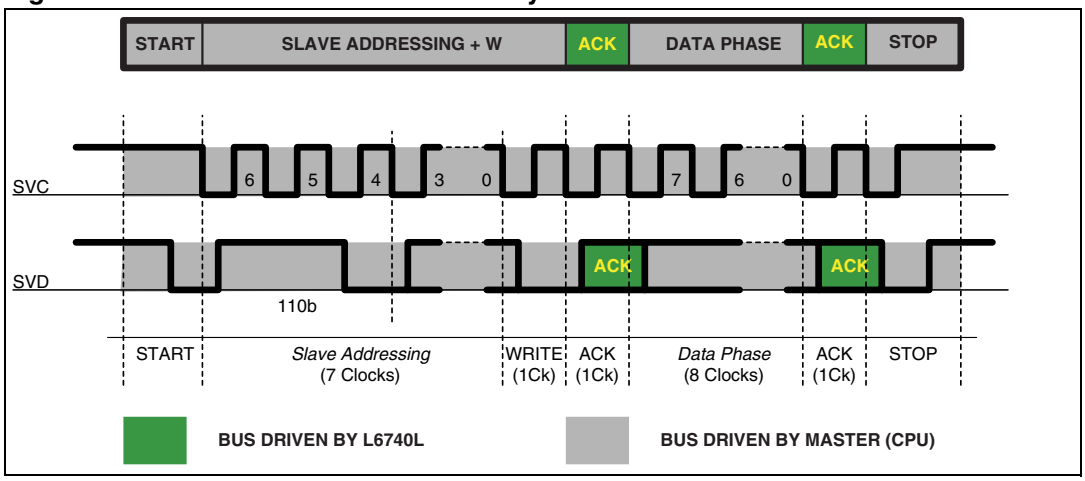



**Table 8. SVI send byte - Address and data phase description**

| bits | Description |
|---|---|
| **Address phase** | |
| 6:4 | Always 110b. |
| 3 | Not applicable, ignored. |
| 2 | Not applicable, ignored. |
| 1 | CORE section(1).<br>If set then the following data byte contains the VID code for CORE section. |
| 0 | NB section(1).<br>If set then the following data byte contains the VID code for NB section. |
| **Data phase** | |
| 7 | PSI_L Flag (active low).When asserted, the VR is allowed to enter power-saving mode. See *Section 5.4.3*. |
| 6:0 | VID code. See *Table 9*. |

1. Assertion in both bit 1 and 0 will address the VID code to both CORE and NB simultaneously.

**Table 9. Data phase - serial VID codes**

| SVI [6:0] | Output voltage | SVI [6:0] | Output voltage | SVI [6:0] | Output voltage | SVI [6:0] | Output voltage |
|---|---|---|---|---|---|---|---|
| 000_0000 | 1.5500 | 010_0000 | 1.1500 | 100_0000 | 0.7500 | 110_0000 | 0.3500 |
| 000_0001 | 1.5375 | 010_0001 | 1.1375 | 100_0001 | 0.7375 | 110_0001 | 0.3375 |
| 000_0010 | 1.5250 | 010_0010 | 1.1250 | 100_0010 | 0.7250 | 110_0010 | 0.3250 |
| 000_0011 | 1.5125 | 010_0011 | 1.1125 | 100_0011 | 0.7125 | 110_0011 | 0.3125 |
| 000_0100 | 1.5000 | 010_0100 | 1.1000 | 100_0100 | 0.7000 | 110_0100 | 0.3000 |
| 000_0101 | 1.4875 | 010_0101 | 1.0875 | 100_0101 | 0.6875 | 110_0101 | 0.2875 |
| 000_0110 | 1.4750 | 010_0110 | 1.0750 | 100_0110 | 0.6750 | 110_0110 | 0.2750 |
| 000_0111 | 1.4625 | 010_0111 | 1.0625 | 100_0111 | 0.6625 | 110_0111 | 0.2625 |
| 000_1000 | 1.4500 | 010_1000 | 1.0500 | 100_1000 | 0.6500 | 110_1000 | 0.2500 |
| 000_1001 | 1.4375 | 010_1001 | 1.0375 | 100_1001 | 0.6375 | 110_1001 | 0.2375 |
| 000_1010 | 1.4250 | 010_1010 | 1.0250 | 100_1010 | 0.6250 | 110_1010 | 0.2250 |
| 000_1011 | 1.4125 | 010_1011 | 1.0125 | 100_1011 | 0.6125 | 110_1011 | 0.2125 |
| 000_1100 | 1.4000 | 010_1100 | 1.0000 | 100_1100 | 0.6000 | 110_1100 | 0.2000 |
| 000_1101 | 1.3875 | 010_1101 | 0.9875 | 100_1101 | 0.5875 | 110_1101 | 0.1875 |
| 000_1110 | 1.3750 | 010_1110 | 0.9750 | 100_1110 | 0.5750 | 110_1110 | 0.1750 |
| 000_1111 | 1.3625 | 010_1111 | 0.9625 | 100_1111 | 0.5625 | 110_1111 | 0.1625 |
| 001_0000 | 1.3500 | 011_0000 | 0.9500 | 101_0000 | 0.5500 | 111_0000 | 0.1500 |
| 001_0001 | 1.3375 | 011_0001 | 0.9375 | 101_0001 | 0.5375 | 111_0001 | 0.1375 |
| 001_0010 | 1.3250 | 011_0010 | 0.9250 | 101_0010 | 0.5250 | 111_0010 | 0.1250 |
| 001_0011 | 1.3125 | 011_0011 | 0.9125 | 101_0011 | 0.5125 | 111_0011 | 0.1125 |
| 001_0100 | 1.3000 | 011_0100 | 0.9000 | 101_0100 | 0.5000 | 111_0100 | 0.1000 |
| 001_0101 | 1.2875 | 011_0101 | 0.8875 | 101_0101 | 0.4875 | 111_0101 | 0.0875 |
| 001_0110 | 1.2750 | 011_0110 | 0.8750 | 101_0110 | 0.4750 | 111_0110 | 0.0750 |
| 001_0111 | 1.2625 | 011_0111 | 0.8625 | 101_0111 | 0.4625 | 111_0111 | 0.0625 |
| 001_1000 | 1.2500 | 011_1000 | 0.8500 | 101_1000 | 0.4500 | 111_1000 | 0.0500 |
| 001_1001 | 1.2375 | 011_1001 | 0.8375 | 101_1001 | 0.4375 | 111_1001 | 0.0375 |
| 001_1010 | 1.2250 | 011_1010 | 0.8250 | 101_1010 | 0.4250 | 111_1010 | 0.0250 |
| 001_1011 | 1.2125 | 011_1011 | 0.8125 | 101_1011 | 0.4125 | 111_1011 | 0.0125 |
| 001_1100 | 1.2000 | 011_1100 | 0.8000 | 101_1100 | 0.4000 | 111_1100 | OFF |
| 001_1101 | 1.1875 | 011_1101 | 0.7875 | 101_1101 | 0.3875 | 111_1101 | OFF |
| 001_1110 | 1.1750 | 011_1110 | 0.7750 | 101_1110 | 0.3750 | 111_1110 | OFF |
| 001_1111 | 1.1625 | 011_1111 | 0.7625 | 101_1111 | 0.3625 | 111_1111 | OFF |

### 5.4.2 PWROK de-assertion

Anytime PWROK de-asserts while EN is asserted, the controller uses the previously stored *Pre-PWROK Metal VID* and regulates all the planes to that level performing an On-the-Fly transition to that level.

PWRGOOD is treated appropriately being de-asserted in case the *Pre-PWROK Metal VID* voltage is out of the initial voltage specifications.

### 5.4.3 PSI_L and efficiency optimization at light-load

PSI_L is an active-low flag (i.e. low logic level when asserted) that can be set by the CPU to allow the VR to enter power-saving mode to maximize the system efficiency when in light-load conditions. The status of the flag is communicated to the controller through the SVI bus and it is reported on the PSI_L pin (open-drain).

The controller monitors the PSI_L pin also to define the PSI Strategy, that is the action performed by the controller when PSI_L is asserted. According to *Table 10*, by programming different voltage divider on PSI_L, it is possible to configure the device to disable one or two phases while PSI_L is asserted. The device can also be configured to take no action so phase number will not change after PSI_L assertion.

In case the phase number is changed, the device will disable one or two phases starting from the highest one (i.e. if working at 3 phases, phase 3 will be disabled in case of 1 phase reduction; phase 2 and 3 in case of 2phase reduction). To disable Phases, the controller will set HiZ on the related PWM and re-configure internal phase-shift to maintain the interleaving. Furthermore, the internal current-sharing will be adjusted to consider the phase number reduction. ENDRV will remain asserted.

When PSI_L is de-asserted, the device will return to the original configuration.

Start-up is performed with all the configured phases enabled. In case of on-the-fly VID transitions, the device will maintain the phase configuration set before.

PSI strategy (i.e. the voltage across PSI_L) is read and stored when PWRGOOD is asserted at the end of the Soft-Start phase.

The phase number management is affected by the external driver selected.

- If the external driver features the EN function, PSI_L can be tied directly to the EN of the drivers of the phases that will be disabled.

  Furthermore, in case the desired strategy is to work in single phase when 4phases are configured, PSI_L can be tied also to the EN of the driver connected to Phase2 (apparently, from 4phases the max reduction would be to 2phase min.) in order to disable also this phase during low-power mode.
- If the external driver manages HiZ through the PWM input, PSI_L will be connected only to the external divider used to set the strategy. The system can be down-graded to single-phase only if configured for three phases.

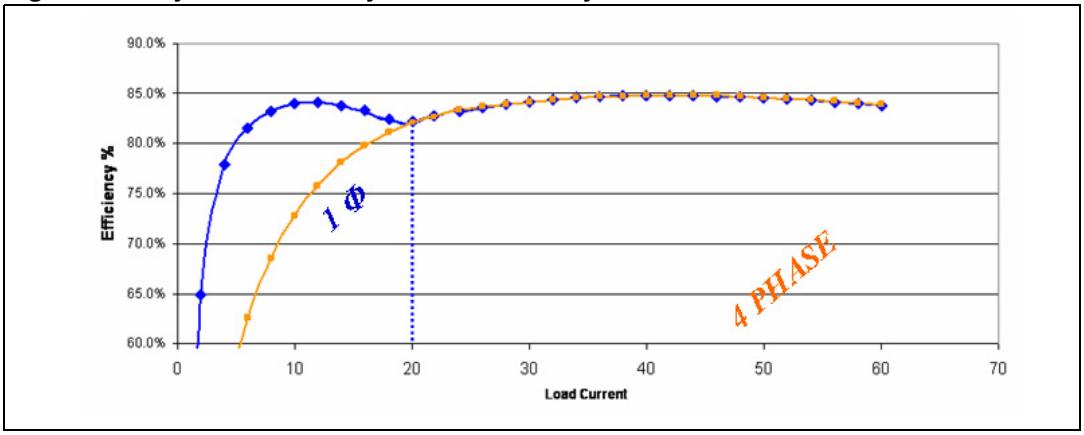
Since PSI_L can be used to enable some of the external drivers connected, the status of the pin is the logic AND between the PSI_L Flag and the status of the ENDRV pin: if the controller wants to disable the external drivers pulling low ENDRV (because of protections or simply for start-up synchronization) also PSI_L will be tied low.

NB section is not impacted by PSI_L status change. *Figure 8* shows an example of the efficiency improvement that can be achieved by enabling the PSI management.

**Table 10. PSI strategy**

| PSI_L | PSI strategy |
|---|---|
| GND | No strategy.<br>PSI_L still reproduces the status of the PSI Flag |
| Pull-Up to <3V | Phase number is cut by 1 while PSI_L is asserted. |
| Pull-Up to 3.3V | Phase number is cut by 2 while PSI_L is asserted. |

**Figure 8. System efficiency enhancement by PSI**




### 5.4.4 HiZ management

L6740L is able to manage HiZ through both the PWMx and driver enable signals. When the controller wants to set in high impedance the output of one section, it set the relative PWM floating and, at the same time, pulls-low the related ENDRV.

### 5.4.5 Hardware jumper override - V_FIX

Anytime the pin OVP/V_FIX is driven low, the controller enters V_FIX mode.

When in V_FIX mode, both NB and CORE section voltages are governed by the information shown in *Table 7*. Regardless of the state of PWROK, the device will work in SVI mode. SVC and SVD are considered as static VID and the output voltage will change according to their status. Dynamic SVC/SVD-change management is provided in this condition.

V_FIX mode is intended for system debug only.

Protection management differs in this case, see *Section 7.1* for details.

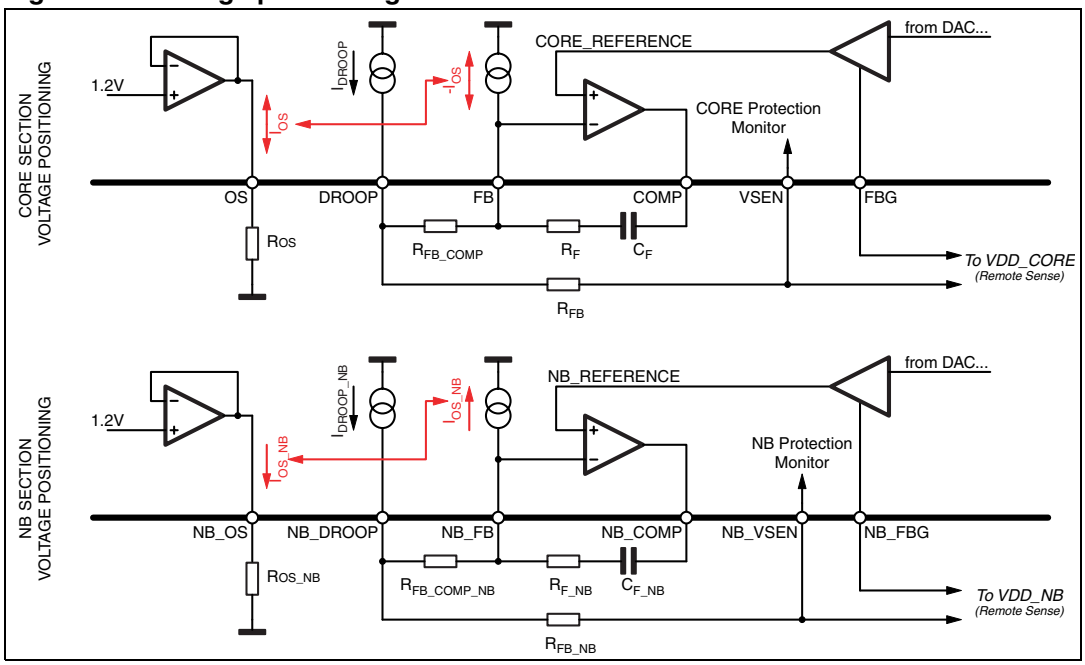
# 6 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode (*SVI, PVI* and *V_FIX*) and by programming the droop function and offset to the reference of both the sections (See *Figure 9*). The controller reads the current delivered by each section by monitoring the voltage drop across the low-side MOSFET for NB section or DCR Inductors for CORE section. The current ($I_{DROOP}$ / $I_{DROOP\_NB}$) sourced from the DROOP / NB_DROOP pin, directly proportional to the read current, causes the related section output voltage to vary according to the external $R_{FB}$ / $R_{FB\_NB}$ resistor so implementing the desired load-line effect. The current ($I_{OS}$ / $I_{OS\_NB}$) programmed through the OS / NB_OS pins is sunk from the FB / NB_FB pins causing the output voltage to be offset according to the resistance $R_{FB}$ / $R_{FB\_NB}$ connected.

L6740L embeds a dual remote-sense buffer to sense remotely the regulated voltage of each section without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Both DROOP and OFFSET function can be disabled: see *Section 6.3* and *Section 6.4* for details about CORE section and *Section 6.6* and *Section 6.7* for details about NB section. In case DROOP effect is not desired, the current information sourced from the DROOP pin may be used to implement a Load Indicator as reported in *Section 6.3* and *Section 6.6*.

**Figure 9. Voltage positioning**



## 6.1 CORE section - phase # programming

CORE section implements a flexible 2 to 4 interleaved-phase converter. To program the desired number of phase, simply short to SGND the PWMx signal that is not required to be used according to *Table 11*. For three phase operation, short PWM4 to SGND while for two phase operation, short PWM3 and PWM4 to SGND.

**Caution:** For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSx+ needs to be connected to the regulated output voltage while CSx- needs to be connected to CSx+ through the same Rg resistor used for the active phases.

**Table 11. CORE section - phase number programming**

| Phase number | PWM1 | PWM2 | PWM3 | PWM4 |
|---|---|---|---|---|
| 1 | n/a | | | |
| 2 | to Driver | | SGND | SGND |
| 3 | to Driver | | | SGND |
| 4 | to Driver | | | |

## 6.2 CORE section - current reading and current sharing loop

L6740L embeds a flexible, fully-differential current sense circuitry for the CORE section that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy. The trans-conductance ratio is issued by the external resistor Rg placed outside the chip between CSx- pin toward the reading points. The current sense circuit always tracks the current information, the pin CSx+ is used as a reference keeping the CSx- pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSx- pin is then given by the following equation (See *Figure 10*):

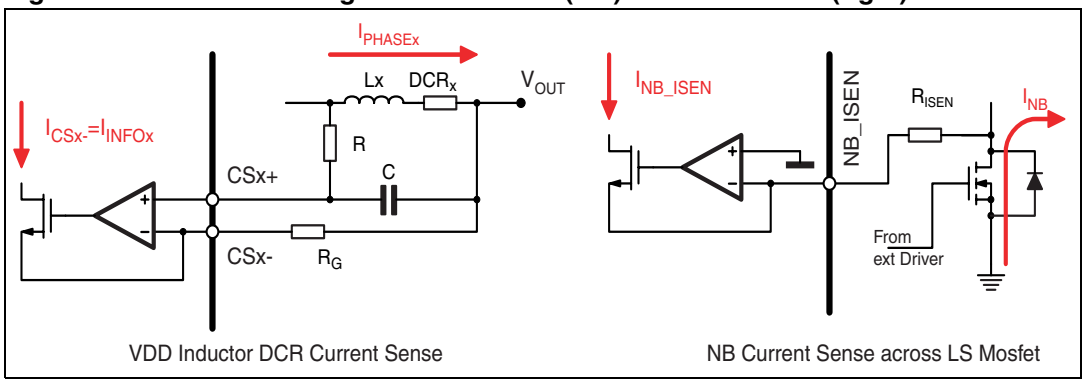
$$I_{CSx-} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

$$\frac{L}{R_L} = R \cdot C \quad \Rightarrow \quad I_{CSx-} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

$R_G$ resistor is typically designed in order to have an information current $I_{INFOx}$ in the range of about 35 µA ($I_{OCTH}$) at the OC threshold.

**Figure 10. Current reading - CORE section (left) and NB section (right)**




The current read through the CSx+ / CSx- pairs is converted into a current $I_{INFOx}$ proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current $I_{INFOx}$ and the reference $I_{AVG}$ is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

## 6.3 CORE section - load-line and load-indicator (optional)

L6740L is able to introduce a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

*Figure 10* shows the Current Sense Circuit used to implement the Load-Line. The current flowing across the inductor(s) is read through the R - C filter across CSx+ and CSx- pins. $R_G$ programs a trans conductance gain and generates a current $I_{CSx}$ proportional to the current of the phase. The sum of the $I_{CSx}$ current is then sourced by the FB pin ($I_{DROOP}$). $R_{FB}$ gives the final gain to program the desired load-line slope (*Figure 9*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system so avoiding over and/or under shoot of the output voltage as a consequence of a load transient. See *Section 6.2*. The output characteristic vs. load current is then given by (Offset disabled):

$$V_{CORE} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

Where $R_{LL}$ is the resulting load-line resistance implemented by the CORE section.

The whole power supply can be then represented by a “real” voltage generator with an equivalent output resistance $R_{LL}$ and a voltage value of VID.

$R_{FB}$ resistor can be then designed according to the $R_{LL}$ specifications as follow:

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

**Caution:** Load-line (DROOP) implementation is optional, in case it is not desired, the resulting current information may be employed for other purposes, such as an additional load indicator (LI). In