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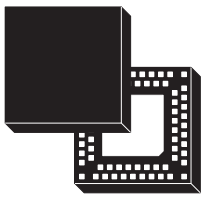
# L6751C

## Digitally controlled dual PWM for Intel VR12 and AMD SVI

**Datasheet - production data**



WPLGA72 6 x 6 mm

## Features

- VR12 compliant with 25 MHz SVID bus rev. 1.5
  - SerialVID with programmable IMAX, TMAX, VBOOT, ADDRESS
- AMD SVI compliant
- Second generation LTB Technology™
- Flexible driver/DrMOS support
- JMode support
- Fully configurable through PMBus™
- Dual controller:
  - Up to 6 phases for CORE and memory
  - 1 phase for graphics (GFX), system agent (VSA) or Northbridge (VDDNB)
- Single NTC design for TM, LL and IMON thermal compensation (for each section)
- VFDE and GDC - gate drive control for efficiency optimization
- DPM - dynamic phase management
- Dual remote sense; 0.5% $V_{OUT}$ accuracy
- Full-differential current sense across DCR
- AVP - adaptive voltage positioning
- Dual independent adjustable oscillator
- Dual current monitor
- Pre-biased output management
- Average and per-phase OC protection
- OV, UV and FB disconnection protection
- Dual VR_RDY
- WPLGA72 6 x 6 mm package

## Applications

- High-current VRM / VRD for desktop / server / workstation Intel® / AMD CPUs
- DDR3 memory supply

## Description

The L6751C device is a universal digitally controlled dual PWM DC-DC designed to power Intel's VR12 and AMD SVI processors and memories: all required parameters are programmable through dedicated pin-strapping and PMBus interface. The device features up to 6-phase programmable operation for multi-phase sections and a single-phase with independent control loops. When configured for memory supply, single-phase (VTT) reference is always tracking multi-phase (VDDQ) scaled by a factor of 2. The L6751C supports power state transitions featuring VFDE, programmable DPM and GDC maintaining the best efficiency over all loading conditions without compromising transient response. The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in WPLGA72 6 x 6 mm package.

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| L6751C | WPLGA72 6 x 6 mm | Tray |
| L6751CTR | WPLGA72 6 x 6 mm | Tape and reel |

# Contents

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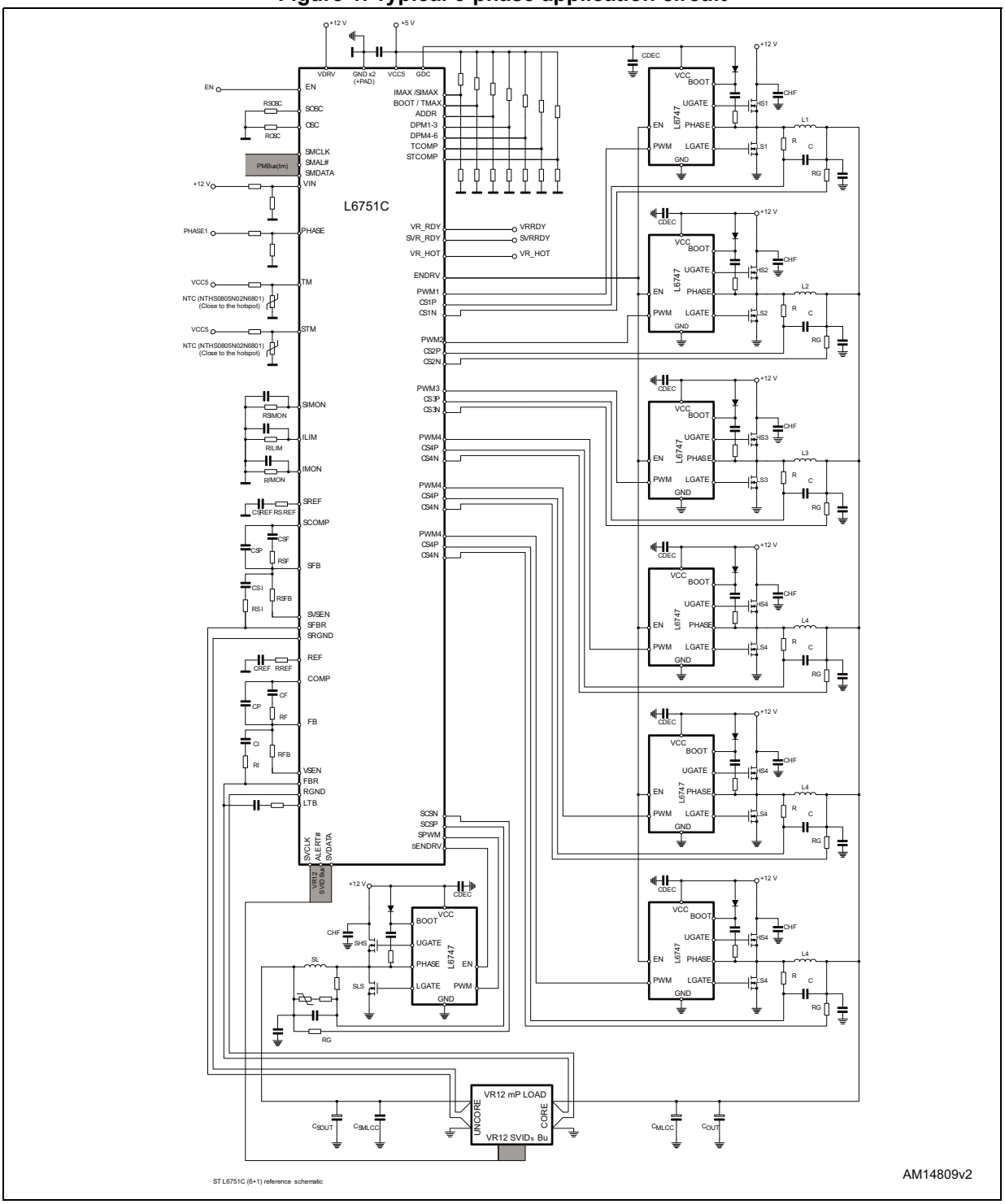
# 1 Typical application circuit and block diagram

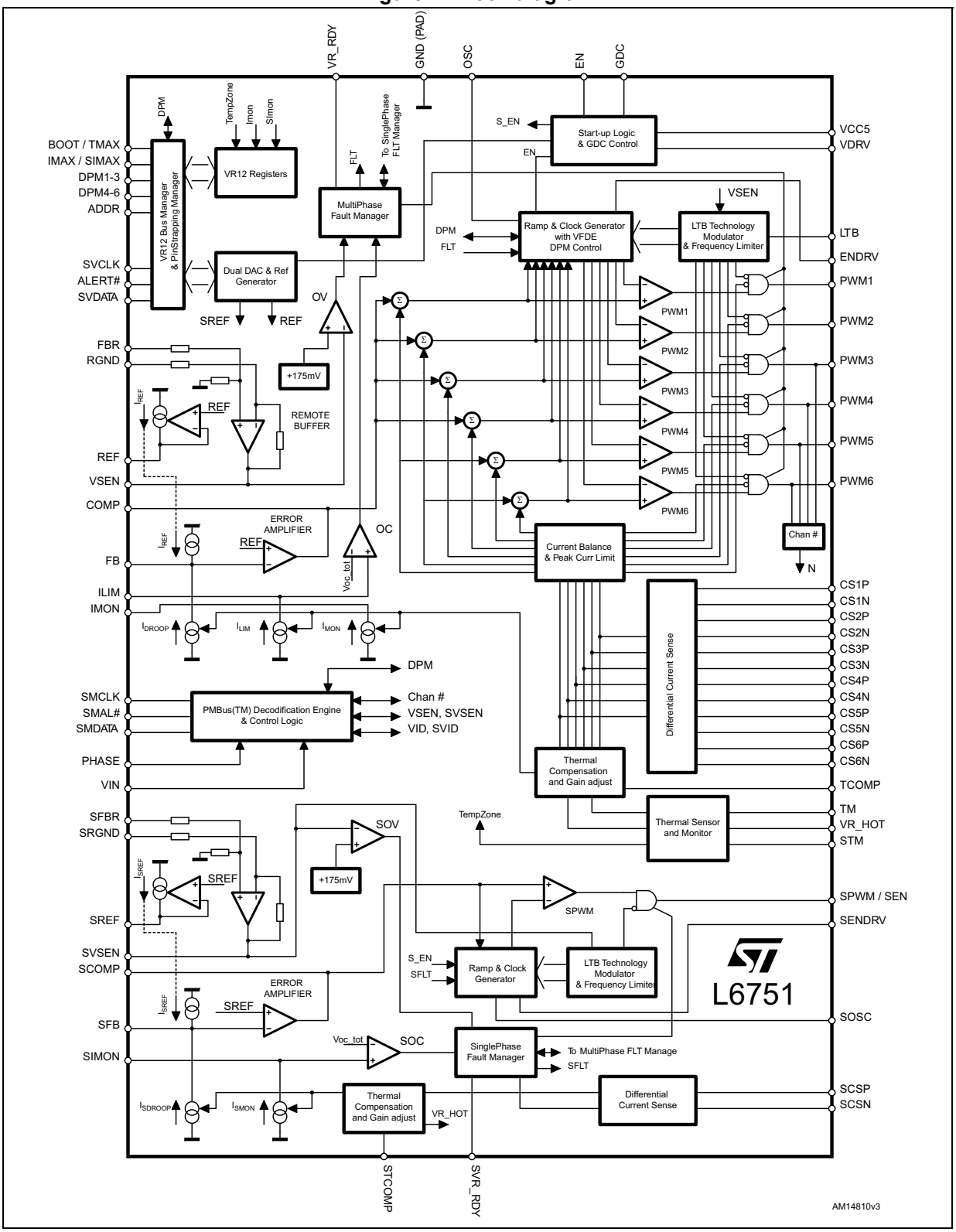
## 1.1 Application circuit

**Figure 1. Typical 6-phase application circuit**



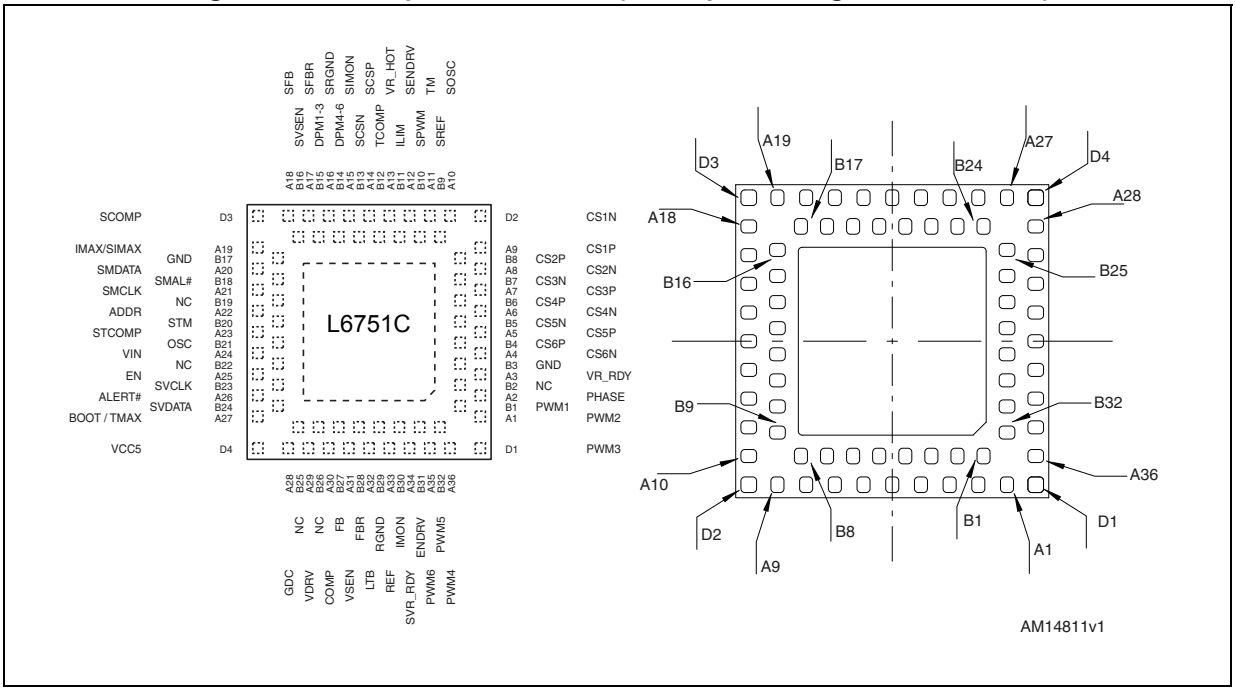
## 1.2 Block diagram

**Figure 2. Block diagram**



# 2 Pin description and connection diagrams

**Figure 3. L6751C pin connections (left: top view - right: bottom view)**




## 2.1 Pin description

**Table 2. Pin description**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| D1 | PWM3 | D(1) | MULTI-PHASE SECTION | PWM output.<br>Connect to multi-phase channel 3 external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to a fixed predefined voltage. See *Table 7 on page 20* for phase number programming. |
| A1 | PWM2 | D | | PWM output. |
| B1 | PWM1 | D | | Connect to multi-phase external drivers PWM input. These pins are also used to configure Hi-Z levels for compatibility with drivers and DrMOS. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to the predefined fixed voltage. |
| A2 | PHASE | A | | Connect through resistor divider to multi-phase channel1 switching node. |
| B2 | NC | - | | Not internally bonded. |
| A3 | VR_RDY | D | | VR Ready. Open drain output set free after SS has finished in multi-phase section and pulled low when triggering any protection on multi-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating. |
| B3 | GND | A | | GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 with proper MLCC capacitor and connect to the PCB GND plane. |

**Table 2. Pin description (continued)**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| A4 | CS6N | A | MULTI-PHASE SECTION | Channel 6 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 6 phases, still connect through Rg to CS6P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| B4 | CS6P | A | | Channel 6 current sense positive input. Connect through an R-C filter to the phase-side of the channel 6 inductor. When working at < 6 phases, short to the regulated voltage. |
| A5 | CS5P | A | | Channel 5 current sense positive input. Connect through an R-C filter to the phase-side of the channel 5 inductor. When working at < 5 phases, short to the regulated voltage. |
| B5 | CS5N | A | | Channel 5 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 5 phases, still connect through Rg to CS5P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| A6 | CS4N | A | | Channel 4 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 4 phases, still connect through Rg to CS4P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| B6 | CS4P | A | MULTI-PHASE SECTION | Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at < 4 phases, short to the regulated voltage. |
| A7 | CS3P | A | | Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at < 3 phases, short to the regulated voltage. |
| B7 | CS3N | A | | Channel 3 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at < 3 phases, still connect through Rg to CS3P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| A8 | CS2N | A | | Channel 2 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| B8 | CS2P | A | | Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. |
| A9 | CS1P | A | | Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor. |
| D2 | CS1N | A | | Channel 1 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| A10 | SOSC | A | SINGLE-PHASE SECTION | Oscillator pin.<br>It allows the switching frequency $F_{SSW}$ to be programmed for the single-phase section. The pin is internally set to 1.02 V, frequency for single-phase is programmed according to the resistor connected to GND or VCC with a gain of 11.5 kHz/µA. Leaving the pin floating programs a switching frequency of 230 kHz. See *Section 10 on page 44* for details. |

**Table 2. Pin description (continued)**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| B9 | SREF | A | SINGLE-PHASE SECTION | The reference used for the single-phase section regulation is available on this pin with -125 mV offset. Connect through an $R_{SREF}$-$C_{SREF}$ to GND to optimize DVID transitions. Connect through $R_{SOS}$ resistor to the SFB pin to implement small positive offset to the regulation. |
| A11 | TM | A | MULTI-PHASE SECTION | Thermal monitor sensor.<br>Connect with proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring.<br>By programming proper TCOMP gain, the IC also implements load-line and IMON/ILIM thermal compensation for the multi-phase section.<br>In JMode, the pin disables the single-phase section if shorted to GND.<br>Pull up to VCC5 with 1 kΩ to disable thermal sensor.<br>See *Section 8 on page 39* for details. |
| B10 | SPWM / SEN | D | SINGLE-PHASE SECTION | PWM output.<br>Connect to single-phase external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the pin to a fixed voltage defined by PWMx strapping.<br>Connect to VCC5 with 1 kΩ to disable the single-phase section. |
| A12 | SENDRV | D | SINGLE-PHASE SECTION | Enable driver.<br>CMOS output driven high when the IC commands the driver. Used in conjunction with the Hi-Z window on the SPWM pin to optimize the single-phase section overall efficiency. Connect directly to external driver enable pin. |
| B11 | ILIM | A | MULTI-PHASE SECTION | Multi-phase section current limit.<br>A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor $R_{LIM}$ to GND. When the pin voltage reaches 2.5 V, the overcurrent protection is set and the IC latches. Filter through $C_{LIM}$ to GND to delay OC intervention. |
| A13 | VR_HOT | D | | Voltage regulator HOT.<br>Open drain output, this is an alarm signal asserted by the controller when the temperature sensed through the ST or TM pins exceed TMAX (active low). See *Section 8 on page 39* for details. |
| B12 | TCOMP | A | | Thermal monitor sensor gain.<br>Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by the TM to implement thermal compensation for the multi-phase section. Short to GND to disable temperature compensation (but not thermal sensor). See *Section 8 on page 39* for details. |

**Table 2. Pin description (continued)**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| A14 | SCSP | A | SINGLE-PHASE SECTION | Single-phase section current senses positive input.<br>Connect through an R-C filter to the phase-side of the channel 1 inductor. |
| B13 | SCSN | A | | Single-phase section current senses negative input.<br>Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND. |
| A15 | SIMON | A | | Current monitor output.<br>A current proportional to the single-phase current is sourced from this pin. Connect through a resistor $R_{SIMON}$ to GND.<br>When the pin voltage reaches 1.55 V, overcurrent protection is set and the IC latches. Filtering through $C_{SIMON}$ to GND allows the delay for OC intervention to be controlled. |
| B14 | DPM4-6 | A | PINSTRAPPING | Connect a resistor divider to GND/VCC5 in order to define the DPM and GDC strategies. See *Table 11 on page 24* and *Table 12 on page 26* for details. |
| A16 | SRGND | A | SINGLE-PHASE SECTION | Remote buffer ground sense.<br>Connect to the negative side of the single-phase load to perform remote sense. |
| B15 | DPM1-3 | A | PINSTRAPPING | Connect a resistor divider to GND/VCC5 in order to define the DPM and GDC strategies. See *Table 11 on page 24* and *Table 12 on page 26* for details. |
| A17 | SFBR | A | SINGLE-PHASE SECTION | Remote buffer positive sense.<br>Connect to the positive side of the single-phase load to perform remote sense. |
| B16 | SVSEN | A | | Remote buffer output.<br>Output voltage monitor, manages OV and UV protection.<br>Connect with a resistor $R_{SFB}$ // ($R_{SI}$ - $C_{SI}$) to SFB. |
| A18 | SFB | A | | Error amplifier inverting input.<br>Connect with a resistor $R_{SFB}$ // ($R_{SI}$ - $C_{SI}$) to SVSEN and with an ($R_{SF}$ - $C_{SF}$)// $C_{SH}$ to SCOMP. |
| D3 | SCOMP | A | | Error amplifier output.<br>Connect with an ($R_{SF}$ - $C_{SF}$)// $C_{SH}$ to SFB. The device cannot be disabled by pulling low this pin. |
| A19 | IMAX / SIMAX | A | PINSTRAPPING | Connect a resistor divider to GND/VCC5 in order to define the IMAX and SIMAX registers. See *Table 8 on page 21* and *Table 6 on page 20* for details. |

**Table 2. Pin description (continued)**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| B17 | GND | A | | GND connection. All internal references and logic are referenced to this pin. Filter to VCC5 with proper MLCC capacitor and connect to the PCB GND plane. |
| A20 | SMDATA | D | PMBus | PMBus data. |
| B18 | SMAL# | D | | PMBus alert. |
| A21 | SMCLK | D | | PMBus clock. |
| B19 | NC | - | | Not internally bonded. |
| A22 | ADDR | A | PINSTRAPPING | Connect a resistor divider to GND/VCC5 in order to configure the IC operating mode. See *Table 9 on page 22* and *Table 6 on page 20* for details. |
| B20 | STM | A | SINGLE-PHASE SECTION | Thermal monitor sensor.<br>Connect with proper network embedding NTC to the single-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature monitoring.<br>By programming proper STCOMP gain, the IC also implements load-line and SIMON thermal compensation for the single-phase section when applicable. Short to GND if not used. See *Section 8 on page 39* for details. |
| A23 | STCOMP | A | | Thermal monitor sensor gain.<br>Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by ST to implement thermal compensation for the single-phase section. Short to GND to disable temperature compensation. See *Section 8 on page 39* for details. |
| B21 | OSC | A | MULTI-PHASE SECTION | Oscillator pin.<br>It allows the programming of the switching frequency $F_{SW}$ for the multi-phase section. The pin is internally set to 1.02 V, frequency for multi-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 Hz/µA. Leaving the pin floating programs a switching frequency of 200 Hz per phase. Effective frequency observable on the load results as being multiplied by the number of active phases N. See *Section 10 on page 44* for details. |
| A24 | VIN | A | | Input voltage monitor.<br>Connect to input voltage monitor point through a divider $R_{VUP}$ / $R_{VDWN}$ to perform VIN sense through PMBus ($R_{UP}$ = 118.5 Ω; $R_{DOWN}$ = 10 kΩ typ.). |
| B22 | NC | - | | Not internally bonded. |
| A25 | EN | D | | Level sensitive enable pin (3.3 V compatible).<br>Pull low to disable the device, pull up above the turn-on threshold to enable the controller. |
| B23 | SVCLK<br>SVC | D | SVI BUS | Serial clock. |
| A26 | ALERT#<br>V_FIX | D | | Alert (Intel mode).<br>V_FIX (AMD mode). Pull to 3.3 V to enter V_FIX mode. |

**Table 2. Pin description (continued)**

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| B24 | SVDATA SVD | D | SVI BUS | Serial data. |
| A27 | BOOT / TMAX | A | PINSTRAPPING | Connect a resistor divider to GND/VCC5 in order to define BOOT and TMAX registers. See *Table 10 on page 23* for details. |
| D4 | VCC5 | A | | Main IC power supply.<br>Operative voltage is 5 V ± 5%. Filter with 1 µF MLCC to GND (typ.). |
| A28 | GDC | A | | Gate drive control pin.<br>Used for efficiency optimization, see *Section 9 on page 41* for details. If not used, it can be left floating. Always filter with 1 µF MLCC to GND. |
| B25 | NC | - | | Not internally bonded. |
| A29 | VDRV | A | | Driving voltage for external drivers.<br>Connect to the selected voltage rail to drive external MOSFET when in maximum power conditions. IC switches GDC voltage between VDRV and VCC5 to implement efficiency optimization according to selected strategies. |
| B26 | NC | - | | Not internally bonded. |
| A30 | COMP / ADDR | A | MULTI-PHASE SECTION | Error amplifier output.<br>Connect with an ($R_F$ - $C_F$)// $C_P$ to FB. The device cannot be disabled by pulling low this pin.<br>Connect $R_{COMP}$ = 12.5 kΩ to GND to extend PMBus addressing range (see *Table 9 on page 22*). |
| B27 | FB | A | | Error amplifier inverting input.<br>Connect with a resistor $R_{FB}$ // ($R_I$ - $C_I$) to VSEN and with an ($R_F$ - $C_F$)// $C_P$ to COMP. |
| A31 | VSEN | A | | Output voltage monitor, manages OV and UV protection.<br>Connect to the positive side of the load to perform remote sense. |
| B28 | FBR | A | | Remote buffer positive sense.<br>Connect to the positive side of the multi-phase load to perform remote sense. |
| A32 | LTB | A | | LTB Technology input pin. See *Section 11.2 on page 47* for details. |
| B29 | RGND | A | | Remote ground sense.<br>Connect to the negative side of the multi-phase load to perform remote sense. |
| A33 | REF | A | | The reference used for the multi-phase section regulation is available on this pin with -125 mV offset. Connect through an $R_{REF}$ - $C_{REF}$ to GND to optimize DVID transitions. Connect through $R_{OS}$ resistor to FB pin to implement small positive offset to the regulation. |
| B30 | IMON | A | | Current monitor output.<br>A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor $R_{MON}$ to GND. The information available on this pin is used for the current reporting and DPM. The pin can be filtered through $C_{IMON}$ to GND. |

Table 2. Pin description (continued)

| Pin no. | Name | Type | | Function |
|---|---|---|---|---|
| A34 | SVR_RDY (PWROK) | D | SINGLE-PHASE SECTION | VR Ready (Intel mode). Open drain output set free after SS has finished and pulled low when triggering any protection for the single-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.<br>PowerOK (AMD mode). System-wide Power Good input. When low, the device decodes SVC and SVD to determine the boot voltage. |
| B31 | ENDRV | D | MULTI-PHASE SECTION | Enable driver.<br>CMOS output driven high when the IC commands the drivers. Used in conjunction with the Hi-Z window on the PWMx pins to optimize the multi-phase section overall efficiency. Connect directly to external driver enable pin. |
| A35 | PWM6 | D | MULTI-PHASE SECTION | PWM output.<br>Connect to related multi-phase channel external driver PWM input. During normal operation the device is able to manage Hi-Z status by setting and holding the PWMx pin to fixed voltage defined before. See *Table 7 on page 20* for phase number programming. |
| B32 | PWM5 | D | | |
| A36 | PWM4 | D | | |
| PAD | GND | A | | GND connection. All internal references and logic are referenced to this pin. Filter to VCC with proper MLCC capacitor and connect to the PCB GND plane. |

1. D = digital, A = analog.

## 2.2 Thermal data

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{THJA}$ | Thermal resistance junction-to-ambient (device soldered on 2s2p PC board) | 40 | °C/W |
| $R_{THJC}$ | Thermal resistance junction-to-case | 1 | °C/W |
| $T_{MAX}$ | Maximum junction temperature | 150 | °C |
| $T_{STG}$ | Storage temperature range | -40 to 150 | °C |
| $T_J$ | Junction temperature range | 0 to 125 | °C |

# 3 Electrical specifications

## 3.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VDRV, GDC | to GND | -0.3 to 14 | V |
| VCC5, TM, STM, SPWM, PWMx, SENDRV, ENDRV, SCOMP, COMP, SMDATA, SMAL#, SMCLK | to GND | -0.3 to 7 | V |
| All other pins | to GND | -0.3 to 3.6 | V |

## 3.2 Electrical characteristics

($V_{CC5}$ = 5 V ± 5%, $T_J$ = 0 °C to 70 °C unless otherwise specified.)

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply current and power-on** | | | | | | |
| $I_{VCC5}$ | VCC5 supply current | EN = high | | 28 | | mA |
| | | EN = low | | 22 | | mA |
| $UVLO_{VCC5}$ | VCC5 turn-ON | VCC5 rising | | | 4.1 | V |
| | VCC5 turn-OFF | VCC5 falling | 3 | | | V |
| $UVLO_{VDRV}$ | VDRV turn-ON | VDRV rising | | | 6.0 | V |
| | VDRV turn-OFF | VDRV falling | 3 | | 4.1 | V |
| $UVLO_{VIN}$ | VIN turn-ON | VIN rising, $R_{UP}$ = 118.5 kΩ; $R_{DOWN}$ = 10 kΩ | | | 6.0 | V |
| | VIN turn-OFF | VIN falling, $R_{UP}$ = 118.5 kΩ; $R_{DOWN}$ = 10 kΩ | 3 | | 4.1 | V |
| **Oscillator, soft-start and enable** | | | | | | |
| $F_{SW}$ | Main oscillator accuracy | OSC = Open | 170 | 200 | 230 | kHz |
| | Oscillator adjustability | $R_{OSC}$ / $R_{SOSC}$ = 47 kΩ to GND | 378 | 420 | 462 | kHz |
| $F_{SSW}$ | Main oscillator accuracy | SOSC = Open | 212 | 250 | 287 | kHz |
| | Oscillator adjustability | $R_{OSC}$ / $R_{SOSC}$ = 47 kΩ to GND | 450 | 500 | 550 | kHz |
| $\Delta V_{OSC}$ | PWM ramp amplitude(1) | | | 1.5 | | V |
| FAULT | Voltage at pin OSC, SSOSC | Latch active for related section | 3 | | | V |

Table 5. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Soft-start | SS time - Intel CPU mode | Vboot > 0, from pin-strapping; multi-phase section | 5 | | | mV/µs |
| | | Vboot > 0, from pin-strapping; single-phase section | 2.5 | | | mV/µs |
| | | Vboot > 0, from pin-strapping; single-phase section, JMode ON | 2.5 | | | mV/µs |
| | SS time - Intel DDR mode | Vboot > 0, from pin-strapping; multi-phase section | 2.5 | | | mV/µs |
| | | Vboot > 0, from pin-strapping; single-phase section | 1.25 | | | mV/µs |
| | SS time - AMD mode | Vboot > 0, from pin-strapping; both sections | | 6.25 | | mV/µs |
| EN | Turn-ON | $V_{EN}$ rising | | | 0.6 | V |
| | Turn-OFF | $V_{EN}$ falling | 0.4 | | | V |
| | Leakage current | | | 1 | | µA |
| **SVI serial bus** | | | | | | |
| SVCLCK, SVDATA | Input high | | 0.65 | | | V |
| | Input low | | | | 0.45 | V |
| SVDATA, ALERT# | Voltage low (ACK) | $I_{SINK}$ = -5 mA | | | 50 | mV |
| **PMBus** | | | | | | |
| SMDATA, SMCLK | Input high | | 1.75 | | | V |
| | Input low | | | | 1.45 | V |
| SMAL# | Voltage low | $I_{SINK}$ = -4 mA | | | 13 | Ω |
| **Reference and DAC** | | | | | | |
| $k_{VID}$ | $V_{OUT}$ accuracy (MPhase) | $I_{OUT}$ = 0 A; N = 6; $R_G$ = 540 Ω; $R_{FB}$ = 1.108 kΩ; VID > 1.000 V | -0.5 | | 0.5 | % |
| $k_{SVID}$ | $V_{OUT}$ accuracy (SPhase) | $I_{OUT}$ = 0 A; $R_G$ = 1.3 kΩ; VID > 1.000 V | -0.5 | | 0.5 | % |
| | | $I_{OUT}$ = 0 A; $R_G$ = 1.3 kΩ; VID > 1.000 V; JMODE = ON | -5 | | 5 | mV |
| $k_{VID}$, $k_{SVID}$ | $V_{OUT}$ accuracy | VID = 0.8 V to 1 V | -5 | | 5 | mV |
| | | VID < 0.8 V | -8 | | 8 | mV |
| $k_{VOUT}$ | $V_{OUT}$ accuracy - AMD mode | | -20 | | 20 | mV |
| $\Delta_{DROOP}$ | LL accuracy (MPhase) 0 to full load | $I_{INFOx}$ = 0; N = 6; $R_G$ = 540 Ω; $R_{FB}$ = 1.108 kΩ | -3 | | 2 | µA |
| | | The same as above, $I_{INFOx}$ = 20 µA | -4.5 | | 4.5 | µA |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\Delta_{SDROOP}$ | LL accuracy (SPhase) 0 to full load | $I_{SCSN}$ = 0; $R_G$ = 1.3 kΩ | -1.75 | | 1 | µA |
| | | $I_{SCSN}$ = 20 µA; $R_G$ = 1.3 kΩ | -1 | | 1 | µA |
| $k_{IMON}$ | IMON accuracy (MPhase) | $I_{INFOx}$ = 0 µA; N = 6; $R_G$ = 540 Ω; $R_{FB}$ = 1.108 kΩ | 0 | | 0.75 | µA |
| | | Same as above, $I_{INFOx}$ = 20 µA | -4.5 | | 4.5 | µA |
| $k_{SIMON}$ | SIMON accuracy (SPhase) | $I_{SCSN}$ = 0 µA; $R_G$ = 1.3 kΩ | 0 | | 0.5 | µA |
| | | $I_{SCSN}$ = 20 µA; $R_G$ = 1.3 kΩ | -1 | | 1 | µA |
| $A_0$ | EA DC Gain(1) | | | 100 | | dB |
| SR | Slew rate(1) | COMP to SGND = 10 pF | | 20 | | V/µs |
| DVID - Intel CPU mode | Slew rate fast | Multi-phase section | 20 | | | mV/µs |
| | Slew rate slow | | 5 | | | mV/µs |
| | Slew rate fast | Single-phase section | 10 | | | |
| | Slew rate slow | | 2.5 | | | |
| DVID - Intel DDR mode | Slew rate fast | Multi-phase section | 10 | | | mV/µs |
| | Slew rate slow | | 2.5 | | | mV/µs |
| DVID - AMD mode | Slew rate | Both sections | | 5 | | mV/µs |
| IMON ADC | GetReg(15h) | V(IMON) = 0.992 V | | CC | | Hex |
| | Accuracy | | C0 | | CF | Hex |
| **PWM outputs and ENDRV** | | | | | | |
| PWMx, SPWM | Output high | I = 1 mA | | 5 | | V |
| | Output low | I = -1 mA | | | 0.2 | V |
| $I_{PWM1}$ | Test current | Sourced from pin, EN = 0. | | 10 | | µA |
| $I_{PWM2}$ | Test current | | | 0 | | µA |
| $I_{PWMx, SPWM}$ | Test current | Sourced from pin, EN = 0. | | -10 | | µA |
| ENDRV | Voltage low | $I_{ENDRV}$ = -4 mA; both sections | | | 0.4 | V |
| **Protection (both sections)** | | | | | | |
| OVP | Overvoltage protection | VSEN rising; wrt VID | 100 | | 200 | mV |
| UVP | Undervoltage protection | VSEN falling; wrt VID; VID > 500 mV | -525 | | -375 | mV |
| FBR DISC | FB disconnection | $V_{CS-}$ rising, above VSEN/SVSEN | 650 | 700 | 750 | mV |
| FBG DISC | FBG disconnection | FBR input wrt VID | 950 | 1000 | 1050 | mV |
| VR_RDY, SVR_RDY | Voltage low | $I_{SINK}$ = -4 mA | | | 0.4 | V |
| $V_{OC\_TOT}$ | OC threshold, MPhase | $V_{ILIM}$ rising, to GND | | 2.5 | | V |
| $V_{SOC\_TOT}$ | OC threshold, SPhase | $V_{SIMON}$ rising, to GND | | 1.55 | | V |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OC\_TH}$ | Constant current(1) | MPhase only | | 35 | | µA |
| VR_HOT | Voltage low | $I_{SINK}$ = -4 mA | | | 13 | Ω |
| **Gate drive control** | | | | | | |
| GDC | Max. current | Any PS. | | 200 | | mA |
| | Impedance | PS00h (GDC = VCC12) | | 6 | | Ω |
| | | > PS00h; (GDC = VCC5) | | 6 | | Ω |

1. Guaranteed by design, not subject to test.

# 4 Device configuration and pin-strapping tables

The L6751C device features a universal serial data bus fully compliant with Intel VR12/IMVP7 Protocol rev 1.5, document #456098 and AMD SVI specifications, document #40182. To guarantee proper device and CPU operation, refer to these documents for bus design, layout guidelines and any additional information required for the bus architecture. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing among SVI bus lines must be followed.

The controller configures itself automatically upon detection of different pin-strappings which are monitored at the IC power-up. See *Table 6*, *8*, *9*, *Table 10 on page 23*, and *Table 11 on page 24* for details.

## 4.1 JMode

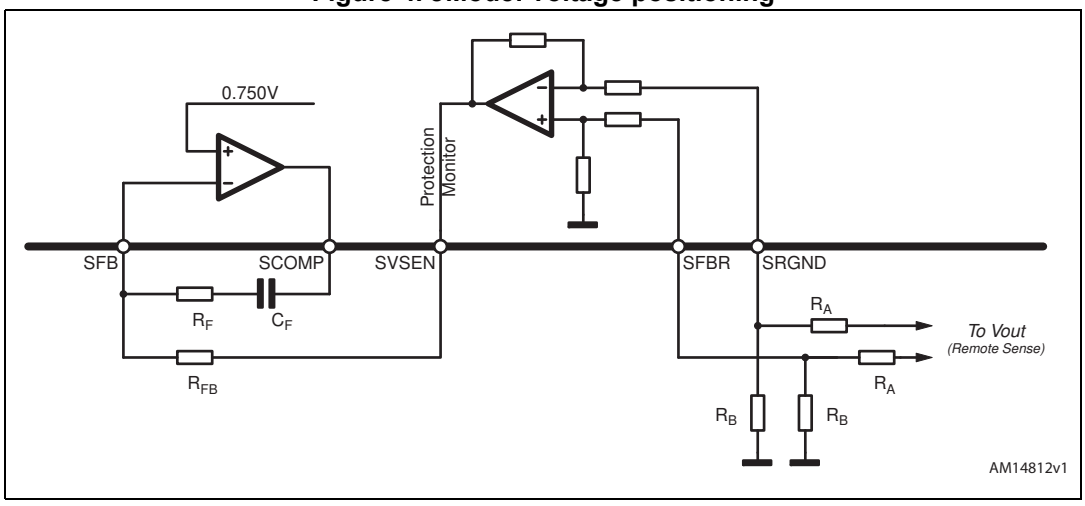
When enabled, multi-phase acts as if in DDR mode, while single-phase is an independent regulator with 0.75 V fixed reference (load-line disabled - TM can be used as enable for the single-phase).

Output voltage higher than the internal reference may be achieved by adding a proper resistor divider ($R_A$, $R_B$ - see *Figure 4*). To maintain precision in output voltage regulation, it is recommended to provide both SFBR and SRGND with the same divider.

**Equation 1**

$$V_{OUT} = 0.750 \cdot \frac{R_A + R_B}{R_B}$$

**Figure 4. JMode: voltage positioning**



## 4.2 Programming Hi-Z level

The L6751C is able to manage different levels for Hi-Z on PWMx guaranteeing flexibility in driving different external drivers as well as DrMOS ICs.

After EN assertion and before soft-start, the device uses PWM1 and PWM2 to detect the driver/DrMOS connected in order to program the suitable Hi-Z level of PWMx signals. During regulation, the Hi-Z level is used to force the external MOSFETs in high impedance state.

- PWM1 sources a constant 10 µA current, if its voltage results higher than 2.8 V, Hi-Z level used during the regulation is 1.4 V, if lower, PWM2 information is used.
- PWM2 is kept in Hi-Z, if its voltage results higher than 2 V, Hi-Z level used during the regulation is 2 V, if lower, 1.6 V.

An external resistor divider can be placed on PWM1 and PWM2 to force the detection of the correct Hi-Z level. They must be designed considering the external driver/DrMOS selected and the Hi-Z level requested.

**Table 6. Device configuration**

| | SVI address | DROOP (see *Table 8*) | IMAX / SIMAX | BOOT / TMAX | DPM |
|---|---|---|---|---|---|
| VR12 | 0000b | Enabled. | See *Table 8* | See*Table 10* | Supported |
| VR12[1] () | 0010b<br>0100b | MPhase: as per *Table 9*.<br>SPhase: disabled | | | |
| AMD | n/a | MPhase: enabled. SPhase: as per *Table 9*. | Ignored | TMAX[2] supported | |

1. In DDR mode, single-phase reference is multi-phase $V_{OUT}/2$ (JMode disabled).
2. Refer to *Table 10* and choose any of the resistor combinations leading to the desired TNMAX. Other settings are ignored.

**Table 7. Phase number programming**

| PHASE # | PWM1 to PWM3 | PWM4 | PWM5 | PWM6 |
|---|---|---|---|---|
| 3 | To driver | 1 kΩ to VCC5 | | |
| 4 | To driver | | 1 kΩ to VCC5 | |
| 5 | To driver | | | 1 kΩ to VCC5 |
| 6 | To driver | | | |

**Table 8. IMAX, SIMAX pinstrapping(1)**

| Rdown [kΩ] | Rup [kΩ] | IMAX / SIMAX | | |
|---|---|---|---|---|
| | | IMAX [A](2) | SIMAX [A] | |
| | | | GFX | VSA/DDR |
| 10 | 1.5 | N · 25 + 56 | 40 | 29 |
| 10 | 2.7 | | 35 | 21 |
| 22 | 6.8 | | 30 | 13 |
| 10 | 3.6 | | 25 | 5 |
| 27 | 11 | N · 25 + 48 | 40 | 29 |
| 12 | 5.6 | | 35 | 21 |
| 82 | 43 | | 30 | 13 |
| 13 | 7.5 | | 25 | 5 |
| 56 | 36 | N · 25 + 40 | 40 | 29 |
| 18 | 13 | | 35 | 21 |
| 15 | 12 | | 30 | 13 |
| 18 | 16 | | 25 | 5 |
| 15 | 14.7 | N · 25 + 32 | 40 | 29 |
| 10 | 11 | | 35 | 21 |
| 18 | 22 | | 30 | 13 |
| 56 | 75 | | 25 | 5 |
| 10 | 15 | N · 25 + 24 | 40 | 29 |
| 12 | 20 | | 35 | 21 |
| 12 | 22.6 | | 30 | 13 |
| 39 | 82 | | 25 | 5 |
| 47 | 110 | N · 25 + 16 | 40 | 29 |
| 10 | 27 | | 35 | 21 |
| 22 | 68 | | 30 | 13 |
| 10 | 36 | | 25 | 5 |
| 18 | 75 | N · 25 + 8 | 40 | 29 |
| 15 | 75 | | 35 | 21 |
| 10 | 59 | | 30 | 13 |
| 10 | 75 | | 25 | 5 |
| 10 | 100 | N · 25 | 40 | 29 |
| 10 | 150 | | 35 | 21 |
| 10 | 220 | | 30 | 13 |
| 10 | Open | | 25 | 5 |

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. N is the number of phase programmed for the multi-phase section.

**Table 9. ADDR pin-strapping(1), (2)**

| Rdown [kΩ] | Rup [kΩ] | ADDR | | | | |
|---|---|---|---|---|---|---|
| | | ADDR (3) | PMBADDR(4) | JMode | DROOP multi-phase | DROOP single-phase |
| 10 | 1.5 | AMD mode | CCh | n/a | ON | ON |
| 10 | 2.7 | | | | | OFF |
| 22 | 6.8 | | C8h | | | ON |
| 10 | 3.6 | | | | | OFF |
| 27 | 11 | | C4h | | | ON |
| 12 | 5.6 | | | | | OFF |
| 82 | 43 | | C0h | | | ON |
| 13 | 7.5 | | | | | OFF |
| 56 | 36 | 0100b (VR12) | EEh | n/a | ON | OFF |
| 18 | 13 | | | | OFF | |
| 15 | 12 | | EAh | | ON | |
| 18 | 16 | | | | OFF | |
| 15 | 14.7 | | E6h | | ON | |
| 10 | 11 | | | | OFF | |
| 18 | 22 | | E2h | | ON | |
| 56 | 75 | | | | OFF | |
| 10 | 15 | 0010b (VR12) | ECh | n/a | ON | OFF |
| 12 | 20 | | | | OFF | |
| 12 | 22.6 | | E8h | | ON | |
| 39 | 82 | | | | OFF | |
| 47 | 110 | | E4h | | ON | |
| 10 | 27 | | | | OFF | |
| 22 | 68 | | E0h | | ON | |
| 10 | 36 | | | | OFF | |
| 18 | 75 | 0000b (VR12) | CCh / 8Ch | ON | ON | According to VBOOT settings (GFX / VSA) |
| 15 | 75 | | | OFF | | |
| 10 | 59 | | C8h / 88h | ON | | |
| 10 | 75 | | | OFF | | |
| 10 | 100 | | C4h / 84h | ON | | |
| 10 | 150 | | | OFF | | |

**Table 9. ADDR pin-strapping(1), (2) (continued)**

| Rdown [kΩ] | Rup [kΩ] | ADDR | | | | |
|---|---|---|---|---|---|---|
| | | ADDR (3) | PMBADDR(4) | JMode | DROOP multi-phase | DROOP single-phase |
| 10 | 220 | 0000b (VR12) | C0h / 80h | ON | ON | According to VBOOT settings (GFX / VSA) |
| 10 | Open | | | OFF | | |

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. In DDR mode, when enabled, droop has 1/4th scaling factor.
3. SVI address for multi-phase. Single-phase is further offset by 0001b. In AMD mode, SVI address defaults according to AMD specifications.
4. PMBus address for multi-phase (read/write). Single-phase is further offset by 02h. When in VR12 CPU mode, RCOMP = 12.5 kΩ to GND, select between Cxh (Open) and 8xh (if installed) PMBus address.

**Table 10. BOOT / TMAX pin-strapping(1), (2)**

| Rdown [kΩ] | Rup [kΩ] | BOOT - Intel address 0000b(3) | | | Intel address 0010b, 0100b (3) | | | TMAX [C] |
|---|---|---|---|---|---|---|---|---|
| | | Multi-phase | Single-phase | Link rest | JMode | VBOOT | Link rest | |
| 10 | 1.5 | 1.000 V | 0.000 V VSA | 32 µsec (debug) | ON | 1.500 V | 32 µsec (debug) | 130 |
| 10 | 2.7 | | | | | | | 120 |
| 22 | 6.8 | | | | | | | 110 |
| 10 | 3.6 | | | | | | | 100 |
| 27 | 11 | 1.000 V | 1.000 V VSA | 32 µsec (debug) | | | 10 µsec (functional) | 130 |
| 12 | 5.6 | | | | | | | 120 |
| 82 | 43 | | | | | | | 110 |
| 13 | 7.5 | | | | | | | 100 |
| 56 | 36 | 0.000 V | 1.100 V VSA | 10 µsec (functional) | ON | 1.350 V | 32 µsec (debug) | 130 |
| 18 | 13 | | | | | | | 120 |
| 15 | 12 | | | | | | | 110 |
| 18 | 16 | | | | | | | 100 |
| 15 | 14.7 | 0.000 V | 1.000 V VSA | 10 µsec (functional) | | | 10 µsec (functional) | 130 |
| 10 | 11 | | | | | | | 120 |
| 18 | 22 | | | | | | | 110 |
| 56 | 75 | | | | | | | 100 |

**Table 10. BOOT / TMAX pin-strapping(1), (2) (continued)**

| Rdown [kΩ] | Rup [kΩ] | BOOT - Intel address 0000b(3) | | | Intel address 0010b, 0100b (3) | | | TMAX [C] |
|---|---|---|---|---|---|---|---|---|
| | | Multi-phase | Single-phase | Link rest | JMode | VBOOT | Link rest | |
| 10 | 15 | 0.000 V | 0.900 V VSA | 10 µsec (functional) | OFF | 1.500 V | 32 µsec (debug) | 130 |
| 12 | 20 | | | | | | | 120 |
| 12 | 22.6 | | | | | | | 110 |
| 39 | 82 | | | | | | | 100 |
| 47 | 110 | 0.000 V | 1.000 V GFX | 32 µsec (debug) | | | 10 µsec (functional) | 130 |
| 10 | 27 | | | | | | | 120 |
| 22 | 68 | | | | | | | 110 |
| 10 | 36 | | | | | | | 100 |
| 18 | 75 | 1.000 V | 1.000 V GFX | 32 µsec (debug) | OFF | 1.350 V | 32 µsec (debug) | 130 |
| 15 | 75 | | | | | | | 120 |
| 10 | 59 | | | | | | | 110 |
| 10 | 75 | | | | | | | 100 |
| 10 | 100 | 0.000 V | 0.000 V GFX | 10 µsec (functional) | | | 10 µsec (functional) | 130 |
| 10 | 150 | | | | | | | 120 |
| 10 | 220 | | | | | | | 110 |
| 10 | Open | | | | | | | 100 |

1. Recommended values, divider needs to be connected between VCC5 pin and GND.
2. BOOT is ignored in AMD mode, only TMAX is operative.
3. Operative mode defined by ADDR pin. See *Table 9* for details.

**Table 11. DPM pin-strapping(1)**

| Rdown [kΩ] | Rup [kΩ] | DPM1-3(2), (3) | | | DPM4-6(2), (3) | | |
|---|---|---|---|---|---|---|---|
| | | DPM12 | DPM23 | GDC0 | DPM34 | DPM46 | GDC1 |
| 10 | 1.5 | 16 A | +20 A | 1 | +30 A | +22 A | 1 |
| 10 | 2.7 | | | 0 | | | 0 |
| 22 | 6.8 | | +16 A | 1 | | +14 A | 1 |
| 10 | 3.6 | | | 0 | | | 0 |
| 27 | 11 | | +10 A | 1 | | +8 A | 1 |
| 12 | 5.6 | | | 0 | | | 0 |
| 82 | 43 | | +6 A | 1 | | DPM OFF | 1 |
| 13 | 7.5 | | | 0 | | | 0 |

**Table 11. DPM pin-strapping(1) (continued)**

| Rdown [kΩ] | Rup [kΩ] | DPM1-3(2), (3) | | | DPM4-6(2), (3) | | |
|---|---|---|---|---|---|---|---|
| | | DPM12 | DPM23 | GDC0 | DPM34 | DPM46 | GDC1 |
| 56 | 36 | 12 A | +20 A | 1 | +22 A | +22 A | 1 |
| 18 | 13 | | | 0 | | | 0 |
| 15 | 12 | | +16 A | 1 | | +14 A | 1 |
| 18 | 16 | | | 0 | | | 0 |
| 15 | 14.7 | | +10 A | 1 | | +8 A | 1 |
| 10 | 11 | | | 0 | | | 0 |
| 18 | 22 | | +6 A | 1 | | DPM OFF | 1 |
| 56 | 75 | | | 0 | | | 0 |
| 10 | 15 | 8 A | +20 A | 1 | +14 A | +22 A | 1 |
| 12 | 20 | | | 0 | | | 0 |
| 12 | 22.6 | | +16 A | 1 | | +14 A | 1 |
| 39 | 82 | | | 0 | | | 0 |
| 47 | 110 | | +10 A | 1 | | +8 A | 1 |
| 10 | 27 | | | 0 | | | 0 |
| 22 | 68 | | +6 A | 1 | | DPM OFF | 1 |
| 10 | 36 | | | 0 | | | 0 |
| 18 | 75 | OFF (12 A)(4) | +20 A | 1 | +8 A | +22 A | 1 |
| 15 | 75 | | | 0 | | | 0 |
| 10 | 59 | | +16 A | 1 | | +14 A | 1 |
| 10 | 75 | | | 0 | | | 0 |
| 10 | 100 | | +10 A | 1 | | +8 A | 1 |
| 10 | 150 | | | 0 | | | 0 |
| 10 | 220 | | +6 A | 1 | | DPM OFF(5) | 1 |
| 10 | Open | | | 0 | | | 0 |

1. Suggested values, divider needs to be connected between VCC5 pin and GND.
2. Transition threshold specified as delta with respect to previous step (DPM23 is wrt DPM12).
3. GDC threshold is defined by combining GDC0 and GDC1 bits defined between the two different pin-strappings DPM1-3 and DPM4-6. See *Table 12* for details.
4. Transition between 1Phase and 2Phase operation is set to 12 A but disabled in PS00h.
5. Dynamic phase management disabled, IC always working at maximum possible number of phases except from when in >PS00h when transitioning between 1Phase and 2Phase at 12 A.