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L6756D

2/3/4 phase buck controller
for VR10, VR11 and VR11.1 processor applications

Features

- LTB Technology® enhances load transient response
- 2 to 4 scalable phase operation
- Dual-edge asynchronous architecture
- PSI# input with programmable strategy
- Imon output
- Flexible driver support
- 7/8 bit programmable output - VR10/11.1 DAC
- 0.5% output voltage accuracy
- Full-differential current sense across DCR
- Integrated remote sense buffer
- Feedback disconnection protection
- Adjustable oscillator from 100 kHz to 1 MHz
- LSLess startup to manage pre-biased output
- Programmable soft-start
- Threshold sensitive enable pin for VTT Sensing
- VFQFPN40 6x6 mm package

Applications

- High-current VRM / VRD for desktop / server / workstation CPUs
- Graphic cards
- Low-voltage, high-current power supplies
- High-density DC / DC converters

VFQFPN40 6x6 mm
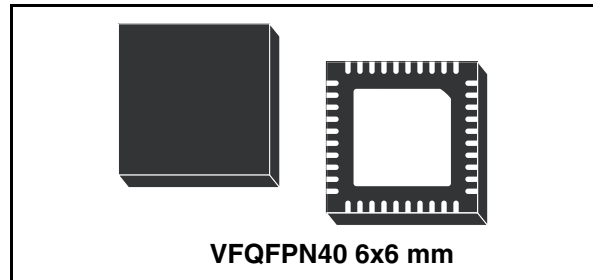
Description

L6756D is a two-to-four phase controller designed to power Intel's most demanding processors and, most in general, low-voltage, high-current power supplies. The device features LTB Technology® to provide the fastest response to load transients thus minimizing the output

filter composition.

L6756D embeds selectable DAC: output voltage is programmable up to 1.6000 V (Intel VR10 and VR11.x DACs) managing DVID transitions with ±0.5% output voltage accuracy over line, load and temperature variations.

The device assures fast protection against load over current and under / over voltage. Feedback disconnection prevents from damaging the load in case of misconnections in the system board.

Low-side-less start-up allows soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side.

L6756D is available in VFQFPN 6x6 mm package

Table 1. Device summary

Order code	Package	Packing
L6756D	VFQFPN40	Tube
L6756DTR	VFQFPN40	Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. **Typical 4phase application circuit**
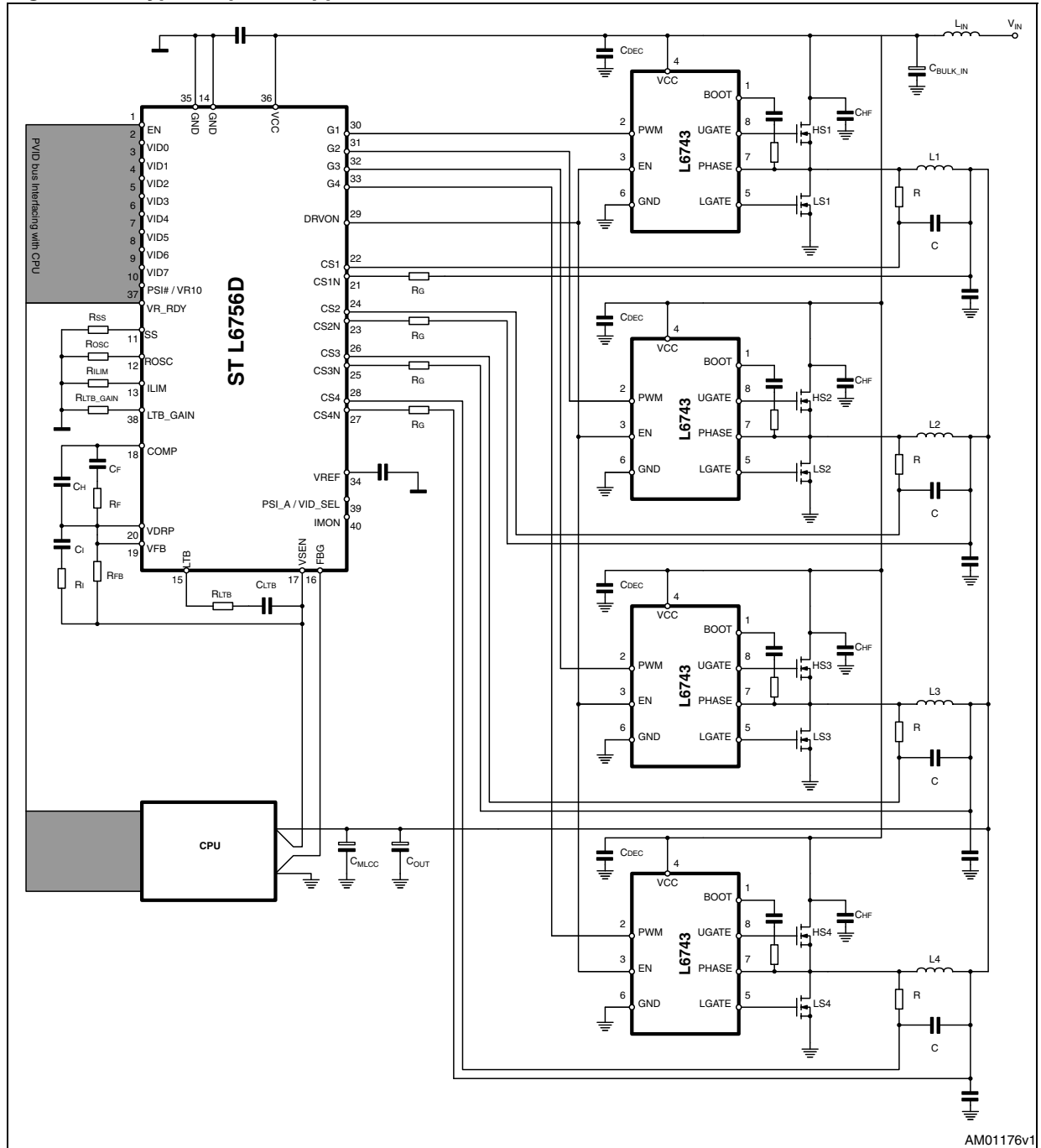
AM01176v1

Figure 2.   Typical 3phase application circuit
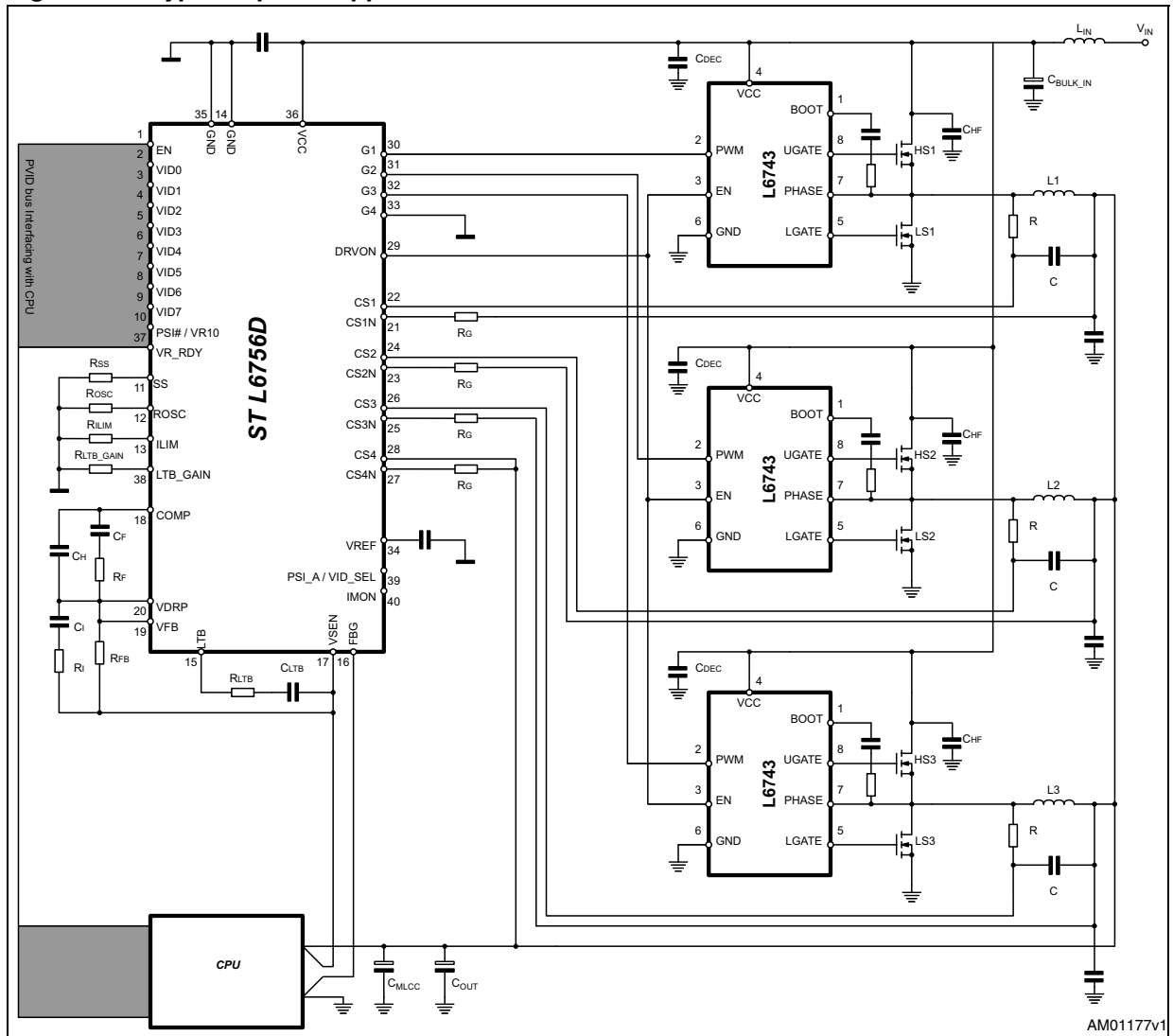
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Figure 3.   Typical 2phase application circuit

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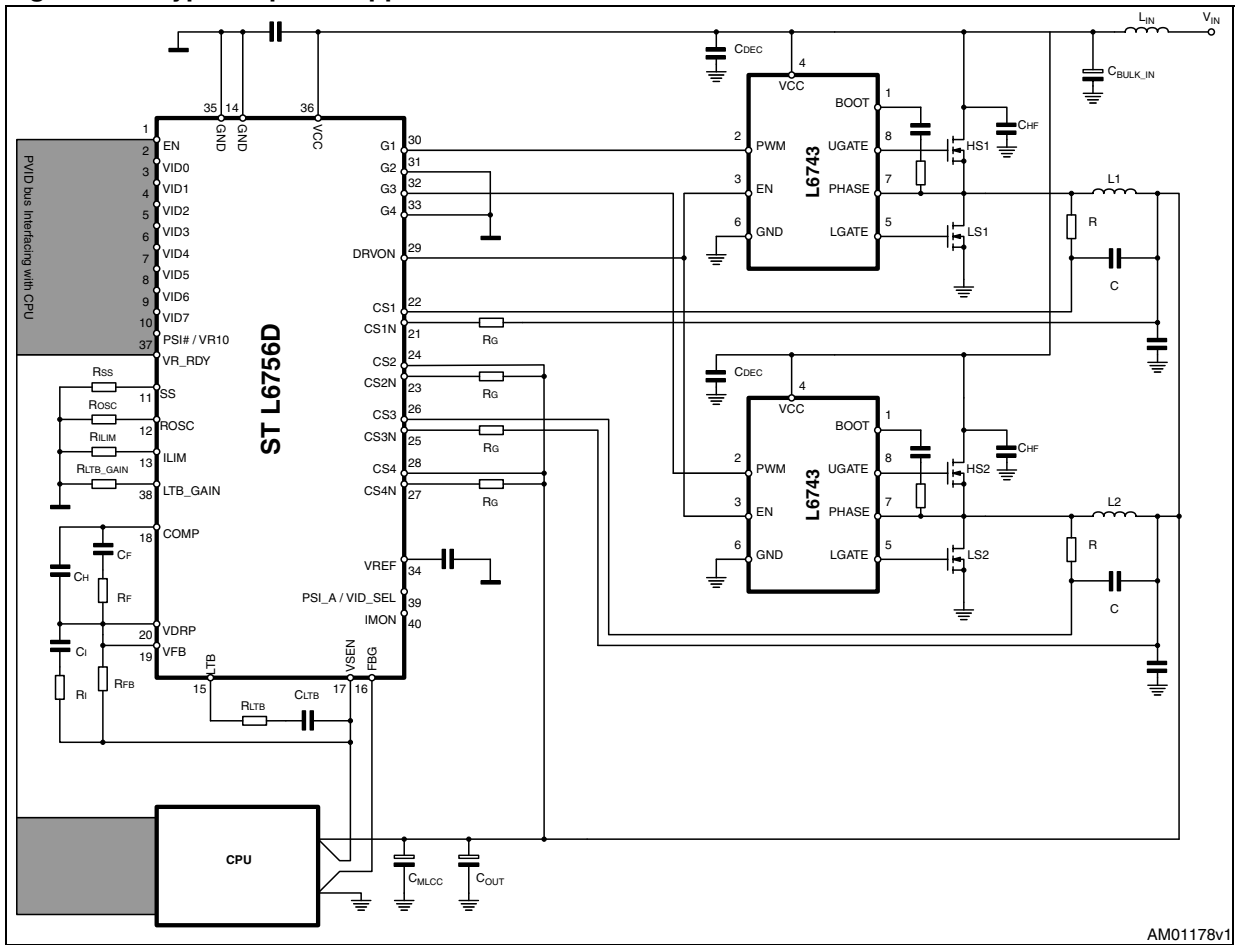
1.2 Block diagram

Figure 4. Block diagram

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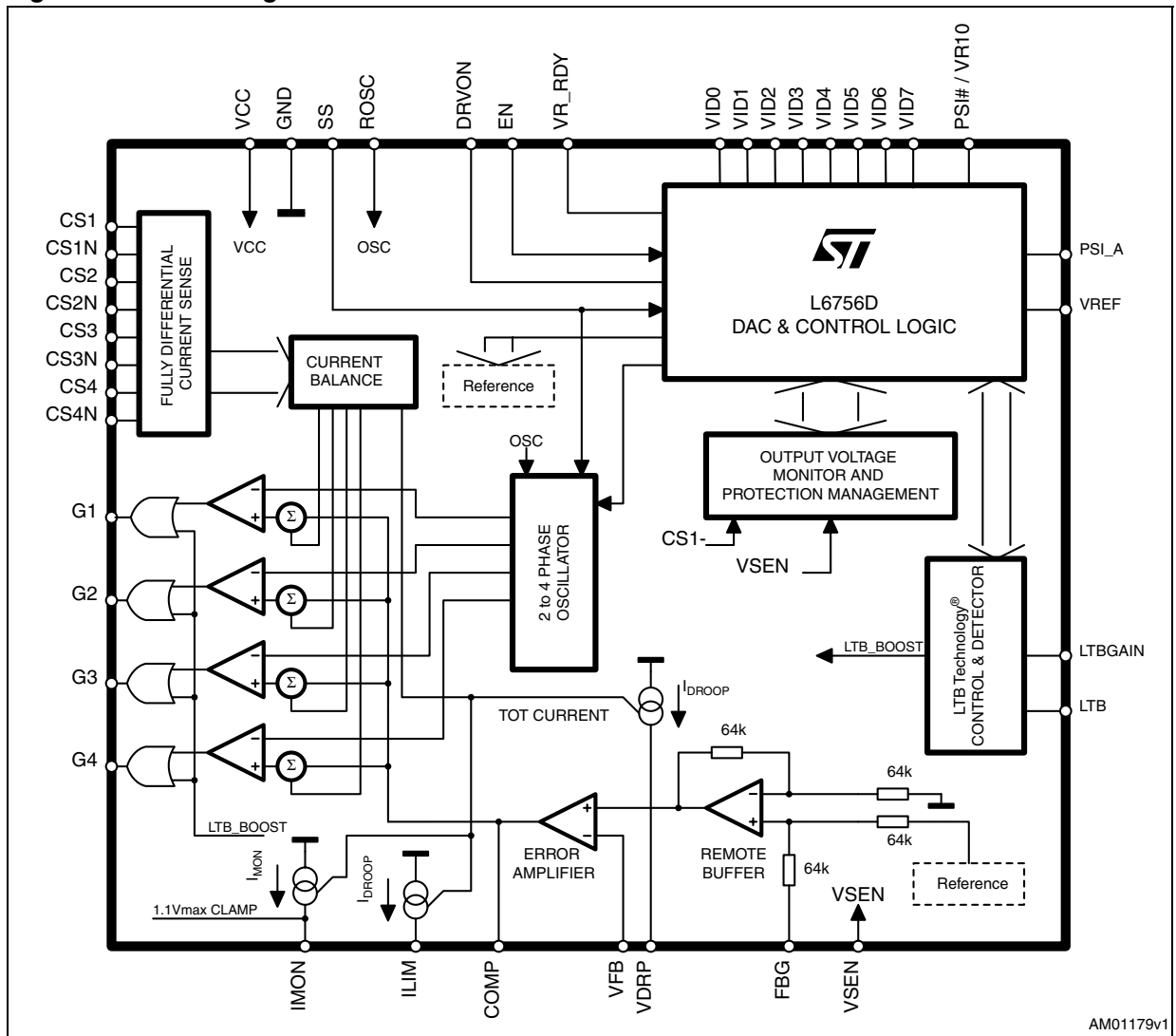
2 Pins description and connection diagrams

Figure 5. **Pins connection (top view)**

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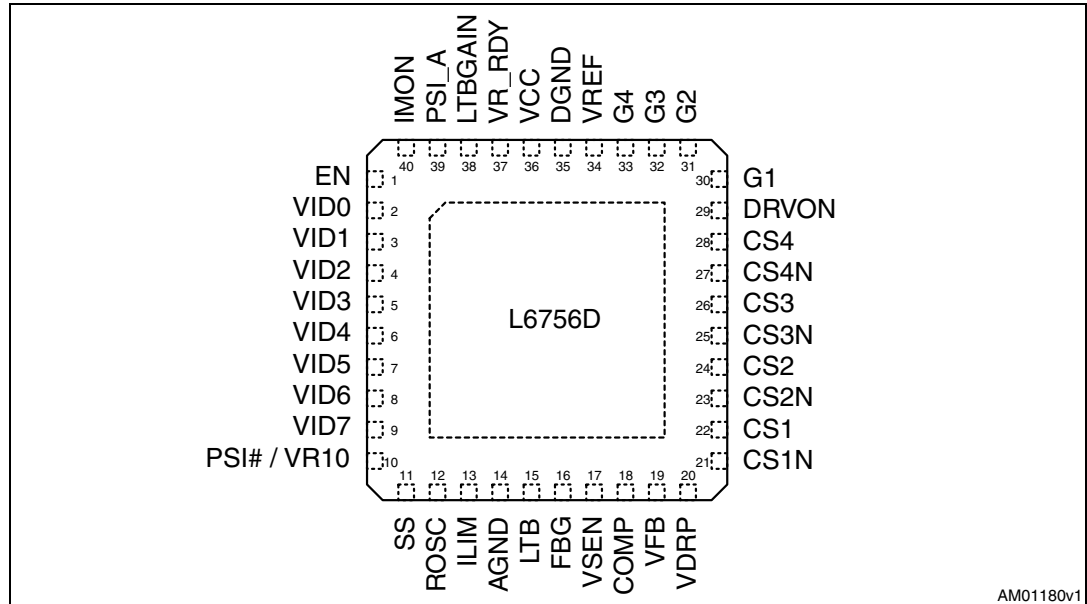
2.1 Pin descriptions

Table 2. **Pin description**

Pin#	Name	Function
1	EN	VR enable. Internally pulled-up by 10 μA to 3.3 V. Pull-low to disable the device, set free or pull up above turn-on threshold to enable the controller.
2 to 9	VID0 to VID7	Voltage IDentification pins. 3.3 V compatible, they allow programming output voltage as specified in *Table 6* and *Table 7* according to VR10/1 pin status.
10	PSI# / VR10	According to the status of PSI_A, the functionality of this pin changes as below: *PSI#*: Power state indicator input. Connect to the PSI# pin on the CPU to manage low-power state. When asserted (pulled low), the controller will act as programmed on the PSI_A pin. *VR10*: It allows selecting between VR10 (short to SGND, See *Table 6*) or VR11 (floating, See *Table 7*) DACs.
11	SS	By connecting a resistor R_{SS} to GND, it allows programming the soft-start time. soft-start time T_{SS} will proportionally change with a gain of 18.52 [μs / kΩ]. Connect 27 kΩ resistor to program T2 = 500 μs. The same slope implemented to reach V_{BOOT} has to be considered also when the reference moves from V_{BOOT} to the programmed VID code. The pin is kept to a fixed 1.24 V.

Table 2.   Pin description (continued)

Pin#	Name	Function
12	ROSC	Oscillator pin. It allows programming the switching frequency F_{SW} of each channel: the equivalent switching frequency at the load side results in being multiplied by the phase number N. Frequency is programmed according to the resistor connected from the pin to GND or VCC with a gain of 10 kHz/μA. Leaving the pin floating programs a switching frequency of 200 kHz per phase.
13	ILIM	Over current SET pin. Connect to GND through a R_{ILIM} resistor to set the OC threshold. this pin sources a copy of the DROOP current; OC is set when the voltage at the pin crosses 1.7 V (typ). See *Section 6.4* for details.
14	GND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
15	LTB	Load transient boost Technology® input pin. See *Section 9.2* for details.
16	FBG	Remote ground sense. Connect to the negative side of the load to perform remote sense.
17	VSEN	Output voltage monitor, manages OVP and UVP protections. Connect to the positive side of the load to perform remote sense. A fixed 50 μA current is sunk through this pin to implement small positive offset for the regulated voltage. See *Section 5.4* for details.
18	COMP	Error Amplifier Output. Connect with an R_F - C_F // C_H to VFB. The device cannot be disabled by pulling low this pin.
19	VFB	error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an R_F - C_F // C_H to COMP.
20	VDRP	A current proportional to the total current read is sourced from this pin according to the current reading gain. Short to VFB to implement voltage positioning or connect to GND through a resistor and filter with 1 nF capacitor to implement an additional load indicator.
21	CS1N	Channel 1 current sense negative input. Connect through a Rg resistor to the output-side of the channel inductor.
22	CS1	Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
23	CS2N	Channel 2 current sense negative input. Connect through a Rg resistor to the output-side of the channel inductor. When working at 2 phase, still connect through Rg to CS2 and then to the regulated voltage.
24	CS2	Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor. When working at 2 phase, short to the regulated voltage.
25	CS3N	Channel 3 current sense negative input. Connect through a Rg resistor to the output-side of the channel inductor.
26	CS3	Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor.
27	CS4N	Channel 4 current sense negative input. Connect through a Rg resistor to the output-side of the channel inductor. When working at 2 or 3 phase, still connect through Rg to CS3 and then to the regulated voltage.

Table 2.   Pin description (continued)

Pin#	Name	Function
28	CS4	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at 2 or 3 phase, short to the regulated voltage.
29	DRVON	External driver enable. CMOS output used to control the external driver status: pulled-low to manage HiZ conditions or pulled-high for normal driver switching.
30 to 33	G1 to G4	PWM outputs. Connect to external drivers PWM inputs. The device is able to manage HiZ status by setting the pins floating. By shorting to GND G4 or G2 and G4, it is possible to program the device to work at 3 or 2 phase respectively.
34	VREF	This pin provide a 2.5 V reference. Filter with 1 nF (max) to SGND.
35	GND	All the internal references are referred to this pin. Connect to the PCB signal ground.
36	VCC	Device power supply. Operative voltage is 12 V ±15 %. Filter with at least 1 μF MLCC vs. ground.
37	VR_RDY	Open drain output set free after SS has finished and pulled low when triggering any protection. Pull up to a voltage lower than 3.3 V (typ), if not used it can be left floating.
38	LTB_GAIN	Load transient boost technology® gain pin. See *Section 9.2* for details.
39	PSI_A	PSI action configuration pin. This pins configures the functionality of the PSI# / VR10 pin according to *Table 9* as follow: VR10: Short to SGND to configure the VID_SEL functionality. The controller will not manage low power-states but will be backward compatible with VR10 / VR11 platforms. PSI#: The device will work in VR11 mode and perform low power-states management through the PSI# pin. See *Section 7* for details.
40	IMON	Current monitor output. A current proportional to the read current is sourced from this pin. Connect through a resistor R_{MON} to FBG to implement a load indicator. Connect the load indicator directly to VR11.1 CPUs.The pin voltage is clamped to 1.1V max to preserve the CPU from excessive voltages.
	Thermal pad	Thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PGND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (Device soldered on 2s2p PC board)	35	°C/W
R_{thJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to PGND	15	V
	All other Pins to PGNDx	-0.3 to 3.6	V

3.2 Electrical characteristics

Table 5. Electrical characteristics
(V_{CC} = 12 V ± 15 %, T_J = 0 °C to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current			25		mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising			9.75	V
	VCC turn-OFF	VCC falling	7			V
Oscillator, soft-start and ENABLE						
F_{SW}	Main oscillator accuracy		185	200	215	kHz
	Oscillator adjustability	R_{OSC} = 33 kΩ		500		kHz
ΔV_{OSC}	PWM ramp amplitude			1.5		V
FAULT	Voltage at pin OSC	OV, UV latch active	3		3.6	V
SOFT-START		T_{D1} - initial delay	1	2	3	ms
		T_{D2} - R_{SS} = 27 kΩ	400	500	600	μs
		T_{D3} - V_{BOOT}	100	200	300	μs
		Boot voltage - V_{BOOT}	1.026	1.081	1.136	V
EN		V_{EN} rising	0.80	0.85	0.90	V
		Hysteresis		100		mV
Reference and DAC						
K_{VID}	V_{OUT} accuracy	VSEN to V_{CORE}; FBG to GND_{CORE}	-0.5		0.5	%
I_{OS}	OFFSET	VSEN = 0.5000 V to 1.6000 V	-40	-50	-60	μA
A_0	EA DC gain			130		dB
SR	Slew rate	COMP to SGND = 10 pF		25		V/μs
VID_{IL}	VID threshold,	Input low			0.3	V
VID_{IH}		Input high	0.8			V

Table 5.   **Electrical characteristics (continued)**
                  (V_{CC} = 12 V ± 15 %, T_J = 0 °C to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PSI#/VR10	Input threshold	Input low			0.3	V
		Input high	0.8			V
VREF	Reference voltage		2.450	2.500	2.550	V
LTBGAIN	LTBGAIN voltage			1.24		V
Differential current sense and current monitor						
k_{IDROOP}	DROOP accuracy	Rg = 1 kΩ; I_{DROOP} < 100 μA	-4		4	μA
k_{IMON}	IMON accuracy	Rg = 1 kΩ; I_{MON} < 100 μA	-6		6	μA
k_{ILIM}	ILIM accuracy	Rg = 1 kΩ; I_{ILIM} < 100 μA	-8		8	μA
PWM outputs						
Gx	Output high	I = 1 mA	3			V
	Output low	I = -1 mA			0.2	V
I_{Gx}	Test current			10		μA
DRVON	Output low	I = -5 mA			0.4	V
Protections						
OVP		VSEN rising; wrt Ref.	150	175	200	mV
UVP	Under voltage protection	VSEN falling; wrt Ref; Ref > 500mV		-400		mV
VR_RDY	Voltage low	I_{VR_RDY} = -4 mA			0.4	V
$V_{FB-DISC}$	FB disconnection	V_{CSN} rising, above VSEN	550	650	750	mV
FBG DISC	FBG disconnection	EA NI input wrt VID	400	500	600	mV
V_{ILIM_OC}	OC threshold	V_{ILIM} rising	1.6	1.7	1.8	V
		V_{ILIM} rising, during DVID		2.5		V

Table 6.   Voltage identification (VID) for Intel VR11.x mode

HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage
0	0	OFF	4	0	1.21250	8	0	0.81250	C	0	0.41250
0	1	OFF	4	1	1.20625	8	1	0.80625	C	1	0.40625
0	2	1.60000	4	2	1.20000	8	2	0.80000	C	2	0.40000
0	3	1.59375	4	3	1.19375	8	3	0.79375	C	3	0.39375
0	4	1.58750	4	4	1.18750	8	4	0.78750	C	4	0.38750
0	5	1.58125	4	5	1.18125	8	5	0.78125	C	5	0.38125
0	6	1.57500	4	6	1.17500	8	6	0.77500	C	6	0.37500
0	7	1.56875	4	7	1.16875	8	7	0.76875	C	7	0.36875
0	8	1.56250	4	8	1.16250	8	8	0.76250	C	8	0.36250
0	9	1.55625	4	9	1.15625	8	9	0.75625	C	9	0.35625
0	A	1.55000	4	A	1.15000	8	A	0.75000	C	A	0.35000
0	B	1.54375	4	B	1.14375	8	B	0.74375	C	B	0.34375
0	C	1.53750	4	C	1.13750	8	C	0.73750	C	C	0.33750
0	D	1.53125	4	D	1.13125	8	D	0.73125	C	D	0.33125
0	E	1.52500	4	E	1.12500	8	E	0.72500	C	E	0.32500
0	F	1.51875	4	F	1.11875	8	F	0.71875	C	F	0.31875
1	0	1.51250	5	0	1.11250	9	0	0.71250	D	0	0.31250
1	1	1.50625	5	1	1.10625	9	1	0.70625	D	1	0.30625
1	2	1.50000	5	2	1.10000	9	2	0.70000	D	2	0.30000
1	3	1.49375	5	3	1.09375	9	3	0.69375	D	3	0.29375
1	4	1.48750	5	4	1.08750	9	4	0.68750	D	4	0.28750
1	5	1.48125	5	5	1.08125	9	5	0.68125	D	5	0.28125
1	6	1.47500	5	6	1.07500	9	6	0.67500	D	6	0.27500
1	7	1.46875	5	7	1.06875	9	7	0.66875	D	7	0.26875
1	8	1.46250	5	8	1.06250	9	8	0.66250	D	8	0.26250
1	9	1.45625	5	9	1.05625	9	9	0.65625	D	9	0.25625
1	A	1.45000	5	A	1.05000	9	A	0.65000	D	A	0.25000
1	B	1.44375	5	B	1.04375	9	B	0.64375	D	B	0.24375
1	C	1.43750	5	C	1.03750	9	C	0.63750	D	C	0.23750
1	D	1.43125	5	D	1.03125	9	D	0.63125	D	D	0.23125
1	E	1.42500	5	E	1.02500	9	E	0.62500	D	E	0.22500
1	F	1.41875	5	F	1.01875	9	F	0.61875	D	F	0.21875
2	0	1.41250	6	0	1.01250	A	0	0.61250	E	0	0.21250
2	1	1.40625	6	1	1.00625	A	1	0.60625	E	1	0.20625

Table 6. **Voltage identification (VID) for Intel VR11.x mode (continued)**

HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage	HEX code VID[7:0]		Output voltage
2	2	1.40000	6	2	1.00000	A	2	0.60000	E	2	0.20000
2	3	1.39375	6	3	0.99375	A	3	0.59375	E	3	0.19375
2	4	1.38750	6	4	0.98750	A	4	0.58750	E	4	0.18750
2	5	1.38125	6	5	0.98125	A	5	0.58125	E	5	0.18125
2	6	1.37500	6	6	0.97500	A	6	0.57500	E	6	0.17500
2	7	1.36875	6	7	0.96875	A	7	0.56875	E	7	0.16875
2	8	1.36250	6	8	0.96250	A	8	0.56250	E	8	0.16250
2	9	1.35625	6	9	0.95625	A	9	0.55625	E	9	0.15625
2	A	1.35000	6	A	0.95000	A	A	0.55000	E	A	0.15000
2	B	1.34375	6	B	0.94375	A	B	0.54375	E	B	0.14375
2	C	1.33750	6	C	0.93750	A	C	0.53750	E	C	0.13750
2	D	1.33125	6	D	0.93125	A	D	0.53125	E	D	0.13125
2	E	1.32500	6	E	0.92500	A	E	0.52500	E	E	0.12500
2	F	1.31875	6	F	0.91875	A	F	0.51875	E	F	0.11875
3	0	1.31250	7	0	0.91250	B	0	0.51250	F	0	0.11250
3	1	1.30625	7	1	0.90625	B	1	0.50625	F	1	0.10625
3	2	1.30000	7	2	0.90000	B	2	0.50000	F	2	0.10000
3	3	1.29375	7	3	0.89375	B	3	0.49375	F	3	0.09375
3	4	1.28750	7	4	0.88750	B	4	0.48750	F	4	0.08750
3	5	1.28125	7	5	0.88125	B	5	0.48125	F	5	0.08125
3	6	1.27500	7	6	0.87500	B	6	0.47500	F	6	0.07500
3	7	1.26875	7	7	0.86875	B	7	0.46875	F	7	0.06875
3	8	1.26250	7	8	0.86250	B	8	0.46250	F	8	0.06250
3	9	1.25625	7	9	0.85625	B	9	0.45625	F	9	0.05625
3	A	1.25000	7	A	0.85000	B	A	0.45000	F	A	0.05000
3	B	1.24375	7	B	0.84375	B	B	0.44375	F	B	0.04375
3	C	1.23750	7	C	0.83750	B	C	0.43750	F	C	0.03750
3	D	1.23125	7	D	0.83125	B	D	0.43125	F	D	0.03125
3	E	1.22500	7	E	0.82500	B	E	0.42500	F	E	OFF
3	F	1.21875	7	F	0.81875	B	F	0.41875	F	F	OFF

Table 7.   Voltage identifications (VID) for Intel VR10 mode + 6.25 mV

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Output voltage	VID4	VID3	VID2	VID1	VID0	VID5	VID6	Output voltage
0	1	0	1	0	1	1	1.60000	1	1	0	1	0	1	1	1.20000
0	1	0	1	0	1	0	1.59375	1	1	0	1	0	1	0	1.19375
0	1	0	1	1	0	1	1.58750	1	1	0	1	1	0	1	1.18750
0	1	0	1	1	0	0	1.58125	1	1	0	1	1	0	0	1.18125
0	1	0	1	1	1	1	1.57500	1	1	0	1	1	1	1	1.17500
0	1	0	1	1	1	0	1.56875	1	1	0	1	1	1	0	1.16875
0	1	1	0	0	0	1	1.56250	1	1	1	0	0	0	1	1.16250
0	1	1	0	0	0	0	1.55625	1	1	1	0	0	0	0	1.15625
0	1	1	0	0	1	1	1.55000	1	1	1	0	0	1	1	1.15000
0	1	1	0	0	1	0	1.54375	1	1	1	0	0	1	0	1.14375
0	1	1	0	1	0	1	1.53750	1	1	1	0	1	0	1	1.13750
0	1	1	0	1	0	0	1.53125	1	1	1	0	1	0	0	1.13125
0	1	1	0	1	1	1	1.52500	1	1	1	0	1	1	1	1.12500
0	1	1	0	1	1	0	1.51875	1	1	1	0	1	1	0	1.11875
0	1	1	1	0	0	1	1.51250	1	1	1	1	0	0	1	1.11250
0	1	1	1	0	0	0	1.50625	1	1	1	1	0	0	0	1.10625
0	1	1	1	0	1	1	1.50000	1	1	1	1	0	1	1	1.10000
0	1	1	1	0	1	0	1.49375	1	1	1	1	0	1	0	1.09375
0	1	1	1	1	0	1	1.48750	1	1	1	1	1	0	1	OFF
0	1	1	1	1	0	0	1.48125	1	1	1	1	1	0	0	OFF
0	1	1	1	1	1	1	1.47500	1	1	1	1	1	1	1	OFF
0	1	1	1	1	1	0	1.46875	1	1	1	1	1	1	0	OFF
1	0	0	0	0	0	1	1.46250	0	0	0	0	0	0	1	1.08750
1	0	0	0	0	0	0	1.45625	0	0	0	0	0	0	0	1.08125
1	0	0	0	0	1	1	1.45000	0	0	0	0	0	1	1	1.07500
1	0	0	0	0	1	0	1.44375	0	0	0	0	0	1	0	1.06875
1	0	0	0	1	0	1	1.43750	0	0	0	0	1	0	1	1.06250
1	0	0	0	1	0	0	1.43125	0	0	0	0	1	0	0	1.05625
1	0	0	0	1	1	1	1.42500	0	0	0	0	1	1	1	1.05000
1	0	0	0	1	1	0	1.41875	0	0	0	0	1	1	0	1.04375
1	0	0	1	0	0	1	1.41250	0	0	0	1	0	0	1	1.03750
1	0	0	1	0	0	0	1.40625	0	0	0	1	0	0	0	1.03125
1	0	0	1	0	1	1	1.40000	0	0	0	1	0	1	1	1.02500
1	0	0	1	0	1	0	1.39375	0	0	0	1	0	1	0	1.01875

Table 7. **Voltage identifications (VID) for Intel VR10 mode + 6.25 mV (continued)**

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Output voltage	VID4	VID3	VID2	VID1	VID0	VID5	VID6	Output voltage
1	0	0	1	1	0	1	1.38750	0	0	0	1	1	0	1	1.01250
1	0	0	1	1	0	0	1.38125	0	0	0	1	1	0	0	1.00625
1	0	0	1	1	1	1	1.37500	0	0	0	1	1	1	1	1.00000
1	0	0	1	1	1	0	1.36875	0	0	0	1	1	1	0	0.99375
1	0	1	0	0	0	1	1.36250	0	0	1	0	0	0	1	0.98750
1	0	1	0	0	0	0	1.35625	0	0	1	0	0	0	0	0.98125
1	0	1	0	0	1	1	1.35000	0	0	1	0	0	1	1	0.97500
1	0	1	0	0	1	0	1.34375	0	0	1	0	0	1	0	0.96875
1	0	1	0	1	0	1	1.33750	0	0	1	0	1	0	1	0.96250
1	0	1	0	1	0	0	1.33125	0	0	1	0	1	0	0	0.95625
1	0	1	0	1	1	1	1.32500	0	0	1	0	1	1	1	0.95000
1	0	1	0	1	1	0	1.31875	0	0	1	0	1	1	0	0.94375
1	0	1	1	0	0	1	1.31250	0	0	1	1	0	0	1	0.93750
1	0	1	1	0	0	0	1.30625	0	0	1	1	0	0	0	0.93125
1	0	1	1	0	1	1	1.30000	0	0	1	1	0	1	1	0.92500
1	0	1	1	0	1	0	1.29375	0	0	1	1	0	1	0	0.91875
1	0	1	1	1	0	1	1.28750	0	0	1	1	1	0	1	0.91250
1	0	1	1	1	0	0	1.28125	0	0	1	1	1	0	0	0.90625
1	0	1	1	1	1	1	1.27500	0	0	1	1	1	1	1	0.90000
1	0	1	1	1	1	0	1.26875	0	0	1	1	1	1	0	0.89375
1	1	0	0	0	0	1	1.26250	0	1	0	0	0	0	1	0.88750
1	1	0	0	0	0	0	1.25625	0	1	0	0	0	0	0	0.88125
1	1	0	0	0	1	1	1.25000	0	1	0	0	0	1	1	0.87500
1	1	0	0	0	1	0	1.24375	0	1	0	0	0	1	0	0.86875
1	1	0	0	1	0	1	1.23750	0	1	0	0	1	0	1	0.86250
1	1	0	0	1	0	0	1.23125	0	1	0	0	1	0	0	0.85625
1	1	0	0	1	1	1	1.22500	0	1	0	0	1	1	1	0.85000
1	1	0	0	1	1	0	1.21875	0	1	0	0	1	1	0	0.84375
1	1	0	1	0	0	1	1.21250	0	1	0	1	0	0	1	0.83750
1	1	0	1	0	0	0	1.20625	0	1	0	1	0	0	0	0.83125

Table 8.   **Gate output connections for phase # definition**

Mode	Gate output connections			
	G1	**G2**	**G3**	**G4**
2-phase	to driver	GND	to driver	GND
3-phase	to driver	to driver	to driver	GND
4-phase	to driver	to driver	to driver	to driver

4   Device description and operation

L6756D is a programmable two-to-four phase PWM controller providing complete control logic and protections for a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor power supply. The device is a dual-edge asynchronous PWM controller featuring patented LTB Technology®: through a load transient detector, it turns on simultaneously all the phases allowing to minimize output voltage deviation so minimizing the system cost by providing the fastest response to a load transition.

Multi-phase buck is the simplest and most cost-effective topology employable to satisfy the increasing current demand of newer microprocessors and modern high current VRM modules. It allows distributing equally load and power between the phases using smaller, cheaper and most common external power MOSFETs and inductors. Moreover, thanks to the equal phase shift between each phase, the input and output capacitor count results in being reduced. Phase interleaving causes in fact input rms current and output ripple voltage reduction and show an effective output switching frequency increase: the 200 kHz free-Running frequency per phase, externally adjustable through a resistor, results multiplied on the output by the number of phases.

L6756D permits easy system design by allowing current reading across inductor in fully differential mode. Also a sense resistor in series to the inductor can be considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

The controller includes multiple DACs, selectable through an apposite pin, allowing compatibility with Intel VR10, VR11 and VR11.1 processors specifications, also performing D-VID transitions accordingly.

The device is VR11.1 compatible implementing the Imon signal and managing the PSI# signal to enhance the system performances at low current in low power-states.

Low-side-less start-up allows soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side.

L6756D provides overvoltage protection to protect the load from dangerous over stress latching immediately by turning ON the lower driver and driving high the FAULT pin.

The device is available in a compact VFQFPN40 with 6x6 mm body package.

5 Output voltage positioning

Output voltage positioning is performed by selecting the controller operation mode (*VR10, VR11 or VR11.1*) and by programming the droop function and offset to the reference of both the sections (See *Figure 6*). The controller reads the current delivered by monitoring the voltage drop across the Inductors DCR. The current (I_{DROOP}) sourced from the DROOP pin, directly proportional to the read current, causes the output voltage to vary according to the external R_{FB} resistor so implementing the desired load-line effect. A fixed current (I_{OS}) is sunk through the VSEN pins causing the output voltage to be offset according to the resistance R_{OS} connected.

L6756D allows to recover from GND losses in order to regulate remotely the programmed voltage without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Both DROOP and OFFSET function can be disabled. In case DROOP effect is not desired, the current information source from the DROOP pin may be used to implement a secondary load indicator as reported in *Section 5.3*.

Figure 6. Voltage positioning
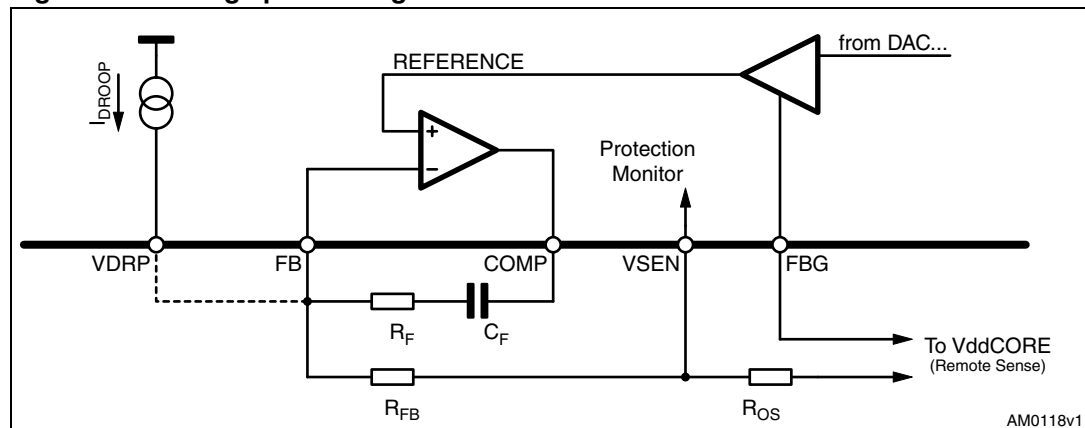
5.1 Phase # programming

L6756D implements a flexible 2 to 4 interleaved-phase converter. To program the desired number of phase, refer to *Table 8*.

For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSx needs to be connected to the regulated output voltage while CSxN needs to be connected to CSx with the same R_G resistor used for the other phases.

5.2 Current reading and current sharing loop

L6756D embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows placing sensing element in different locations without affecting the measurement's accuracy. The trans-conductance ratio is issued by the external resistor R_G placed outside the chip between CSxN pin toward the reading points. The current sense circuit always tracks the current information, the pin CSx is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (See *Figure 7*):

$$I_{CSx-} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L / DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now to match the time constant between the inductor and the R-C filter applied (Time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

$$\frac{L}{R_L} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{Rg} \cdot I_{PHASEx} = I_{INFOx}$$

R_G resistor is tipical designed in order to have an information current I_{INFOx} in the range of $35\mu A$ at the OC Threshold.

The current read through the CSx / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

Figure 7. Current reading connections
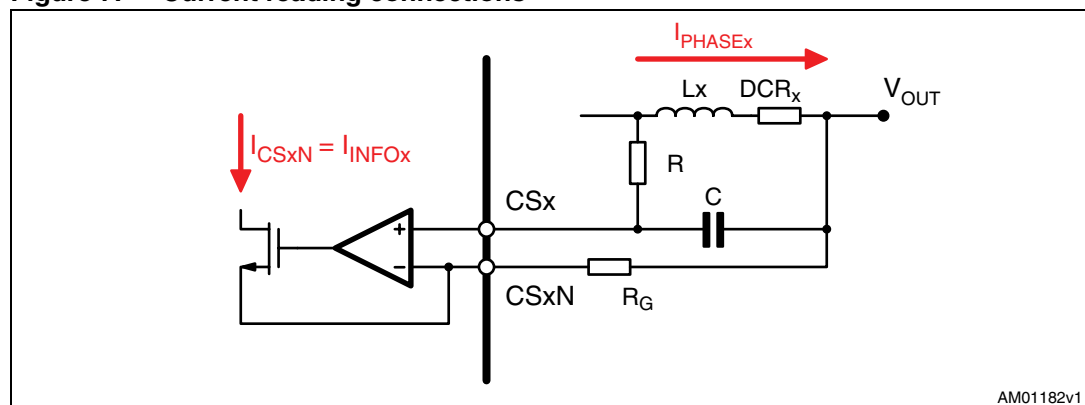
5.3 Output voltage load-line definition

L6756D is able to introduce a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 7 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R - C filter across CSx and CSxN pins. R_G programs a transconductance gain and generates a current I_{CSx} proportional to the current of the phase x. The sum of the I_{CSx} current is then sourced by the VFB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope (*Figure 6*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system so avoiding over and/or under shoot of the output voltage as a consequence of a load transient. The output characteristic vs. load current is then given by (Offset disabled):

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

Where R_{LL} is the resulting load-line resistance implemented by the controller. The whole power supply can be then represented by a "real" voltage generator with an equivalent output resistance R_{LL} and a voltage value of VID.

R_{FB} resistor can be then designed according to the R_{LL} specifications as follow:

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

Note: *Load-Line (DROOP) implementation is optional, in case it is not desired, the resulting current information available on VDRP may be employed for other purposes, such as an additional Load Indicator (LI2). In this case, simply connect a resistor R_{LI2} to SGND: the resulting voltage drop across R_{LI2} will be proportional to the delivered current according to the following relationship:*

$$V_{LI2} = R_{LI2} \cdot \frac{DCR}{R_G} \cdot I_{OUT}$$

In case no additional information about the delivered current is requested, the VDRP pin can be shorted to SGND.

5.4 Output voltage offset

The current (I_{OS}) sunk from the VSEN pin allows programming a positive offset (V_{OS}) for the output voltage by connecting a resistor R_{OS} to V_{OUT} in series to the FB loop. The sunk current generates a voltage drop according to the connected R_{OS}. Output voltage is then programmed as follow:

$$V_{CORE} = VID - (R_{FB} + R_{OS}) \cdot I_{DROOP} + R_{OS} \cdot I_{OS}$$

Caution: Offset resistor impacts the voltage positioning! It need to be considered in series to R_{FB}.

Note: *Offset implementation is optional: in case it is not desired, simply consider using $R_{OS} = 0\ \Omega$*

5.5 Dynamic VID transitions

L6756D manages dynamic VID transitions that allow the output voltage to modify during normal device operation for CPU power management purposes. OV and UV signals are properly masked during every DVID Transition and they are re-activated with a 16 clock cycle delay to prevent from false triggering.

When changing dynamically the regulated voltage (DVID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current I_{DVID} needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the over current threshold of both the sections. This current results:

$$I_{DVID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the operative mode (typically externally driven).

Dynamic VID transition is managed by checking for VID code modifications (See *Figure 8*) on the rising edge of an internal additional DVID-clock and waiting for a confirmation on the following falling edge. Once the new code is stable, on the next rising edge, the reference starts stepping up or down in LSB increments every two DVID-clock cycle until the new VID code is reached.

DVID-clock frequency (F_{DVID}) is 1 MHz (Typ).

Caution: Overcoming the OC threshold during the DVID causes the device latch and disable.

Caution: If the new VID code is more than 1 LSB different from the previous, the device will execute the transition stepping the reference with the DVID-clock frequency F_{DVID} until the new code has reached. The output voltage rate of change will be of [LSB]mV * F_{DVID}!

Figure 8.   DVID transitions
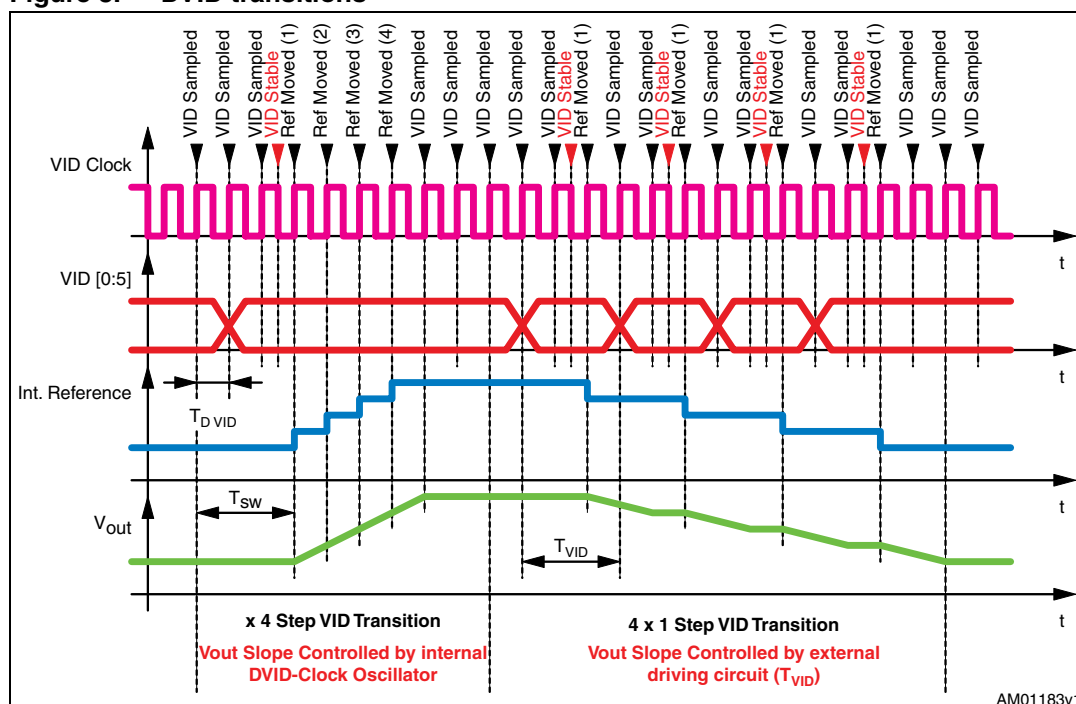
5.6 Soft-start

L6756D implements a soft-start to smoothly charge the output filter avoiding high in-rush currents to be required to the input power supply. During this phase, the device increases the reference from zero up to the programmed reference in closed loop regulation. Soft-start is implemented only when all the power supplies are above their own turn-on thresholds and the EN pin is set free. At the end of the digital soft-start, VR_RDY signal is set free.

Soft-start phase is initiated with a T1 = 2 ms (min) delay. After that, the reference ramps up to V_{BOOT} = 1.081 V in T2 according to the R_{SS} settings and waits for T3 = 200 μsec (typ) during which the device reads the VID lines. Output voltage will then ramps up to the programmed value in T4 with the same slope as before (See *Figure 9*).

SS sets the output voltage dv/dt during soft-start according to the resistor R_{SS} connected to SGND. soft-start time T_{SS} will proportionally change with a gain of 18.52 [μs / kΩ]. Connect 27 kΩ resistor to program T2 = 500 μs.

Protections are active during soft-start, UVP is enabled after the reference reaches 0.5 V while OVP is always active with a fixed 1.24 V threshold before V_{BOOT} and with the threshold coming from the VID after V_{BOOT} (See red-dashed line in *Figure 9*).

Note: *If during T3 the programmed VID selects an output voltage lower than V_{BOOT}, the output voltage will ramp to the programmed voltage starting from V_{BOOT}.*

Note: *The VID code is checked at the end of T3. In case the device is enabled over an OFF code, the output voltage will rise up to V_{BOOT} and then device will latch. VID lines does not show any pull-up and/or pull-down before T3.*

Figure 9.   Soft-start timings
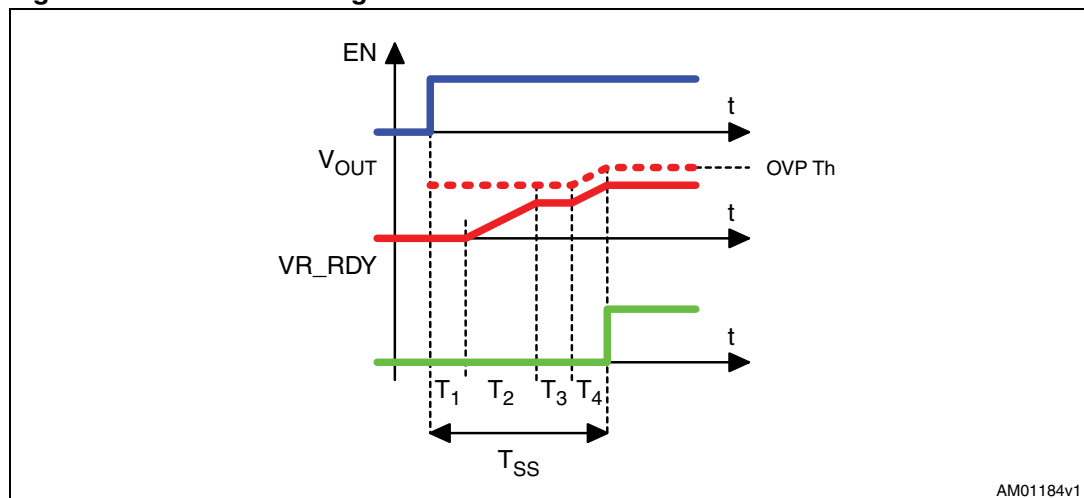
5.6.1 LSLESS start-up

In order to avoid any kind of negative undershoot on the load side during start-up, L6756D performs a special sequence in enabling the drivers for both sections: during the soft-start phase, the LS driver results to be disabled (LS = OFF - Gx set to HiZ and DRVON = 0) until the first PWM pulse. After the first PWM pulse, Gx outputs switches between logic "0" and logic "1" and DRVON is set to logic "1".

This particular sequence avoids the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output.

Low-side MOSFET turn-on is masked only from the control loop point of view: protections are still allowed to turn-ON the low-side MOSFET in case of overvoltage if needed.

Figure 10. LSLESS start-up: enabled (left) and disabled (right)

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