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L6759D

3+1 dual controller for VR12 with PMBus

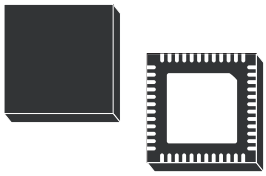
Datasheet – production data

Features

- VR12 compliant with 25 MHz SVID bus Rev1.5
  - SerialVID with programmable IMAX, TMAX, VBOOT, ADDRESS
- Second generation LTB Technology™
- Flexible driver/DrMOS support
- JMode support
- Fully configurable through PMBus
- Dual controller:
  - 3-phase for VDDQ
  - 1-phase for VTT
- Single NTC design for TM, LL and Imon thermal compensation
- VFDE and GDC - gate drive control for efficiency optimization
- DPM - dynamic phase management
- Dual remote sense
- 0.5% output voltage accuracy
- Full-differential current sense across DCR
- AVP - adaptive voltage positioning
- Dual independent adjustable oscillator
- Dual current monitor
- Pre-biased output management
- Average and per-phase OC protection
- OV, UV and FB disconnection protection
- Dual VR_RDY
- VFQFPN48 6x6 mm package

Application

- DDR3 memory supply for VR12 servers



VFQFPN48 - 6x6mm

Description

The L6759D is a dual controller designed to power Intel's VR12 processor memories: all required parameters are programmable through dedicated pin-strapping and PMBus interface.

The device features 3-phase programmable operation for the multi-phase section and a single-phase with independent control loops. Single-phase (VTT) reference is always tracking multi-phases (VDDQ) scaled by a factor of 2.

The L6759D supports power state transitions featuring VFDE, programmable DPM and GDC maintaining the best efficiency over all loading conditions without compromising transient response.

The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in a VFQFPN48 6x6 mm package.

Table 1. Device summary

Order code	Package	Packing
L6759D	VFQFPN48 6x6mm	Tray
L6759DTR		Tape and reel

Contents

List of Tables

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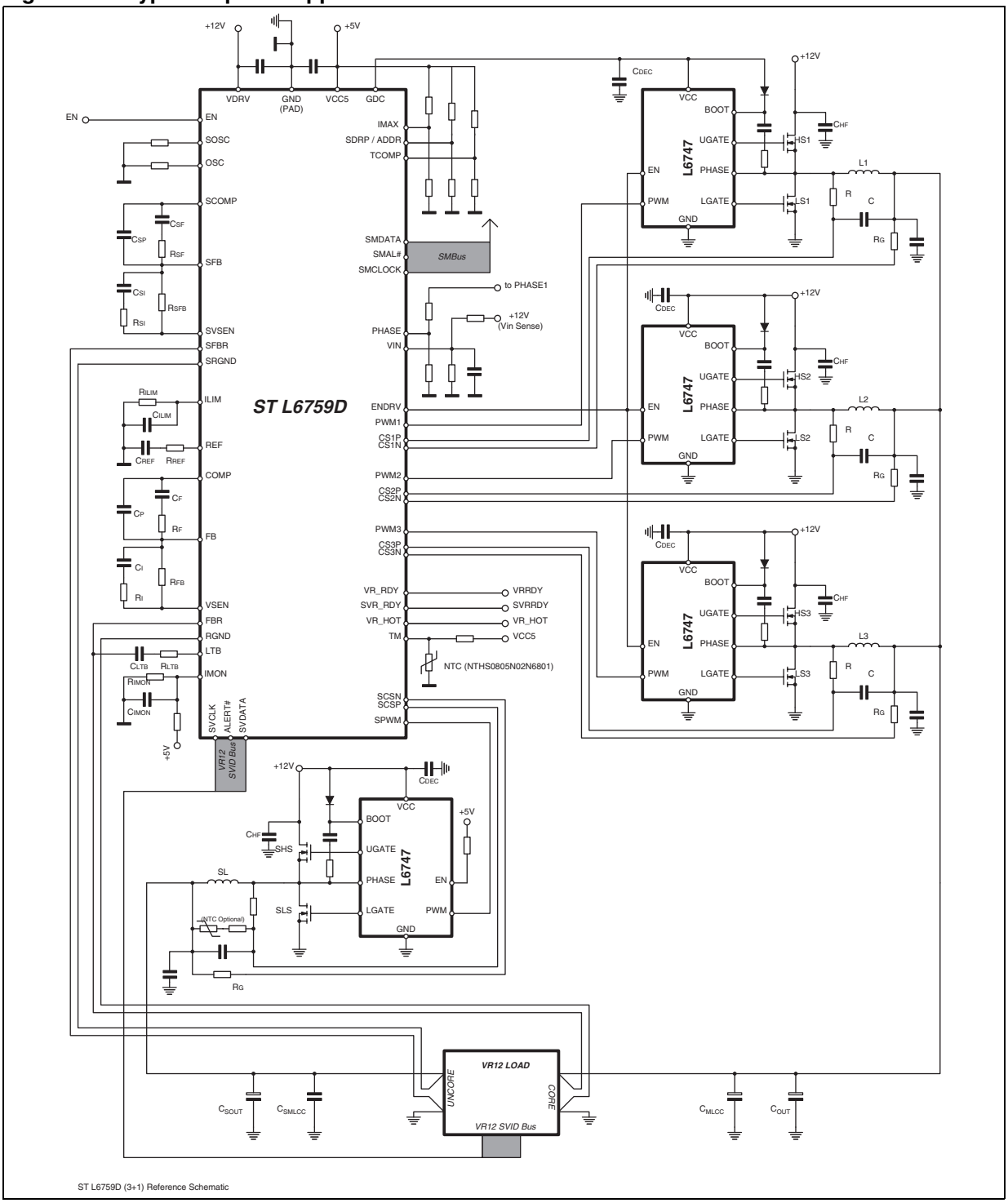
1 Typical application circuit and block diagram

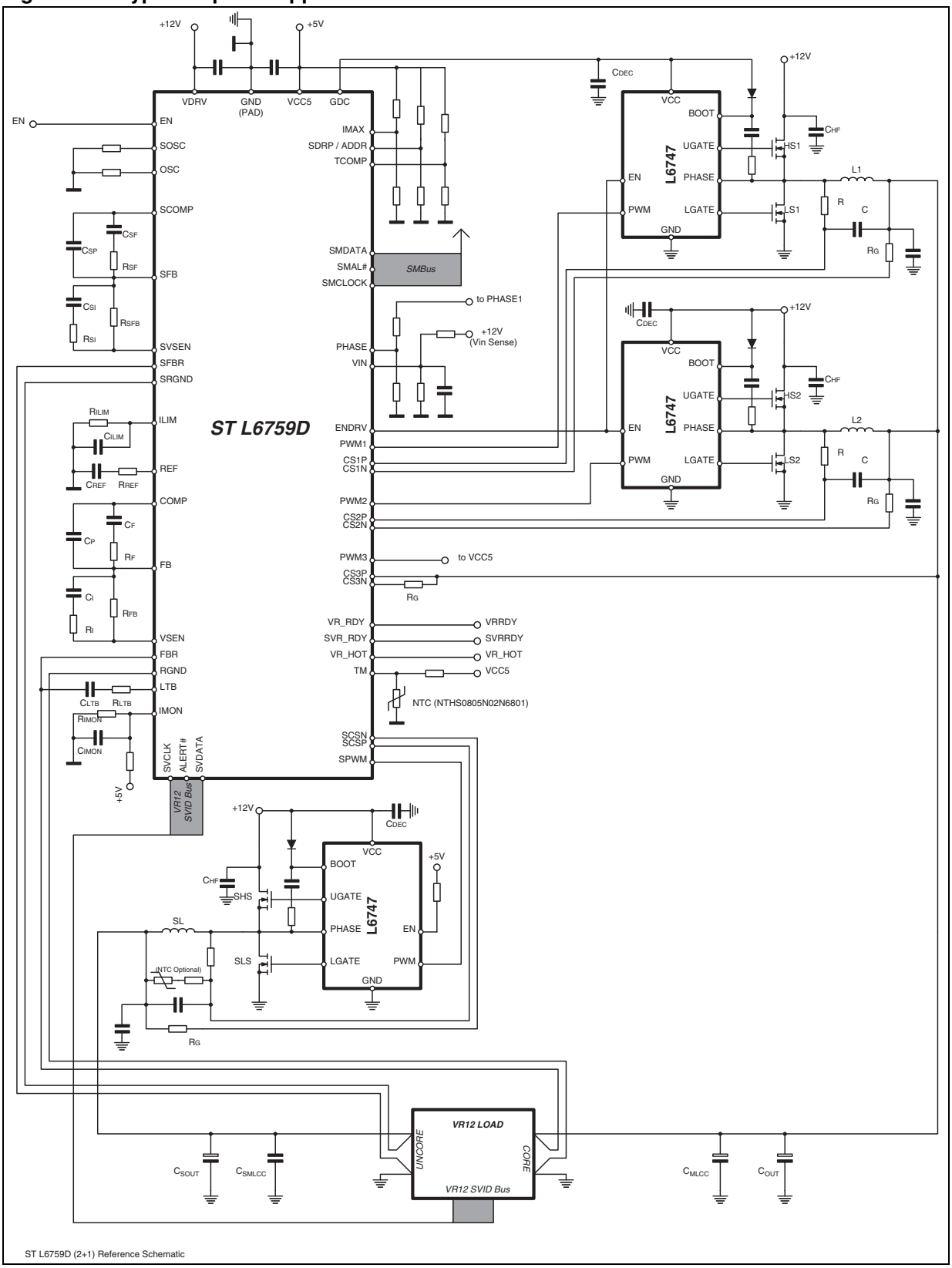
1.1 Application circuit

Figure 1. Typical 3-phase application circuit



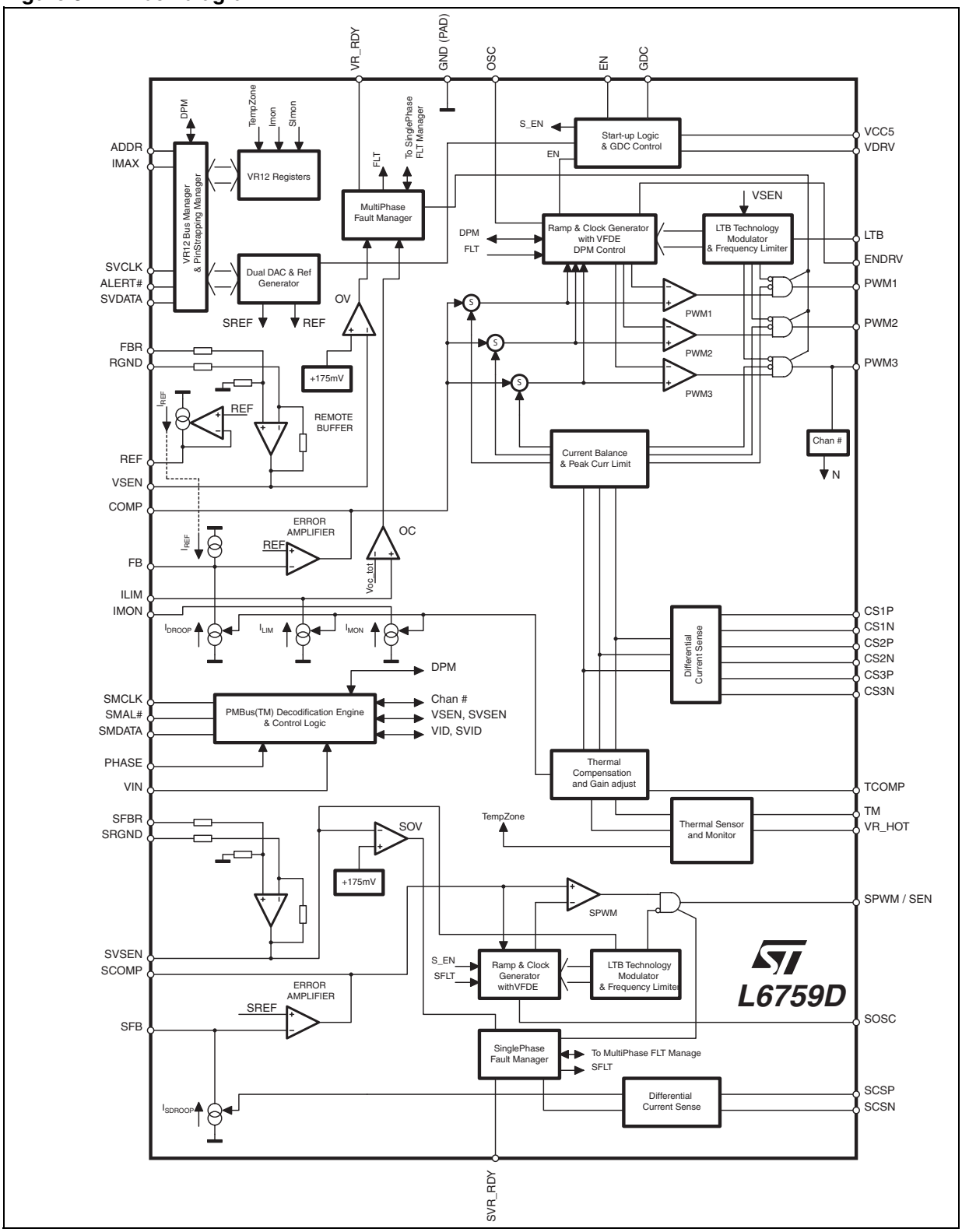
ST L6759D (3+1) Reference Schematic

Figure 2. Typical 2-phase application circuit



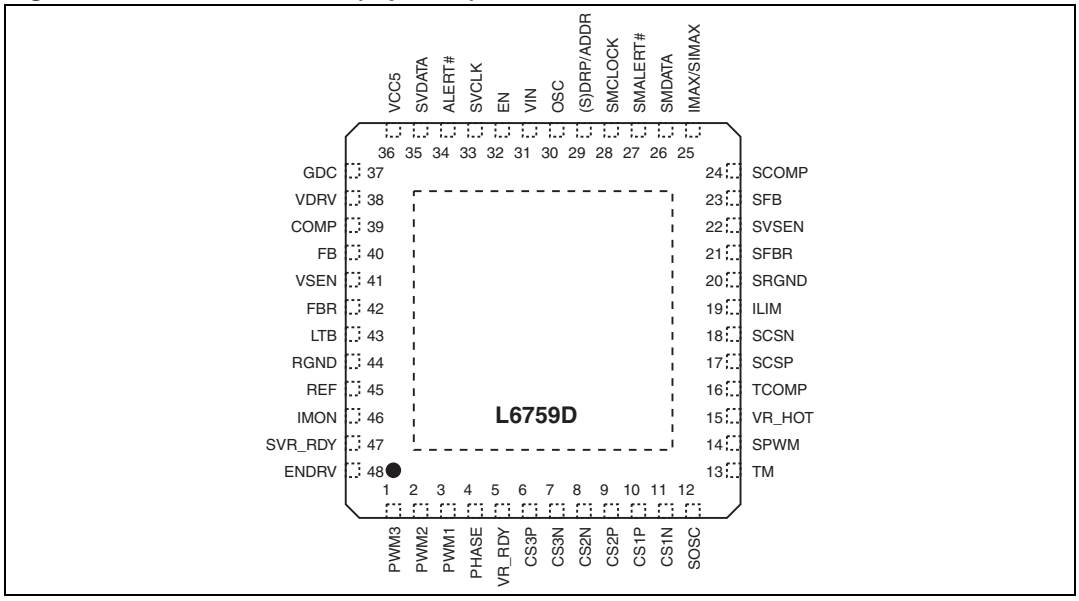
1.2 Block diagram

Figure 3. Block diagram



2 Pin description and connection diagrams

Figure 4. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin#	Name		Function
1 to 3	PWM3 to PWM1	Multi-phase section	PWM outputs. Connect to multi-phase external drivers PWM input. These pins are also used to configure HiZ levels for compatibility with drivers and DrMOS. During normal operations the device is able to manage the HiZ status by setting and holding the PWMx pin to a pre-defined fixed voltage. Connect PWM3 to 5 V through 1 kW resistor to program 2-phase operation.
4	PHASE		Connect through resistor divider to Channel1 multi-phase switching node.
5	VR_RDY		VR ready. Open drain output set free after SS has finished in multi-phase and pulled low when triggering any protection on the multi-phase section. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
6	CS3P		Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2-phase, short to the regulated voltage.
7	CS3N		Channel 3 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at 2-phase, still connect through Rg to CS3P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
8	CS2N	Multi-phase section	Channel 2 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
9	CS2P		Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.
10	CS1P		Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
11	CS1N		Channel 1 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
12	SOSC	SIngle-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SSW} for the single-phase section. The pin is internally set to 1.02 V, frequency for single-phase is programmed according to the resistor connected to GND or VCC with a gain of 11.5 kHz/µA. Leaving the pin floating programs a switching frequency of 230 kHz. See *Section 10* for details.
13	TM	Multi-phase section	Thermal monitor sensor. Connect with the proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature zone register. By programming proper TCOMP gain, the IC also implements load-line thermal compensation for the multi-phase section. In JMode, the pin disables the single-phase section if shorted to GND. Pull up to VCC5 with 1 kΩ to disable the thermal sensor. See *Section 6* for details.
14	SPWM / SEN	Single-phase section	PWM output. Connect to single-phase external driver PWM input. During normal operations the device is able to manage HiZ status by setting and holding the SPWM pin to a fixed voltage defined by PWMx strapping. Connect to VCC5 with 1 kΩ to disable the single-phase section.
15	VR_HOT		Voltage regulator HOT. Open drain output, this is an alarm signal asserted by the controller when the temperature sensed through the TM pin exceeds TMAX (active low). See *Section 6* for details.
16	TCOMP	Multi-phase section	Thermal monitor sensor gain. Connect the proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by TM to implement thermal compensation for the multi-phase section. Short to GND to disable temperature compensation (but not thermal monitor). See *Section 6* for details.
17	SCSP	Single-phase section	Single-phase section current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
18	SCSN		Single-phase section current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
19	I_{LIM}	Single-phase section	Multi-phase section current limit. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{LIM} to GND. When the pin voltage reaches 2.5 V, the overcurrent protection is set and the IC latches. Filter through C_{LIM} to GND to delay OC intervention.
20	SRGND		Remote buffer ground sense. Connect to the negative side of the single-phase load to perform remote sense.
21	SFBR		Remote buffer positive sense. Connect to the positive side of the single-phase load to perform remote sense.
22	SVSEN		Remote buffer output. Output voltage monitor, manages OV and UV protection. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SFB.
23	SFB		Error amplifier inverting input. Connect with a resistor R_{SFB} // (R_{SI} - C_{SI}) to SVSEN and with an (R_{SF} - C_{SF})// C_{SH} to SCOMP.
24	SCOMP		Error amplifier output. Connect with an (R_{SF} - C_{SF})// C_{SH} to SFB. The device cannot be disabled by pulling low this pin.
25	IMAX	Pin-strapping	Connect a resistor divider to GND/VCC5 in order to define the IMAX register. JMode and BOOT voltage can be controlled through this pin. See *Table 6* and *Section 6* for details.
26	SMDATA	PMBus	PMBus data.
27	SMAL#		PMBus alert.
28	SMCLOCK		PMBus clock.
29	ADDR	Pin-strapping	Connect a resistor divider to GND/VCC5 in order to define the IC address, to define the GDC and DPM thresholds and to control the droop function on multi-phase. See *Table 6* and *Section 6* for details.
30	OSC	Multi-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SW} for the multi-phase section. The pin is internally set to 1.02 V, the frequency for multi-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 kHz/µA. Leaving the pin floating programs a switching frequency of 200 kHz per phase. The effective frequency observable on the load results being multiplied by the number of active phases N. See *Section 10* for details.
31	VIN		Input voltage monitor. Connect to input voltage monitor point through a divider R_{UP} / R_{DOWN} to perform VIN sense through PMBus (R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ typ.). See *Section 12.3* for details.

Table 2. Pin description (continued)

Pin#	Name		Function
32	EN		VTT level sensitive enable pin (3.3 V compatible). Pull low to disable the device, pull up above the turn-on threshold to enable the controller.
33	SVCLK	SVI BUS	Serial clock.
34	ALERT#		Alert.
35	SVDATA		Serial data.
36	VCC5		Main IC power supply. Operative voltage is 5 V ±5%. Filter with 1 µF MLCC to GND (typ.).
37	GDC		Gate drive control pin. Used for efficiency optimization, see *Section 9* for details. If not used, it can be left floating. Always filter with 1 µF MLCC to GND.
38	VDRV		Driving voltage for external drivers. Connect to the selected voltage rail to drive the external MOSFET when in maximum power conditions. IC switches GDC voltage between VDRV and VCC5 to implement efficiency optimization according to selected strategies.
39	COMP / ADDR	Multi-phase section	Error amplifier output. Connect with an (R_F - C_F)// C_P to FB. The device cannot be disabled by pulling low this pin. Connect R_{COMP} to GND to extend PMBus addressing range (see *Table 6*).
40	FB		Error amplifier inverting input. Connect with a resistor R_{FB} // (R_I - C_I) to VSEN and with an (R_F - C_F)// C_P to COMP.
41	VSEN		Output voltage monitor, manages OV and UV protection. Connect to the positive side of the load to perform remote sense.
42	FBR		Remote buffer positive sense. Connect to the positive side of the multi-phase load to perform remote sense.
43	LTB		Load transient boost technology® input pin. See *Section 11.2* for details.
44	RGND		Remote ground sense. Connect to the negative side of the multi-phase load to perform remote sense.
45	REF		The reference used for the multi-phase section regulation is available on this pin with -125 mV offset. Connect through an R_{REF}-C_{REF} to GND to optimize DVID transitions. Connect through R_{OS} resistor to FB pin to implement small positive offset to the regulation.
46	IMON		Current monitor output. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{MON} to GND. The information available on this pin is used for the current reporting and DPM. The pin can be filtered through C_{IMON} to GND.

Table 2. Pin description (continued)

Pin#	Name		Function
47	SVR_RDY	Single-phase section	VR ready. Open drain output set free after SS has finished in single-phase section and pulled low when triggering any protection for the single-phase section.Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
48	ENDRV	Multi-phase section	Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the HiZ window on the PWMx pins to optimize the multi-phase section overall efficiency. Connect directly to external driver enable pin.
PAD	GND		GND connection. All internal references and logic are referenced to this pin. Filter to VCC with proper MLCC capacitor and connect to the PCB GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient (device soldered on 2s2p PC board)	40	°C/W
R_{thJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VDRV, GDC	to GND	-0.3 to 14	V
VCC5, TM, STM, SPWM, PWMx, SENDRV, ENDRV, SCOMP, COMP, SMDATA, SMAL#, SMCLK	to GND	-0.3 to 7	V
All other pins	to GND	-0.3 to 3.6	V

3.2 Electrical characteristics

V_{CC5} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{VCC5}	VCC5 supply current	EN = high		28		mA
		EN = low		22		mA
$UVLO_{VCC5}$	VCC5 turn-ON	VCC5 rising			4.1	V
	VCC5 turn-OFF	VCC5 falling	3			V
$UVLO_{VDRV}$	VDRV turn-ON	VDRV rising			6	V
	VDRV turn-OFF	VDRV falling	3		4.1	V
$UVLO_{VIN}$	VIN turn-ON	VIN rising, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ			6	V
	VIN turn-OFF	VIN falling, R_{UP} = 118.5 kΩ; R_{DOWN} = 10 kΩ	3		4.1	V
Oscillator, Soft-start and enable						
F_{SW}	Main oscillator accuracy	OSC = open	170	200	230	kHz
	Oscillator adjustability	R_{OSC} = 47 kΩ to GND	378	420	462	kHz
F_{SSW}	Main oscillator accuracy	SOSC = open	195	230	265	kHz
	Oscillator adjustability	R_{SOSC} = 47 kΩ to GND	432	480	528	kHz
ΔV_{OSC}	PWM ramp amplitude(1)			1.5		V
FAULT	Voltage at pin OSC, SSOSC	Latch active for related section	3			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SOFT-START	SS time	Vboot > 0, from pin-strapping; multi-phase section	2.5			mV/µS
		Vboot > 0, from pin-strapping; single-phase section	1.25			mV/µS
		Vboot > 0, from pin-strapping; single-phase section, JMode ON	2.5			mV/µS
EN	Turn-ON	V_{EN} rising			0.6	V
	Turn-OFF	V_{EN} falling	0.4			V
	Leakage current			1		µA
SVI serial bus						
SVCLCK, SVDATA	Input high		0.65			V
	Input low				0.45	V
SVDATA, ALERT#	Voltage low (ACK)	I_{SINK} = -5 mA			50	mV
PMBus						
SMDATA, SMCLK	Input high		1.75			V
	Input low				1.45	V
SMAL#	Voltage low	I_{SINK} = -4 mA			13	Ω
Reference and DAC						
K_{VID}	V_{OUT} accuracy (MPhase)	FBR to V_{CORE}; RGND to GND_{CORE} VID>1.000 V	-0.5		0.5	%
K_{SVID}	V_{OUT} accuracy (SPhase)	JMODE=OFF; V_{UNCORE}/V_{CORE} SFBR to V_{UNCORE}; SRGND to GND_{UNCORE}; VID>1.000 V	0.49		0.51	
		JMODE=ON; SFBR to V_{UNCORE}; SRGND to GND_{UNCORE};	-5		5	mV
Δ_{DROOP}	LL accuracy (MPhase) 0 to full load	I_{INFOx} = 0 µA; N=3; R_G=866 Ω	-2.25		1.75	µA
		I_{INFOx} = 20 µA; N=3; R_G=866 Ω	-2.5		2.5	µA
k_{IMON}	IMON accuracy (MPhase)	I_{INFOx} = 0; N=3; R_G=866 Ω	0		0.75	µA
		I_{INFOx} = 20 µA; N=3; R_G=866 Ω	-1		1	µA
A_0	EA DC gain(1)			100		dB
SR	Slew-rate(1)	COMP to SGND = 10 pF		20		V/µs
DVID	Slew-rate fast	Multi-phase section	10			mV/µs
	Slew-rate slow		2.5			mV/µs
DVID	Slew-rate fast	Single-phase section	5			mV/µs
	Slew-rate slow		1.25			mV/µs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IMON ADC	GetReg(15h)	V(IMON) = 0.992 V		CC		Hex
	Accuracy		C0		CF	Hex
PWM outputs and ENDRV						
PWMx, SPWM	Output high	I = 1 mA		5		V
	Output low	I = -1 mA			0.2	V
I_{PWM1}	Test current	Sourced from pin, EN=0		10		µA
I_{PWM2}		Sourced from pin, EN=0		0		µA
$I_{PWM3, SPWM}$		Sourced from pin, EN=0		-10		µA
ENDRV	Voltage low	I_{ENDRV} = -4 mA			0.4	V
Protection (both sections)						
OVP	Overvoltage protection	VSEN rising; wrt Ref.	100		200	mV
UVP	Undervoltage protection	VSEN falling; wrt Ref; Ref > 500 mV	-525		-375	mV
FBR DISC	FB disconnection	V_{CS-} rising, above VSEN/SVSEN	650	700	750	mV
FBG DISC	FBG disconnection	FBR rising wrt VID	950	1000	1050	mV
VR_RDY, SVR_RDY	Voltage low	I_{SINK} = -4 mA			0.4	V
V_{OC_TOT}	OC threshold	V_{ILIM} rising, to GND	2.45	2.5	2.55	V
I_{OC_TH}	Constant current(1)	MPhase only		35		µA
VR_HOT	Voltage low	I_{SINK} = -4 mA			13	Ω
Gate drive control						
GDC	Max. current(1)	Any PS		200		mA
	Impedance	PS00h (GDC = VDRV)		6		Ω
		> PS00h (GDC = VCC5)		6		Ω

1. Guaranteed by design, not subject to test.

4 Device configuration and pin-strapping tables

The L6759D is fully compliant with Intel® VR12/IMVP7 SVID protocol Rev1.5, document # 456098. To guarantee proper device and CPU operations, refer to this document for bus design and layout guidelines. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing between SVDATA, SVCLK, and ALERT# must be followed.

4.1 JMode

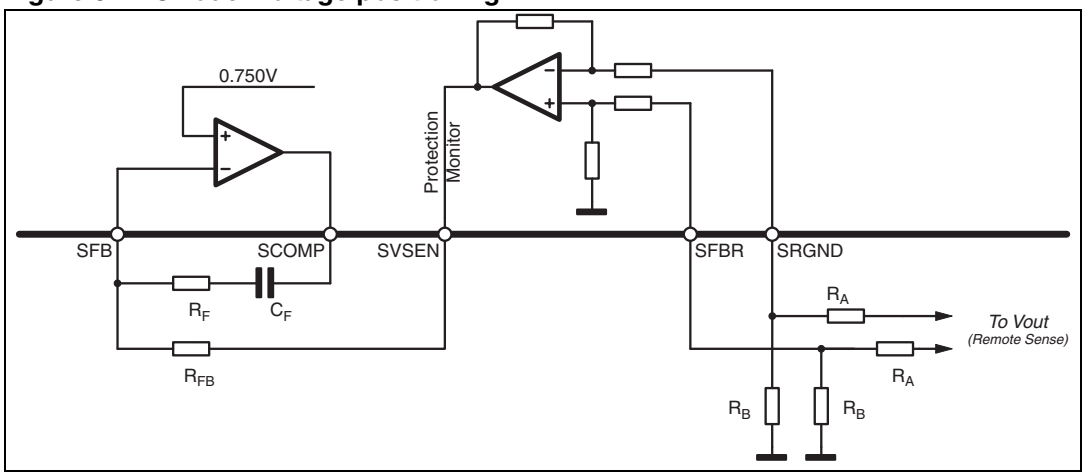
When enabled, single-phase is an independent regulator with 0.75 V fixed reference (load-line disabled - TM can be used as enable for the single-phase).

Output voltage higher than the internal reference may be achieved by adding a proper resistor divider (RA, RB - see *Figure 5*). To maintain precision in output voltage regulation, it is recommended to provide both SFBR and SRGND with the same divider.

Equation 1

$$V_{OUT} = 0.750V \cdot \frac{RA + RB}{RB}$$

Figure 5. JMode: voltage positioning



4.2 Programming HiZ level

The L6759D is able to manage different levels for HiZ on PWMx guaranteeing flexibility in driving different external drivers as well as DrMOS ICs.

Once VCC5, VDRV, and VIN voltages are above the respective UVLO (undervoltage lockout) thresholds (see *Figure 6*), the device uses PWM1 and PWM2 to detect the driver/DrMOS connected in order to program the suitable Hiz level of PWMx signals. During regulation, the Hiz level is used to force the external MOSFETs into high impedance state.

- PWM1 sources a constant 10 µA current, if its voltage results higher than 2.8 V, the HiZ level used during the regulation is 1.4 V, if lower, PWM2 information is used.
- PWM2 is kept in HiZ, if its voltage results higher than 2 V, the HiZ level used during the regulation is 2 V, if lower, 1.6 V.

An external resistor divider can be placed on PWM1 and PWM2 to force the detection of the correct HiZ level. They must be designed considering the external driver/DrMOS selected and the HiZ level requested.

Table 6. Pin-strapping (1)

Rdown [kΩ]	Rup [kΩ]	IMAX			ADDR				
		IMAX [A] (2)	JMode	VBOOT	SVI ADDR (3)	VFDE	DPM12	DPM23	Droop core
10	1.5	N · 25 + 56	ON	1.500 V	0100b	OFF	12 A	24 A	ON
10	2.7			1.350 V					OFF
22	6.8		OFF	1.500 V			10 A	20 A	ON
10	3.6			1.350 V					OFF
27	11	N · 25 + 48	ON	1.500 V			8 A	18 A	ON
12	5.6			1.350 V					OFF
82	43		OFF	1.500 V			OFF	OFF	ON
13	7.5			1.350 V					OFF
56	36	N · 25 + 40	ON	1.500 V		ON	12 A	24 A	ON
18	13			1.350 V					OFF
15	12		OFF	1.500 V			10 A	20 A	ON
18	16			1.350 V					OFF
15	14.7	N · 25 + 32	ON	1.500 V			8 A	18 A	ON
10	11			1.350 V					OFF
18	22		OFF	1.500 V			OFF	OFF	ON
56	75			1.350 V					OFF

Table 6. Pin-strapping (1) (continued)

Rdown [kΩ]	Rup [kΩ]	IMAX			ADDR				
		IMAX [A] (2)	JMode	VBOOT	SVI ADDR (3)	VFDE	DPM12	DPM23	Droop core
10	15	N · 25 + 24	ON	1.500 V	0010b	OFF	12 A	24 A	ON
12	20			1.350 V					OFF
12	22.6		OFF	1.500 V			10 A	20 A	ON
39	82			1.350 V					OFF
47	110	N · 25 + 16	ON	1.500 V			8 A	18 A	ON
10	27			1.350 V					OFF
22	68		OFF	1.500 V			OFF (4)	OFF (5)	ON
10	36			1.350 V					OFF
18	75	N · 25 + 8	ON	1.500 V		ON	12 A	24 A	ON
15	75			1.350 V					OFF
10	59		OFF	1.500 V			10 A	20 A	ON
10	75			1.350 V					OFF
10	100	N · 25	ON	1.500 V			8 A	18 A	ON
10	150			1.350 V					OFF
10	220		OFF	1.500 V			OFF (4)	OFF (5)	ON
10	Open			1.350 V					OFF

1. Suggested values, divider needs to be connected between VCC5 pin and GND.
2. N is the number of phase programmed for the multi-phase section.
3. Address for multi-phase. Single-phase not accessible.
4. Transition between 1Phase and 2Phase operation is set to 12 A but disabled in PS00h (minimum phase number in PS00h is 2).
5. Dynamic phase management disabled, IC always working at maximum possible number of phases except when in >PS00h when transitioning between 1Phase and 2Phase at 12 A.

Table 7. PMBus address definition

SVI address (see *Table 6*)	COMP to GND	PMBus address
0100b	4.99 k	EEh
	14.99 k	EAh
	24.99 k	E6h
	Open	E2h
0010b	4.99 k	ECh
	14.99 k	E8h
	24.99 k	E4h
	Open	E0h

5 Device description and operation

The L6759D is a programmable 2/3-phase PWM controller that provides complete control logic and protection to realize a high performance step-down DC-DC voltage regulator optimized for advanced DDR memory power supply. The device features 2nd generation LTB Technology™: through a load transient detector, it is able to turn on simultaneously all the phases. This allows the output voltage deviation to be minimized and, in turn, to minimize system costs by providing the fastest response to a load transition.

The L6759D implements current reading across the inductor in fully differential mode. A sense resistor in series to the inductor can be also considered to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

The controller supports VR12 specifications featuring 25 MHz SVI bus and all the required registers. The platform may program the defaults for these registers through dedicated pin-strapping.

A complete set of protection is available: overvoltage, undervoltage, overcurrent (per-phase and total) and feedback disconnection guarantee the load to be safe under all conditions.

Special power management features like DPM, VFDE and GDC modify the phase number, gate driving voltage and switching frequency to optimize the efficiency over the load range.

The L6759D is available in VFQFPN48 with a 6x6 mm body package.

5.1 Device initialization

Figure 6. Device initialization: default

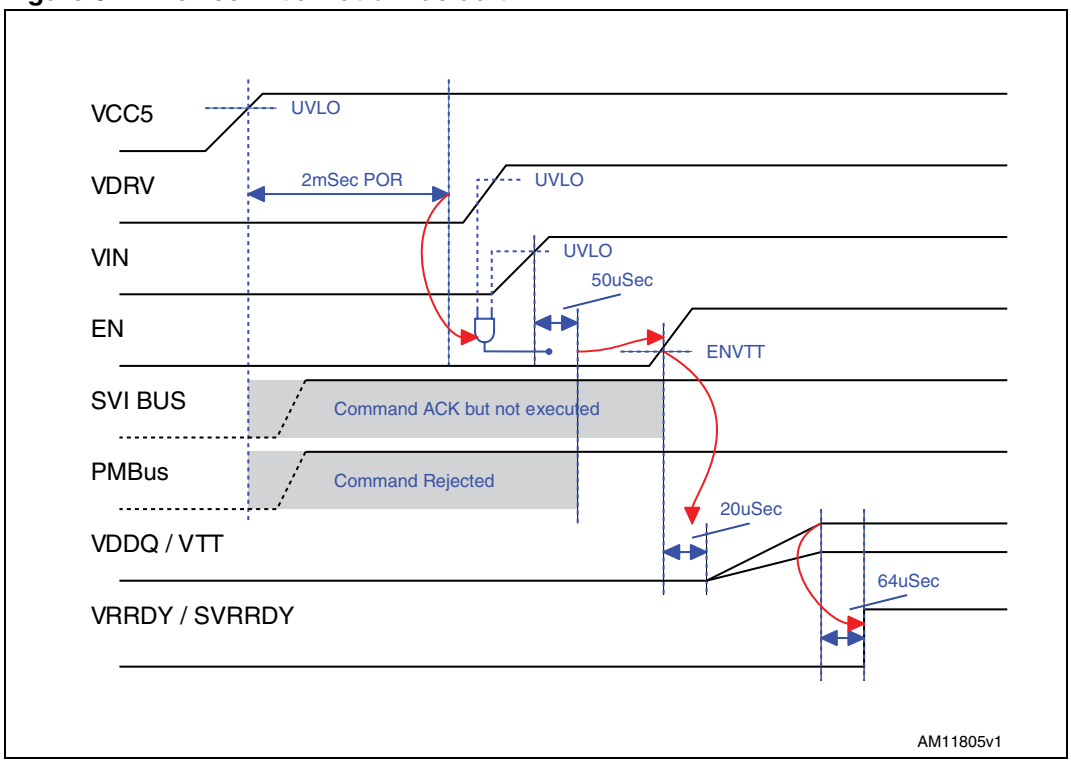
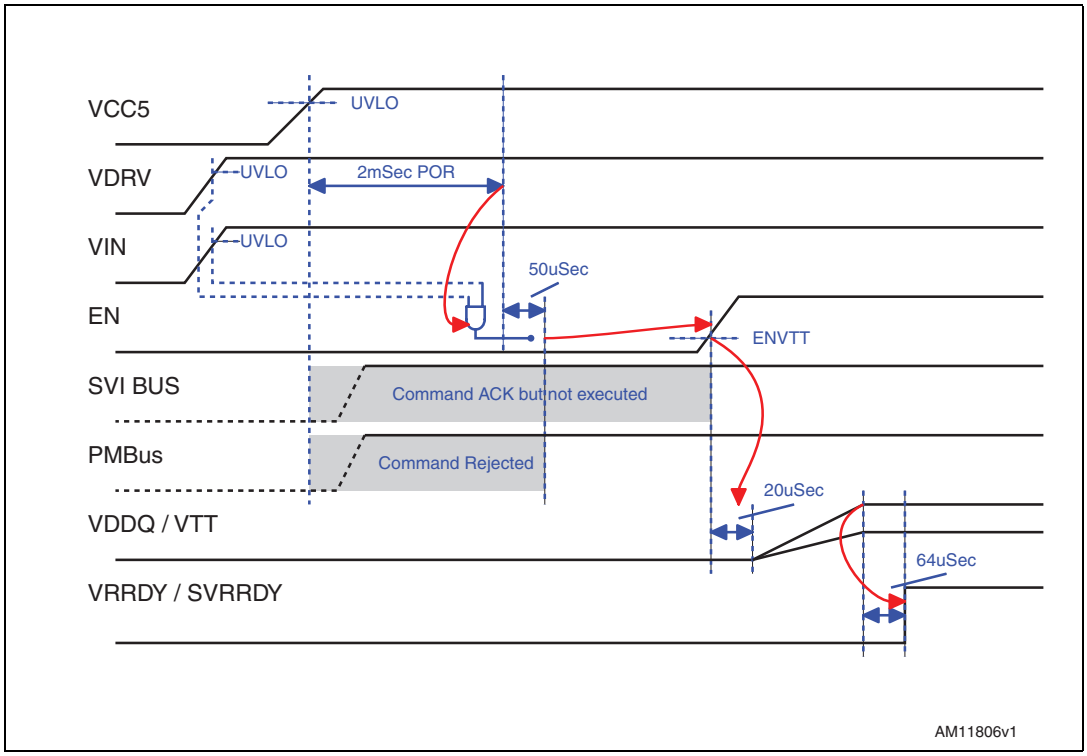


Figure 7. Device initialization: alternative sequence

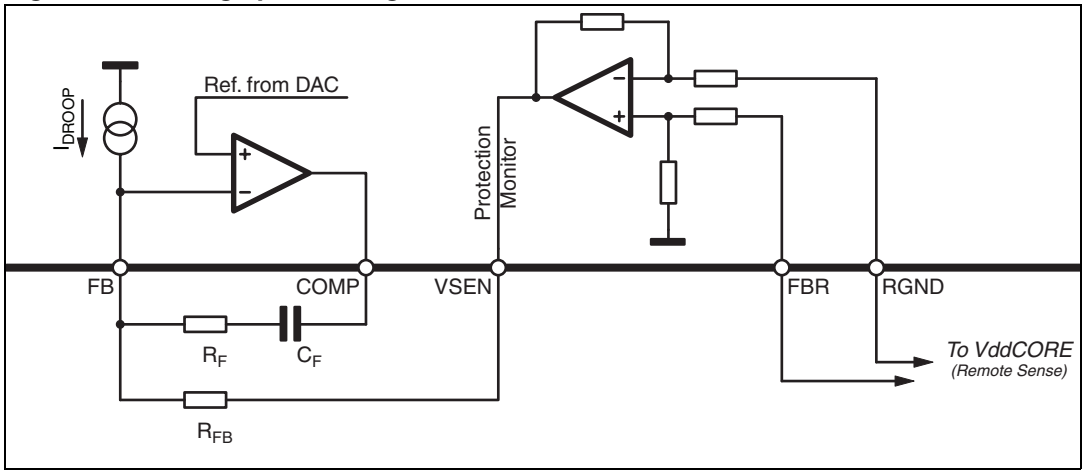


6 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode for the two sections and by programming the droop function effect (see *Figure 8*). The controller reads the current delivered by each section by monitoring the voltage drop across the DCR inductors. The current (I_{DROOP} / I_{SDROOP}) sourced from the FB / SFB pins, directly proportional to the read current, causes the related section output voltage to vary according to the external R_{FB} / R_{SFB} resistor, so implementing the desired load-line effect.

The L6759D embeds a dual remote-sense buffer to sense remotely the regulated voltage of each section without any additional external components. In this way, the output voltage programmed is regulated, compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 8. Voltage positioning



6.1 Multi-phase section - phase # programming

The multi-phase section implements a flexible 2 to 3 interleaved-phase converter. To program the desired number of phases, pull up with a 1 kΩ resistor to VCC5 the PWMx signal that is not required to be used.

Caution: For the disabled phase(s), the current reading pins need to be properly connected to avoid errors in current-sharing and voltage-positioning: CSxP needs to be connected to the regulated output voltage while CSxN needs to be connected to CSxP through the same R_G resistor used for the active phases. See *Figure 2* for details on 2-phase connections.

6.2 Multi-phase section - current reading and current sharing loop

The L6759D embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows the placing of the sensing element in different locations without affecting the measurement's accuracy. The

trans-conductance ratio is issued by the external resistor R_G placed outside the chip between the CSxN pin toward the reading points. The current sense circuit always tracks the current information, the CSxP pin is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current, an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (see *Figure 9*):

Equation 2

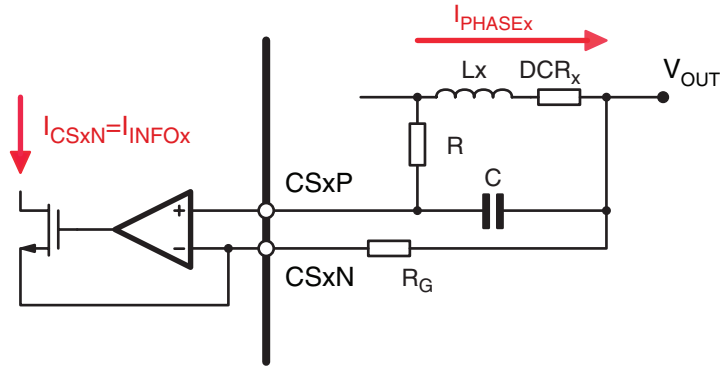
$$I_{CSxN} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering the matching of the time constant between the inductor and the R-C filter applied (time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance) it results:

Equation 3

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

Figure 9. Current reading



Inductor DCR Current Sense

The current read through the CSxP / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that, with a proper gain, is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

6.3 Multi-phase section - defining load-line

The L6759D introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 9 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R-C filter across the CSxP and CSxN pins. R_G programs a trans-conductance gain and generates a current I_{CSx} proportional to the current of the phase. The sum of the I_{CSx} current, with proper gain eventually adjusted by the PMBus commands, is then sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope (*Figure 8*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system, so voiding over and/or undershoot of the output voltage as a consequence of a load transient. The output voltage characteristic vs. load current is then given by:

Equation 4

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

where R_{LL} is the resulting load-line resistance implemented by the multi-phase section.

The R_{FB} resistor can be then designed according to the R_{LL} specifications as follows:

Equation 5

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

6.4 Multi-phase section - IMON information

The voltage on the IMON pin contains the analog information related to the current delivered by the VR and it is digitized for VR12 current reporting. The pin sources a copy of the droop current:

Equation 6

$$I_{IMON} = I_{DROOP} = \frac{DCR}{R_G} \cdot I_{OUT}$$

See *Section 6* for details about current reading.

The Iout register contains analog-to-digital conversion of the voltage present on the IMON pin considering the following relationships:

a) $V_{IMON} = I_{IMON} \cdot R_{IMON}$ where R_{IMON} is the resistor connected between IMON and GND.

b) V_{IMON}=1.24 V corresponds to IMAX. R_{IMON} is designed according to this relationship.

Note: Current reporting precision may be affected by external layout. The internal ADC is referenced to the device GND pin: in order to perform the highest accuracy in the current monitor, R_{IMON} must be routed to the GND pin with a dedicated net to avoid GND plane drops affecting the precision of the measurement.

6.5 Single-phase section - disable

The single-phase section can be disabled by pulling high the SPWM pin. The related command is rejected.

6.6 Single-phase section - current reading

The single-phase section performs the same differential current reading across DCR as the multi-phase section. According to *Section 6.2*, the current that flows from the SCSN pin is then given by the following equation (see *Figure 9*):

Equation 7

$$I_{SCSN} = \frac{DCR}{R_{SG}} \cdot I_{SOUT} = I_{SDROOP}$$

6.7 Single-phase section - defining load-line

This method introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 9 shows the current sense circuit used to implement the load-line. The current flowing across the inductor DCR is read through R_{SG}. R_{SG} programs a trans-conductance gain and generates a current I_{SDROOP} proportional to the current delivered by the single-phase section that is then sourced from the SFB pin with proper gain eventually adjusted by the PMBus commands. R_{SFB} gives the final gain to program the desired load-line slope (*Figure 8*).

The output characteristic vs. load current is then given by:

Equation 8

$$V_{SOUT} = VID - R_{SFB} \cdot I_{SDROOP} = = VID - R_{SFB} \cdot \frac{DCR}{R_{SG}} \cdot I_{SOUT} = VID - R_{SLL} \cdot I_{SOUT}$$

where R_{SLL} is the resulting load-line resistance implemented by the single-phase section.

The R_{SFB} resistor can be then designed according to R_{SLL} as follows:

Equation 9

$$R_{SFB} = R_{SLL} \cdot \frac{R_{SG}}{DCR}$$

6.8 Dynamic VID transition support

The L6759D manages dynamic VID transitions that allow the output voltage of both sections to modify during normal device operation for power management purposes. OV, UV, and per-phase OC signals are masked during every DVID transition and they are re-activated with proper delay to prevent false triggering. Total OC is active even during DVID.