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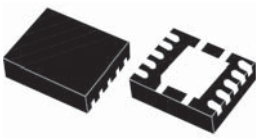
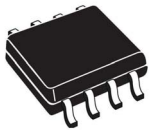
L7986

3 A step-down switching regulator

Datasheet - production data



VFQFPN10 3 x 3 mm



HSOP8 exp. pad

Features

- 3 A DC output current
- 4.5 V to 38 V input voltage
- Output voltage adjustable from 0.6 V
- 250 KHz switching frequency, programmable up to 1 MHz
- Internal soft-start and enable
- Low dropout operation: 100% duty cycle
- Voltage feed-forward
- Zero load current operation
- Overcurrent and thermal protection
- VFQFPN 3 x 3 - 10L and HSOP8 package

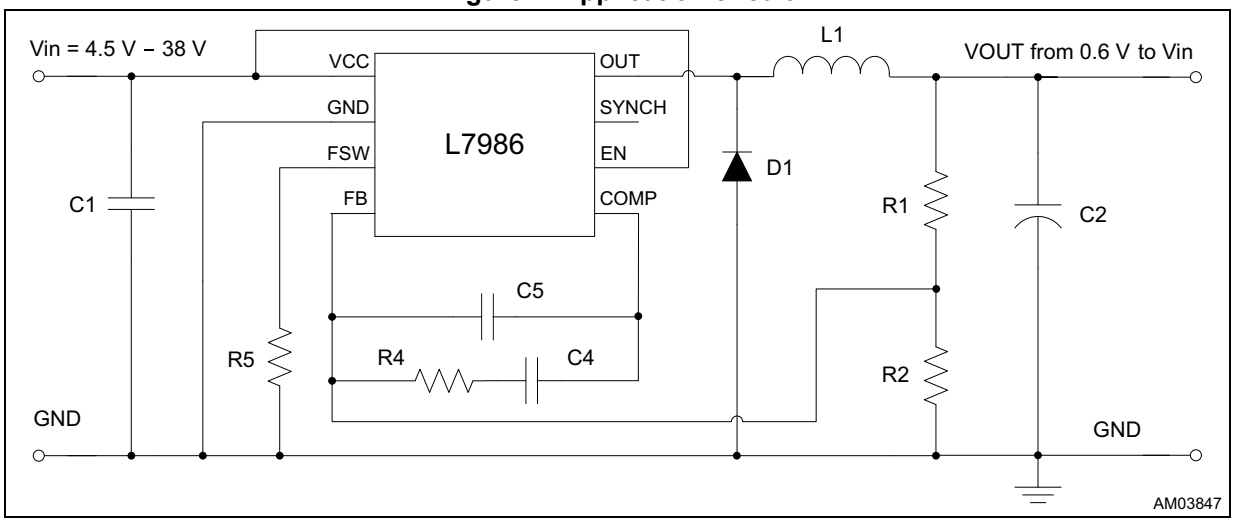
Applications

- Consumer: STB, DVD, DVD recorder, car audio, LCD TV and monitors
- Industrial: PLD, PLA, FPGA, chargers
- Networking: XDSL, modems, DC-DC modules
- Computer: optical storage, hard disk drive, printers, audio/graphic cards
- LED driving

Description

The L7986/A is a step-down switching regulator with a 3.7 A (minimum) current limited embedded power MOSFET, so it is able to deliver up to 3 A current to the load depending on the application conditions. The input voltage can range from 4.5 V to 38 V, while the output voltage can be set starting from 0.6 V to V_{IN}. Requiring a minimum set of external components, the device includes an internal 250 kHz switching frequency oscillator that can be externally adjusted up to 1 MHz. The QFN and the HSOP packages with exposed pad allow reducing the R_{thJA} down to 60 °C/W and 40 °C/W respectively.

Figure 1. Application circuit

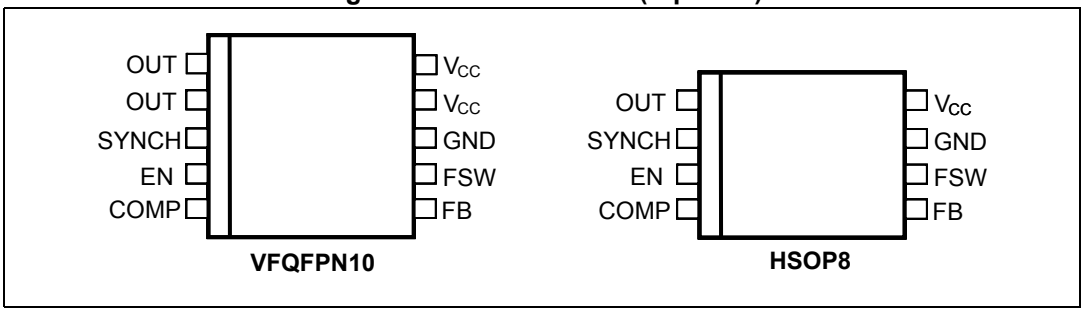


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No. (VFQFPN)	No. (HSOP)	Type	Description
1 - 2	1	OUT	Regulator output
3	2	SYNCH	Master/slave synchronization. When it is left floating, a signal with a phase shift of half a period, with respect to the power turn-on is present at the pin. When connected to an external signal at a frequency higher than the internal one, the device is synchronized by the external signal, with zero phase shift. Connecting together the SYNCH pin of two devices, the one with a higher frequency works as master and the other one as slave; so the two powers turn-ons have a phase shift of half a period.
4	3	EN	A logical signal (active high) enables the device. With EN higher than 1.2 V the device is ON and with EN lower than 0.3 V the device is OFF.
5	4	COMP	Error amplifier output to be used for loop frequency compensation.
6	5	FB	Feedback input. By connecting the output voltage directly to this pin the output voltage is regulated at 0.6 V. To have higher regulated voltages an external resistor divider is required from Vout to the FB pin.
7	6	F_{SW}	The switching frequency can be increased connecting an external resistor from the FSW pin and ground. If this pin is left floating, the device works at its free-running frequency of 250 KHz.
8	7	GND	Ground
9 - 10	8	V_{CC}	Unregulated DC input voltage.

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
Vcc	Input voltage		45	V
OUT	Output DC voltage		-0.3 to V_{CC}	
F_{SW}, COMP, SYNCH	Analog pin		-0.3 to 4	
EN	Enable pin		-0.3 to V_{CC}	
FB	Feedback voltage		-0.3 to 1.5	
P_{TOT}	Power dissipation at T_A < 60 °C	VFQFPN	1.5	W
		HSOP	2	
T_J	Junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient(1)	VFQFPN	60	°C/W
		HSOP	40	

1. Package mounted on demonstration board.

4 Electrical characteristics

T_J = 25 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating input voltage range	(1)	4.5		38	V
V_{CCON}	Turn-on V_{CC} threshold	(1)			4.5	
V_{CCHYS}	V_{CC} UVLO hysteseris	(1)	0.1		0.4	
R_{DSON}	MOSFET on resistance			200		mΩ
		(1)			400	
I_{LIM}	Maximum limiting current		3.7	4.2	4.7	A
Oscillator						
F_{SW}	Switching frequency	(1)	210	250	275	KHz
V_{FSW}	FSW pin voltage			1.254		V
D	Duty cycle		0		100	%
F_{ADJ}	Adjustable switching frequency	R_{FSW} = 33 kΩ		1000		KHz
Dynamic characteristics						
V_{FB}	Feedback voltage	4.5 V < V_{CC} < 38 V	0.593	0.6	0.607	V
		4.5 V < V_{CC} < 38 V(1)	0.582	0.6	0.618	
DC characteristics						
I_Q	Quiescent current	Duty cycle = 0, V_{FB} = 0.8 V			2.4	mA
I_{QST-BY}	Total standby quiescent current			20	30	µA
Enable						
V_{EN}	EN threshold voltage	Device OFF level			0.3	V
		Device ON level	1.2			
I_{EN}	EN current	EN = V_{CC}		7.5	10	µA
Soft start						
T_{SS}	Soft-start duration	FSW pin floating	7.4	8.2	9.1	ms
		F_{SW} = 1 MHz, R_{FSW} = 33 kΩ		2		
Error amplifier						
V_{CH}	High level output voltage	V_{FB} < 0.6 V	3			V
V_{CL}	Low level output voltage	V_{FB} > 0.6 V			0.1	
$I_{O\ SOURCE}$	Source COMP pin	V_{FB} = 0.5 V, V_{COMP} = 1 V		19		mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
$I_{O\ SINK}$	Sink COMP pin	V_{FB} = 0.7 V, V_{COMP} = 1 V		30		mA
G_V	Open-loop voltage gain	(2)		100		dB
Synchronization function						
$V_{S\_IN,HI}$	High input voltage		2		3.3	V
$V_{S\_IN,LO}$	Low input voltage				1	
$t_{S\_IN\_PW}$	Input pulse width	$V_{S\_IN,HI}$ = 3 V, $V_{S\_IN,LO}$ = 0 V	100			ns
		$V_{S\_IN,HI}$ = 2 V, $V_{S\_IN,LO}$ = 1 V	300			
$I_{SYNCH,LO}$	Slave sink current	V_{SYNCH} = 2.9 V		0.7	1	mA
$V_{S\_OUT,HI}$	Master output amplitude	I_{SOURCE} = 4.5 mA	2			V
$t_{S\_OUT\_PW}$	Output pulse width	SYNCH floating		110		ns
Protection						
T_{SHDN}	Thermal shutdown			150		°C
	Hystereris			30		

1. Specifications referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

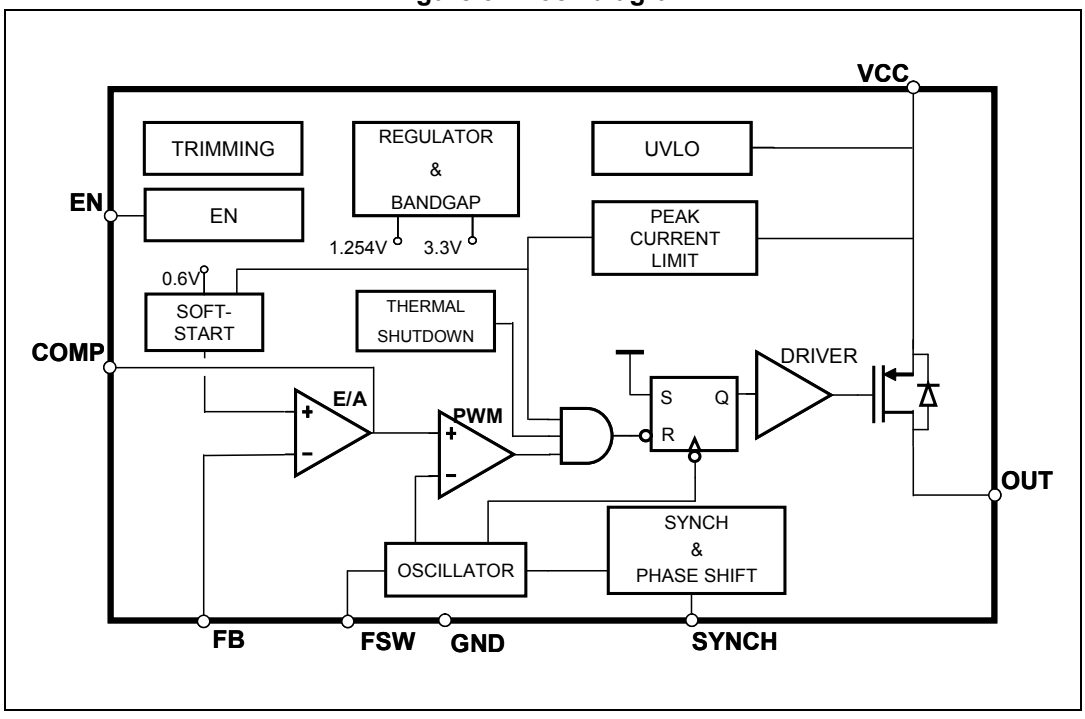
5 Functional description

The L7986 device is based on a “voltage mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.6 V) providing an error signal that, compared to a fixed frequency sawtooth, controls the on- and off-time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides sawtooth to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The voltage and frequency feed-forward are implemented.
- The soft-start circuitry to limit inrush current during the startup phase.
- The voltage mode error amplifier.
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch.
- The high-side driver for embedded P-channel power MOSFET switch.
- The peak current limit sensing block, to handle overload and short-circuit conditions.
- A voltage regulator and internal reference. To supply the internal circuitry and provide a fixed internal reference.
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- A thermal shutdown block, to prevent thermal runaway.

Figure 3. Block diagram



5.1 Oscillator and synchronization

Figure 4 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock. Its frequency depends on the resistor externally connected to the FSW pin. If the FSW pin is left floating, the frequency is 250 kHz; it can be increased as shown in *Figure 6* by an external resistor connected to ground.

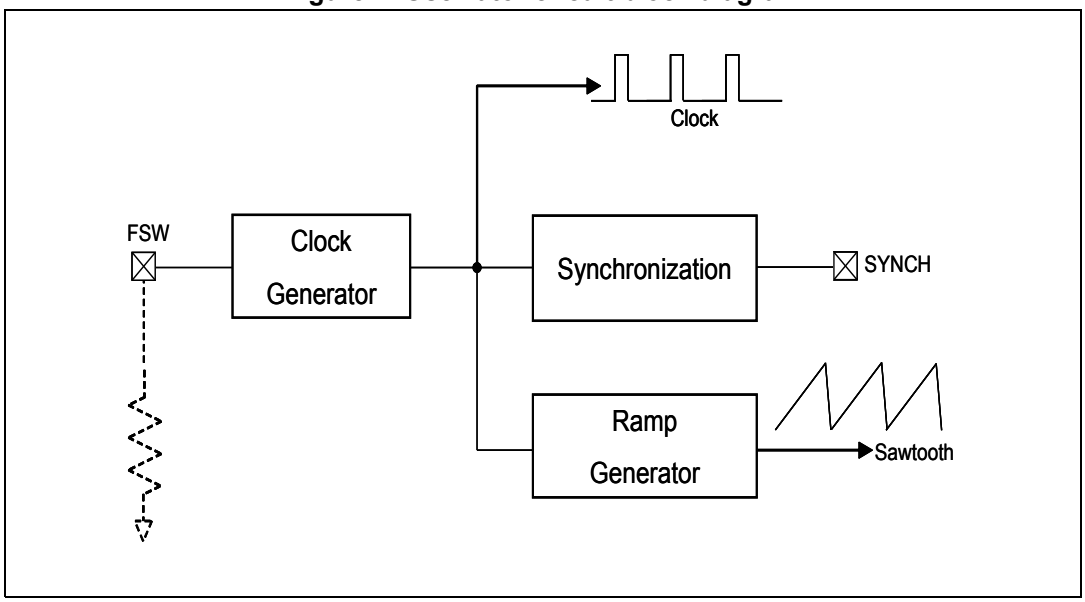
To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the voltage feed-forward is implemented by changing the slope of the sawtooth according to the input voltage change (see *Figure 5*.a).

The slope of the sawtooth also changes if the oscillator frequency is increased by the external resistor. In this way a frequency feed-forward is implemented (*Figure 5*.b) in order to keep the PWM gain constant versus the switching frequency (see *Section 6.4 on page 18* for PWM gain expression).

On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency typically works as a master, so the slave device switches at the frequency of the master but with a delay of half a period. This minimizes the RMS current flowing through the input capacitor (see the L5988D datasheet).

The SYNCH circuitry is also able to synchronize with a slightly lower external frequency, so the frequency pre-adjustment with the same resistor on the FSW pin, as described below, is suggested for a proper operation.

Figure 4. Oscillator circuit block diagram



The device can be synchronized to work at a higher frequency feeding an external clock signal. The synchronization changes the sawtooth amplitude, changing the PWM gain (*Figure 5*.c). This change must be taken into account when the loop stability is studied. To minimize the change of PWM gain, the free-running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency. This pre-adjusting of the frequency changes the sawtooth slope in order to render the truncation of sawtooth negligible, due to the external synchronization.

Figure 5. Sawtooth: voltage and frequency feed-forward; external synchronization

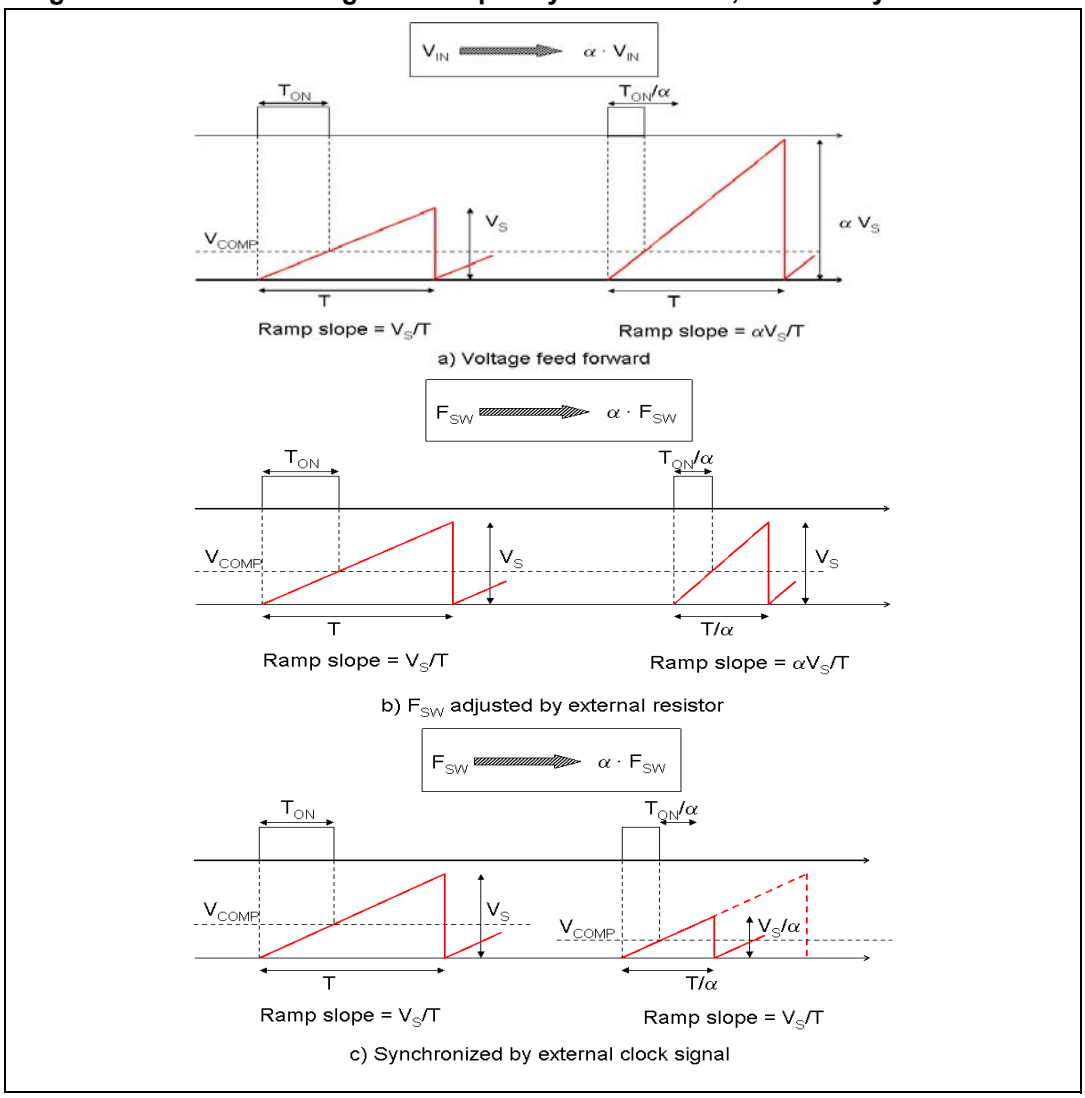
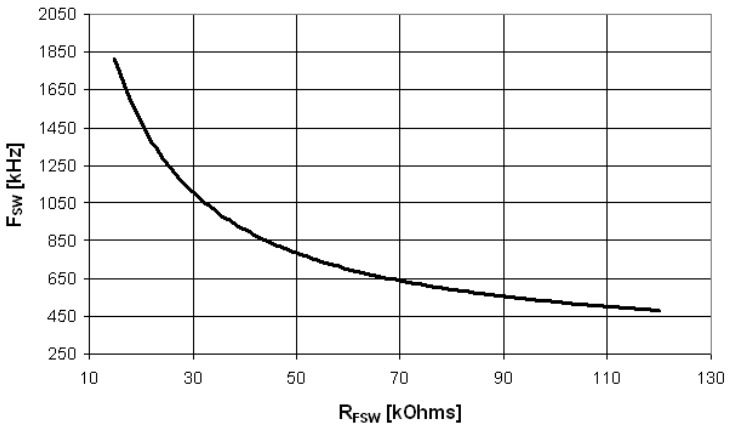


Figure 6. Oscillator frequency vs. FSW pin resistor



5.2 Soft-start

The soft-start is essential to assure correct and safe startup of the step-down converter. It avoids inrush current surge and makes the output voltage increase monothonically.

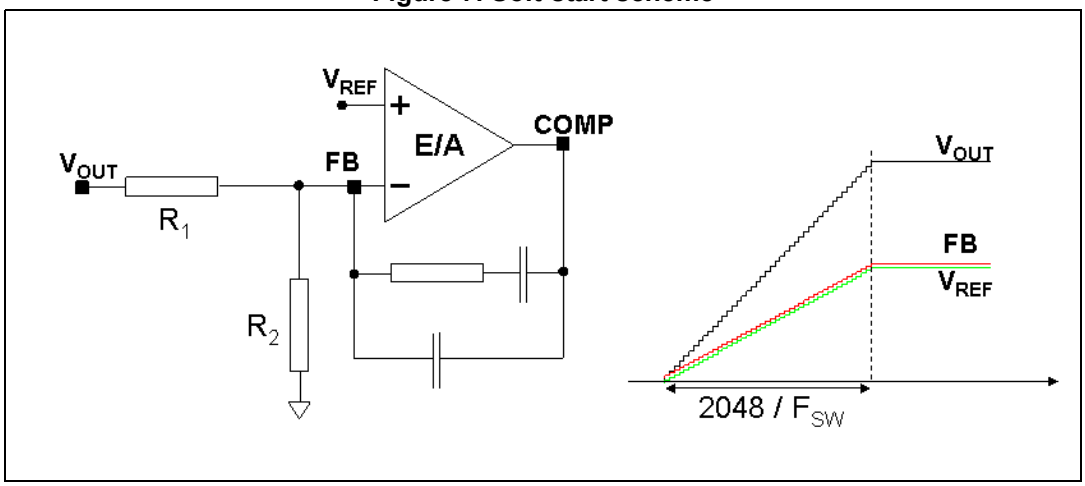
The soft-start is performed by a staircase ramp on the non inverting input (V_{REF}) of the error amplifier. So the output voltage slew rate is:

Equation 1

$$SR_{OUT} = SR_{VREF} \cdot \left(1 + \frac{R1}{R2}\right)$$

where SR_{VREF} is the slew rate of the non inverting input, while *R1*and *R2* is the resistor divider to regulate the output voltage (see *Figure 7*). The soft-start staircase consists of 64 steps of 9.5 mV each, from 0 V to 0.6 V. The time base of one step is of 32 clock cycles. So the soft-start time and then the output voltage slew rate depend on the switching frequency.

Figure 7. Soft-start scheme



Soft-start time results:

Equation 2

$$SS_{TIME} = \frac{32 \cdot 64}{Fsw}$$

For example, with a switching frequency of 250 kHz, the SS_{TIME} is 8 ms.

5.3 Error amplifier and compensation

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non inverting input is internally connected to a 0.6 V voltage reference, while its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier, therefore, with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are the following:

Table 5. Uncompensated error amplifier characteristics

Parameter	Value
Low frequency gain	100 dB
GBWP	4.5 MHz
Slew rate	7 V/µs
Output voltage swing	0 to 3.3 V
Maximum source/sink current	17 mA/25 mA

In continuous conduction mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor. If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see *Section 6.4 on page 18* for details of the compensation network selection).

Anyway, the methodology to compensate the loop is to introduce zeroes to obtain a safe phase margin.

5.4 Overcurrent protection

The L7986 device implements overcurrent protection by sensing current flowing through the power MOSFET. Due to the noise created by the switching activity of the power MOSFET, the current sensing is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 200 ns.

If the overcurrent limit is reached, the power MOSFET is turned off implementing pulse by pulse overcurrent protection. In the overcurrent condition, the device can skip turn-on pulses in order to keep the output current constant and equal to the current limit. If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the power MOSFET is turned off and one pulse is skipped. If, at the following switching on, when the “masking time” ends, the current is still higher than the overcurrent threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses. While, if at the end of the “masking time”, the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit (see *Figure 8*).

So, the overcurrent/short-circuit protection acts by switching off the power MOSFET and reducing the switching frequency down to one eighth of the default switching frequency, in order to keep constant the output current around the current limit.

This kind of overcurrent protection is effective if the output current is limited. To prevent the current from diverging, the current ripple in the inductor during the on-time must not be higher than the current ripple during the off-time. That is:

Equation 3

$$\frac{V_{IN} - V_{OUT} - R_{DSON} \cdot I_{OUT} - DCR \cdot I_{OUT}}{L \cdot F_{SW}} \cdot D = \frac{V_{OUT} + V_F + R_{DSON} \cdot I_{OUT} + DCR \cdot I_{OUT}}{L \cdot F_{SW}} \cdot (1-D)$$

If the output voltage is shorted, $V_{OUT} \cong 0$, $I_{OUT} = I_{LIM}$, $D / F_{SW} = T_{ON\_MIN}$, $(1 - D) / F_{SW} \cong 1 / F_{SW}$. So, from *Equation 3*, the maximum switching frequency that guarantees to limit the current results:

Equation 4

$$F_{SW}^{*} = \frac{(V_F + DCR \cdot I_{LIM})}{(V_{IN} - (R_{DSON} + DCR) \cdot I_{LIM})} \cdot \frac{1}{T_{ON\_MIN}}$$

With R_{DSON} = 300 mΩ, DCR = 0.08 Ω, the worst condition is with V_{IN} = 38 V, I_{LIM} = 3.7 A; the maximum frequency to keep the output current limited during the short-circuit results 88 kHz.

The pulse-by-pulse mechanism, which reduces the switching frequency down to one eighth the maximum F_{SW}, adjusted by the FSW pin, that assures a full effective output current limitation, is 88 kHz * 8 = 706 kHz.

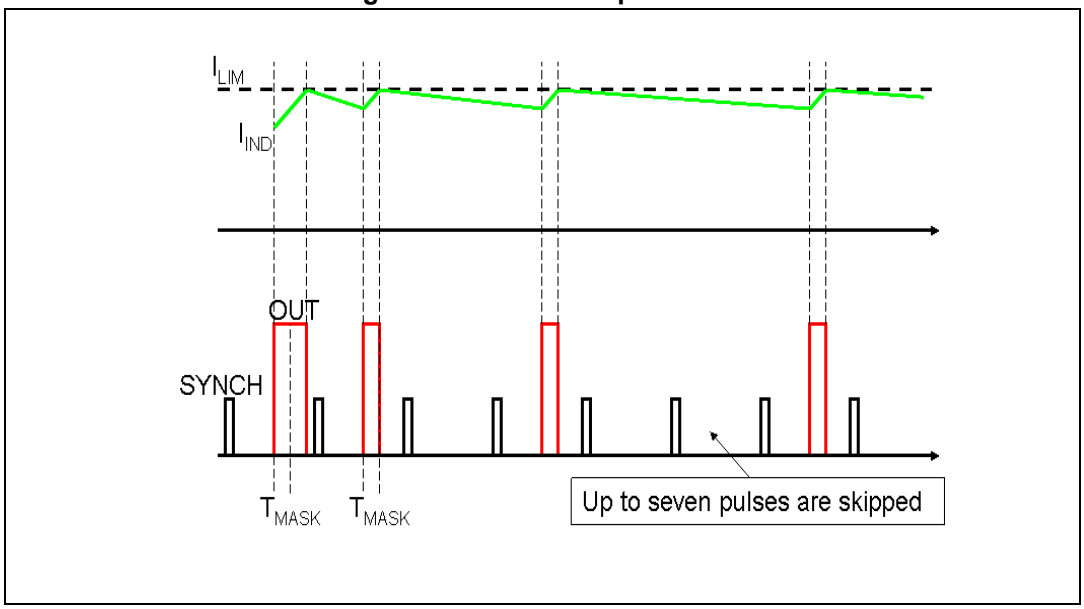
If, with V_{IN} = 38 V, the switching frequency is set higher than 706 kHz, during short-circuit condition the system finds a different equilibrium with higher current. For example, with F_{SW} = 800 kHz and the output shorted to ground, the output current is limited around:

Equation 5

$$I_{OUT} = \frac{V_{IN} \cdot F_{SW}^{*} - V_F / T_{ON\_MIN}}{(DCR / T_{ON\_MIN}) + (R_{DSON} + DCR) \cdot F_{SW}^{*}} = 4.2A$$

where F_{SW}^{*} is 800 kHz divided by eight.

Figure 8. Overcurrent protection



5.5 Enable function

The enable feature allows to put the device into standby mode. With the EN pin lower than 0.3 V the device is disabled and the power consumption is reduced to less than 30 µA. With the EN pin lower than 1.2 V, the device is enabled. If the EN pin is left floating, an internal pull-down ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{CC} compatible.

5.6 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature returns to about 120 °C, the device restarts in normal operation. The sensing element is very close to the PDMOS area, so ensuring an accurate and fast temperature detection.

6 Application information

6.1 Input capacitor selection

The capacitor connected to the input must be capable of supporting the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So, the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 6

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where I_O is the maximum DC output current, D is the duty cycle, η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and it is equal to $I_O/2$.

In a specific application, the range of possible duty cycles must be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 7

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 8

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F is the forward voltage on the freewheeling diode and V_{SW} is the voltage drop across the internal PDMOS.

The peak-to-peak voltage across the input capacitor can be calculated as:

Equation 9

$$V_{PP} = \frac{I_O}{C_{IN} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

where *ESR* is the equivalent series resistance of the capacitor.

Given the physical dimension, ceramic capacitors can well meet the requirements of the input filter sustaining a higher input RMS current than electrolytic/tantalum types.

In this case the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

Equation 10

$$C_{IN} = \frac{I_O}{V_{PP} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

neglecting the small ESR of ceramic capacitors.

Considering $\eta = 1$, this function has its maximum in D = 0.5, therefore, given the maximum peak-to-peak input voltage (V_{PP_MAX}), the minimum input capacitor (C_{IN_MIN}) value is:

Equation 11

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot F_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-to-peak voltage in the order of 1% of V_{INMAX}.

In *Table 6* some multi-layer ceramic capacitors suitable for this device are reported.

Table 6. Input MLCC capacitors

Manufacture	Series	Cap value (µF)	Rated voltage (V)
Taiyo Yuden	UMK325BJ106MM-T	10	50
	GMK325BJ106MN-T	10	35
Murata	GRM32ER71H475K	4.7	50

A ceramic bypass capacitor, as close to the VCC and GND pins as possible, so that additional parasitic ESR and ESL are minimized, is suggested in order to prevent instability on the output voltage due to noise. The value of the bypass capacitor can go from 100 nF to 1 µF.

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value, in order to have the expected current ripple, must be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current.

In the continuous current mode (CCM), the inductance value can be calculated by the following equation:

Equation 12

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT} + V_F}{L} \cdot T_{OFF}$$

where T_{ON} is the conduction time of the internal high-side switch and T_{OFF} is the conduction time of the external diode [in CCM, $F_{SW} = 1 / (T_{ON} + T_{OFF})$]. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} which is at minimum duty cycle (see *Section 6.1* to calculate minimum duty). So, by fixing ΔI_L = 20% to 30% of the maximum output current, the minimum inductance value can be calculated:

Equation 13

$$L_{MIN} = \frac{V_{OUT} + V_F}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency, 1 / (T_{ON} + T_{OFF}).

For example, for V_{OUT} = 5 V, V_{IN} = 24 V, I_O = 3 A and F_{SW} = 250 kHz, the minimum inductance value to have ΔI_L = 30% of I_O is about 18 µH.

The peak current through the inductor is given by:

Equation 14

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So, if the inductor value decreases, then the peak current (that must be lower than the minimum current limit of the device) increases. According to the maximum DC output current for this product family (3 A), the higher the inductor value, the higher the average output current that can be delivered, without triggering the overcurrent protection.

In *Table 7* some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	MSS1038	3.8 to 10	3.9 to 6.5
	MSS1048	12 to 22	3.84 to 5.34
Wurth	PD type L	8.2 to 15	3.75 to 6.25
	PD type M	2.2 to 4.7	4 to 6
SUMIDA	CDRH6D226/HP	1.5 to 3.3	3.6 to 5.2
	CDR10D48MN	6.6 to 12	4.1 to 5.7

6.3 Output capacitor selection

The current in the capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 15

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi-layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and the zero due to its ESR. *Section 6.4* illustrates how to consider its effect in the system stability.

For example, with V_{OUT} = 5 V, V_{IN} = 24 V, ΔI_L = 0.9 A (resulting from the inductor value), in order to have a $\Delta V_{OUT} = 0.01 \cdot V_{OUT}$, if the multi-layer ceramic capacitors are adopted, 10 µF are needed and the ESR effect on the output voltage ripple can be neglected. In the case of non-negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value. So, in case of 330 µF with ESR = 30 mΩ, the resistive component of the drop dominates and the voltage ripple is 28 mV.

The output capacitor is also important to sustain the output voltage when a load transient with high slew rate is required by the load. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. So, if the high slew rate load transient is required by the application, the output capacitor and system bandwidth must be chosen in order to sustain the load transient.

In *Table 8* some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

6.4 Compensation network

The compensation network must assure stability and good dynamic performance. The loop of the L7986 is based on the voltage mode control. The error amplifier is a voltage operational amplifier with high bandwidth. So, by selecting the compensation network the E/A is considered as ideal, that is, its bandwidth is much larger than the system one.

The transfer functions of the PWM modulator and the output LC filter are studied (see *Figure 10*). The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the OUT pin, results:

Equation 16

$$G_{PW0} = \frac{V_{IN}}{V_s}$$

where V_S is the sawtooth amplitude. As seen in *Section 5.1 on page 9*, the voltage feed-forward generates a sawtooth amplitude directly proportional to the input voltage, that is:

Equation 17

$$V_S = K \cdot V_{IN}$$

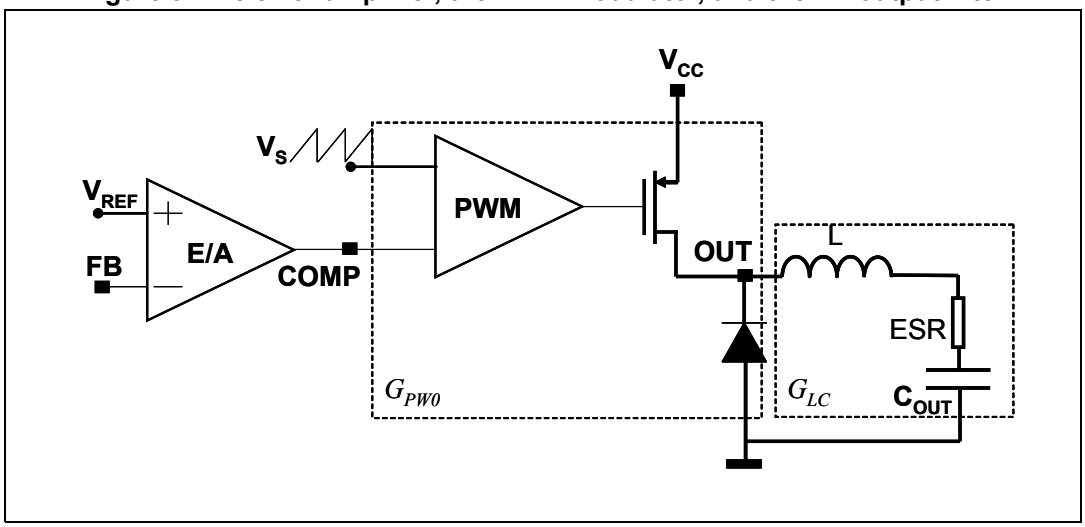
In this way the PWM modulator gain results constant and equal to:

Equation 18

$$G_{PW0} = \frac{V_{IN}}{V_s} = \frac{1}{K} = 18$$

The synchronization of the device with an external clock provided through the SYNCH pin can modify the PWM modulator gain (see *Section 5.1 on page 9* to understand how this gain changes and how to keep it constant in spite of the external synchronization).

Figure 9. The error amplifier, the PWM modulator, and the LC output filter



The transfer function on the LC filter is given by:

Equation 19

$$G_{LC}(s) = \frac{1 + \frac{s}{2\pi \cdot f_{zESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2}$$

where:

Equation 20

$$f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}} \cdot \sqrt{1 + \frac{ESR}{R_{OUT}}}}, \qquad f_{zESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

Equation 21

$$Q = \frac{\sqrt{R_{OUT} \cdot L \cdot C_{OUT} \cdot (R_{OUT} + ESR)}}{L + C_{OUT} \cdot R_{OUT} \cdot ESR}, \qquad R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

As seen in *Section 5.3 on page 12*, two different kinds of network can compensate the loop. In the following two paragraphs the guidelines to select the type II and type III compensation network are illustrated.

6.4.1 Type III compensation network

The methodology to stabilize the loop consists of placing two zeroes to compensate the effect of the LC double pole, therefore increasing phase margin; then, to place one pole in the origin to minimize the DC error on regulated output voltage; and finally, to place other poles far from the zero dB frequency.

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency higher than the desired bandwidth (that is: $2\pi * ESR * C_{OUT} < 1 / BW$), the type III compensation network is needed. Multi-layer ceramic capacitors (MLCC) have very low ESR (< 1 mΩ), with very high frequency zero, so a type III network is adopted to compensate the loop.

In *Figure 10* the type III compensation network is shown. This network introduces two zeroes (f_{Z1}, f_{Z2}) and three poles (f_{P0}, f_{P1}, f_{P2}). They are expressed as:

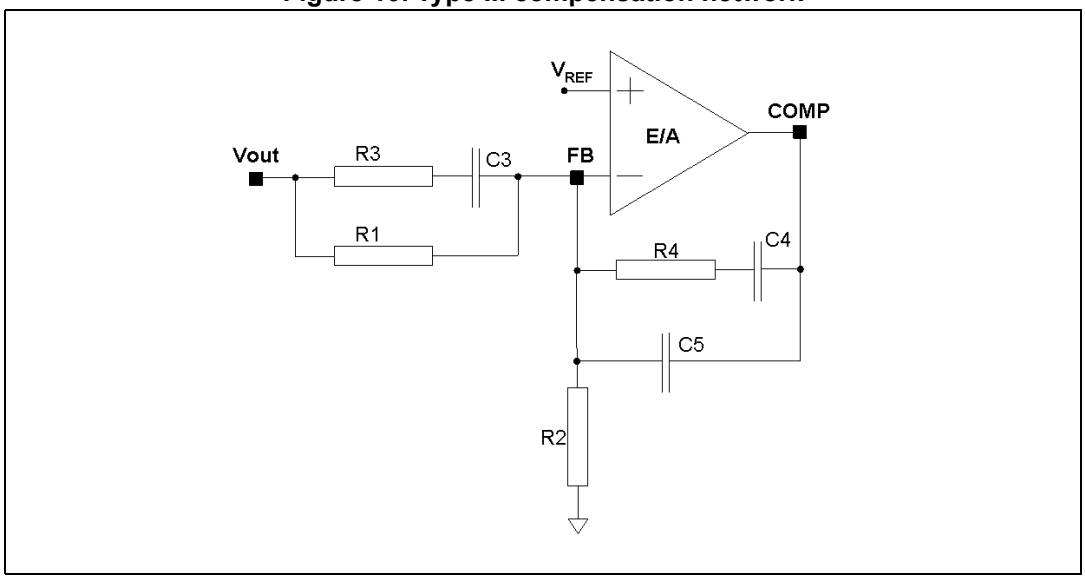
Equation 22

$$f_{Z1} = \frac{1}{2\pi \cdot C_3 \cdot (R_1 + R_3)}, \quad f_{Z2} = \frac{1}{2\pi \cdot R_4 \cdot C_4}$$

Equation 23

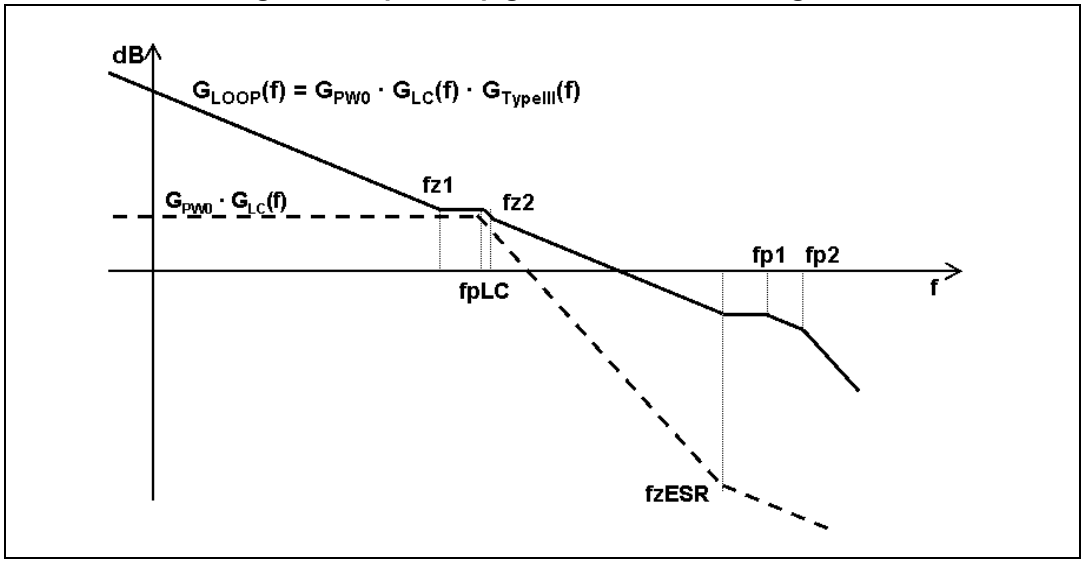
$$f_{P0} = 0, \quad f_{P1} = \frac{1}{2\pi \cdot R_3 \cdot C_3}, \quad f_{P2} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

Figure 10. Type III compensation network



In *Figure 11* the Bode diagram of the PWM and LC filter transfer function [$G_{PW0} \cdot G_{LC}(f)$] and the open-loop gain [$G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEIII}(f)$] are drawn.

Figure 11. Open-loop gain: module Bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follows:

1. Choose a value for R_1, usually between 1 kΩ and 5 kΩ.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 24

$$R_4 = \frac{BW}{f_{LC}} \cdot K \cdot R_1$$

where *K* is the feed-forward constant and 1/K is equal to 18.

3. Calculate C_4 by placing the zero at 50% of the output filter double pole frequency (f_{LC}):

Equation 25

$$C_4 = \frac{1}{\pi \cdot R_4 \cdot f_{LC}}$$

4. Calculate C_5 by placing the second pole at four times the system bandwidth (BW):

Equation 26

$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$

5. Set also the first pole at four times the system bandwidth and also the second zero at the output filter double pole:

Equation 27

$$R_3 = \frac{R_1}{\frac{4 \cdot BW}{f_{LC}} - 1}, \qquad C_3 = \frac{1}{2\pi \cdot R_3 \cdot 4 \cdot BW}$$

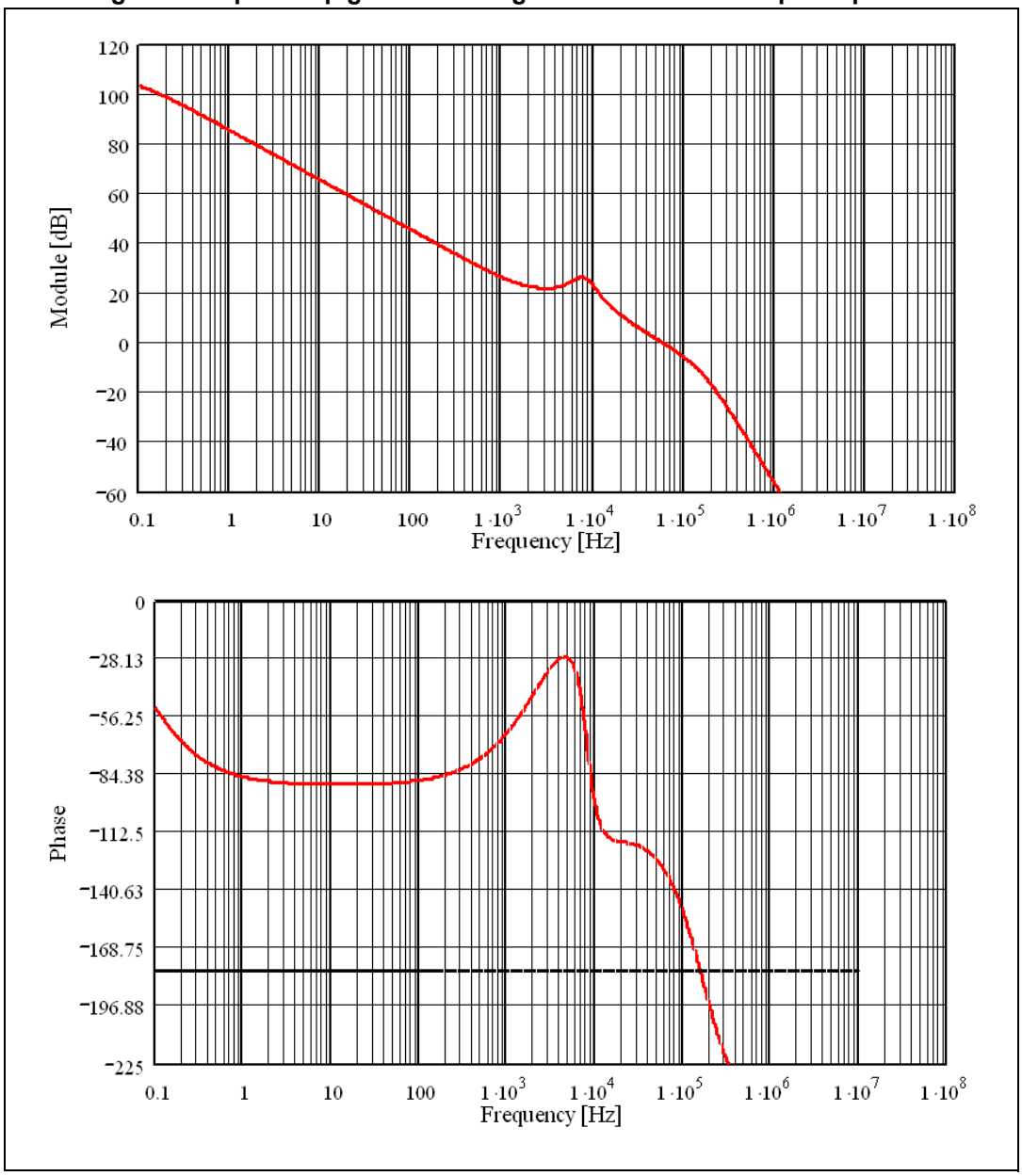
The suggested maximum system bandwidth is equal to the switching frequency divided by 3.5 (F_{SW} / 3.5), anyway, lower than 100 kHz if the F_{SW} is set higher than 500 kHz.

For example, with V_{OUT} = 5 V, V_{IN} = 24 V, I_O = 3 A, L = 18 µH, C_{OUT} = 22 µF, ESR < 1 mΩ, the type III compensation network is:

$R_1 = 4.99k\Omega$, $R_2 = 680\Omega$, $R_3 = 200\Omega$, $R_4 = 2k\Omega$, $C_3 = 3.3nF$, $C_4 = 22nF$, $C_5 = 220pF$

In *Figure 12* the module and phase of the open-loop gain is shown. The bandwidth is about 58 kHz and the phase margin is 50°.

Figure 12. Open-loop gain Bode diagram with ceramic output capacitor

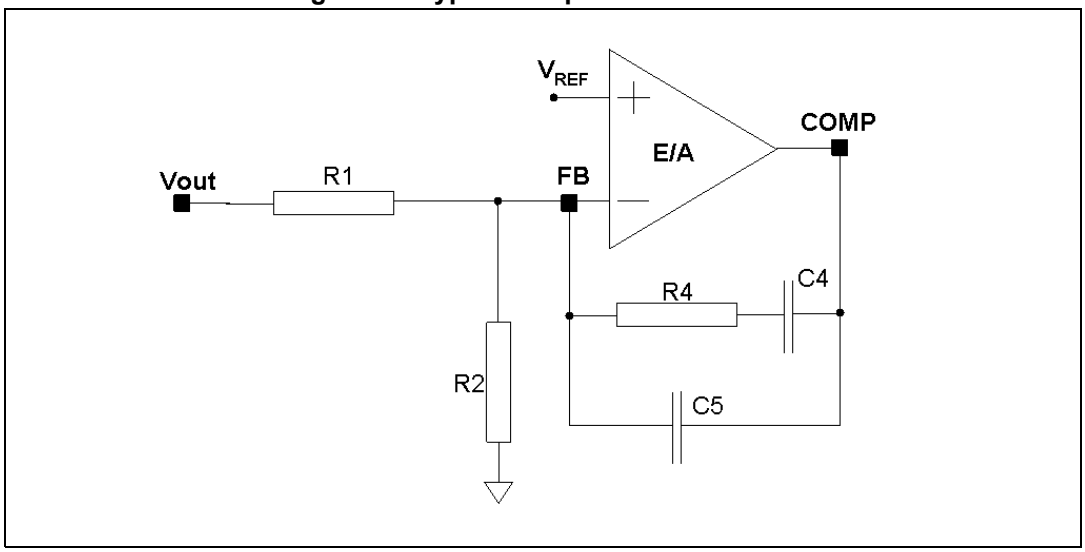


6.4.2 Type II compensation network

If the equivalent series resistance (ESR) of the output capacitor introduces a zero with a frequency lower than the desired bandwidth (that is: $2\pi * ESR * C_{OUT} > 1 / BW$), this zero helps stabilize the loop. Electrolytic capacitors show non-negligible ESR (> 30 mΩ), so with this kind of output capacitor the type II network combined with the zero of the ESR allows to stabilize the loop.

In *Figure 13* the type II network is shown.

Figure 13. Type II compensation network



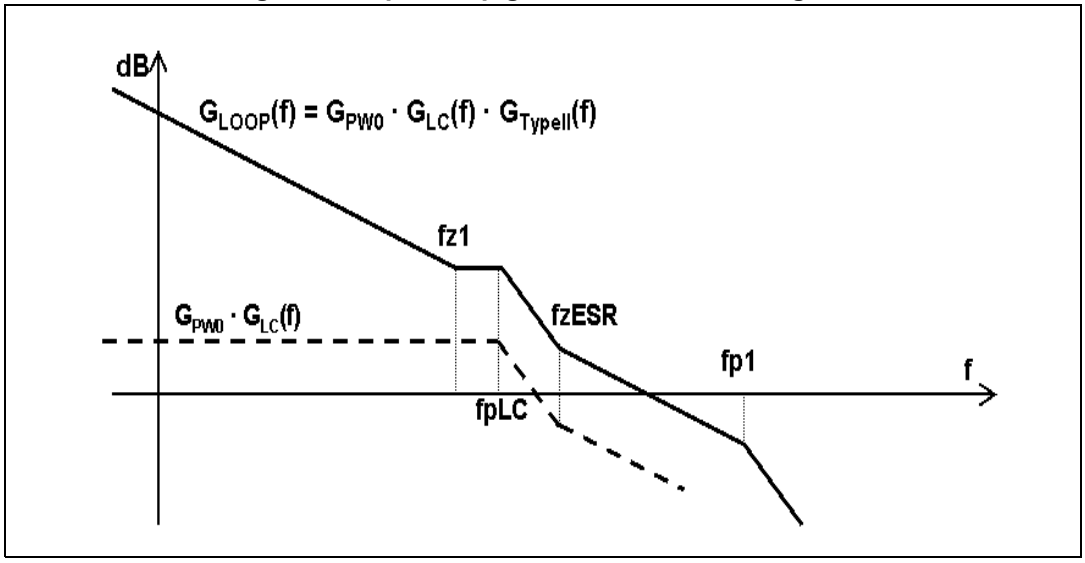
The singularities of the network are:

Equation 28

$$f_{Z1} = \frac{1}{2\pi \cdot R_4 \cdot C_4}, \quad f_{P0} = 0, \quad f_{P1} = \frac{1}{2\pi \cdot R_4 \cdot \frac{C_4 \cdot C_5}{C_4 + C_5}}$$

In *Figure 14* the Bode diagram of the PWM and LC filter transfer function [$G_{PW0} \cdot G_{LC}(f)$] and the open-loop gain [$G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEII}(f)$] are drawn.

Figure 14. Open-loop gain: module Bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follows:

1. Choose a value for R_1, usually between 1 kΩ and 5 kΩ, in order to have values of C4 and C5 not comparable with parasitic capacitance of the board.
2. Choose a gain (R_4/R_1) in order to have the required bandwidth (BW), that means:

Equation 29

$$R_4 = \left(\frac{f_{ESR}}{f_{LC}}\right)^2 \cdot \frac{BW}{f_{ESR}} \cdot \frac{V_S}{V_{IN}} \cdot R_1$$

where f_{ESR} is the ESR zero:

Equation 30

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

and V_S is the sawtooth amplitude. The voltage feed-forward keeps the ratio V_S/V_{IN} constant.

3. Calculate C_4 by placing the zero one decade below the output filter double pole:

Equation 31

$$C_4 = \frac{10}{2\pi \cdot R_4 \cdot f_{LC}}$$

4. Then calculate C_3 in order to place the second pole at four times the system bandwidth (BW):

Equation 32

$$C_5 = \frac{C_4}{2\pi \cdot R_4 \cdot C_4 \cdot 4 \cdot BW - 1}$$