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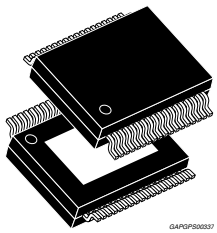
# L9301

# Automotive octal low side driver or quad low side plus quad high side driver

**Datasheet - production data**



**PowerSSO36**

## Features

- AEC-Q100 qualified
- Eight integrated PowerMOS configurable as:
  - 8 low side ON-OFF with $R_{ON(max)}$ = 0.3 Ω @ $T_j$ = 175 °C
  - High/low side PWM with $R_{ON(max)}$ = 0.6 Ω @ $T_j$ = 175 °C and 4 Low side with $R_{ON(max)}$ = 0.3 Ω @ $T_j$ = 175 °C
- Operating battery supply voltage 5 V to 18 V
- Operating $V_{dd}$ supply voltage 4.75 V to 5.25 V
- Logic inputs TTL/CMOS-compatible
- Output voltage clamping 37 V typ. in low-side configuration
- SPI interface for outputs control and for diagnosis data communication
- Additional PWM inputs for 8 outputs
- Over temperature protection
- Open load, short to GND, short to VB
- Overcurrent diagnostics in latched or unlatched mode for each channel
- Controlled SR for improved EMC behavior

## Description

The L9301 is a SPI (Serial Peripheral Interface) controlled octal channel with 4 high/low and 4 low side drivers with the possibility to use four integrated PowerMOS as recirculation diodes for PWM load driving.

L9301 contains 12 PowerMOS: 4 configurable High/Low side drivers with $R_{onmax}$ = 0.6 Ω (DRN1-4, SRC1-4), 4 low side drivers with $R_{onmax}$ = 0.6 Ω (OUT1-4) and 4 low side drivers with $R_{onmax}$ = 0.3 Ω (OUT5-8).

The power DRN/SRC1-4 and OUT1-4 can be connected in parallel outside the device in order to get 4 low-side drivers with $R_{onmax}$ = 0.3 Ω: DRN1//DRN2, DRN3//DRN4, OUT1//OUT2, OUT3//OUT4.

In this way there is a total of 8 LS channels for ON-OFF mode with $R_{onmax}$ = 0.3 Ω.

There is also the possibility to connect the OUT1-4 and OUT5-8 in order to drive in PWM mode a load connected to VB or GND without the necessity of a freewheeling diode. In this case the $R_{onmax}$ = 0.6 Ω.

The above configuration can be driven by parallel input or SPI command.

Through the SPI it is possible to configure the device parameters like configuration, Slew-rate, Overcurrent threshold, to send the drivers commands and to read back the diagnosis results.

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| L9301-TR | PowerSSO36 | Tape & Reel |

# Contents

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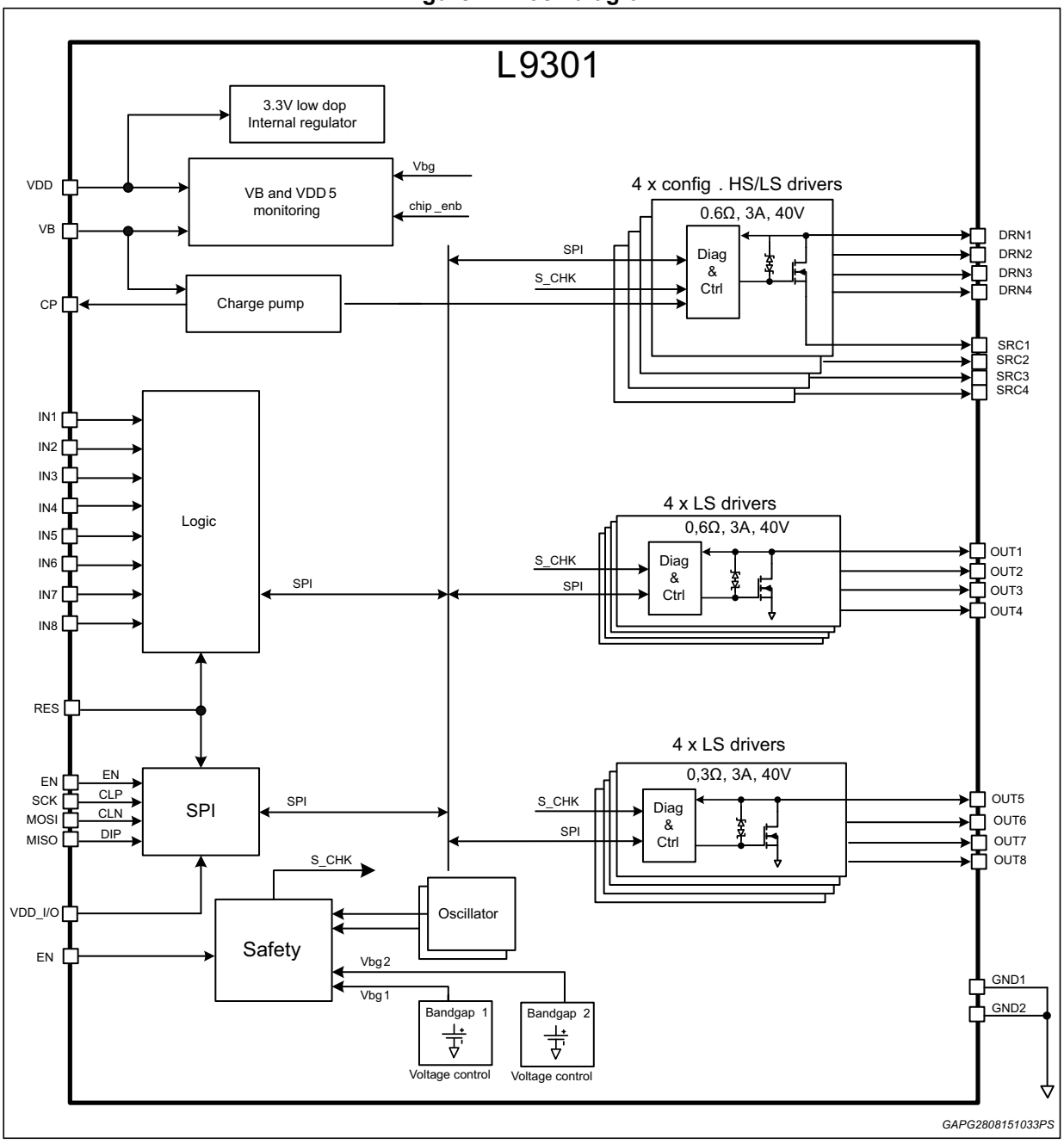
# 1 Block diagram

**Figure 1. Block diagram**



# 2 Pin description

**Figure 2. Pin connection diagram**

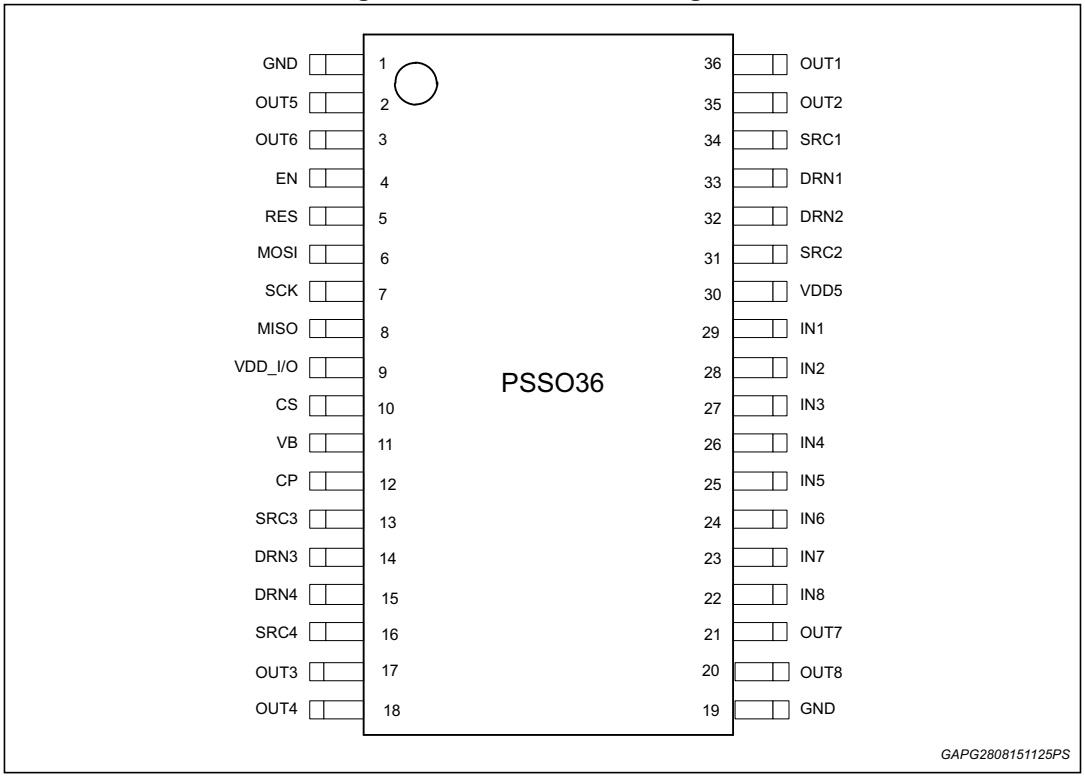



**Table 2. Pin description**

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | Power ground of OUT1,2,5,6 |
| 2 | OUT5 | Output 5 |
| 3 | OUT6 | Output 6 |
| 4 | EN | Enable |
| 5 | RES | Reset input (active low) |
| 6 | MOSI | SPI data in |
| 7 | SCK | SPI serial clock input |
| 8 | MISO | SPI data out |
| 9 | VDD_I/O | Microcontroller logic interface voltage |
| 10 | CS | SPI chip select (active low) |
| 11 | VB | Battery supply voltage |
| 12 | CP | Charge pump |
| 13 | SRC3 | Source pin of configurable driver #3 |
| 14 | DRN3 | Drain pin of configurable driver #3 |

Table 2. Pin description (continued)

| Pin | Symbol | Function |
|---|---|---|
| 15 | DRN4 | Drain pin of configurable driver #4 |
| 16 | SRC4 | Source pin of configurable driver #4 |
| 17 | OUT3 | Output 3 |
| 18 | OUT4 | Output 4 |
| 19 | GND | Power ground of OUT3,4,7,8 |
| 20 | OUT8 | Output 8 |
| 21 | OUT7 | Output 7 |
| 22 | IN8 | Discrete input used to PWM output driver #8 |
| 23 | IN7 | Discrete input used to PWM output driver #7 |
| 24 | IN6 | Discrete input used to PWM output driver #6 |
| 25 | IN5 | Discrete input used to PWM output driver #5 |
| 26 | IN4 | Discrete input used to PWM output driver #4 |
| 27 | IN3 | Discrete input used to PWM output driver #3 |
| 28 | IN2 | Discrete input used to PWM output driver #2 |
| 29 | IN1 | Discrete input used to PWM output driver #1 |
| 30 | VDD5 | 5 Volt supply input |
| 31 | SRC2 | Source pin of configurable driver #2 |
| 32 | DRN2 | Drain pin of configurable driver #2 |
| 33 | DRN1 | Drain pin of configurable driver #1 |
| 34 | SRC1 | Source pin of configurable driver #1 |
| 35 | OUT2 | Output 2 |
| 36 | OUT1 | Output 1 |
| EP | GND | Exposed pad: connected to GND |

# 3 Electrical specifications

## 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value [DC voltage] | Unit |
|---|---|---|---|
| VB | Supply voltage | -0.3 to 35 | V |
| VDD, VDD_I/O | Stabilized supply voltage | -0.3 to 18(1) | V |
| $V_{CS}$, $V_{SCK}$, $V_{MOSI}$, $V_{MISO}$, $V_{EN}$, $V_{IN1-8}$, $V_{RES}$ | Logic input/output voltage range | -0.3 to 18(1) | V |
| OUT1-8 | - | -1 to VCL | V |
| SRC1-4 | - | -1 to VB | V |
| DRN1-4 | - | -1 to VCL | V |
| CP | - | -0.3 to (VB+CP_DELTA) | V |
| GND | - | -0.3 to +0.3 | V |

1. Short to 18 V for 100 h max.

*Note: A suitable device to clamp the voltage during 'load dump' event to a value ≤35 V must be present at application level.*

## 3.2 ESD protection

**Table 4. ESD protection**

| Parameter | Value | Unit |
|---|---|---|
| ESD according to Human Body Model (HBM), Q100-002 for pins (1); (100 pF/1.5 kΩ) | ±4000 | V |
| ESD according to Human Body Model (HBM), Q100-002 for all other pins; (100 pF/1.5 kΩ) | ±2000 | V |
| ESD according to Charged Device Model (CDM), Q100- 011 Corner pins | ±750 | V |
| ESD according to Charged Device Model (CDM), Q100-011 Non-corner pins | ±500 | V |

1. VB, DRN1-4, SRC1-4, OUT1-8.

## 3.3 Operating range

**Table 5. Operating range**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| VB | Supply voltage | VB_UV | 18 | V |
| VDD | Stabilized supply voltage | VDD_UV | VDD_OV | V |
| VDD_IO | Logic output supply voltage | 3.0 | 5.5 | V |

## 3.4 Thermal data

**Table 6. Thermal data**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{amb}$ (1) | Operating ambient temperature | -40 | - | 125 | °C |
| $T_{stg}$ | Storage temperature | -40 | - | 150 | °C |
| $T_j$ | Junction temperature | -40 | - | 175 | °C |
| $T_{sd}$ | Thermal shutdown temperature | 180 | - | 195 | °C |
| $T_{sd\text{-}hys}$ | Thermal shutdown temperature hysteresis | - | 10 | - | °C |

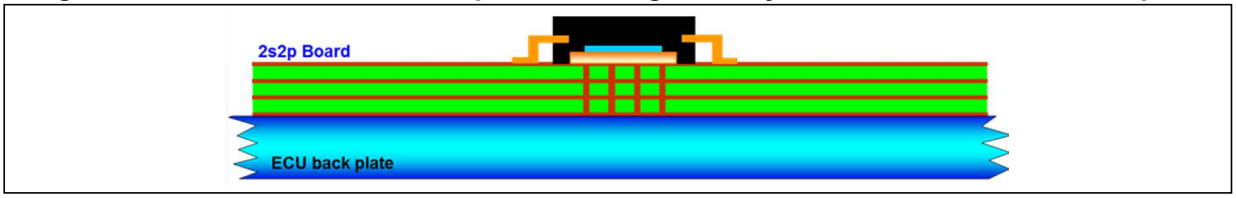
1. For information only, in any case $T_j$ limits must not exceed.

**Table 7. Thermal resistance**

| Symbol | Parameter | Working conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Junction to ambient | 2s2p (4L) board; Natural convection(1) | 27 | °C/W |
| | | 2s2p (4L) board on ECU metal plate(2) | 8 | °C/W |
| $R_{th\ j\text{-}bottom\ case}$ | Junction to bottom case | Bottom cold plate(3) | 1 | °C/W |
| $R_{th\ j\text{-}top\ case}$ | Junction to top case | Top cold plate(4) | 21 | °C/W |
| $Psi_{j\text{-}top\ case}$ | Psi Junction to top case | 2s2p (4L) board; Natural convection (1) | 2 | °C/W |

1. Jedec STD. JESD51.
2. Package assembled on 2s2p (4L) board. The board bottom side is in contact with a metal plate as per typical automotive application (ECU system). See *Figure 3*.
3. Thermal resistance between the die and the bottom case surface in ideal contact and measured by cold plate as per Jedec best practice guidelines (JESD51).
4. Thermal resistance between the die and the top case surface in ideal contact and measured by cold plate as per Jedec best practice guidelines (JESD51).

**Figure 3. Device assembled on 2s2p PCB with high density vias in contact with a metal plate**



# 4 Supply pins

## 4.1 VDD

An external +5.0 ±0.25 VDC supply provided from an external source is the primary power source to the L9301. This supply is used as the power source for all of its internal logic circuitry and other miscellaneous functions.

The VDD is monitored for under and over voltage and a dedicated SPI flag of each event is set to report those conditions. The device behavior in case of VDD fault detection can be defined using the proper configuration bit that allows to choose if the OUT must be disabled or not.

**Table 8. VDD**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VDD | VDD_UV | VDD undervoltage detection threshold | VDD decreasing | 4.5 | - | 4.7 | V |
| | VDD_uv_filt | VDD undervoltage filter time for output disable | Tested by scan | 90 | - | 145 | µs |
| | VDD_OV | VDD overvoltage detection threshold | VDD increasing | 5.25 | - | 5.5 | V |
| | VDD_ov_filt | VDD overvoltage filter time for output disable | Tested by scan | 90 | - | 145 | µs |

## 4.2 VB

This input is the supply for the on board charge pump and it shall be connected to protected battery line. In case of high-side configuration, to get the specified Ron value this pin must be connected to the same VB where the loads are connected. If it is present an additional voltage drop between the two VB, the $R_{dson}$ of that given output will be higher than the specified maximum.

The VB is monitored for under and over voltage and a dedicated SPI flag of each event is set to report those conditions. The device behavior in case of VB fault detection can be defined using the proper configuration bit that allows to choose if the OUT must be disabled or not.

Table 9. VB

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VB | VB_UV | VB undervoltage detection threshold | VB decreasing | 3.5 | - | 4 | V |
| | VB_UV_on | VB undervoltage detection threshold | VB increasing | 4 | - | 4.5 | V |
| | VB_UV_hys | VB undervoltage hysteresis | - | 0.1 | - | 1 | V |
| | VB_UV_filt | VB undervoltage filtering time | Tested by scan | 90 | - | 145 | us |
| | VB_OV | VB overvoltage detection threshold | VB increasing | 19 | - | 22 | V |
| | VB_OV_on | VB overvoltage detection threshold | VB decreasing | 19 | - | 21 | V |
| | VB_UV_hys | VB overvoltage hysteresis | - | 0.1 | - | 1 | V |
| | VB_OV_filt | VB overvoltage filtering time | Tested by scan | 90 | - | 145 | µs |

## 4.3 VDD_IO

This pin is used to supply the discrete MISO output stage of L9301 and must be connected to the same voltage used to supply the peripherals of the processor interfaced to L9301.

# 5 Discrete inputs

## 5.1 Output enable EN

The EN pin is the general output enable which allows the µC to immediately switch off the output in case of need. Output driving is allowed only if this pin is driven to high level. The device configuration can be changed only with EN pin driven to low level.

An internal pull down is present on the pin.

## 5.2 Output enable input IN1 to IN8

These inputs allow the outputs, depending on the configuration selected, to be enabled without the use of the SPI. The SPI command and the IN1-8 input are logically OR'd together.

A logic ‘1’ on this input will enable the correspondent output no matter what the status of the SPI command register is. A logic ‘0’ on this input will disable this output if the SPI command register is not commanding this output on. These pins can be left ‘open’ if the internal power stages are controlled only via the SPI. This input has a nominal 100 kΩ pull down resistor to GND, which will pull this pin to ground if an open circuit condition occurs. This input is ideally suited for loads that are pulse width modulated (PWM'd). This allows PWM control without the use of the SPI inputs.

**Table 10. Output enable input IN1 to IN8**

| EN | RESET | INx | OUTx/DRNx/SRCx |
|---|---|---|---|
| X | 0 | X | OFF |
| 0 | X | X | OFF |
| 1 | 1 | 0 | OFF |
| 1 | 1 | 1 | ON |

## 5.3 Reset input

When this input goes low it resets all the internal registers and switches off all the output stages. This input has a nominal 100 kΩ resistor connected from this pin to the internal 3.3 V regulator, which will pull this pin to 3.3 V if an open circuit condition occurs.

**Table 11. Electrical characteristic of EN, IN1...8, RES pin**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| IN1...8, EN, RES | V_IH | Logic input high voltage | - | 1.75 | | VDD+0.3 | V |
| | V_IL | Logic input low voltage | - | -0.3 | | 0.75 | V |
| | V_Ihys | Logic input hysteresis | - | 100 | | 1000 | mV |
| IN1...8, EN | Ri_pd | Pull down resistor | Tested at 1.5 V | 50 | 100 | 150 | kΩ |
| RES | Ri_pu | Pull up resistor | Tested at 1.5 V, $R = (3.3\text{-}1.5)/I_{measure}$ | 50 | 100 | 150 | kΩ |

# 6 Configuration

The selected configuration can be configured by SPI, there are 2 bits dedicated to configuration selection:

**Table 12. Configuration**

| Bit1 | Bit0 | Configuration | Input → Output | Description |
|---|---|---|---|---|
| 0 | 0 | 1 | IN1-4 → DRN1-4, OUT1-4<br>IN5-8 → OUT5-8 | 8 low side channels with $R_{dson}$ = 0.3 Ω |
| 0 | 1 | 2 | IN1-4 → OUT1-4<br>IN5-8 → OUT5-8 | 4 low side channels with $R_{dson}$ = 0.6 Ω<br>4 low side channels with $R_{dson}$ = 0.3 Ω |
| 1 | 0 | 3 | IN1-4 → SRC1-4,<br>IN5-8 → OUT5-8 | 4 high side channels with $R_{dson}$ = 0.6 Ω<br>4 low side channels with $R_{dson}$ = 0.3 Ω |
| 1 | 1 | 4 | IN1-4 → OUT1-4,<br>IN5-8 → OUT5-8,<br>SPI → DRN/SRC1-4 | 4 low side channels with $R_{dson}$ = 0.6 Ω<br>4 low side channels with $R_{dson}$ = 0.3 Ω<br>4 low/high side ch. with $R_{dson}$ = 0.6 Ω |

The configuration is enabled only when EN pin is logic 0.

In configuration 4, the output DRN/SRC1-4 can be controlled by SPI only; for those outputs the selection between high side and low side configuration can be done through the dedicated bit (bit8 of Device general configuration register).

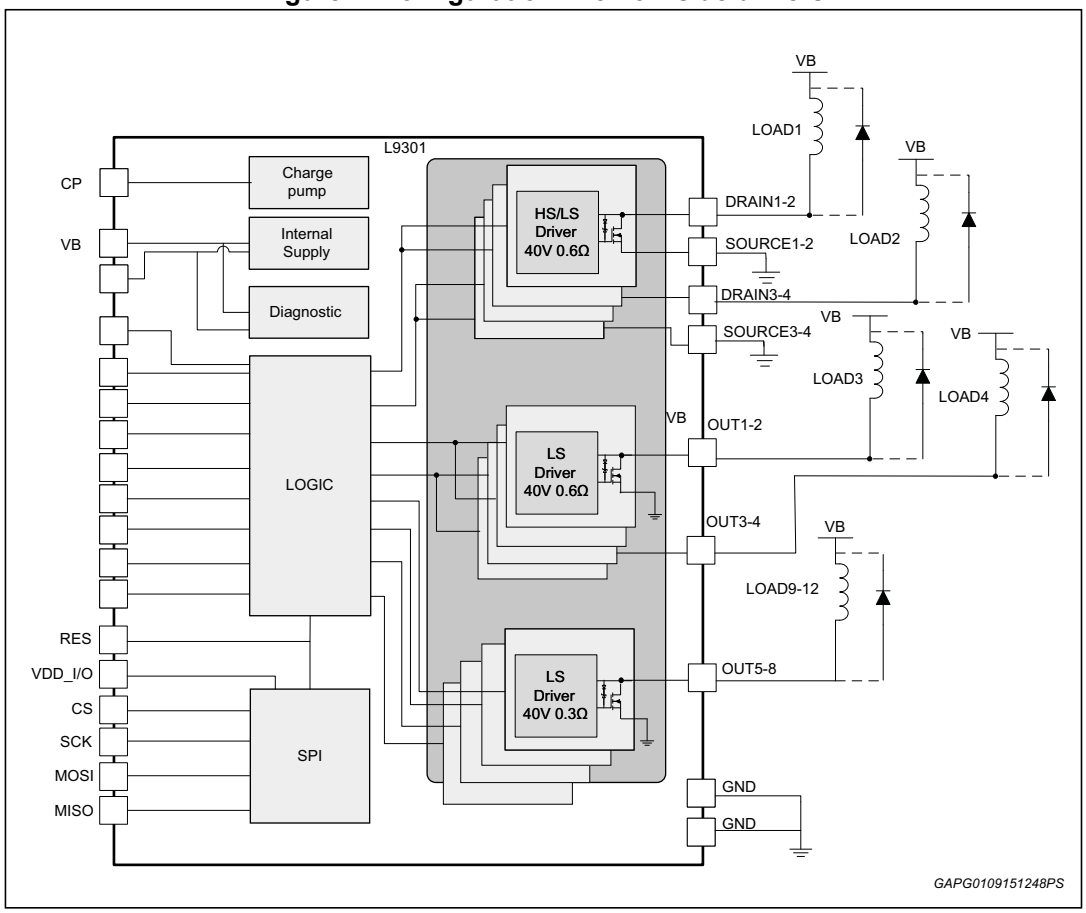
# 7 Configuration 1: 8 low side drivers

In this configuration there are 8 low side drivers available that can be driven by SPI or by the parallel input: IN1-4 control both DRAIN1-4 and OUT1-4 that must be turned on and off simultaneously while IN5-8 control OUT5-8.

The corresponding relations are:

- IN1: OUT1 & OUT2;
- IN2: OUT3 & OUT4;
- IN3: DRN1 & DRN2;
- IN4: DRN3 & DRN4

**Figure 4. Configuration 1: 8 Low side drivers**



## 7.1 Configuration 2: 4 low-side PWM mode and 4 low-side drivers

In this configuration there are 4 low side drivers with integrated free-wheeling diodes and 4 low side drivers available. All the channels can be driven by SPI or by the parallel input. To enable the OUT1-4 driving, the PWM enable SPI bit for OUT1-4 and SRC1-4 must be set.

The IN1-4 control the low side power OUT1-4 used to drive the LOAD1-4 and the device should assure that when the low-side is switched off, the high-side, acting as a free-wheeling diode, must be turned on. To avoid cross conduction the LS VGS voltage is monitored.

When OUT1-4 are commanded ON either by INx or SPI, the L9301 switches off the HS first, then with 2 µs delay after detecting HS VGS low, it switches on LS.

When OUT1-4 are commanded OFF either by INx or SPI, the L9301 switches off the LS first, then with 2 µs delay after detecting LS VGS low, it switches on the HS.

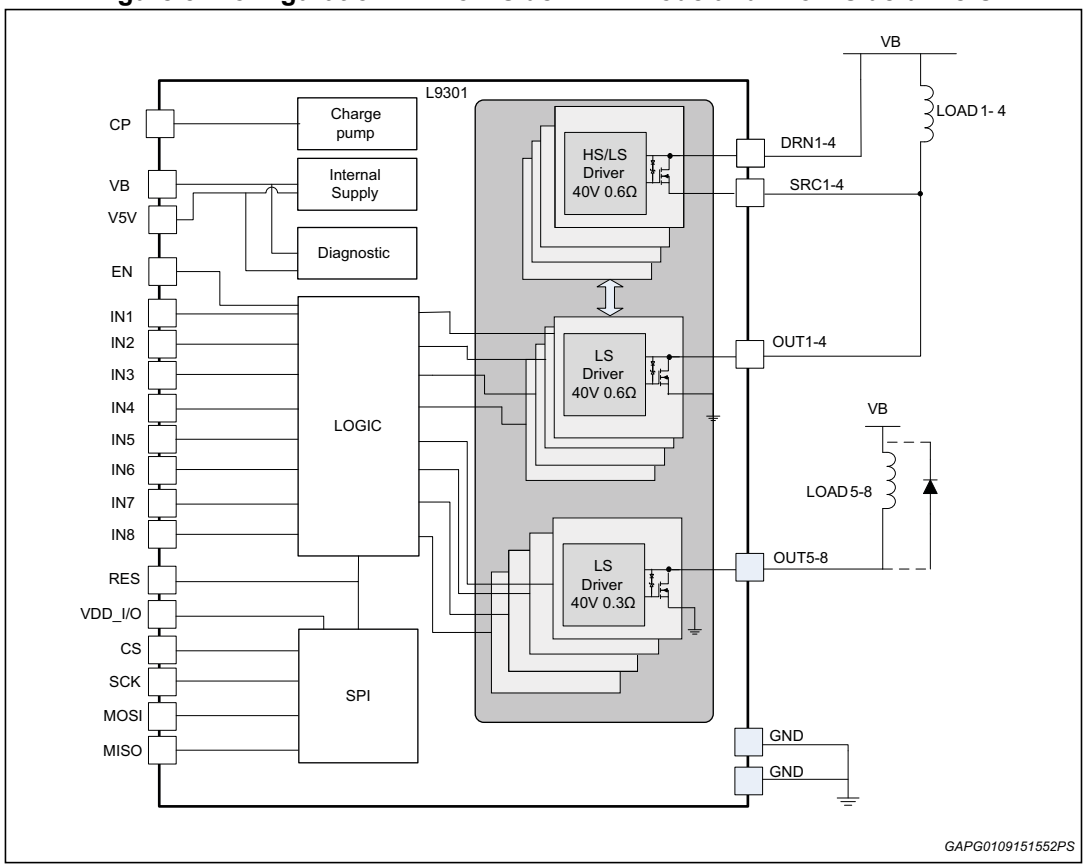
IN5-8 control OUT5-8

The selected configuration must be configured by SPI.

The corresponding relations are:

– IN1: OUT1 ↔ SRC2;
– IN2: OUT2 ↔ SRC1;
– IN3: OUT3 ↔ SRC4;
– IN4: OUT4 ↔ SRC3

**Figure 5. Configuration 2: 4 low-side PWM mode and 4 low-side drivers**



## 7.2 Configuration 3: 4 high-side PWM mode and 4 low-side drivers

In this configuration there are 4 high side drivers with integrated free-wheeling diodes and 4 low side drivers available. All the channels can be driven by SPI or by the parallel input. To enable the SRC1-4 driving, the PWM enable SPI bit for SRC1-4 and OUT1-4 must be set.

The IN1-4 control the high side power SRC1-4 used to drive the LOAD1-4 and the device should assure that when the high-side is switched off, the low-side, acting as a free-wheeling diode, must be turned on. To avoid cross conduction the HS VGS voltage is monitored.

When SRC1-4 is commanded ON either by INx or SPI, the L9301 switches off the HS first, then with 2 µs delay after detecting HS VGS low, it switches on LS.

When SRC1-4 is commanded OFF either by INx or SPI, the L9301 switches off the HS first, then with 2 µs delay after detecting HS VGS low, it switches on the LS.

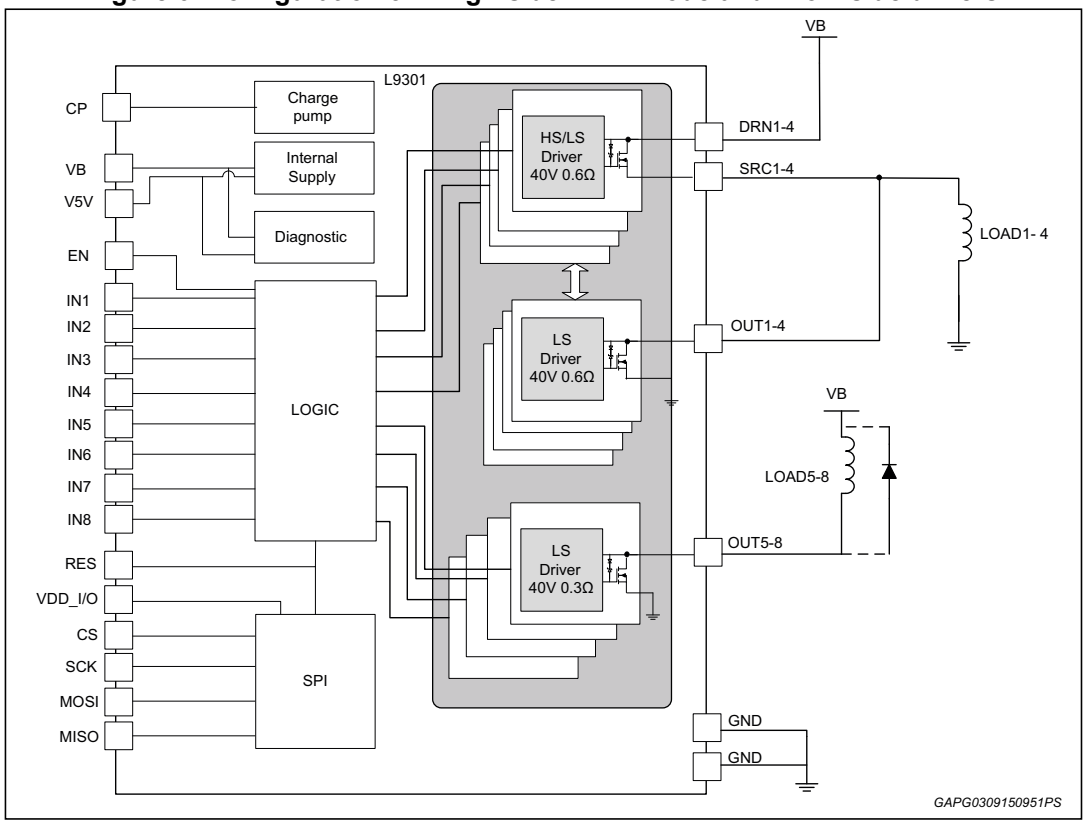
IN5-8 control OUT5-8

The selected configuration must be configured by SPI.

Note: The corresponding relations are:

- IN1: SRC1 ↔ OUT2;
- IN2: SRC2 ↔ OUT1;
- IN3: SRC3 ↔ OUT4;
- IN4: SRC4 ↔ OUT3

**Figure 6. Configuration 3: 4 high-side PWM mode and 4 low-side drivers**



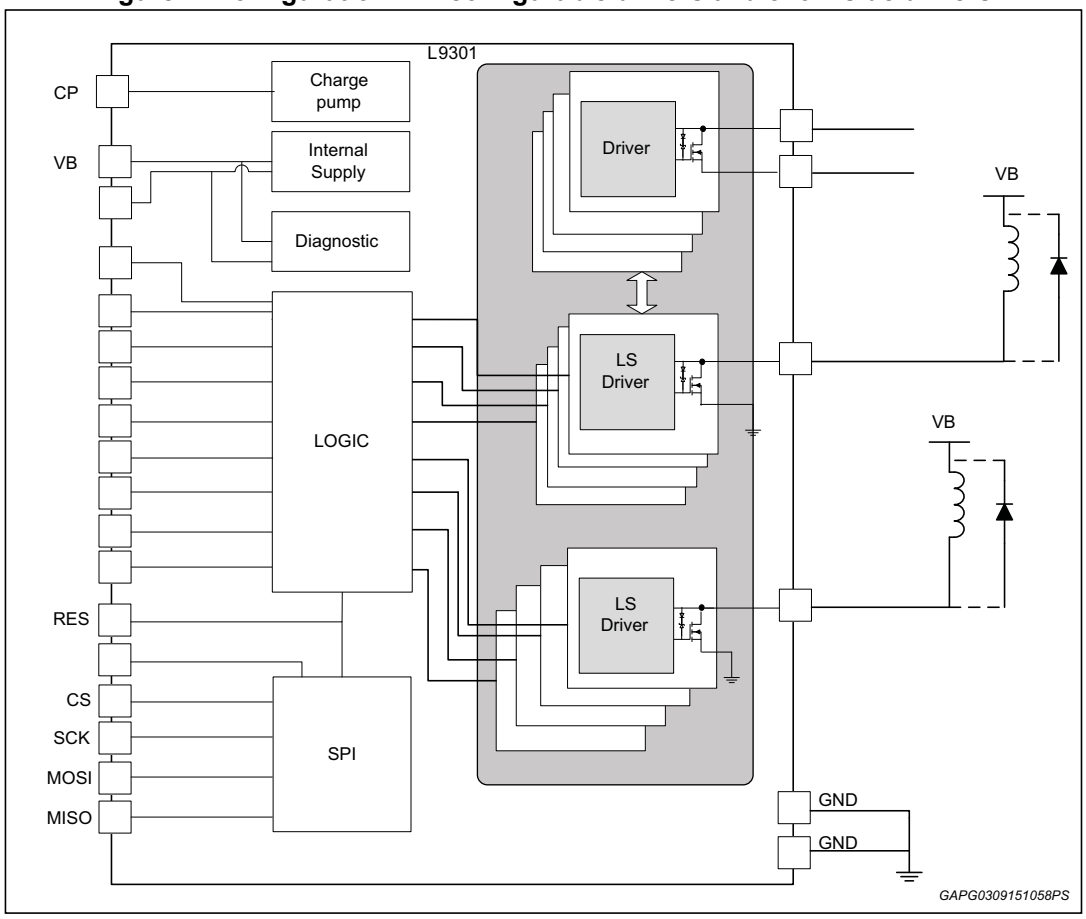
## 7.3 Configuration 4: 4 configurable drivers and 8 low-side drivers

In this configuration there are 4 HS/LS drivers and 8 low side drivers available. All the LS can be driven by SPI or by the parallel input.

The IN1-8 control OUT1-8 while the configurable driver can only be controlled by SPI.

– The four configurable drivers (DRN1-4, SRC1-4) can be configured separately as LS or HS using the dedicated SPI bit.

**Figure 7. Configuration 4: 4 configurable drivers and 8 low-side drivers**

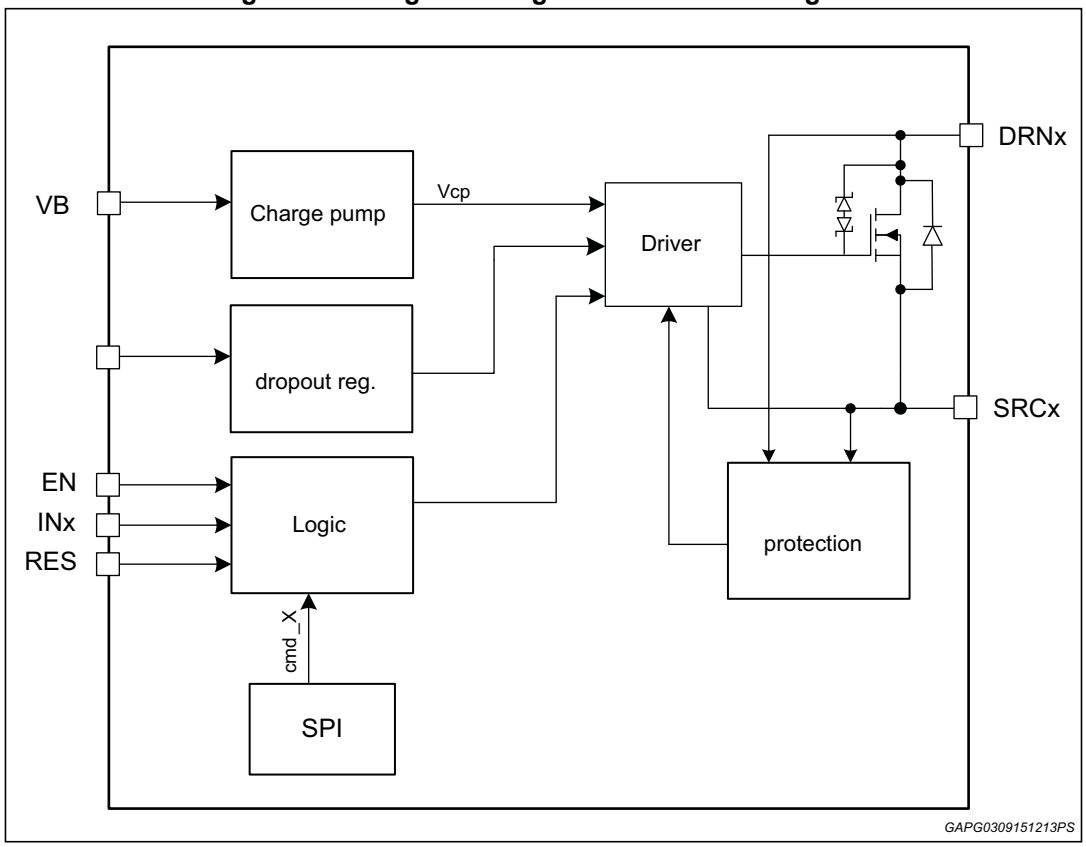


# 8 Configurable high/low side driver

The channels 1 to 4 can be configured as high or low side. In the low side configuration an internal clamp is present.

In high side configuration, the DRNx are connected to VB pin in PCB. To guarantee the OC (over current) function, the DRNx voltage is within the range of (VB-1 V, VB+1 V).

**Figure 8. Configurable high/low side driver diagram**




## 8.1 Electrical characteristics DRN/SRC1-4

5 V ≤ VB < 18 V; -40°C ≤ $T_j$ ≤ 175°C unless otherwise specified.

**Table 13. Configurable high/low side drivers 1-4 electrical characteristics**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DRN1-4<br>SRC1-4 | $R_{DS\text{-}on\_HLS}$ | - | HS/LS configuration<br>VB = 13.5 V; I_load = 1 A | - | - | 0.6 | Ω |

**Table 13. Configurable high/low side drivers 1-4 electrical characteristics (continued)**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DRN1-4<br>SRC1-4 | $I_{OUT\_LK\_HLS}$ | Output leakage current | HS configuration<br>DRNx = 13.5 V; SRCx = 0 V | - | - | 10 | µA |
| | | | LS configuration<br>DRNx = 13.5 V; SRCx = 0 V | - | - | 10 | µA |
| | $V_{S/R\_HLS}$ | Voltage S/R on/off | HS/LS configuration<br>VB 13.5 V<br>Load: 8 Ω, 10 nF – From 80% to 30% of DRNx(SRCx) | 2 | 4 | 6 | V/µs |
| | | | HS/LS configuration<br>VB 13.5 V<br>Load: 8 Ω, 10 nF – From 80% to 30% of DRNx(SRCx) | 5 | 10 | 15 | V/µs |
| | $T_{turn\text{-}on\_HLS}$ | Turn-on delay time | HS configuration<br>VB 13.5 V<br>From command to 10% SRCx<br>Load: 8 Ω, 10 nF | - | - | 3 | µs |
| | | | LS configuration<br>VB 13.5 V<br>From command to 90% DRNx<br>Load: 8 Ω, 1 0nF | - | - | 3 | µs |
| | $T_{turn\text{-}off\_HLS}$ | Turn-off delay time | HS configuration<br>VB 13.5 V<br>From command to 90% SRCx<br>Load: 8 Ω, 10 nF | - | - | 3 | µs |
| | | | LS configuration<br>VB 13.5 V<br>From command to 10% DRNx<br>Load: 8 Ω, 10 nF | - | - | 3 | µs |
| | $V_{CL\_LS}$ | Output clamping voltage | LS configuration<br>I_load= 0.6 A T = 130 °C | 34 | 37.5 | 41 | V |
| | | | LS configuration<br>I_load = 0.6 A, T = -40 °C and 25 °C | 35 | 37.5 | 41 | |
| | $E_{clampSP\_LS}$ | Clamp repetitive pulse energy ATE test | LS configuration<br>I_load = 0.7 A, $T_j$ = 150 °C, 100 kpulses | - | - | 5 | mJ |
| | $E_{clampSP\_LS}$ | Clamp single pulse energy ATE test | LS configuration<br>I_load = 0.7 A, $T_j$ = 150 °C | - | - | 10 | |

## 8.2 Driver diagnostic

### 8.2.1 Thermal protection

Each solenoid channel has a dedicated temperature sensor that continuously monitors the temperature of the PowerMOS.

In case the shutdown temperature $T_{sd}$ is reached the related channel is turned off and the dedicated diagnostic bits are set. t_sdl_x is the bit that latches the thermal shut down and it is cleared after sending dedicated SPI to clear the bit, t_sd_x is the other thermal shut down bit and once it is set by thermal shut down condition it is cleared only when the $T_j$ decreases below the thermal shut down threshold (hysteresis). If the microcontroller, when the device is still in temperature shut down condition (t_sd_x = 1), clears the t_sdl_x and tries to turn on the output, the actuation is not performed and the t_sdl_x will be set again. To avoid these multiple interrupts the microcontroller can poll the t_sd_x bit and enable the next actuation only when the bit is zero.

To re-switch on the channel after thermal shut down, the SPI needed to switch off the channel is required.

### 8.2.2 Overcurrent protection

An overcurrent protection is present for each driver DRN/SRC1...4. The overcurrent threshold is selectable through oc_thres_x (where x indicates the channel). In case of overcurrent the output driver is turned off, the related SPI command bit is set to 0 and a dedicated diagnostic bit is set oc_x where x indicates the channel where the fault occurred.

If bit oc_restart = 0, to restart the channel the microcontroller has to clear the fault bit (reading the fault register), and to write to 1 the SPI command bit or to provide a rising edge on the parallel input command.

If bit oc_restart = 1, the restart function is activated. The slew rate of the channel in fault condition is automatically set to the higher value to limit dissipation issue then to restart the channel the microcontroller has to write to 1 the SPI command bit or to provide a rising edge on the parallel input command. The diagnostic bit oc_x can be cleared only by writing it to 0 in the corresponding driver status register by SPI however the channel can be restarted as described above.

### 8.2.3 Output status

During the ON phase, the output voltage is compared with the VTopen threshold voltage in order to verify if the output status is aligned with the ON command:

- in case of low side usage if the DRNx voltage is above the VTopen threshold a dedicated bit is set to indicate the anomaly
- in case of high side usage if the SRCx voltage is below the VTopen threshold a dedicated bit is set to indicate the anomaly

### 8.2.4 Charge Pump (CP)

The charge pump is enabled when the selected configuration includes high side drivers (like configuration 2, 3, 4). In configuration 1 the charge pump is internally shorted to VB.

On the CP pin it's required to connect a 100 nF capacitor toward the VB line.

The charge pump is ON if VB > UV threshold & VDD > UV threshold

The charge pump is OFF if VB< UV threshold or VDD< UV threshold. The CP voltage is equal to VB-Vbe.

When the CP is ON, the low CP diagnosis is enabled. When any HS is switched on but CP voltage is not high enough to switch on HS, low CP fault is detected. A SPI bit allows configuring the actions to be taken in case of low CP fault.

**Table 14. Charge pump**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| CP | CP_DELTA | Delta voltage CP-VB | VB>5V | 3 | - | 6 | V |

### 8.2.5 DLOSS

When the L9301 is configured with low side and external diodes are used for freewheeling, there is the possibility through a dedicated SPI bit to enable the ‘diode loss’ diagnosis that is used to detect if the external diode is no more connected checking if during the OFF phase the internal clamp is activated. Another SPI bit allows configuring the actions to be taken in case of DLOSS fault.

When the L9301 is configured as high side and internal/external diodes are used for freewheeling, there is the possibility through a dedicated SPI bit to enable the ‘diode loss’ diagnosis that is used to detect if the diode is no more connected checking if during the OFF phase the HS is forced to switch on. Another SPI bit allows configuring the actions to be taken in case of DLOSS fault.

In addition, diode loss on LS (including configurable channels configured as LS) is only detected when VBOV is not present.

### 8.2.6 OFF state diagnostic

The device provides the off-state diagnostic for each channel.

In low-side configuration the short to ground and open load faults can be detected. The fault is reported in a SPI register.

**Figure 9. LS configuration diagnostic**

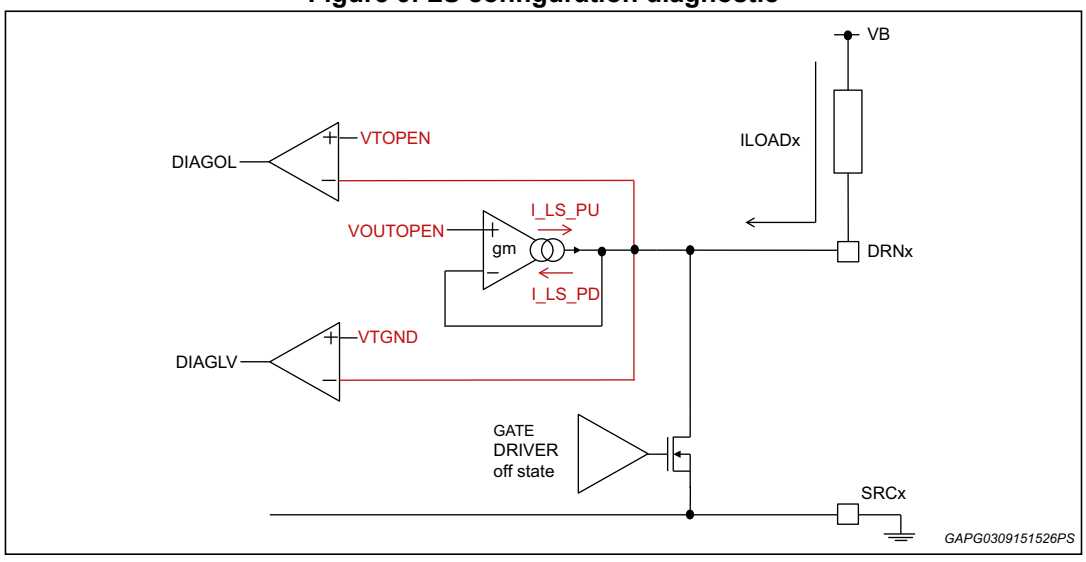


**Table 15. LS diagnostic**

| DIAGOL | DIAGLV | FAULT DETECTION |
|---|---|---|
| 0 | 0 | no fault |
| 0 | 1 | not possible |
| 1 | 0 | open load |
| 1 | 1 | short to ground |

In high-side configuration the short to battery and open load faults can be detected. The fault is reported in a SPI register.

**Figure 10. HS configuration diagnostic**

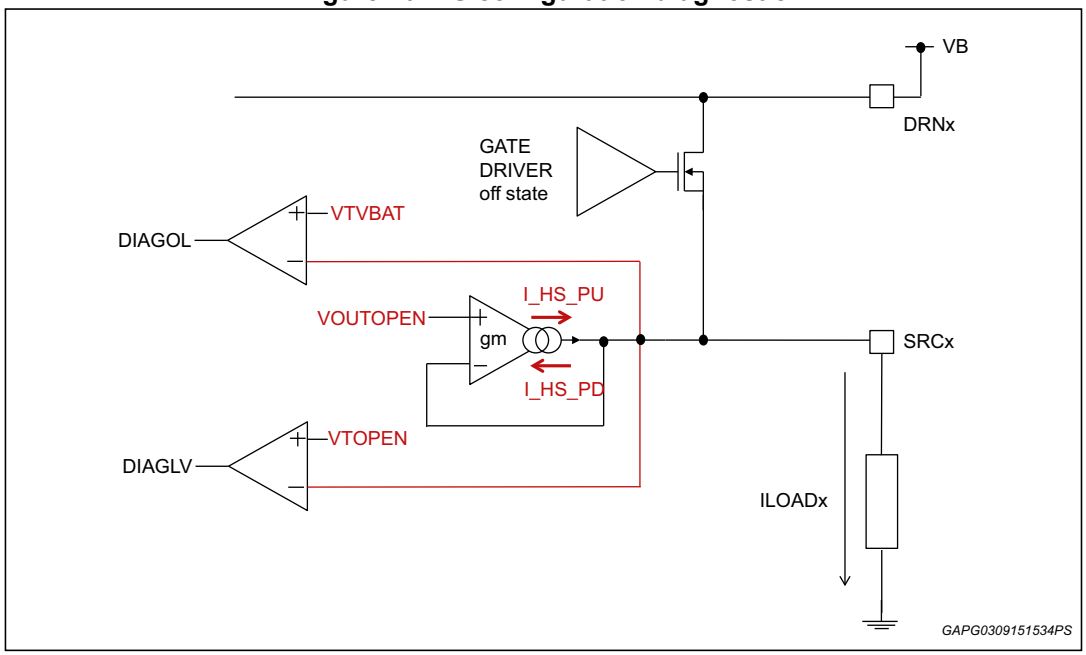



**Table 16. HS diagnostic**

| DIAGOL | DIAGLV | FAULT DETECTION |
|---|---|---|
| 0 | 0 | short to ground |
| 0 | 1 | not possible |
| 1 | 0 | open load |
| 1 | 1 | no fault |

The diagnostic blanking time is configurable through the dedicated diagoff_blank_sel bit.

The OFF diagnosis is triggered at driver OFF CMD and will not be refreshed after clearing the flags. To recover the OFF diagnosis in OFF stage, send SPI to disable OFF diagnosis and then enable it.

### 8.2.7 Over current (OC) comparator self-test

L9301 provides driver OC (over current) comparator self-test function. During OFF phase, the OC comparator still works and the expected result is '1' due to high drain-source voltage. If L9301 detects OC '0' during OFF phase, the SPI bit oc_comparator_f is set to '1'.

For DRN1-4, when they are configured as LS, a Short To Ground (STG) fault will not trigger OC '1', so L9301 will report both STG and OC comparator self-test fail, when they are configured as HS, a short-to-battery (STB) fault will not trigger OC '1', so L9301 will report both STB and OC comparator self-test fail.

### 8.2.8 Electrical characteristics related to diagnosis

**Table 17. Electrical characteristics related to diagnosis**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DRN1-4<br>SRC1-4 | $T_{Over\_temperature\_blanking}$ | Over temperature blanking time | Tested by scan | 1 | - | 1.5 | µs |
| | $T_{Over\_temperature\_filter}$ | Over temperature filter time | Tested by scan | 2 | - | 5 | µs |
| | $T_{Charge\_pump\_low}$ | Charge pump low filter time | Tested by scan | 3 | - | 5 | µs |
| | $T_{Charge\_pump\_low\_blanking}$ | Charge pump low blanking time | Tested by scan | 25 | - | 40 | µs |
| | $T_{diode\_loss\_filter\_time}$ | Diode loss filter time | Tested by scan | 3 | - | 5 | µs |
| | $R_{open\_load\_HLS}$ | Min. resistor value open load detection | Not tested | 10 | - | | kΩ |
| | $I_{OC\_HLS}$ | Over current threshold 1 | - | 1 | 2 | 3 | A |
| | $I_{OC\_HLS}$ | Over current threshold 2 | - | 3 | 4 | 5 | A |
| | $T_{FLT\_OC\_HLS}$ | Over current filtering time | Tested by scan | 3 | - | 5 | µs |
| | $T_{FLT\_diagoff\_HLS}$ | Filtering open load and short to GND diag. off | Tested by scan | 55 | - | 80 | µs |
| | $T_{d\_blank0\_HLS}$ | Diagnosis blanking time after switch-off | Tested by scan | 900 | - | 1300 | µs |
| | $T_{d\_blank1\_HLS}$ | Diagnosis blanking time after switch-off | Tested by scan | 450 | - | 650 | µs |
| | $V_{TOPEN\_HS}$ | Open load threshold voltage | HS configuration | 1.9 | 2.1 | 2.3 | V |
| | $V_{TOPEN\_LS}$ | | LS configuration | 2.7 | 2.9 | 3.1 | V |