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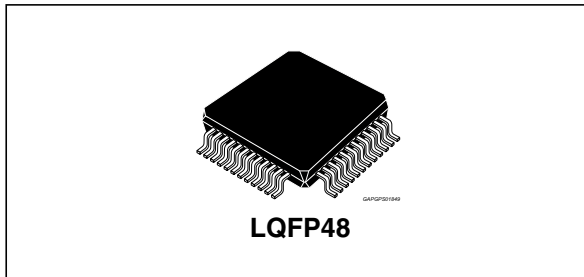
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Quad squib driver and dual sensor interface ASIC for safety application

Datasheet - production data



Features

- 4 deployment drivers sized to deliver 1.2 A (min) for 2 ms (min) and 1.75 A (min) for 1ms (min).
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib with 1.2 A (min.) or 1.75 A under 35 V load-dump condition and the low-side MOS is shorted to ground
- Capability to deploy the squib with 1.2 A (min.) at 6.9 V V_{RES} and 1.75 A at 12 V V_{RES} .
- Interface with 2 satellite sensors
- Programmable independent current trip points for each satellite channel

- Support Manchester protocol for satellite sensors
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 5.5 MHz SPI interface
- Satellite message error detection
- Low voltage internal reset
- 2 kV ESD capability on all pins
- Package: 48 lead LQFP
- Technology: ST Proprietary BCD5s (0.57 μm)

Description

L9654 is intended to deploy up to 4 squibs and to interface up to 2 satellites.

Squib drivers are sized to deploy 1.2 A (min.) for 2 ms (min.) during load dump and 1.75 A (min.) for 1 ms (min.) during load dump.

Diagnostic of squib driver and squib resistance measurement is controlled by micro controllers.

Satellite interfaces support Manchester decoder with variable bit rates.

Table 1. Device summary

Order code	Package	Packing
L9654	LQFP48	Tray
L9654TR	LQFP48	Tape and reel

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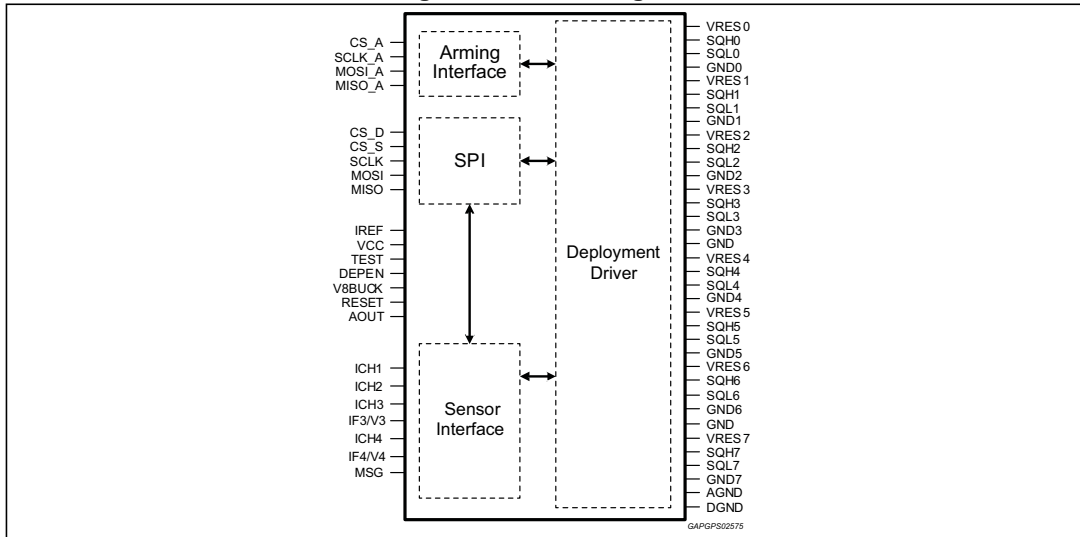
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1 Block diagram and application schematic

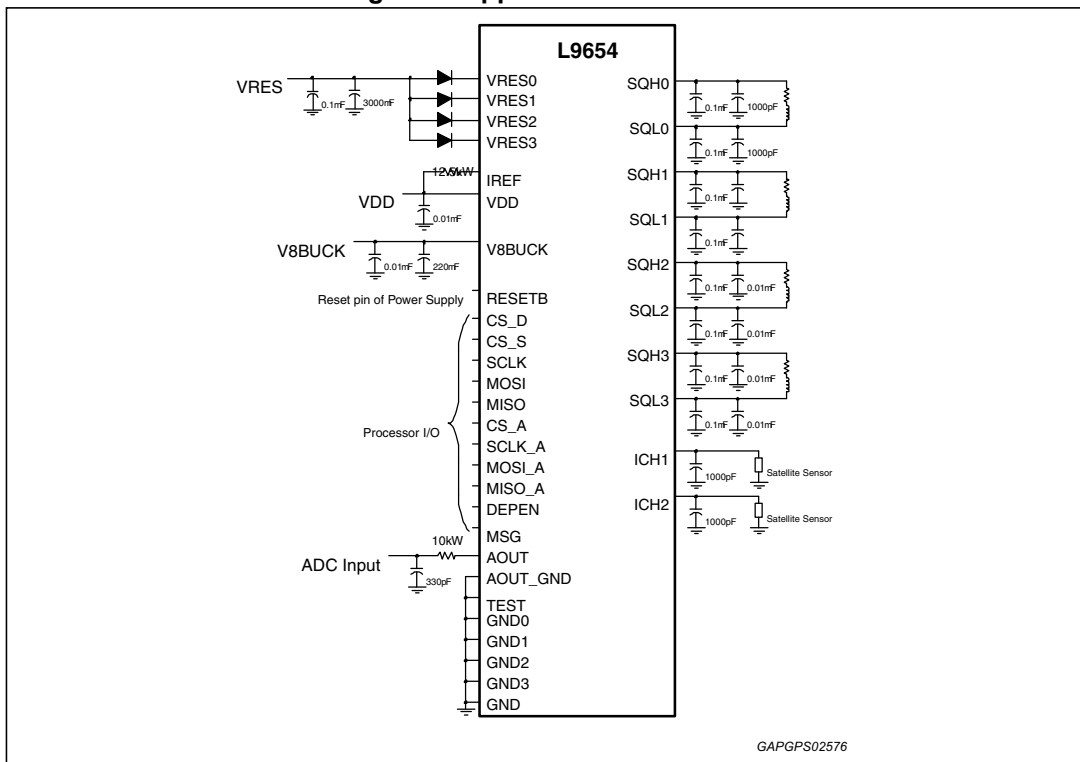
1.1 Block diagram

Figure 1. Block diagram



1.2 Application schematic

Figure 2. Application schematic



2 Pin description

Table 2. Pin function

Pin #	Pin name	Description	I/O type	Reset state
1	MISO_A	Arming SPI data out	Output	Hi-Z
2	NC	No connect	-	-
3	RESETB	Reset pin	Input	Pullup
4	GND	Signal ground (analog & digital)	-	-
5	VDD	VDD supply voltage	Input	-
6	NC	No connect	-	-
7	CS_A	SPI chip select for arming interface	Input	Pulldown
8	CS_S	SPI chip select for satellite interface	Input	Pulldown
9	CS_D	SPI Chip select for deployment driver	Input	Pulldown
10	DEPEN	Deployment enable	Input	Pulldown
11	MOSI	SPI data in	Input	Hi-Z
12,13	NC	No connect	-	-
14	MOSI_A	Arming SPI data in	Input	Hi-Z
15	SCLK_A	Arming SPI clock	Input	Hi-Z
16	SCLK	SPI clock	Input	Hi-Z
17	GND2	Power ground for loop channel 2	-	-
18	SQL2	Low-side driver output for channel 2	Output	Pulldown
19	SQH2	High-side driver output for channel 2	Output	Hi-Z
20	VRES2	Reserve voltage for loop channel 2	Input	-
21	VRES3	Reserve voltage for loop channel 3	Input	-
22	SQH3	High-side driver output for channel 3	Output	Hi-Z
23	SQL3	Low-side driver output for channel 3	Output	Pulldown
24	GND3	Power ground for loop channel 3	-	-
25	TEST	Test pin	Input	Pulldown
26	NC	No connect	-	-
27	V8BUCK	Supply Voltage for Satellite Interface and Resistance Measurement	Input	-
28	NC	No connect	-	-
29	ICH2	Current sense output for channel 2	Output	Hi-Z
30	NC	No connect	-	-
31	ICH1	Current sense output for channel 1	Output	Hi-Z
32	NC	No connect	-	-
33	IREF	External current reference resistor	Output	-

Table 2. Pin function (continued)

Pin #	Pin name	Description	I/O type	Reset state
34	AOUT_GND	Ground reference for AOUT	-	-
35	AOUT	Analog output for loop diagnostics	Output	Hi-Z
36	NC	No connect	-	-
37	GND1	Power ground for loop channel 1	-	-
38	SQL1	Low-side driver output for channel 1	Output	Pulldown
39	SQH1	High-side driver output for channel 1	Output	Hi-Z
40	VRES1	Reserve voltage for loop channel 1	Input	-
41	VRES0	Reserve voltage for loop channel 0	Input	-
42	SQH0	High-side driver output for channel 0	Output	Hi-Z
43	SQL0	Low-side driver output for channel 0	Output	Pulldown
44	GND0	Power ground for loop channel 0	-	-
45	NC	No connect	-	-
46	MSG	Message waiting	Output	Pulldown
47	MISO	SPI data out	Output	Hi-Z
48	NC	No connect	-	-

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value.	Unit
$R_{th\ j-amb}$	Thermal resistance junction-to-ambient	68	°C/W

3 Electrical specification

3.1 Maximum ratings

The device may not operate properly if maximum operating condition is exceeded.

Table 4. Maximum operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.9 to 5.1	V
V_{8BUCK}	V8BUCK voltage	7 to 8.5	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3)	35	V
V_I	Discrete input voltage (RESETB, DEPEND, CS_A, CS_D, CS_S, SCLK, SCLK_A, MOSI, MOSI_A, MISO, MISO_A)	0.3 to ($V_{DD} + 0.3$)	V
T_j	Junction temperature	-40 to 150	°C

3.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 5.5	V
V_{8BUCK}	V8BUCK voltage	0.3 to 40	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3)	0.3 to 40	V
SQ_{L-H}	Squib high and low-side drivers (SQH0, SQH1, SQH2, SQH3, SQL0, SQL1, SQL2, SQL3)	0.3 to 40	V
V_I	Discrete input voltage (RESETB, DEPEND, CS_A, CS_D, CS_S, SCLK, SCLK_A, MOSI, MOSI_A, MISO, MISO_A)	-0.3 to 5.5	V
ICHx	Satellite input voltage (ICH1, ICH2, ICH3, ICH4)	-3 to 40	V
-	Analog/digital outputs voltage (AOUT, IREF, MSG, IF3V3, IF4V4)	-0.3 to 5.5	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C

3.3 Electrical characteristics

3.3.1 DC characteristics

$V_{RES} = 6.5$ to 35 V, $V_{DD} = 4.9$ to 5.1 V, $V_{8BUCK} = 7.0$ V to 8.5 V, $T_{amb} = -40^{\circ}\text{C}$ to $+95^{\circ}\text{C}$.

Table 6. DC specification general

Symbol	Parameter	Test condition	Min.	Typ	Max.	Unit
$V_{RST}^{(1)}$	Internal voltage reset V_{DD}	V_{DD} drops until deployment drivers are disabled	4.0	-	4.5	V
$V_{RST_L}^{(2)}$			2.1	-	3.0	
I_{DD}	Input current V_{DD}	Normal operation; $I_{CH1-2} = 0$ A	4.5	-	7.0	mA
		Short to -0.3 V on SQH; $I_{CH1-2} = 0$ A	4.2	-	7.9	
		Short to -0.3 V on SQL; $I_{CH1-2} = 0$ A	4.2	-	7.9	
		Deployment; $I_{CH1-2} = 0$ A	4.2	-	7.9	
R_{IREF_H}	Resistance threshold I_{REF}	-	20.0	-	60.0	k Ω
R_{IREF_L}		-	2.0	-	9.0	k Ω
V_{IH_RESETB}	Input voltage threshold RESETB	-	-	-	2.0	V
V_{IL_RESETB}		-	0.8	-	-	V
V_{HYS}		-	100	-	400	mV
V_{IH_DEPEN}	Input voltage threshold DEPEN	-	-	-	2.0	V
V_{IL_DEPEN}		-	0.8	-	-	V
I_{PD}	Input pull-down current DEPEN	$V_{IN} = V_{IL}$ to V_{DD}	10	-	50	μ A
V_{IH_TEST}	Input voltage threshold TEST	-	-	-	3.6	V
V_{IL_TEST}		-	0.8	-	-	V
I_{TEST}	Input pull-down current TEST	TEST = 5 V	1.0	-	2.5	mA
I_{PU}	Input pull-up current RESETB	RESETB = V_{IH} to GND	10	-	60	μ A
I_{V8BUCK}	Current consumption V8BUCK	-	25	-	40	μ A
V_{IH}	Input voltage threshold MOSI, MOSI_A, SCLK, SCLK_A, CS_S, CS_D, CS_A	Input Logic = 1	-	-	2.0	V
V_{IL}		Input Logic = 0	0.8	-	-	V
V_{HYS}		-	100	-	400	mV
I_{LKG}	Input leakage current MOSI, MOSI_A, SCLK, SCLK_A	$V_{IN} = V_{DD}$	-	-	1	μ A
		$V_{IN} = 0$ to V_{IH}	-1	-	-	μ A
I_{PD}	Input pulldown current CS_S, CS_D, CS_A	$V_{IN} = V_{IL}$ to V_{DD}	10	-	50	μ A
V_{OH}	Output voltage MISO, MISO_A, MSG	$I_{OH} = -800$ μ A	$V_{DD}-0.8$	-	-	V
V_{OL}		$I_{OL} = 1.6$ mA	-	-	0.4	V
I_{HI_Z}	Tri-state current MISO, MISO_A,	MISO = VDD	-	-	1	μ A
		MISO = 0 V	-1	-	-	μ A

1. V_{RST} shall have a POR de-glitch timer.

2. V_{RST_L} shall have no timer.

$V_{RES} = 6.5$ to 40 V, $V_{DD} = 4.9$ to 5.1 V, $V_{8BUCK} = 7.0$ V to 8.5 V, $T_{amb} = -40$ °C to $+95$ °C.

Table 7. DC specification: deployment drivers

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Units
V_{OH}	Output voltage AOUT	High Saturation Voltage; $I_{AOUT} = -500\mu A$	$V_{DD} - 0.4$	-	-	V
V_{OL}		Low Saturation Voltage; $I_{AOUT} = +500\mu A$	-	-	0.3	V
I_Z	Tri-state current AOUT	$AOUT = V_{DD}$	-	-	1	μA
		$AOUT = 0V$	-1	-	-	μA
I_{LKG}	Leakage current SQH	$V_{8BUCK} = V_{DD} = 0$, $V_{RES} = 36$ V, $V_{SQH} = 0$ V	-	-	50	μA
I_{STG}		$V_{8BUCK} = 18$ V; $V_{DD} = 5$ V; $V_{SQH} = -0.3$ V	-5	-	-	mA
I_{LKG}	Bias current $V_{RES}^{(1)}$	$V_{8BUCK} = 18$ V; $V_{DD} = 5$ V; $V_{RES} = 36$ V; SQH shorted to SQL	-	-	10	μA
I_{LKG}	Leakage current SQL	$V_{8BUCK} = V_{DD} = 0$, $V_{SQL} = 18$ V	-10	-	10	μA
I_{STG}		$V_{8BUCK} = 18$ V; $V_{DD} = 5$ V; $V_{SQL} = -0.3$ V	-5	-	-	mA
I_{STB}		$V_{8BUCK} = 18$ V; $V_{DD} = 5$ V; $V_{SQL} = 18$ V	-	-	5	mA
I_{PD}	Pull-down current SQL	$V_{SQL} = 1.8$ V to V_{DD}	900	-	1300	μA
I_{PD_SQH}	Pull-down current SQH	$V_{SQH} = SBTH$ to V_{RES}	900	-	1300	μA
V_{BIAS}	Diagnostics bias voltage	$I_{SQH} = -1.5$ mA (nominal: 2.0 V)	1.80	-	2.20	V
I_{BIAS}	Diagnostics bias current	$V_{SQH} = 0V$	-7	-	-	I_{PD}
V_{STB}	Short to battery threshold	(Nominal 3.0 V)	2.70	-	3.30	V
V_{STG}	Short to ground threshold	(Nominal 1.0 V)	0.90	-	1.10	V
V_{L_th}	MOS test load voltage detection	-	100	-	300	mV
I_{SRC}	Resistance measurement current source	$V_{DD} = 5.0$ V; $V_{8BUCK} = 7.0$ V to 26.5 V	38	-	42	mA
I_{SINK}	Resistance measurement current sink	-	45	-	55	mA
R_{DSon}	Total high and low-side MOS On resistance	High-side MOS + Low-side MOS $V_{RES} = 6.9$ V; $I = 1.2$ A @95 °C	-	-	2.0	Ω
R_{DSon}	High-side MOS on resistance	$V_{RES} = 35$ V; $I_{VRES} = 1.2$ A; $T_{amb} = 95$ °C	-	-	0.8	Ω
R_{DSon}	Low-side MOS on resistance	$V_{RES} = 35$ V; $I_{VRES} = 1.2$ A; $T_{amb} = 95$ °C	-	-	1.2	Ω
I_{DEPL_12A}	Deployment current	MOSI Register mode bit D10="0" $R_{LOAD} = 1.7$ Ω ; $V_{RES} = 6.9$ to 35 V	1.20	-	1.47	A
I_{DEPL_175A}		MOSI Register mode Bit D10="1" $R_{LOAD} = 1.7$ Ω ; ; $V_{RES} = 12$ to 35 V	1.75	-	2.14	A
I_{LIM}	Low-side MOS current limit	$R_{LOAD} = 1.75$ Ω	2.15	-	3.5	A
R_{L_RANGE}	Load resistance range ⁽²⁾		0	-	10.0	Ω

1. Not applicable during a diagnostic.

2. Test conditions for load resistance measurements

$V_{DD} = 4.9$ to 5.1 V, $V_{8BUCK} = 7.0$ V to 8.5 V, $T_{amb} = -40$ °C to $+95$ °C.

Table 8. Satellite interface DC specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_Lim	Current limit	High-side short to -0.3 V	(-)75	-	(-)150	mA
		High-side short to Battery	-	-	5	mA
		V8BUCK =Vcc=0 measured @ V8BUCK	-	-	5	mA
Vhdp	High-side voltage drop	I=50 mA @105°C; V8BUCK=7.0V	-	-	1	V
		I=25 mA @105°C; V8BUCK=7.0V	-	-	0.5	V
Itr	Low to high transition current threshold	SPI channel configuration				
		Bit <2:0>≥111	54.00	-	66.00	mA
		Bit <2:0>≥110	43.65	-	53.35	mA
		Bit <2:0>≥101	35.10	-	42.90	mA
		Bit <2:0>≥100	28.80	-	34.20	mA
		Bit <2:0>≥011	24.85	-	29.15	mA
		Bit <2:0>≥010	20.25	-	24.75	mA
		Bit <2:0>≥001	17.10	-	20.90	mA
		Bit <2:0>≥000	14.85	-	18.15	mA
Ihyst	Current threshold hysteresis	Sink current = Ithr at the output (ICHX). Ihyst=trip point high – trip point low	0.05*Itr	-	0.15*Itr	mA
Vos	Short to BAT feedback current	V(ICHX)-V8BUCK<50 mV	-	-	25	mA
Olkg	Output leakage current ICH _X	V=18 V @ pin under test	-	-	1	μA

3.3.2 AC characteristics

$V_{RES} = 6.5$ to 35 V, $V_{DD} = 4.9$ to 5.1 V, $V_{8BUCK} = 7.0$ V to 8.5 V, $T_{amb} = -40$ °C to $+95$ °C.

Table 9. AC specification: deployment drivers

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{POR}	POR de-glitch timer	Timer for V_{RST}	10	-	25	μ s
T_{GLITCH}	De-glitch timer	-	5	-	20	μ s
I_{ON}	Diagnostic current	DEPEN pins asserted ; Measured at 150μ s from falling edge CS_D or CS_A; See Figure 4	0.90	-		I_{FINAL}
t_{PULSE}	Pulse stretch timer	See Table 17	0	-	60	ms
t_{P_ACC}	Pulse stretch timer accuracy	-	-20	-	20	%
$t_{DEPLOY-2ms}$	Deployment time	$V_{RES} = 6.9$ to 35 V ⁽¹⁾	2	-	2.5	ms
$t_{DEPLOY-1ms}$	Deployment time	$V_{RES} = 12$ to 35 V ⁽¹⁾	1	-	1.25	ms
t_{FLT_DLY}	Fault detection filter ⁽²⁾	-	10	-	50	μ s
I_{SLEW}	Rmeas current di/dt	10 % - 90 % of I_{SRC}	2	-	8	mA/ μ s
t_{R_DLY}	Rmeas current delay	From the falling edge of CS to 10% of I_{SRC}		-	15	μ s
t_{R_WAIT}	Rmeas wait time ⁽²⁾	Wait time before AOUT voltage is stable for ADC reading	-	-	100	μ s
$t_{TIMEOUT}$	MOS diagnostic on-time	-	-	-	2.5	ms
t_{ILIM}	SQL high current protection timer	-	90	-	110	μ s
t_{PROP_DLY}	LS/HS MOS turn off propagation delay ⁽²⁾	Time is measured from the valid LS/HS MOS fault to the LS/HS turn off	-	-	10	μ s

1. Application Information; Test is not performed at high voltage.

2. Design Information Only

Figure 3. MOS settling time and turn-on time 1

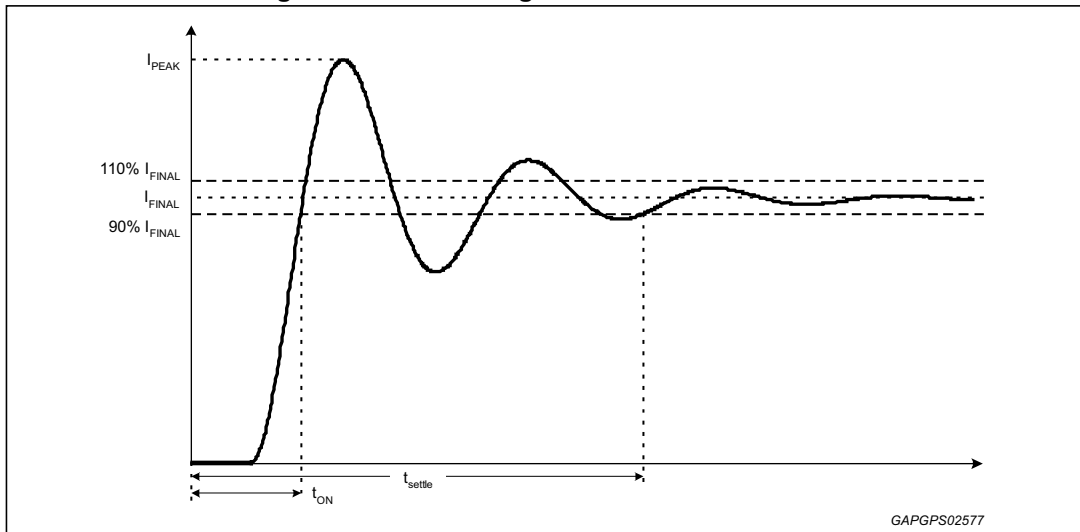
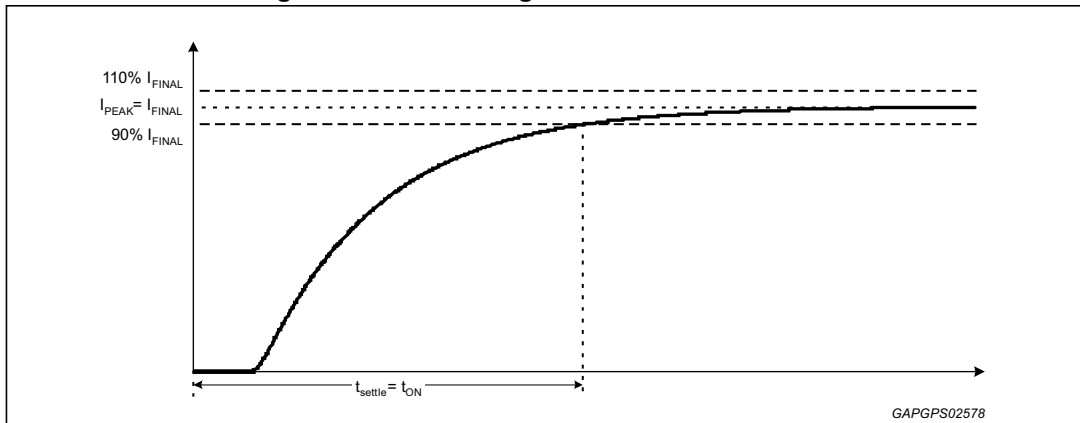


Figure 4. MOS settling time and turn-on time 2



$$V_{DD} = 4.9 \text{ to } 5.1 \text{ V}; V_{8BUCK} = 7.0 \text{ V to } 8.5 \text{ V}, T_{amb} = -40 \text{ }^{\circ}\text{C to } +95 \text{ }^{\circ}\text{C}$$

Table 10. AC specifications: satellite

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Osc	Internal oscillator frequency	Tested with 12.5 K 1% Iref resistor	4.45	-	5.55	MHz
Mdf	De-glitch filter as a function of protocol speed	Manchester Protocol Excluding Osc tolerance Bit<8:7> 00 Bit<8:7> 01 Bit<8:7> 10 Bit<8:7> 11	11.76 %*Bit- Time	-	23.53 % *Bit- Time	μs
Bitr	Minimum frequency operating range (Incoming messages fall within this operating range is guaranteed to be accepted by the IC)	Channel configurations				
		Bit<8:7> 00 Test at frq = 52.33 kHz Test at frq = 13.32 kHz	13.32	-	52.33	kHz
		Bit<8:7> 01 Test at frq = 110.74 kHz Test at frq = 26.32 kHz	26.32	-	110.74	kHz
		Bit<8:7> 10 Test at frq = 164.20 kHz Test at frq = 43.50 kHz	43.50	-	164.20	kHz
		Bit<8:7> 11 Test at frq = 250.63 kHz Test at frq = 62.66 kHz	62.66	-	250.63	kHz
Bitr	Maximum frequency operating range (Incoming messages fall outside this operating range is guaranteed to be rejected by the IC)	Channel configurations				
		Bit<8:7> 00 Test at frq > 59.14 kHz Test at frq < 11.99 kHz	11.99	-	59.14	kHz
		Bit<8:7> 01 Test at frq > 128.37 kHz Test at frq < 23.57 kHz	23.57	-	128.37	kHz
		Bit<8:7> 10 Test at frq > 194.93 kHz Test at frq < 38.71 kHz	38.71	-	194.93	kHz
		Bit<8:7> 11 Test at frq > 309.6 kHz Test at frq < 55.37 kHz	55.37	-	309.6	kHz
Idle	Idle time	Manchester	2	-		Bit Times
Fit	Output fault timer	I_sensor > I_lim	300	-	500	μs

$V_{RES} = 6.5$ to 35 V, $V_{DD} = 4.9$ to 5.1 V. $V_{8BUCK} = 7.0$ V to 8.5 V, $T_{amb} = -40$ °C to $+95$ °C
 All SPI timing is performed with a 200 pF load on MISO unless otherwise noted.

Table 11. SPI timing

No.	Symbol	Parameter	Min	Typ	Max	Unit
-	fop	Transfer frequency	dc	-	5.50	MHz
1	t _{SCK}	SCLK, SCLK_A Period	181	-	-	ns
2	t _{LEAD}	Enable Lead Time	65	-	-	ns
3	t _{LAG}	Enable Lag Time	50	-	-	ns
4	t _{SCLKHS}	SCLK, SCLK_A High Time	65	-	-	ns
5	t _{SCLKLS}	SCLK, SCLK_A Low Time	65	-	-	ns
6	t _{SUS}	MOSI, MOSI_A Input Setup Time	20	-	-	ns
7	t _{HS}	MOSI, MOSI_A Input Hold Time	20	-	-	ns
8	t _A	MISO, MISO_A Access Time	-	-	60	ns
9	t _{DIS}	MISO, MISO_A Disable Time ⁽¹⁾	-	-	100	ns
10	t _{VS}	MISO, MISO_A Output Valid Time	-	-	66	ns
11	t _{HO}	MISO, MISO_A Output Hold Time ⁽¹⁾	0	-	-	ns
12	t _{RO}	Rise Time (Design Information)	-	-	30	ns
13	t _{FO}	Fall Time (Design Information)	-	-	30	ns
14	t _{CSN}	CS_A, CS_D, CS_S Negated Time	640	-	-	ns

1. Parameters t_{DIS} and t_{HO} shall be measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 5. SPI timing diagram

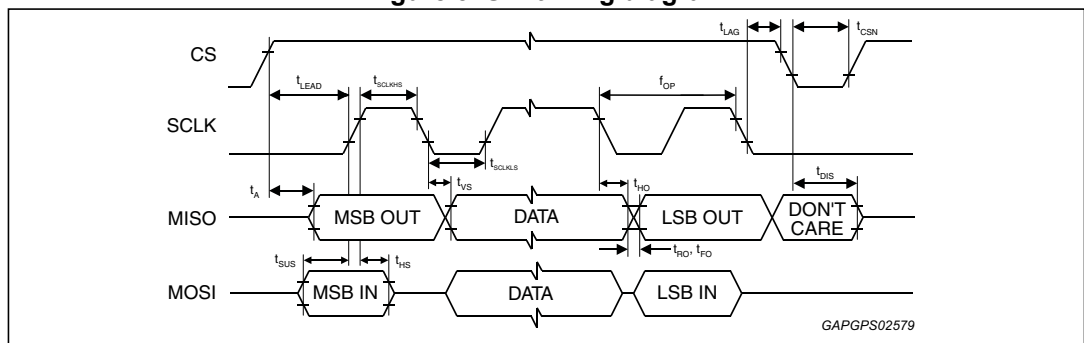
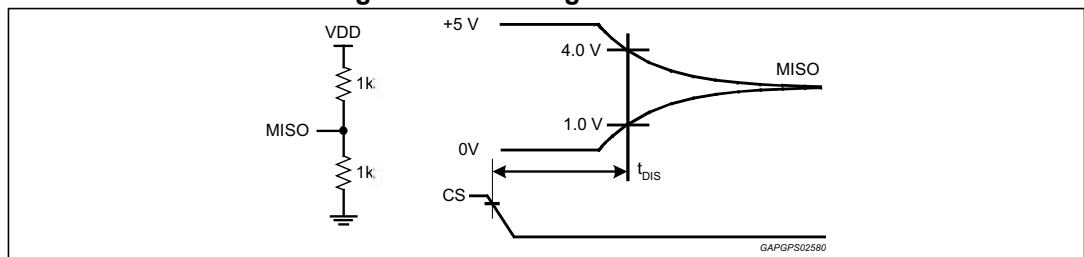


Figure 6. SPI timing measurement



4 Functional description

4.1 Overview

L9654 is an integrated circuit to be used in air bag systems. Its main functions include deployment of air bags, switched-power sources to satellite sensors, diagnostics of SDM (Sensing Deployment Module) and arming inputs. L9654 supports 4 deployment loops, 2 satellite-sensor interfaces, and SPI arming inputs.

4.2 Power on reset (POR)

L9654 has a power on reset (POR) circuit, which monitors V_{DD} voltage. When V_{DD} voltage falls below V_{RST} for longer than or equal to t_{POR} , all outputs are disabled and all internal registers are reset to their default condition.

When V_{DD} falls below V_{RST_L} , all outputs are disabled and all internal registers are reset to their default condition. No delay filter shall be used along with V_{RST_L} threshold.

If V_{DD} voltage falls below V_{RST} for less than t_{POR} , operation shall not be interrupted.

When V_{DD} rises above V_{RST} , the outputs are enabled. Before V_{DD} reaches V_{RST} , and during t_{POR} , none of the outputs turn on.

4.3 RESETB

RESETB pin is active low. The effects of RESETB are similar to those of a POR event, except during a deployment. When L9654 has a deployment in-progress, it ignores the RESETB signal.

However, it shall shut itself down as soon as it detects a POR condition. When the deployment is completed and the RESETB signal is asserted, the device disables its outputs and resets its internal registers to their default states.

A de-glitch timer is provided to the RESETB pin. The timer protects this pin against spurious glitches. UT48 neglects the RESETB signal if it is asserted for shorter than t_{GLITCH} . RESETB has an internal pull-up in case of open circuit. This pin has a de-glitch timer.

4.4 MSG

MSG pin is used to reflect the FIFO status. Its polarity can be configured as well as the strategy of activation.

Polling mode: Message pin shall be active as soon as one of the 4 FIFO is not empty and becomes inactive when all 4 FIFO are empty. A microcontroller can periodically monitor the status of line to understand if there are data received from satellite.

Interrupt mode: Message pin shall be active as soon one of the 4 FIFO is not empty and becomes inactive when an SPI communication on CS_S interface starts. At the end of the SPI communication it shall be active if one of the 4 FIFO is not empty, otherwise it shall be kept inactive. A microcontroller can wait until an edge is present on the line and manage the data available in the FIFO.

4.5 IREF

I_{REF} pin shall be connected to V_{DD} supply through a resistor, R_{IREF}. When the device detects the resistor on I_{REF} pin is larger than R_{IREF_H} or smaller than R_{IREF_L}, it goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

4.6 Loss of ground

When GND pin is disconnected from PC-board ground, L9654 goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions. A loss of power-ground (GND0 – GND3) pin/s disables the respective channel/s. In other words, the channel that loses its power ground connection is not able to deploy. The rest of the device is not affected by a loss of power-ground condition.

A_{OUT_GND} pin is a reference for A_{OUT} pin. When A_{OUT_GND} loses its connection the reset loses it as well.

4.7 Deployment and reset

The following conditions reset and terminate deployments:

- Power On Reset (POR)
- IREF resistance is larger than R_{IREF_H} or smaller than R_{IREF_L}
- Loss of ground condition on GND pin

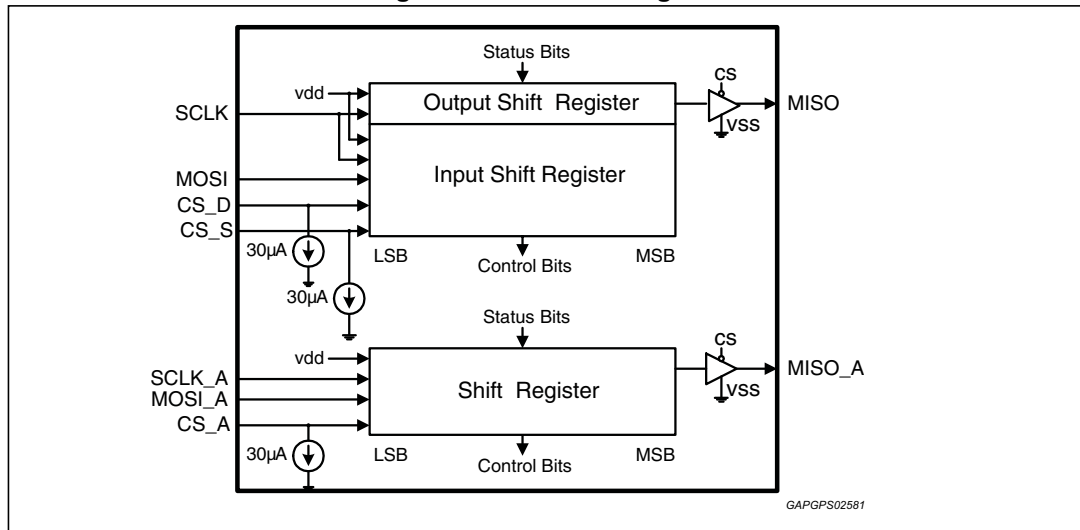
The following conditions are ignored when there is a deployment in-progress:

- RESETB
- Valid soft reset sequences

4.8 Serial peripheral interface (SPI)

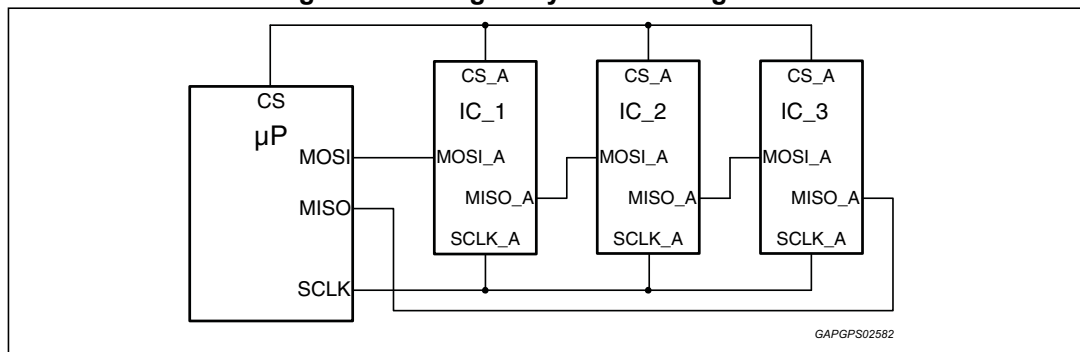
The device contains a serial peripheral interface consisting of Serial Clock (SCLK, SCLK_A), Serial Data Out (MISO, MISO_A), Serial Data In (MOSI, MOSI_A), and two Chip Selects (CS_A, CS_D and CS_S). This device is configured as an SPI slave. The idle state of the communication, Serial Clock (SCLK, SCLK_A) should be in low state.

Figure 7. SPI block diagram



L9654 has a counter to verify the number of clocks in SCLK and SCLK_A. If the number of clocks in SCLK is not equal to 16 clocks while CS_D is asserted, it ignores the SPI message and sends an SPI fault response. If the number of clocks in SCLK is not equal to 64 clocks while CS_S is asserted, it ignores the entire SPI message and pushes the Bad SPI Bit Count fault code into the FIFO. If the number of clocks in SCLK_A is not a multiple of 8, it ignores the command in the arming shift register. Otherwise, the device latches-in the command.

Figure 8. Arming daisy-chain configuration



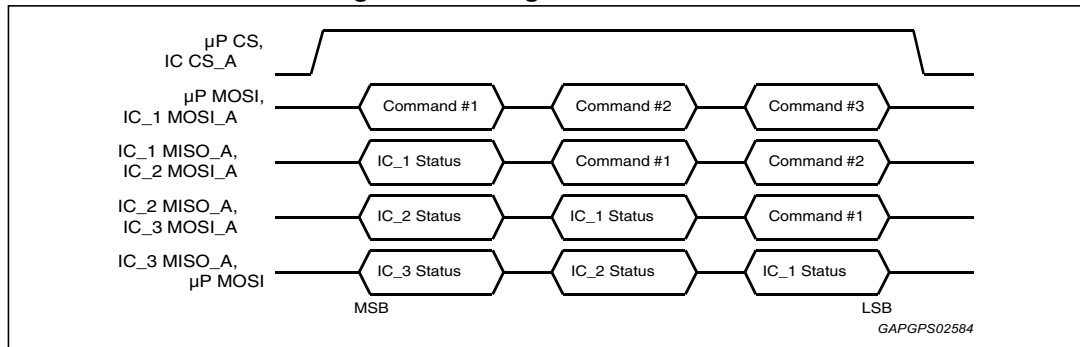
Arming SPI interface is based on 8-bit data transfer. The device is capable of receiving a multiple of 8-bit commands. The first byte of data coming out of MISO_A is the arming status bits. The subsequent bits are the arming command bits received through MOSI_A pin. Refer to below figure for an example of arming SPI transmission. This is an example of arming SPI transmission based on the daisy-chain configuration.

In case of daisy chain connection for arming SPI, device works as following:

All devices IC_1, IC_2, IC_3 shift out data on the falling edge of SCLK_A for the first 8 bits and shift out data on the rising edge of SCLK_A for the bits after 8 bits. Therefore µP, IC_3, IC_2 strobe 24 bits on rising edge of SCLK_A:

- the first 8 bits are produced (by IC_3, IC_2, IC_1 respectively) on the falling edge of SCLK_A.
- the remaining 16 bits are shifted out on the rising edge.

Figure 9. Arming SPI transmission



4.8.1 Chip select (CS_A, CS_D, CS_S)

Chip-select inputs select L9654 for serial transfers. CS_A is independent of CS_D and CS_S.

CS_A can be asserted regardless of CS_D and CS_S. However, either CS_D or CS_S can be asserted at any given time. If both CS_D and CS_S inputs are selected simultaneously, the device ignores MOSI command. When chip-select is asserted, the respective MISO/MISO_A pin is released from tri-state mode, and all status information is latched in the SPI shift register. While chip-select is asserted, register data is shifted into MOSI/MOSI_A pin and shifted out of MISO/MISO_A pin on each subsequent SCLK/SCLK_A. When chip-select is negated, MISO/MISO_A pin is tri-stated. To allow sufficient time to reload the registers, chip-select pin shall remain negated for at least t_{CSN} .

Chip-select is also immune to spurious pulses of 50 ns or shorter (MISO/MISO_A may come out of tri-state, but no status bits are cleared and no control bits are changed).

Chip-select inputs have current sinks on the pins, which pull these pins to the negated state when an open circuit condition occurs. These pins have TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

4.8.2 Serial clock (SCLK, SCLK_A)

SCLK/SCLK_A input is the clock signal input for synchronization of serial data transfer. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply. When chip select is asserted, both the SPI master and this device shall latch input data on the rising edge of SCLK/SCLK_A. L9654 shift data out on the falling edge of SCLK/SCLK_A. The SCLK/SCLK_A must be taken in idle state (LOW) when the CS_A, CS_D, CS_S are in idle state (LOW).^(a)

4.8.3 Serial data output (MISO, MISO_A)

MISO/MISO_A output pin shall be in a tri-state condition when chip select is negated. When chip select is asserted, the MSB is the first bit of the word/byte transmitted on MISO/MISO_A and the LSB is the last bit of the word/byte transmitted. This pin supplies a rail to rail output, so if interfaced to a microprocessor that is using a lower VDD supply, the appropriate microprocessor input pin shall not sink more than $I_{\text{OH}(\text{min})}$ and shall not clamp the MISO/MISO_A output voltage to less than $V_{\text{OH}(\text{min})}$ while MISO/MISO_A pin is in a logic "1" state.

a. Only in daisy chain, it is needed to guarantee on SCLK_A a clock skew of 3ns maximum between any devices.

4.8.4 Serial data input (MOSI, MOSI_A)

MOSI/MOSI_A input takes data from the master processor while chip select is asserted.

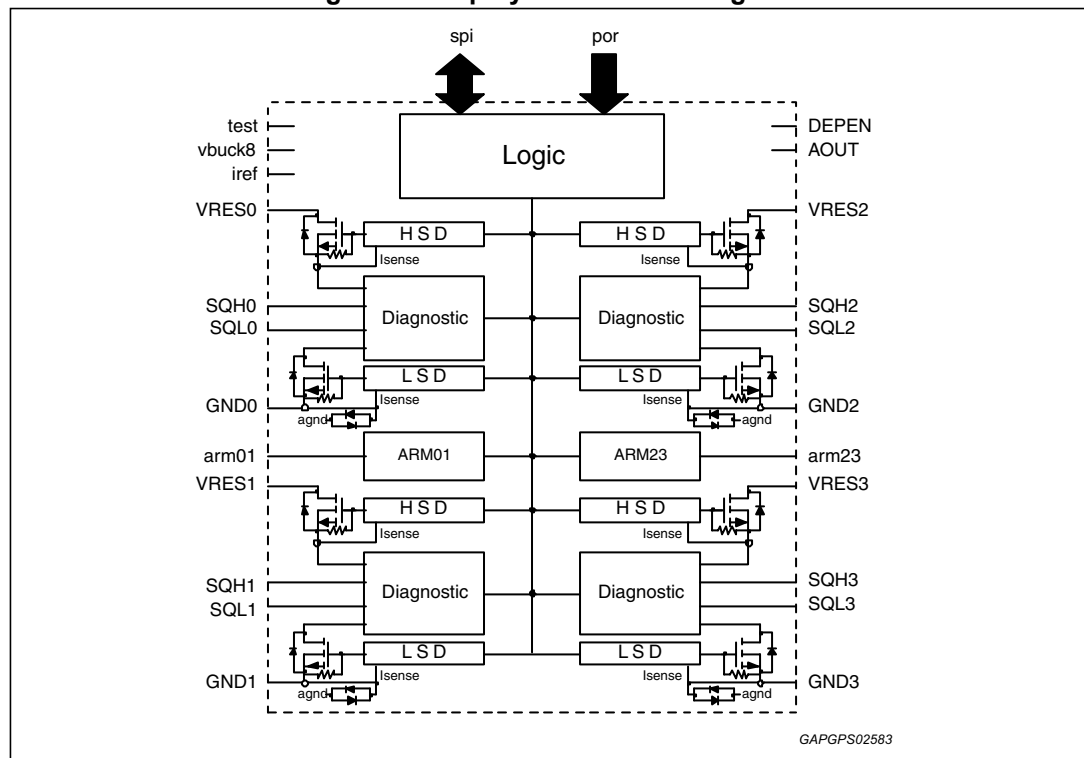
The MSB shall be the first bit of each word/byte received on MOSI/MOSI_A and the LSB shall be the last bit of each word/byte received. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

4.9 Deployment drivers

The on-chip deployment drivers are designed to deliver 1.2 A (min.) at 6.9 V VRES. Deployment current is 1.2 A (min.) for 2 ms (min.). The high-side driver survives deployment with 1.47 A, 35 V at VRES and SQL is shorted to ground for 2.5 ms. Minimum load resistance is 1.7. At the end of a deployment, a deploy success flag is asserted via SPI. Each VRES and GND connection are used to accommodate 4 loops that can be deployed simultaneously.

Upon receiving a valid deployment condition, the respective SQH and SQL drivers are turned on. SQH and SQL drivers are also turned on momentarily during a MOS diagnostic. Otherwise, SQH and SQL are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQH and SQL drivers, a deploy command success flag is asserted via SPI. Refer to "deployment sequence" *Figure 10* for the valid condition and the deploy success flag timing.

Figure 10. Deployment drivers diagram



The following power-up conditions are considered as normal operations . VRES input can be connected to either a power supply output or an ignition voltage. VDD is connected to 5 V output of power supply. When VRES is connected to the power supply, VDD voltage

reaches its regulation voltage before VRES voltage is stabilized. In this condition, the device has the control of its internal logic and that prevents an inadvertent turn-on of the drivers.

When VRES is connected to the ignition, VRES voltage is stabilized before VDD reaches its regulation voltage. In this condition, all drivers are inactive. A pull-down on the gates of high-side drivers (SQH) is provided to prevent these drivers from momentarily turning-on. Any loop driver fault conditions do not turn on the SQH and SQL drivers. Only a valid deployment condition can turn on the respective SQH and SQL drivers.

4.9.1 Arming interface

The arming interface is used as a fail-safe to prevent inadvertent airbag deployment. Along with deployment command, these signals provide redundancy. Pulse stretch timer is provided for each channel/loop. Either ARM signal or deployment command shall start the pulse stretch timer.

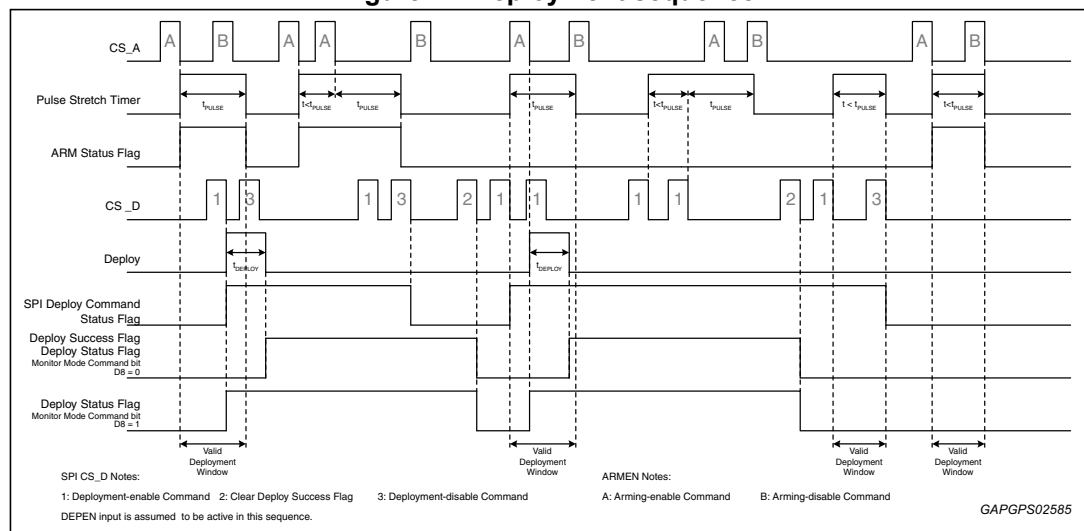
Arming interface has a dedicated 8-bit SPI interface.

When CS_A is negated, L9654 latches ARM signal from the shift register and starts the pulse stretch timer for the respective channel/s. The device can deploy a channel, ONLY when DEPEND is asserted and any of the following conditions are satisfied:

- the respective deployment command is sent during a valid pulse stretch timer, which is initiated by ARM signal
- the respective SPI ARM command is sent during a valid pulse stretch timer, which is initiated by deployment command

During a deployment, the device turns on the respective high-side (SQH) and low-side (SQL) drivers for duration of t_{DEPLOY} . When a deployment is initiated, it can't be terminated, except during a reset event.

Figure 11. Deployment sequence

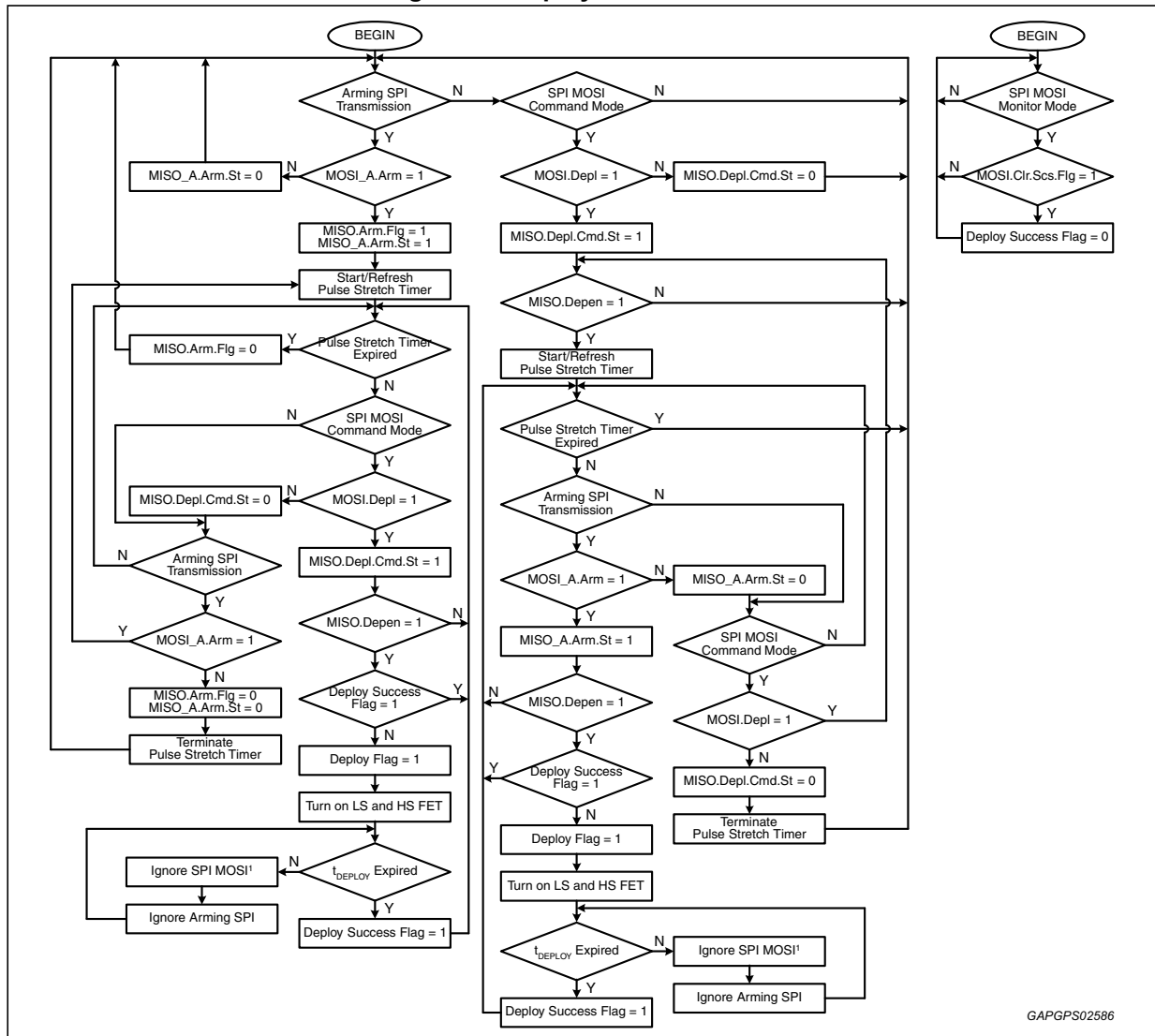


When a deployment-enable command is sent through SPI, the pulse stretcher shall be initiated immediately following the falling edge of CS_D. When another deployment-enable command is sent before the timer for the previous command expired, the timer is refreshed. Sending a deployment-disable command terminates the pulse stretch timer operation. ONLY a timer operation started by a deployment-enable command can be terminated.

A deployment-en/disable command does not affect the timer operation started by arming signal.

When an arming-enable command is sent through SPI, the pulse stretcher is initiated immediately following the falling edge of CS_A. When another arming-enable command is sent before the timer for the previous command expired, the timer is refreshed. Sending an arming disable command terminate the pulse stretch timer operation. ONLY a timer operation started by an arming-enable command can be terminated. An arming-en/disable command does not affect the timer operation started by a valid deployment command.

Figure 12. Deployment flow chart



1. MOSI Register Mode: ignored. Next MISO: SPI fault response
 MOSI Command Mode: execute for channels NOT in deployment, NO effect to deploying channel. Next MISO: Command mode response
 MOSI Diagnostic Mode: ignored. Next MISO: SPI fault response
 MOSI Monitor Mode: execute for all channels. Next MISO: Status response

During the deployment, L9654 turns on the respective high (SQH) and low-side (SQL) drivers for t_{DEPLOY} . Once deployment is initiated it cannot be terminated. When a channel is in deployment, this particular channel shall only act upon certain SPI messages. These SPI

messages and their responses are summarized in the below table. The rest of the channels shall resume their operations and respond to specific SPI commands.

During a deployment, the device ignores arming commands. and does not refresh or terminate the pulse stretch timer when it receives an arming command.

Table 12. SPI transmission during a deployment

SPI MOSI	SPI MISO ⁽¹⁾	Notes
Register mode	SPI fault response	MOSI register mode message shall be ignored
Command mode	Command mode	Execute for channels not in deployment; no effect to deploying channel
Diagnostic mode	SPI fault response	MOSI diagnostic mode message shall be ignored
Monitor mode	Status response	Execute for all channels

1. SPI MISO sent in the next SPI transmission.

4.10 DEPEN

DEPEN is a deployment enable input, which is an active high input. When this pin is asserted, L9654 is able to turn on its high and low-side drivers upon receiving a valid deployment command or a MOS diagnostic request. DEPEN cannot interrupt a deployment that is already in-progress.

When DEPEN is negated, it inhibits the low-side and the high-side MOS from turning on (inhibit the deployment). When a MOS diagnostic is requested, the device executes the diagnostic even without the ability to turn on the MOS. It sets the proper SPI threshold bits. SPI remains functional while this pin is pulled low.

When DEPEN is negated, SPI deploy command is prevented from initiating the pulse stretch timer. Regardless of DEPEN, "SPI deploy command" status bits reports the state of "SPI deploy command" bits sent in the previous SPI transfer. This feature is required so that the processor can diagnose SPI deploy command bits with DEPEN negated.

Regardless of DEPEN, arming signal is able to initiate the pulse stretch timer. This feature is used for the processor to diagnose the arming signal.

When the pulse stretch timer has been running, changes in the state of DEPEN do not affect the pulse stretch timer. The pulse stretch timer is not affected regardless of the pulse stretch timer being started by an arming signal or an SPI deploy command.

A de-glitch timer is provided to DEPEN pin. The timer protects this pin against spurious glitches. The device neglects DEPEN signal if it is asserted/negated for shorter than t_{GLITCH} .