Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

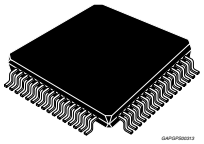
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

L9660

Quad squib driver ASIC for safety application

Datasheet - production data



LQFP64 (10x10x1.4mm)

Features

- 4 deployment drivers with SPI selectable firing current and times
- Capability to deploy the squib with 1.2 A (min)/2 ms, 1.75 A (min)/1.0 ms and 1.75 A (min)/0.65 ms between VRES of 7 V to 37 V
- Capability to deploy the squib with 1.5 A (min)/2 ms between VRES of 7 V to 25 V
- Firing capability to deploy all channels simultaneously
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance measurement
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib when the low side MOS is shorted to ground
- 2 fire enable inputs
- 5.5 MHz SPI interface
- Low voltage internal reset
- 2 kV ESD capability on all pins
- Package: LQFP64
- Technology: ST proprietary BCD5 (0.65µm)
- RoHS compliant

Description

The L9660 is intended to deploy up to 4 squibs. Squib drivers are sized to deploy 1.2 A minimum for 2 ms, 1.75 A minimum for 1 ms and 1.75 A minimum for 0.65 ms during load dump along with 1.5 A minimum for 2 ms for VRES voltages less than 25 V.

Full diagnostic capabilities of the squib interface are provided.

Table 1. Device summary

Order code	Amb. temp range, °C	Package	Packing
L9660	-40 to +95	LQFP64	Tray
L9660TR	-40 to +95	LQFP64	Tape and reel

Contents

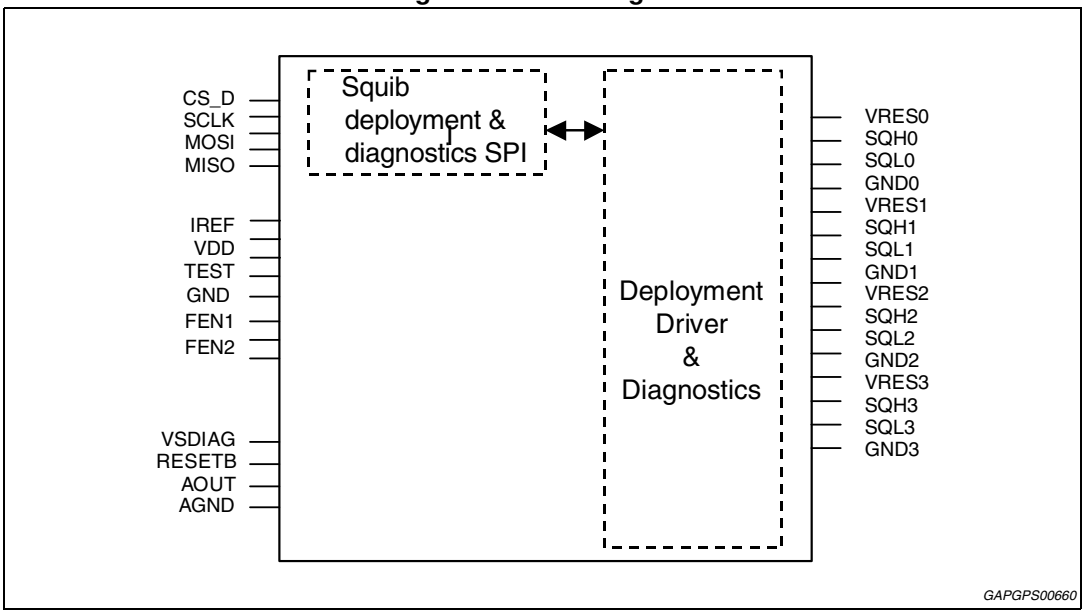
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Table 2. Pin description

Pin Number	Pin name	Description	I/O type	Reset state
1	MISO	SPI Data Out	Output	Hi-Z
2	N.C.	Not connected	-	-
3	FEN1	Fire enable for channels 0 and 1	Input	Pull-down
4	N.C.	Not connected	-	-
5	RESETB	Reset pin	Input	Pull-up
6	GND	Ground (Analog & Digital)	-	-
7	VDD	VDD Supply Voltage	Input	-
8	N.C.	Not connected	-	-
9	FEN2	Fire enable for channels 2 and 3	Input	Pull-down
10	N.C.	Not connected	-	-
11	N.C.	Not connected	-	-
12	CS_D	SPI Chip Select for Deployment Driver	Input	Pull-up
13	MOSI	SPI Data In	Input	Hi-Z
14	N.C.	Not connected	-	-

Table 2. Pin description (continued)

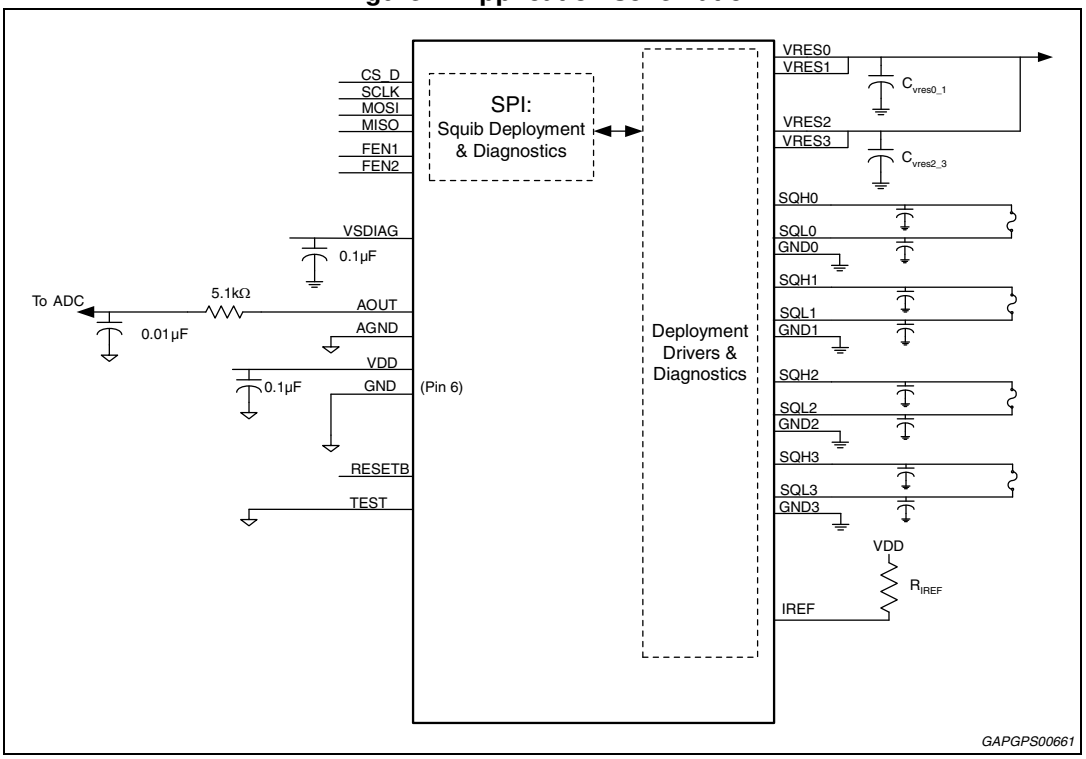
Pin Number	Pin name	Description	I/O type	Reset state
15	N.C.	Not connected	-	-
16	SCLK	SPI Clock	Input	Hi-Z
17	N.C.	Not connected	-	-
18	N.C.	Not connected	-	-
19	N.C.	Not connected	-	-
20	N.C.	Not connected	-	-
21	N.C.	Not connected	-	-
22	N.C.	Not connected	-	-
23	N.C.	Not connected	-	-
24	N.C.	Not connected	-	-
25	GND2	Power Ground for Loop Channel 2	-	-
26	SQL2	Low Side Driver Output for Channel 2	Output	Pull-down
27	SQH2	High Side Driver Output for Channel 2	Output	Hi-Z
28	VRES2	Reserve Voltage for Loop Channel 2	Input	-
29	VRES3	Reserve Voltage for Loop Channel 3	Input	-
30	SQH3	High Side Driver Output for Channel 3	Output	Hi-Z
31	SQL3	Low Side Driver Output for Channel 3	Output	Pull-down
32	GND3	Power Ground for Loop Channel 3	-	-
33	TEST	Test pin	Input	Pull-down
34	VSDIAG	Supply for Deployment Driver Diagnostics	Input	-
35	N.C.	Not connected	-	-
36	Reserved	Factory testmode output	-	-
37	Reserved	Factory testmode output	-	-
38	N.C.	Not connected	-	-
39	N.C.	Not connected	-	-
40	N.C.	Not connected	-	-
41	N.C.	Not connected	-	-
42	N.C.	Not connected	-	-
43	N.C.	Not connected	-	-
44	N.C.	Not connected	-	-
45	N.C.	Not connected	-	-
46	IREF	External Current Reference Resistor	Output	-
47	AGND	Ground Reference for AOUT	-	-
48	AOUT	Analog Output for Loop Diagnostics	Output	Hi-Z
49	N.C.	Not connected	-	-

Table 2. Pin description (continued)

Pin Number	Pin name	Description	I/O type	Reset state
50	N.C.	Not connected	-	-
51	N.C.	Not connected	-	-
52	N.C.	Not connected	-	-
53	N.C.	Not connected	-	-
54	N.C.	Not connected	-	-
55	N.C.	Not connected	-	-
56	N.C.	Not connected	-	-
57	GND1	Power Ground for Loop Channel 1	-	-
58	SQL1	Low Side Driver Output for Channel 1	Output	Pull-down
59	SQH1	High Side Driver Output for Channel 1	Output	Hi-Z
60	VRES1	Reserve Voltage for Loop Channel 1	Input	-
61	VRES0	Reserve Voltage for Loop Channel 0	Input	-
62	SQH0	High Side Driver Output for Channel 0	Output	Hi-Z
63	SQL0	Low Side Driver Output for Channel 0	Output	Pull-down
64	GND0	Power Ground for Loop Channel 0	-	-

1.3 Application schematic

Figure 2. Application schematic



2 Electrical specifications

2.1 Absolute maximum ratings

The following maximum ratings are continuous absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD} (1)	Supply voltage	- 0.3 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	- 0.3 to 40	V
VRESx	VRES voltage (VRES0, VRES1, VRES2, VRES3)	- 0.3 to 40	V
SQHx	Squib high side drivers (SQH0, SQH1, SQH2, SQH3)	- 0.6 to 40	V
SQLx	Squib low side drivers (SQL0, SQL1, SQL2, SQL3)	- 0.3 to 40	V
TEST	Test pin	-0.3 to 40	V
V_I	Discrete input voltage (RESETB, CS_D, SCLK, MOSI, FEN1, FEN2, IREF)	- 0.3 to 5.5	V
V_O	Discrete output voltage (MISO, AOUT)	- 0.3 to 5.5	V
AGND	Analog output reference	-0.3 to 5.5	V
GNDx	Ground (GND0, GND1, GND2, GND3)	-0.3 to 5.5	V
T_j (2)	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance junction to ambient (on FR-4 board)	46	°C/W
The following maximum ratings are up to 48 hours; exceeding any one of these values for longer than a total time of 48 hours may cause permanent damage to the integrated circuit.			
V_{DD}	Supply voltage	- 0.3 to 6.0	V
V_I	Discrete input voltage (RESETB, CS_D, SCLK, MOSI, FEN1, FEN2, IREF)	- 0.3 to 6.0	V
V_O	Discrete output voltage (MISO, AOUT)	- 0.3 to 6.0	V
AGND	Analog output reference	-0.3 to 6.0	V
GNDx	Ground (GND0, GND1, GND2, GND6, GND7)	-0.3 to 6.0	V
T_j (2)	Maximum steady-state junction temperature	150	°C
T^{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance junction to ambient (on FR-4 board)	46	°C/W

1. Exceeding a V_{DD} of 5.1V during a deployment may cause damage
2. To allow for deployment the maximum steady state junction temperature cannot exceed 130°C. Under the operating ratings defined in *Section 2.3* the steady state junction temperature does not exceed 130°C.

2.2 Absolute maximum degraded operating ratings

Under the following deviations to the ratings indicated in *Section 2.3* the L9660 performance is degraded and not meeting the electrical characteristics outlined in *Section 2.4*. The SPI and diagnostics still function but not meet specified electrical parameters.

Table 4. Absolute maximum degraded operating ratings

Symbol	Parameter	Value	Unit
V_{DD} (1)	Supply voltage	4.5 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	7 to 40	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3)	7 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, SCLK, MOSI, FEN1, FEN2, IREF)	- 0.3 to (VDD +0.3)	V
V_O	Discrete output voltage (MISO, AOUT)	-0.3 to (VDD + 0.3)	V
T_j	Junction temperature	-40 to 150	°C

1. Exceeding a V_{DD} of 5.1V during a deployment may cause damage.

Note: The above is provided for informational purposes only and results in degraded operation. Under the above conditions the SPI is functional as well as diagnostics, though the electrical performance may not conform to the parameters outlined in Section 2.4. Firing requirements as indicated in Section 2.4 may not be met with the conditions above.

2.3 Operating ratings

Table 5. Operating ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.9 to 5.1	V
V_{SDIAG}	Supply voltage for squib diagnostics	7 to 37	V
V_{RESx}	VRES voltage (VRES0, VRES1, VRES2, VRES3,)	7 to 37	V
V_I	Discrete input voltage (RESETB, CS_D, SCLK, MOSI, FEN1, FEN2, IREF)	- 0.3 to (V_{DD} +0.3)	V
V_O	Discrete output voltage (MISO, AOUT)	-0.3 to (VDD + 0.3)	V
T_{amb}	Ambient temperature	-40 to 95	°C
$R_{Th\ j\text{-}amb}$	Thermal resistance junction to ambient (on FR-4 board)	46	°C/W

Comments:

VSDIAG supply provides power for squib resistance and HSS diagnostics

VDD is used for all internal functions as well as short to battery/ground and high squib resistance diagnostics.

2.4 Electrical characteristics

2.4.1 General

4.9 V ≤ V_{DD} ≤ 5.1 V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; FEN1 = FEN2 = V_{DD}; R_REF = 10 kΩ, ±1 %, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 6. General - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Osc	Internal oscillator frequency	Tested with 10K, 1%, 100ppm Iref resistor	4.75	-	5.25	MHz
V_{RST1}	Internal voltage reset VDD after de-glitch time (t_{POR}) See *Figure 6*	VDD level for L9660 to report reset condition -deployment drivers are disabled	4.0	-	4.5	V
V_{RST2}	Internal voltage reset VDD with no de-glitch time See *Figure 6*	Guaranteed by design	2.1	-	3.0	V
t_{POR}	POR De-glitch timer	Timer for VRST1	5	-	25	µs
I_{DD}	Input current VDD	No squib diagnostics. No deployment.	-	-	15	mA
		Resistance measurement diagnostics with no fault condition present.	-	-	17	
		Short to –0.3V on SQL; VRCM active	-	-	35	
		During deployment	-	-	15	
R_{IREF_H}	Resistance threshold IREF	-	-	-	60.0	kΩ
R_{IREF_L}		-	2.0	-	-	kΩ
V_{IH_RESETB}	Input voltage threshold RESETB	-	-	-	2.0	V
V_{IL_RESETB}		-	0.8	-	-	V
V_{HYS_RST}		-	100	-	300	mV
V_{IH_TEST}	Input voltage threshold TEST	Guaranteed by design	-	3.2	-	V
I_{TESTPD}	Input pull-down current TEST	-	1.0	-	2.5	mA
I_{AOUT_SHRT}	AOUT pin current limit	AOUT short to ground during squib resistance diagnostics	-	-	20	mA
$I_{RESETPU}$	Input pull-up current RESETB	RESETB = VIH to GND	-10	-	-50	µA
I_{RESx}	Quiescent current for VRESx during HSS test	Current per pin during HSS test excluding selected channel	-	-	10	µA
V_{IH}	Input voltage threshold (MOSI, SCLK, CS_D)	Input Logic = 1	-	-	2.0	V
V_{IL}		Input Logic = 0	0.8	-	-	V
V_{HYST}	Input hysteresis (MOSI, SCLK, CS_D)		100	-	300	mV

Table 6. General - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{LKGD}	Input leakage current MOSI, SCLK	VIN = VDD	-	-	1	µA
		VIN = 0 to VIH	-1	-	-	µA
I_{PU_CS}	Input pull-up current CS_D	VIN = VIH to GND	-10	-	-50	µA
V_{OH}	Output voltage MISO	IOH = -800µA	VDD–0.8	-	-	V
V_{OL}		IOL = 1.6mA	-	-	0.4	V
I_{HI_Z}	Tri-state current MISO	MISO = VDD	-	-	1	µA
		MISO = 0V	-1	-	-	µA

2.4.2 Electrical characteristics - Squib deployment drivers and diagnostics

4.9 V ≤ V_{DD} ≤ 5. 1V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; FEN1 = FEN2 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; C_VRES0_1 ≥ 68nF; C_VRES2_3 ≥ 68nF; unless other specified.

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
I_{LKGSQH}	Leakage current SQH	VSDIAG = VDD = 0, VRES = 37V, VSQH = 0V	-	-	50	µA
$I_{LKGVRES}$	Bias current VRESX	VSDIAG = 18V; VDD = 5V; VRES = 37V; SQH shorted to SQL	-	-	10	µA
I_{LKGSQL}	Leakage current SQL	VSDIAG = VDD = 0, VSQL = 18V	-10	-	10	µA
I_{PD}	Pull-down current SQL	VSQL = 1.5V to 20V	3.3	-	4.1	mA
V_{BIAS}	Diagnostics Bias voltage	Nominal 3.6V	-5%	VDD* 0.72	+5%	V
Short to battery/ground diagnostics - R_{sqb} from 0Ω to Open						
I_{SVRCM}	Maximum diagnostics bias current limit	Short to battery or ground test active VSQH = 0V	5	-	20	mA
R_{STB}	Short to battery resistance threshold	Vbatt = 6.5V	1.92	-	3.42	KΩ
		Vbatt = 16V	8.61	-	13.98	KΩ
		Vbatt = 20V	11.42	-	18.42	KΩ
I_{STB}	Short to battery current threshold	-	0.9	-	1.42	mA
R_{STG}	Short to ground threshold	-	1.07	-	2.1	KΩ
I_{STG}	Short to ground current threshold	-	1.8	-	3.2	mA

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until Test Results are Valid, Output voltage change 0V to VDD * 0.72 C_{SQHx}= 0.12µF C_{SQLx}= 0.12µF	-	-	300	µs
High side safing diagnostics						
I_{SRC_HSS}	Diagnostic current into selected VRESx pin during test	Normal conditions	710	-	950	µA
I_{HSS_4}	Current during diagnostic	All 4 VRESx pins tied together	710	-	1020	µA
$R_{HSSNORM\_th}$	Normal resistance range when running high side safing diagnostics	All 4 VRESx pins tied together	1.4	-	2.5	kΩ
$V_{HSSNORM\_range}$	Normal voltage range between VSDIAG and VRESx pin) when running high side safing diagnostics	All 4 VRESx pins tied together	1.0	-	2.5	V
$V_{HSSSHORT\_th}$	Short voltage threshold between VSDIAG and VRESx pin)	All 4 VRESx pins tied together	0.5	-	1.0	V
$V_{HSSOPEN\_th}$	Open voltage threshold between VSDIAG and VRESx pin)	All 4 VRESx pins tied together	2.5	-	4.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until test results are valid, C_{SQHx}= 0.12µF C_{SQLx}= 0.12µF	-	-	500	µs
Voltage measurement diagnostics (VRESx)						
I_{RESx}	Max diagnostic current into V_{RESx} pin	Normal Conditions	-	-	50	µA
$V_{VRESXLO\_th}$	Low voltage threshold for VRESx pin	-	5.0	-	7	V
$V_{VRESXHI\_th}$	High voltage threshold for VRESx pin	-	13.7	-	18.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until test results are valid.	-	-	100	µs
MOS diagnostics						
I_MOS	MOS test max current	Normal conditions	-	-	I_{SVRCM}	mA
$t_{SHUTOFF}$	LS/HS MOS turn off under fault condition	Time is measured from the valid LS/ HS MOS current > 100mA to the LS/HS turn off	-	-	4	µs

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{FETtimeout}$	FET time-out	Normal Conditions	-	-	100	µs
High squib resistance diagnostics						
R_{SQHIZ}	High load resistance threshold	-	1.07	-	2.1	kΩ
I_{HR}	High resistance current threshold	-	I_{STG}			mA
$t_{DIAGTIMEOUT}$	MOS diagnostic delay time	From/CS ↑ until test results are valid, C_{SQHx} = 0.12µF C_{SQLx} = 0.12µF	-	-	300	µs
Squib resistance diagnostics						
V_{OH}	Output voltage AOUT	High saturation voltage; I_{AOUT} = -500µA	VDD-0.2	-	-	V
V_{OL}		Low Saturation Voltage; I_{AOUT} = +500µA	-	-	0.2	V
I_Z	Tri-State Current AOUT	AOUT = VDD	-	-	1	µA
		AOUT = 0V	-1	-		µA
$R_{SQB\ RANGE}$	Load resistance range	-	0	-	10.0	Ω
V_{AOUT}	Resistance measurement analog output tolerance $V_{AOUT} = VDD \cdot \left[\frac{1}{9.75} + \left(0.08 \cdot \frac{R_{SQB}}{\Omega}\right)\right]$	$0\Omega \le R_{SQB} < 3.5\Omega$	V_{AOUT}- 0.095V	-	V_{AOUT}+ 0.095V	V
		$3.5\Omega \le R_{SQB} \le 10\Omega$	V_{AOUT}· 0.95V	-	V_{AOUT}· 1.05V	V
I_{SRC}	Resistance measurement current source	V_{DD} = 5.0V; V_{SDIAG} = 7.0V to 37V	38	-	42	mA
I_{SINK}	Resistance measurement current sink	IPD OFF, VSQLx = 4 V	45	-	57	mA
I_{SLEW}	Rmeas current di/dt	30% - 70% of ISRC	2	-	11	mA/µs
V_{cmpr}	Voltage threshold on squib pin to shutdown ISRC	-	2.65	-	3.25	V
$t_{isrcshtdwn}$	Shutdown time	Guaranteed by design	-	-	30	µs
VLSDrsqb	LSD (V_SQL) voltage during resistance measure	-	0.8	-	2.2	V
t_{R_WAIT}	Rmeas wait time	Wait time before AOUT voltage is stable for ADC reading R AOUT= 5.1kΩ; C_{AOUT}=10nF	-	-	300	µs
FENx input pins						
$t_{FENfilter}$	Minimum pulse width	-	12	-	16	µs
I_{FENPD}	Internal pull-down current	VIN = VIL to VDD	20	-	50	µA

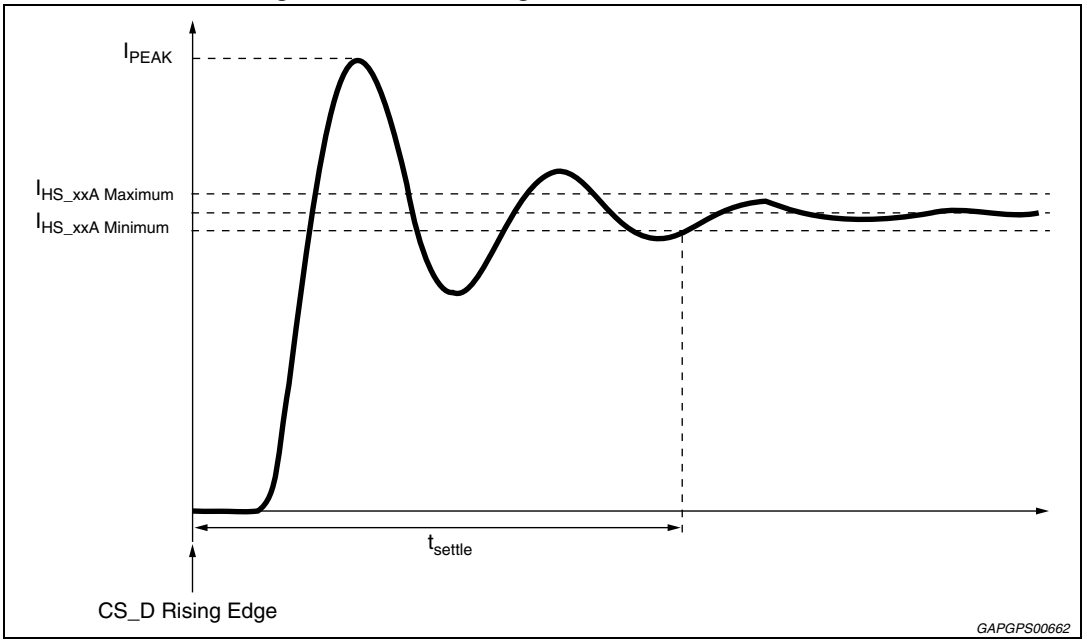
Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{FENLO}	Input low voltage threshold	-	0.8	-	-	V
V_{FENHI}	Input high voltage threshold	-	-	-	2.0	V
$T_{FENLATCH}$	FEN Latch timer	-	0	-	512	ms
t_{FLACC}	FEN latch timer accuracy	-	- 20%	-	20	%
Deployment drivers						
$T_{RESOLUTION}$	Diagnostic timing / resolution	$I_{HS} \geq I_{MEAS}$, $0s \leq T_{MEASURE\_TIME} \leq 3.7ms$ $C_{SQUIB\_HI} = 0.12\mu F$ $C_{SQUIB\_LO} = 0.12\mu F$	22.5	25	27.5	µs
$T_{ACCURACY}$	Diagnostic time accuracy		-	-	2	LSB
I_{MEAS}	High side driver current limit detect threshold	Guaranteed by design	I_{HSX} x 0.90	-	I_{HSX} x 0.99	A
$R_{DSonTOTAL}$	Total high and low side MOS on resistance	High side MOS + low side MOS D9:D8="11"; V_{RES} = 7V; I = 1.6A @95°C	-	-	2.0	Ω
R_{DSonHS}	High side MOS on resistance	D9:D8="11"; VRES = 7V; T_{amb} = 95°C; IVRES = 1.6A;	-	0.3	0.8	Ω
R_{DSonLS}	Low side MOS on resistance		-	0.6	1.2	Ω
I_{HS_12A}	High side deployment current limit	Configuration mode 1 bits D9:D8="00" SQHx shorted to ground; V_{RES} = 7 to 37V	1.21	-	1.47	A
I_{HS_15A}		Configuration Mode 1 bits D9:D8="01" SQHx shorted to ground; V_{RES} = 7 to 25V	1.51	-	1.85	A
I_{HS_175A}		Configuration Mode 1 bits D9:D8="11" SQHx shorted to ground; V_{RES} = 7 to 37V	1.76	-	2.14	A
t_{ILIM}	Low side MOS shutdown under short to battery	V_{sqblo}=18V	90	-	110	µs
I_{LS}	Low side MOS current limit		2.2	-	4.0	A
t_{settle}	Firing current settling time	Time from fire command CS_D rising edge to where firing current remains within specified limits C_{SQUIB_HI} = 0 to 0.12µF C_{SQUIB_LO} = 0 to 0.12µF	-	-	150	µs

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{DEPLOY-2ms}$	Deployment time	VRES = 7Vto 37@ I_{HS_12A} VRES = 7Vto 25@ I_{HS_15A} For I_{HS_12A} and I_{HS_15A} Firing current measured from CS_D rising edge	2.15	-	2.5	ms
$t_{DEPLOY-1ms}$		V_{RES} = 7Vto 37V For I_{HS_175A} Firing current measured from CS_D rising edge	1.15	-	1.40	ms
$t_{DEPLOY-0.65ms}$		V_{RES} = 7Vto 37V For I_{HS_175A} Firing current measured from CS_D rising edge	0.65	-	0.85	ms

Figure 3. MOS settling time and turn-on time 2



2.4.3 SPI timing

All SPI timing is performed with a 150 pF load on MISO unless otherwise noted.

$4.9V \le V_{DD} \le 5.1V$; $7V \le V_{RESX} \le 37V$; $7V \le V_{SDIAG} \le 37V$; (FEN1 = FEN2 = V_{DD}; R_REF = 10KΩ, ±1%, 100PPM; $-40°C \le T_A \le +95°C$; C_VRES0_1 ≥ 68nF; C_VRES2_3 ≥ 68nF; unless other specified.

Table 8. SPI timing - DC electrical characteristics

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
-	fop	Transfer frequency	dc	-	5.50	MHz
1	tSCK	SCLK Period	181	-	-	ns
2	tLEAD	Enable Lead Time	65	-	-	ns
3	tLAG	Enable Lag Time	50	-	-	ns
4	tSCLKHS	SCLK, High Time	65	-	-	ns
5	tSCLKLS	SCLK, Low Time	65	-	-	ns
6	tSUS	MOSI, Input Setup Time	20	-	-	ns
7	tHS	MOSI, Input Hold Time	20	-	-	ns
8	tA	MISO, Access Time	-	-	60	ns
9	tDIS (1)	MISO, Disable Time	-	-	100	ns
10	tVS	MISO, Output Valid Time	-	-	60	ns
11	tHO (1)	MISO, Output Hold Time	0	-	-	ns
12	tRO	Rise Time (Design Information)	-	-	30	ns
13	tFO	Fall Time (Design Information)	-	-	30	ns
14	tCSN	CS_D, Negated Time	640	-	-	ns
15	tCLKN	Time between CS rising edge and first transition of SCLK must be higher than tCLKN. It happens when multiple devices are connected to the same SCLK and MOSI but with different chip select.	500	-	-	ns

1. Parameters t_{DIS} and t_{HO} shall be measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 4. SPI timing diagram

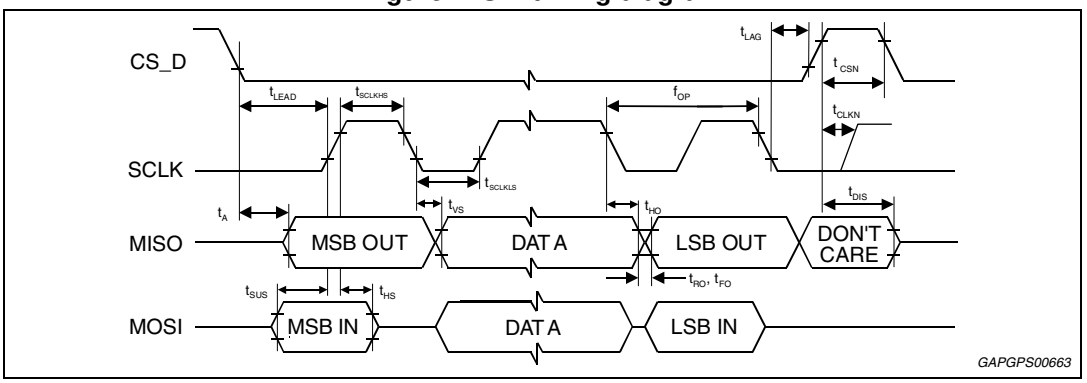
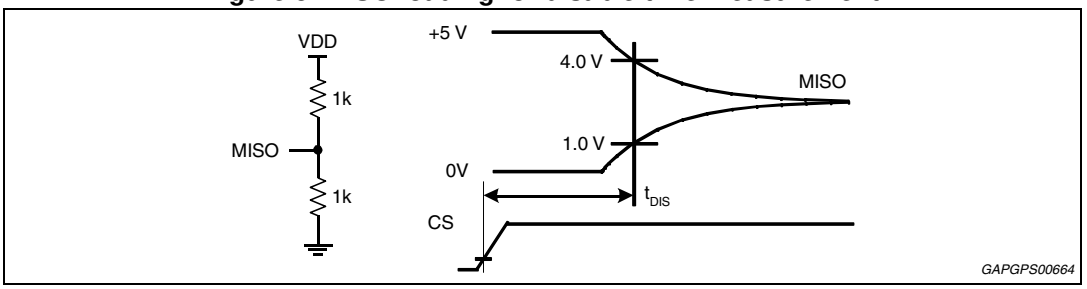


Figure 5. MISO loading for disable time measurement



3 Functional description

3.1 Overview

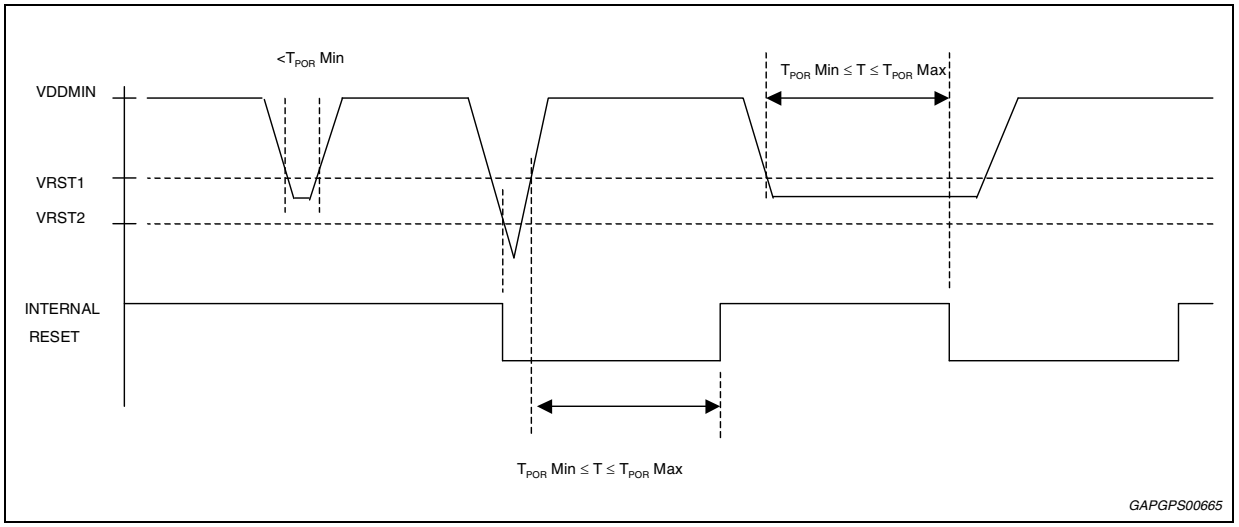
The L9660 is an integrated circuit to be used in air bag systems. Its main functions include deployment of air bags. The L9660 supports 4 deployment loops.

3.2 General functions

3.2.1 Power on reset (POR)

The ASIC has a power on reset (POR) circuit, which monitors VDD voltage. When VDD voltage falls below V_{RST1} for longer than or equal to t_{POR}, all outputs are disabled and all internal registers are reset to their default condition. A second reset level, V_{RST2}, also monitors VDD but uses no filter time, so all outputs are disabled and all internal registers are reset to their default condition when VDD falls below the reset threshold.

Figure 6. POR timing



3.2.2 RESETB

The RESETB pin is active low. The effects of RESETB are similar to those of a POR event, except during a deployment. When a deployment is in-progress, the L9660 ignore the RESETB signal.

However, it shuts itself down as soon as it detects a POR condition. When the deployment is completed and RESETB signal is asserted, the L9660 disables its outputs and reset its internal registers to their default states.

A de-glitch timer is provided for the RESETB pin. The timer protects this pin against spurious glitches. The L9660 neglects RESETB signal if it is asserted for shorter than tGLITCH. RESETB has an internal pull-up in case of an open circuit.

3.2.3 Reference resistor

IREF pin shall be connected to VDD supply through a resistor, RIREF. When the L9660 detects the resistor on IREF pin is larger than RIREF_H or smaller than RIREF_L, it goes into a reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

3.2.4 Loss of ground

GND

When the GND pin is disconnected from PC-board ground, the L9660 goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

GND0-GND3

A loss of power-ground (GND0 – GND3) pin/s disables the respective low side driver/s on SQLx. However, the high side driver of the respective channel is still able to be turned on. Thus under the scenario where the low side is shorted to ground the L9660 is able to provide the programmed firing current for the specified time.

An open GNDx connection on any channel has no affect on the other channels. An open GNDx condition is detected using the low side MOS diagnostics.

AGND

The AGND pin is a reference for AOUT pin. When AGND loses its connection, the voltage on AOUT pin is pulled up to VDD voltage and L9660 goes in reset condition. All outputs are disabled and all internal register are reset to their default conditions.

3.2.5 VRESx capacitance

To properly ensure all diagnostics functions a typical capacitor of equal to or greater than 68nF is required close to the firing supply pins. Thus a minimum of 2 capacitors are required with one placed close to the VRES0 and VRES1 pins and a second capacitor close to the VRES2 and VRES3 pins.

3.2.6 Supply voltages

The primary current sources for the different functions of the ASIC are as follows:

- VRESx - Firing currents along with HSS and HS FET diagnostic currents
- VSDIAG - Squib resistance and HSS diagnostics
- VDD is used for all internal functions as well as short to battery/ground and high squib resistance diagnostics.

3.2.7 Ground connections

GND pin (6) is not connected internally to other ground pins (AGND or power ground GNDx). A ground plane is needed to directly connect the GND pin. This ground plane needs to be isolated from the high current ground for the squib drivers to prevent voltage shifts.

AGND pin should be connected to ground plane too to minimize drop versus ground reference of ADC that capture AOUT voltage.

3.3 Serial peripheral interface (SPI)

The L9660 contains one serial peripheral interface for control of the squib functions. The following table shows features that are accessed/controlled by the SPI.

Table 9. Features that are accessed/controlled for the SPI

Function	Pin names	Features accessed
Squib diagnostic and deployment SPI	SCLK MISO MOSI CS_D	All Squib Diagnostics; Squib related status information; Squib Arming and Firing; Software Reset; Component ID & Revision

The software reset accessed over SPI is resets squib functions. The L9660 has a counter to verify the number of clocks in SCLK. If the number of clocks in SCLK is not equal to 16 clocks while CS_D is asserted, it ignores the SPI message and sends a SPI fault response. L9660 computes SPI error length flag through counting the number of SCLK rising edges occurring when CS_D is active. If the first SCLK rising edge occurs when CS_D is inactive and the falling edge occurs when CS_D is low, it is considered as valid edge.

MOSI commands contain several unused bits, all those bits must be 0. Commands are not recognized valid if one or more unused bits are not 0.

3.3.1 SPI pin descriptions

Chip select (CS_D)

Chip-select inputs select the L9660 for serial transfers. CS_D can be asserted at any given time and are active low. When chip-select is asserted, the respective MISO pin is released from tri-state mode, and all status information is latched into the SPI shift register. While chip-select is asserted, register data is shifted into MOSI pin and shifted out of MISO pin on each subsequent SCLK. When chip-select is negated, MISO pin is tri-stated. To allow sufficient time to reload the registers; chip-select pin shall remain negated for at least tCSN. The chip-select inputs have current sinks which pull these pins to the negated state when there is an open circuit condition. These pins have TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

Serial clock (SCLK)

SCLK input is the clock signal input for synchronization of serial data transfer. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply. When chip select is asserted, both the SPI master and L9660 latch input data on the rising edge of SCLK. The L9660 shifts data out on the falling edge of SCLK.

Serial data output (MISO)

MISO output pins shall be in one tri-state condition when chip select is negated. When chip select is asserted, the MSB is the first bit of the word/byte transmitted on MISO and the LSB is the last bit of the word/byte transmitted. This pin supplies a rail to rail output, so if interfaced to a microprocessor that is using a lower VDD supply, the appropriate microprocessor input pin shall not sink more than $I_{OH(min)}$ and shall not clamp the MISO output voltage to less than $V_{OH(min)}$ while MISO pin is in a logic “1” state. When connecting to a micro using a lower supply, such as 3.3V, a resistor divider shall be used with high enough impedance to prevent excess current flow.

Serial data input (MOSI)

MOSI inputs take data from the master processor while chip select is asserted. The MSB shall be the first bit of each word/byte received on MOSI and the LSB shall be the last bit of each word/byte received.

This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

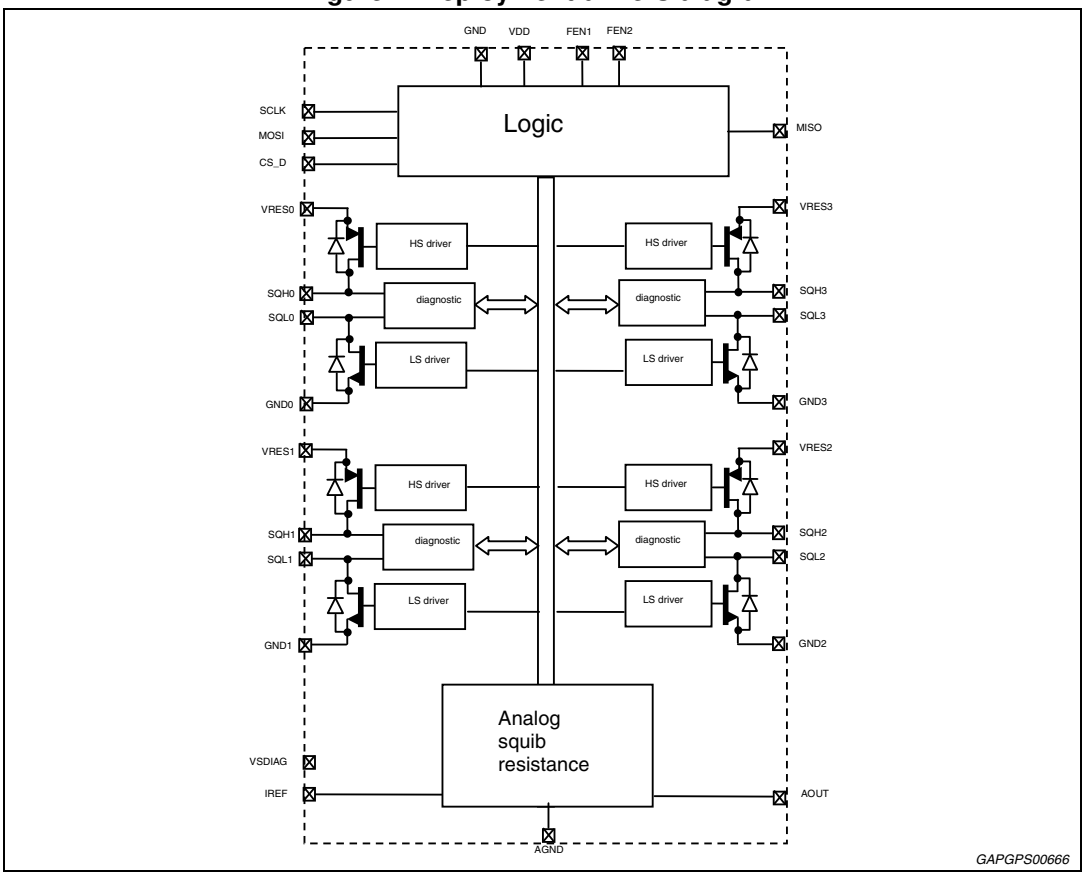
3.4 Squib drivers

3.4.1 Firing

The on-chip deployment drivers are designed to deliver 1.2 A (min) for 2ms (min) and 1.75A (min) for 1ms (min) and 1.75A (min) for 0.65ms (min) with VRESx voltages between 7V and 37 V. In addition the L9660 can provide 1.5A minimum for 2ms for VRESx voltages between 7V and 25V. The firing condition is selectable via the SPI. At the end of a deployment, a deploy success flag is asserted and can be read using the appropriate SPI command. Each VRESx and GNDx connection is used to accommodate 4 loops that can be deployed simultaneously.

Upon receiving a valid deployment condition, the respective SQHx and SQLx drivers are turned on. The only other activation of the SQHx and SQLx drivers is momentarily during a MOS diagnostic. Otherwise, SQHx and SQLx are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQHx and SQLx drivers, a deploy command success flag is asserted via SPI. Refer to *Figure 8* for the valid conditions and the deploy success flag timing.

Figure 7. Deployment drivers diagram



The L9660 is protected against inadvertent turn on of the firing drivers unless the appropriate conditions are present. Non-typical conditions do not cause driver activation. This includes the case where VRESx and/or VSDIAG pins are connected to a supply up to 40V and VDD is between 0V and VDD min. Under these conditions the L9660 ensures that driver activation does not occur. No flow of current shall be allowed through the SQHx and SQLx pins.

Driver activation

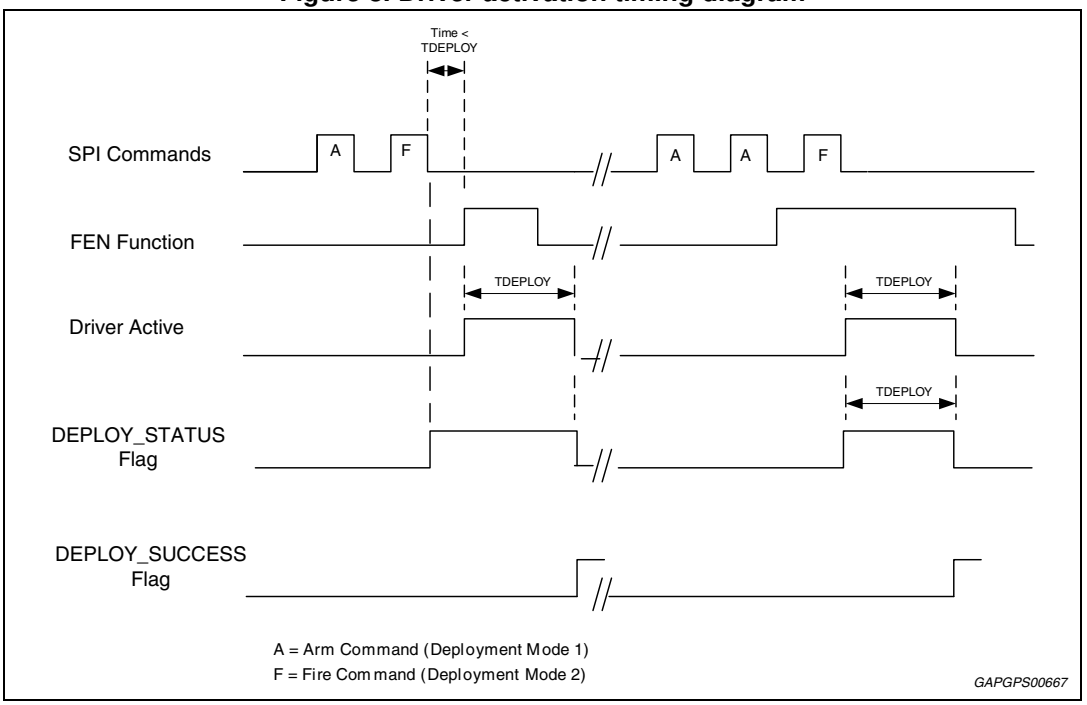
The firing of a squib driver requires the appropriate FEN function to be active and two separate sixteen bit writes be made over the SPI. The FEN function is defined as the result of the FENx pin OR'd with the internal FENx latch. The FENx pin going high initiates the FEN function. With the FEN 1 function being active and the appropriate Arm and Fire commands sent then Squib_0 & 1 drivers would be activated. With the FEN 2 function being active and the appropriate Arm and Fire commands sent then Squib_2 & 3 drivers would be activated.

The first write is to ARM the drivers in preparation of receiving the fire command. The ARM command stops on all channels any diagnostics that are active. Any combination of squibs can be armed. The second write is a FIRE command that must directly follow the ARM command and that activates the desired driver pairs assuming the FEN function is valid. If there is a parity mismatch the data bits are ignored and the squib drivers do not have their status changed, and the two write sequence must then be started again. If there is a mismatch in channels selected then only those channels selected in both the Arm and Fire commands are activated.

During the first write, when the drivers are armed, all diagnostic functions are cleared. The FIRE command must follow the ARM command along with the FEN function active for driver activation. If a command is between the ARM and FIRE command then the sequence must be restarted. An error response is received for the Fire command if the ARM/FIRE sequence is not followed.

The ARM/FIRE commands and FEN function are independent from each other. The L9660 begins the t_{DEPLOY} timer once a valid ARM/FIRE sequence has been received. If a valid ARM/FIRE command has been sent and the FEN function is inactive then the drivers are not activated but the t_{DEPLOY} timer starts. If the FEN function becomes active before t_{DEPLOY} has expired then the drivers become active for the full t_{DEPLOY} time. If the FEN does not become active before t_{DEPLOY} has expired then the sequence needs to be restarted. A diagram illustrating this is shown in *Figure 8.*

Figure 8. Driver activation timing diagram



Only the channels selected in the ARM and, directly following, the FIRE command are activated.

By reading the appropriate registers a status of the deployment is provided. If a valid Arm/Fire sequence has been provided the status flag becomes active. This flag remains active for as long as the T_{DEPLOY} timer is counting. Depending on the state of the FEN function the DEPLOY_STATUS flag is active a minimum of T_{DEPLOY} and a maximum of 2 x T_{DEPLOY}. If driver activation did occur (both a valid Arm/Fire sequence and the appropriate FEN function active within the appropriate time) then the DEPLOY_SUCCESS flag is active following the completion of the driver activation period. This flag is active until cleared by software. If a valid Arm/Fire sequence did occur but the FEN function was never activated within the T_{DEPLOY} time then the DEPLOY_SUCCESS flag remains '0'.

Once the Deploy Success Flag is set, it inhibits the subsequent deployment command until a SPI command to clear this deployment success flag is received. Bits D7 through bit D0 are used to clear/keep the deploy success flag. When these bits are set to '1,' the flag can be

cleared. Otherwise, the state of these flags is not affected. The Success flag must be cleared to allow re-activation of the drivers.

During driver activation the respective high side (SQHx) and low side (SQLx) drivers turn on for t_{DEPLOY}.

L9660 driver activation does not occur or, if firing is in process, is terminated under the following conditions:

- Power On Reset (POR)
- IREF resistance is larger than RIREF_H or smaller than RIREF_L
- Loss of ground condition on GND pin

The following conditions are ignored when driver activation is in progress:

- RESETB
- Valid soft reset sequences
- SPI commands except as noted below. Response for ignored commands is 0xD009
- FEN function

The following table shows the response when sending SPI commands during deployment.

Table 10. SPI MOSI/MISO response

SPI MOSI	SPI MISO	Response
Configuration Commands	SPI fault response	MOSI register mode messages are ignored
Deployment Commands	Command mode	Execute for channels not in deployment; no effect to deploying channel
Diagnostic Commands	SPI fault response	MOSI diagnostic mode messages are ignored
Monitor Commands	Status response	Execute for all channels

Note 1: SPI MISO sent in the next SPI transmission.

The L9660 can only deploy a channel when the FEN function is active. Once the drivers are active the L9660 keeps the drivers on for the required duration regardless of the FEN state. Once complete a status bit is set to indicate firing is complete.

3.4.2 Firing current measurement

All channels have a 7 bit current measurement register that is used to measure the amount of time the current is above I_{MEAS} during firing. The maximum measurement for each channel is 3.175ms nominal based on a bit weight of 25µs. The current measurement register does not increment outside the deployment time. The current measurement begins incrementing once the current has exceeded 95% of the nominal target value. The count continues to increment from the stored value until either a clear command has been issued for that channel or all ‘1’s are present in the corresponding channel measurement register. If all ‘1’s are present for a channel’s measurement register and another firing sequence has been issued the register remains all ‘1’s. Only if a clear command has been issued that particular register resets to all ‘0’s. All other channels shall keep the stored measurement count. During firing the current measurement register cannot be cleared. After a clear command has been issued for a channel then the channel is ready to count if the current exceeds the specified level. After a POR or software reset the L9660 resets all 4 measurement registers to all ‘0’s.

A “real-time” current measurement status of all the channels is available. If a current limit status request is sent then the L9660 reports in the next SPI transfer whether the current is above or below IMEAS for each of the channels. The current status results can be read at any time and correctly reports whether current is flowing. The content of the internal current status register is captured on the falling edge of chip select during the SPI response. The internal status register is updated at a nominal sample time of 25 µs and is independent from SPI transfers.

For this circuit there is a continuously performed compensation of the comparator in order to remove offset errors, which is independent from SPI commands. The compensation is being performed every 12.8 µs based on the internal clock.

3.4.3 Fire enable (FEN) function description

The Fire Enable (FEN) function is the result of the FENx input OR’d with the internal FEN latch. If the FEN latch is not enabled and the FENx pin is low then activations of the FET drivers are disabled except as indicated during the MOS test. All internal diagnostics are active, and results are available through the serial interface. This pin must be pulled high to initiate the FEN latch function (if programmed) and enable firing of the FET drivers.

There are two FEN function blocks

- FEN Function 1 is FEN1 input OR’d with FEN1 latch timer and used for enabling channels 0 & 1
- FEN Function 2 is FEN1 input OR’d with FEN2 latch timer and used for enabling channels 2 & 3

The FEN function is considered active when the pin is active (‘1’ or high) for more than 12 microseconds. Tolerance range for the filter used is 12 to 16 µs.

When the FENx input is active, ‘1’, the FEN function activates. **When the FENx input state transitions from ‘1’ to ‘0’, the programmable latching function holds the FEN function active until the time-out of the FEN timer.** The programmable latch and hold function are capable of delays of 0ms, 128ms, 256ms, and 512ms. There are 2 independent timers with the timer for FEN1 associated with channels 0 & 1, timer for FEN2 associated with channels 2 & 3. **The timer is reset to the programmed time when the FENx pin transitions from ‘0’ to ‘1’.** The programmable counter delay is set through a SPI command.

3.4.4 Squib diagnostics

Overview

The ASIC is able to perform the following diagnostics

- Short to battery and ground on both SQHx and SQLx pins with or without a squib
- Loop to loop diagnostics
- Squib resistance measurement
- Squib High resistance
- High side safing FET diagnostics
- VRESx voltage status
- High and low side FET diagnostics

Below is a block diagram showing the components involved in the squib diagnostics.