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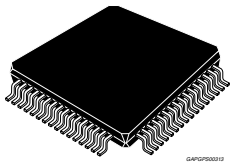
L9662

Octal squib driver and quad Manchester/PSI5 encoded sensor interface ASIC for safety application

Datasheet - production data



LQFP64 (10x10x1.4mm)

Features

- 8 deployment drivers with SPI selectable firing current and times
- Capability to deploy the squib with 1.2 A (min)/2 ms, 1.75 A (min)/1.0 ms and 1.75 A (min)/0.65 ms between VRES of 7 V to 37 V
- Capability to deploy the squib with 1.5 A (min)/2 ms between VRES of 7 V to 25 V
- Firing capability to deploy all channels simultaneously
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance measurement
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib the low side MOS is shorted to ground
- 4 Fire enable inputs
- Interface with 4 satellite sensors
- Programmable independent current trip points for each satellite channel
- Support Manchester 1 or 2 protocol for satellite sensors
- Support PSI5 (Parity) protocol for satellite sensors (reference PSI5 technical specification V 1.2 /14.06.07)
- Support for Sync pulse and minibus for satellites
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 2 independent SPI interfaces
- 5.5 MHz SPI interface
- Satellite message error detection
- Hall effect sensor support on satellite channels 3 and 4.
- Low voltage internal reset
- 2 kV ESD capability on all pins
- Package: LQFP64
- Technology: ST Proprietary BCD5

Description

The device is intended to deploy up to 8 squibs and to interface up to 4 satellites. 2 satellite interfaces can be used to interface Hall sensors. Squib drivers are sized to deploy 1.2 A minimum for 2 ms, 1.75 A minimum for 1 ms and 1.75 A minimum for 0.65 ms during load dump along with 1.5 A minimum for 2 ms for VRES voltages less than 25 V.

Full diagnostic capabilities of the squib interface are provided. Satellite interfaces support Manchester 1, 2 and PSI5 decoding with variable bit rate.

Table 1. Device summary

Order code	Amb. temp range, °C	Package	Packing
L9662	-40 to +85	LQFP64	Tray
L9662TR			Tape & Reel

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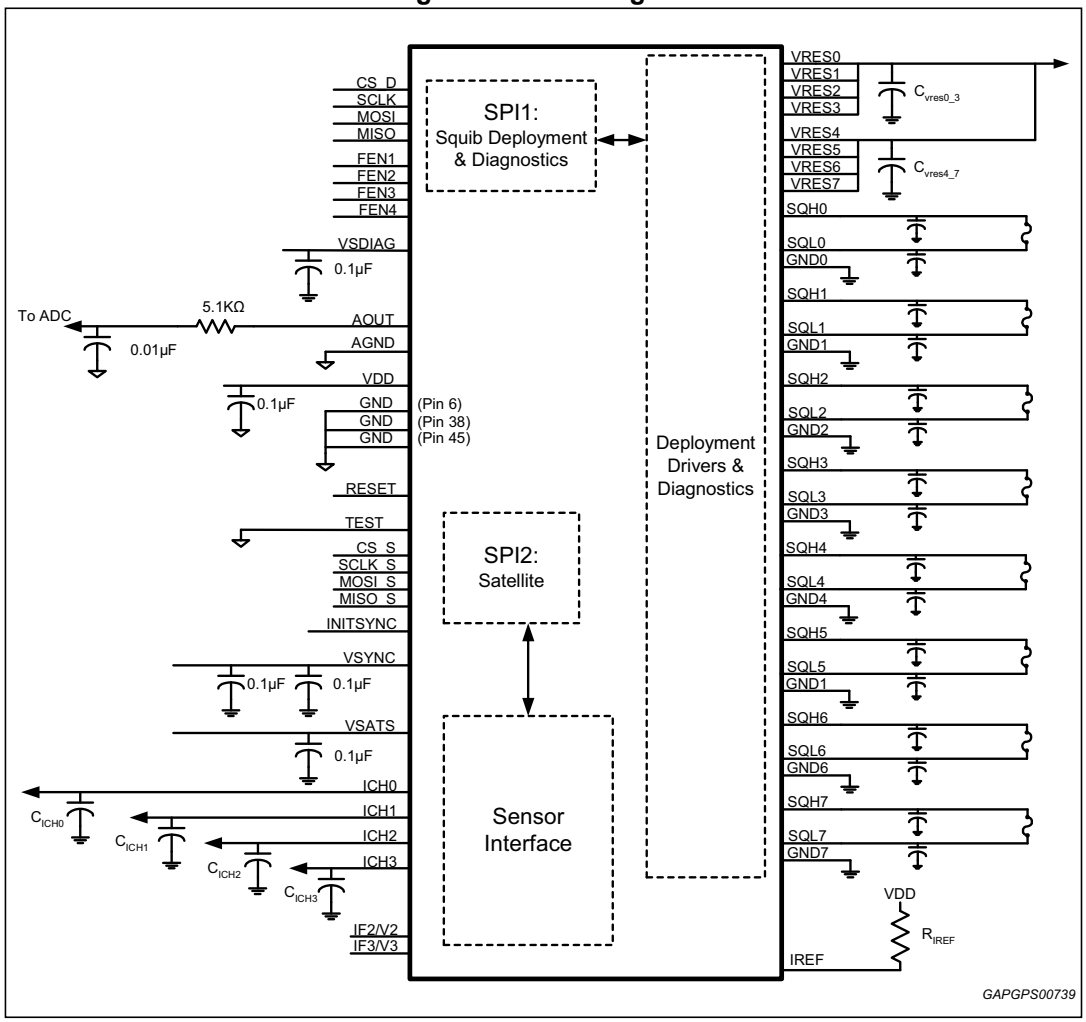
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Table 2. Pin description

Pin Number	Pin name	Description	I/O type	Reset state
1	MISO	SPI Data Out	Output	Hi-Z
2	MISO_S	Satellite SPI Data Out	Output	Hi-Z
3	FEN1	Fire Enable for Channels 0 and 1	Input	Pulldown
4	FEN2	Fire Enable for Channels 2 and 3	Input	Pulldown
5	RESETB	Reset pin	Input	Pullup
6	GND	Ground (Analog & Digital)	-	-
7	VDD	VDD Supply Voltage	Input	-
8	FEN3	Fire Enable for Channels 4 and 5	Input	Pulldown
9	FEN4	Fire Enable for Channels 6 and 7	Input	Pulldown
10	INITSYNC	Initiate Sync Pulse	Input	Pulldown
11	CS_S	SPI Chip Select for Satellite Interface	Input	Pullup
12	CS_D	SPI Chip Select for Deployment Driver	Input	Pullup
13	MOSI	SPI Data In	Input	Hi-Z
14	MOSI_S	Satellite SPI Data In		
15	SCLK_S	Satellite SPI Clock		Hi-Z
16	SCLK	SPI Clock	Input	Hi-Z
17	GND4	Power Ground for Loop Channel 4	-	-
18	SQL4	Low Side Driver Output for Channel 4	Output	Pulldown
19	SQH4	High Side Driver Output for Channel 4	Output	Hi-Z
20	VRES4	Reserve Voltage for Loop Channel 4	Input	-
21	VRES5	Reserve Voltage for Loop Channel 5	Input	-
22	SQH5	High Side Driver Output for Channel 5	Output	Hi-Z
23	SQL5	Low Side Driver Output for Channel 5	Output	Pulldown
24	GND5	Power Ground for Loop Channel 5	-	-
25	GND6	Power Ground for Loop Channel 6	-	-
26	SQL6	Low Side Driver Output for Channel 6	Output	Pulldown
27	SQH6	High Side Driver Output for Channel 6	Output	Hi-Z
28	VRES6	Reserve Voltage for Loop Channel 6	Input	-
29	VRES7	Reserve Voltage for Loop Channel 7	Input	-
30	SQH7	High Side Driver Output for Channel 7	Output	Hi-Z
31	SQL7	Low Side Driver Output for Channel 7	Output	Pulldown
32	GND7	Power Ground for Loop Channel 7	-	-
33	TEST	Test pin	Input	Pulldown

Table 2. Pin description (continued)

Pin Number	Pin name	Description	I/O type	Reset state
34	VSDIAG	Supply for Deployment Driver Diagnostics	Input	-
35	NC	No Connect	-	-
36	IF3/V3	Current Feedback for channel 3 Raw Or Raw Data output For Channel 3	Output	Hi-Z
37	IF2/V2	Current Feedback for channel 2 Raw Or Data output For Channel 2	Output	Hi-Z
38	GND	Ground (Analog & Digital)	-	-
39	ICH3	Current Sense Output for Channel 3	Output	Hi-Z
40	ICH2	Current Sense Output for Channel 2	Output	Hi-Z
41	ICH1	Current Sense Output for Channel 1	Output	Hi-Z
42	ICH0	Current Sense Output for Channel 0	Output	Hi-Z
43	VSYNC	Supply for Satellite Sync Pulse	Input	-
44	VSATS	Supply Voltage for Satellite Interface	Input	-
45	GND	Ground (Analog & Digital)	-	-
46	IREF	External Current Reference Resistor	Output	-
47	AGND	Ground Reference for AOUT	-	-
48	AOUT	Analog Output for Loop Diagnostics	Output	Hi-Z
49	GND3	Power Ground for Loop Channel 3	-	-
50	SQL3	Low Side Driver Output for Channel 3	Output	Pulldown
51	SQH3	High Side Driver Output for Channel 3	Output	Hi-Z
52	VRES3	Reserve Voltage for Loop Channel 3	Input	-
53	VRES2	Reserve Voltage for Loop Channel 2	Input	-
54	SQH2	High Side Driver Output for Channel 2	Output	Hi-Z
55	SQL2	Low Side Driver Output for Channel 2	Output	Pulldown
56	GND2	Power Ground for Loop Channel 2	-	-
57	GND1	Power Ground for Loop Channel 1	-	-
58	SQL1	Low Side Driver Output for Channel 1	Output	Pulldown
59	SQH1	High Side Driver Output for Channel 1	Output	Hi-Z
60	VRES1	Reserve Voltage for Loop Channel 1	Input	-
61	VRES0	Reserve Voltage for Loop Channel 0	Input	-
62	SQH0	High Side Driver Output for Channel 0	Output	Hi-Z
63	SQL0	Low Side Driver Output for Channel 0	Output	Pulldown
64	GND0	Power Ground for Loop Channel 0	-	-

2 Electrical specifications

2.1 Absolute maximum ratings

The following maximum ratings are continuous absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	- 0.3 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	- 0.3 to 40	V
V_{SATS}	Satellite supply voltage	- 0.3 to 40	V
V_{SYNC}	Sync supply voltage	- 0.3 to 40	V
VRESx	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)	- 0.3 to 40	V
SQHx	Squib high side drivers (SQH0, SQH1, SQH2, SQH3, SQH4, SQH5, SQH6, SQH7)	- 0.6 to 40	V
SQLx	Squib low side drivers (SQL0, SQL1, SQL2, SQL3, SQL4, SQL5, SQL6, SQL7)	- 0.3 to 40	V
ICHx	Satellite outputs (ICH0, ICH1, ICH2, ICH3)	-1 to 40	V
TEST	Test pin	-0.3 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)	- 0.3 to 5.5	V
V_O	Discrete output voltage (MISO, MISO_S, AOUT, IF2V2, IF3V3)	- 0.3 to 5.5	V
AGND	Analog output reference	-0.3 to 5.5	V
GND	Ground (GND, GND0, GND1, GND2, GND3, GND4, GND5, GND6, GND7)	-0.3 to 5.5	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance-junction-to-ambient	46	°C/W
The following maximum ratings are up to 48 hours; exceeding any one of these values for longer than a total time of 48 hours may cause permanent damage to the integrated circuit.			
V_{DD}	Supply voltage	- 0.3 to 6.0	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)	- 0.3 to 6.0	V
V_O	Discrete output voltage (MISO, MISO_S, AOUT, IF2V2, IF3V3)	- 0.3 to 6.0	V

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AGND	Analog output reference	-0.3 to 6.0	V
GND	Ground (GND, GND0, GND1, GND2, GND3, GND4, GND5, GND6, GND7)	-0.3 to 6.0	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance junction-to-ambient	46	°C/W

2.2 Absolute maximum degraded operating ratings

Under the following deviations to the ratings indicated in *Section 2.3* the device performance will be degraded and not meet the electrical characteristics outlined in *Section 2.4*. At minimum the SPI and diagnostics will function but not meet specified electrical parameters.

Table 4. Absolute maximum degraded operating ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	7 to 40	V
V_{SATS}	Satellite supply voltage	7 to 14	V
V_{SYNC}	Sync supply voltage	(V_{SATS}+ 5.5 V) to 40	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)	7 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC)	- 0.3 to (VDD +0.3)	V
T_j	Junction temperature	-40 to 150	°C

Note: The above is provided for informational purposes only and will result in degraded operation. Under the above conditions the SPI will be functional as well as diagnostics, though the electrical performance may not conform to the parameters outlined in Section 2.4. Firing requirements as indicated in Section 2.4 may not be met with the conditions above.

2.3 Operating ratings

Table 5. Operating ratings

Symbol	Parameter		Value	Unit
V_{DD}	Supply voltage		4.9 to 5.1	V
V_{SDIAG}	Supply voltage for squib diagnostics		7 to 37	V
V_{SATS}	Satellite supply voltage		7 to 14	V
V_{SYNC}	Sync supply voltage (1))	Continuous	(V_{SATS} + 6) to 25	V
		pulse ≤500 ms	(V_{SATS} + 6) to 40	
V_{RESx}	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)		7 to 37	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)		- 0.3 to (V_{DD} +0.3)	V
T_{amb}	Ambient temperature		-40 to 95	°C
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient		46	°C/W

1. For PSI5 the maximum operating voltage is 16.5V as called out in the PSI5 technical specification (V 1.2 /14.06.07). Depending on the sync supply voltage the sync pulse can be as high as 8 V above idle. To ensure the maximum operating voltage of 16.5 V is not exceeded then the VSATS voltage should be limited to 8.5 V.

2.4 Electrical characteristics

2.4.1 General

4.9 V ≤ V_{DD} ≤ 5.1 V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5 V) ≤ V_{SYNC} ≤ 25 V; 5 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 6. General - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Osc	Internal oscillator frequency	Tested with 10K, 1%, 100ppm I_{ref} resistor	4.75	-	5.25	MHz
V_{RST1}	Internal voltage reset VDD after de-glitch time (tpor) See *Figure 6*	VDD level for device to report reset condition -deployment drivers are disabled	4.0	-	4.5	V
V_{RST2}	Internal voltage reset VDD with no de-glitch time See	Guaranteed by design	2.1	-	3.0	
t_{POR}	POR De-glitch timer	Timer for VRST1	5	-	25	µs
I_{DD}	Input current VDD	No squib diagnostics. No deployment. Satellite channels disabled.	-	-	15	mA
		Resistance measurement diagnostics with no fault condition present. Satellite channels disabled.	-	-	17	

Table 6. General - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD}	Input current VDD	Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx=10mA and no sync pulse.	-	-	17	mA
		Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx = 50 mA and no sync pulse.	-	-	17	
		Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx = 50 mA and sync pulse at high voltage level.	-	-	17	
		Short to -0.3 V on SQHx. Satellite channels disabled.	-	-	15	
		Short to -0.3 V on SQLx. Satellite channels disabled.	-	-	15	
		Deployment. Satellite channels disabled.	-	-	15	
		Short to GND on SQL; VRCM active Satellite channels enabled with I_ICHx = 50 mA and sync pulse at high voltage level.	-	-	35	
R_{IREF_H}	Resistance threshold IREF	-	-	-	60.0	kΩ
R_{IREF_L}		-	2.0	-		kΩ
V_{IH_RESETB}	Input voltage threshold RESETB	-	-	-	2.0	V
V_{IL_RESETB}		-	0.8	-		V
V_{HYS_RST}		-	100	-	300	mV
V_{IH_TEST}	Input voltage threshold TEST	Guaranteed by design	-	3.2		V
I_{TESTPD}	Input pull-down current TEST	-	1.0	-	2.5	mA
I_{AOUT_SHRT}	AOUT pin current limit	AOUT short to ground during squib resistance diagnostics	-	-	20	mA
$I_{RESETPU}$	Input pull-up current RESETB	RESETB = VIH to GND	-10	-	-50	µA
I_{VSATS}	Current consumption VSATS	Satellite channels enabled ICH0-3 = 0 A	-	-	5	mA
I_{VSYNC}	VSYNC supply current	Satellite channels enabled ICH0-3 = 0 A	-	-	5	mA

Table 6. General - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{RESx}	Quiescent current for VRESx during HSS test	Current per pin during HSS test excluding selected channel	-	-	10	µA
V_{IH}	Input voltage threshold (MOSI, MOSI_S, SCLK, SCLK_S, CS_S, CS_D)	Input Logic = 1	-	-	2.0	V
V_{IL}		Input Logic = 0	0.8	-	-	V
V_{HYST}	Input hysteresis	-	100	-	300	mV
I_{LKGD}	Input leakage current MOSI, MOSI_S, SCLK, SCLK_S	VIN = VDD	-	-	1	µA
		VIN = 0 to VIH	-1	-	-	µA
I_{PU_CS}	Input pull-up current CS_S, CS_D	VIN = VIH to GND	-10	-	-50	µA
I_{PD_IS}	Input pull-down current INITSYNC	VIN = VIL to VDD	10	-	50	µA
V_{OH}	Output voltage MISO, MISO_S	IOH = -800 µA	VDD–0.8	-	-	V
V_{OL}		IOL = 1.6 mA	-	-	0.4	V
I_{HI_Z}	Tri-state current MISO, MISO_S,	MISO = VDD	-	-	1	µA
		MISO = 0 V	-1	-	-	µA

2.4.2 Electrical characteristics - Squib deployment drivers and diagnostics

4.9 V ≤ V_{DD} ≤ 5. 1V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5 V) ≤ V_{SYNC} ≤ 25 V; 7 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; C_{VRES0_3}≥ 68 nF; C_{VRES4_7} ≥ 68 nF; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
I_{LKGSQH}	Leakage current SQH	VSDIAG = VDD = 0, VRES = 37 V, VSQH = 0 V	-	-	50	µA
$I_{LKGVRES}$	Bias current VRESX	VSDIAG = 18 V; VDD = 5 V; VRES = 37 V; SQH shorted to SQL	-	-	10	µA
I_{LKGSQL}	Leakage current SQL	VSDIAG = VDD = 0, VSQL = 18 V	-10	-	10	µA
I_{PD}	Pulldown current SQL	VSQL = 1.5 V to 20 V	3.3	-	4.1	mA
V_{BIAS}	Diagnostics Bias voltage	Nominal 3.6 V	-5%	VDD·0.72	+5%	V
Short to battery/ground Diagnostics - Rsqb from 0 Ω to Open						
I_{SVRCM}	Maximum Diagnostics Bias Current limit	Short to battery or ground test active VSQH = 0 V	5	-	20	mA

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{STB}	Short to Battery Resistance Threshold	Vbatt = 6.5V see *Figure 9*	1.92	-	3.42	kΩ
		Vbatt = 16V see *Figure 9*	8.61	-	13.98	kΩ
		Vbatt = 20V see *Figure 9*	11.42	-	18.42	kΩ
I_{STB}	Short to battery current threshold	-	0.9	-	1.40	mA
R_{STG}	Short to Ground Threshold	-	1.2	-	1.8	kΩ
I_{STG}	Short to ground current threshold	-	2	-	3.3	mA
$t_{DIAGTIMEOUT}$	Diagnostic Delay Time	From/CS ↑ until Transistor Test Results are Valid, Output voltage change 0V to 3.5 V C_{SQHx}= 0.12 µF C_{SQLx}= 0.12 µF	-	-	1500	µs
High side safing diagnostics						
I_{SRC_HSS}	Diagnostic current into selected VRESx pin during test	Normal conditions	710	-	950	µA
I_{HSS_8}	Current during diagnostic	All 8 VRESx pins tied together	710	-	1020	µA
$R_{HSSNORM\_th}$	Normal resistance range when running high side safing diagnostics	All 8 VRESx pins tied together	1.4	-	2.5	kΩ
$V_{HSSNORM\_range}$	Normal voltage range between VSDIAG and VRESx pin) when running high side safing diagnostics	All 8 VRESx pins tied together	1.0	-	2.5	V
$V_{HSSSHORT\_th}$	Short voltage threshold between VSDIAG and VRESx pin)	All 8 VRESx pins tied together	0.5	-	1.0	V
$V_{HSSOPEN\_th}$	Open voltage threshold between VSDIAG and VRESx pin)	All 8 VRESx pins tied together	2.5	-	4.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until transistor test results are valid, C_{SQHx}= 0.12 µF C_{SQLx}= 0.12 µF	-	-	500	µs
Voltage measurement diagnostics (VRESx)						
I_{RESx}	Max diagnostic current into V_{RESx} pin	Normal conditions	-	-	50	µA
$V_{VRESXLO\_th}$	Low voltage threshold for VRESx pin	-	5.0	-	7	V

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{VRESXHI\_th}$	High voltage threshold for VRESx pin	-	13.7	-	18.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until transistor test results are valid.	-	-	100	µs
MOS diagnostics						
$I_{\_MOS}$	MOS test max current	Normal conditions guaranteed by design	-	-	I_{SDIAG}	mA
$t_{SHUTOFF}$	LS/HS MOS turn off under fault condition	Time is measured from the valid LS/ HS MOS current > 100mA to the LS/HS turn off	-	-	4	µs
$t_{FETtimeout}$	FET timeout	Normal conditions	-	-	100	µs
High Squib resistance diagnostics						
R_{SQHIZ}	High load resistance threshold	-	1.07	-	2.1	kΩ
I_{HR}	High resistance current threshold	-	I_{STG}			mA
$t_{DIAGTIMEOUT}$	MOS diagnostic delay time	From/CS ↑ until Transistor test results are valid, C_{SQHx}= 0.12 µF C_{SQLx} = 0.12 µF	-	-	300	µs
Squib resistance diagnostics						
V_{OH}	Output voltage AOUT	High saturation voltage; I_{AOUT} = -500 µA	-	-	VDD-0.2V	V
V_{OL}		Low Saturation Voltage; I_{AOUT} = +500 µA	-	-	0.2	V
I_Z	Tri-State Current AOUT	AOUT = VDD	-	-	1	µA
		AOUT = 0 V	-1	-	-	µA
$R_{SQB\ RANGE}$	Load Resistance Range	-	3.5	-	10.0	Ω
V_{AOUT}	Resistance measurement analog output tolerance $V_{AOUT} = VDD \cdot \left[\frac{1}{10} + \left(0.08 \cdot \frac{R_{SQB}}{\Omega}\right)\right]$	0 Ω ≤ R_{SQB} < 3.5 Ω	V_{AOUT}- 0.095V	-	V_{AOUT}+ 0.095V	V
		3.5 Ω ≤ R_{SQB} ≤ 10 Ω	V_{AOUT}· 0.95V	-	V_{AOUT}· 1.05V	V
I_{SRC}	Resistance measurement current source	V_{DD} = 5.0 V; V_{SDIAG} = 7.0 V to 37 V	38	-	42	mA
I_{SINK}	Resistance measurement current sink	-	45	-	57	mA
I_{SLEW}	Rmeas current di/dt	30% - 70% of ISRC	2	-	11	mA-µs
V_{cmpr}	Voltage threshold on squib pin to shutdown ISRC	-	2.65	-	3.25	V

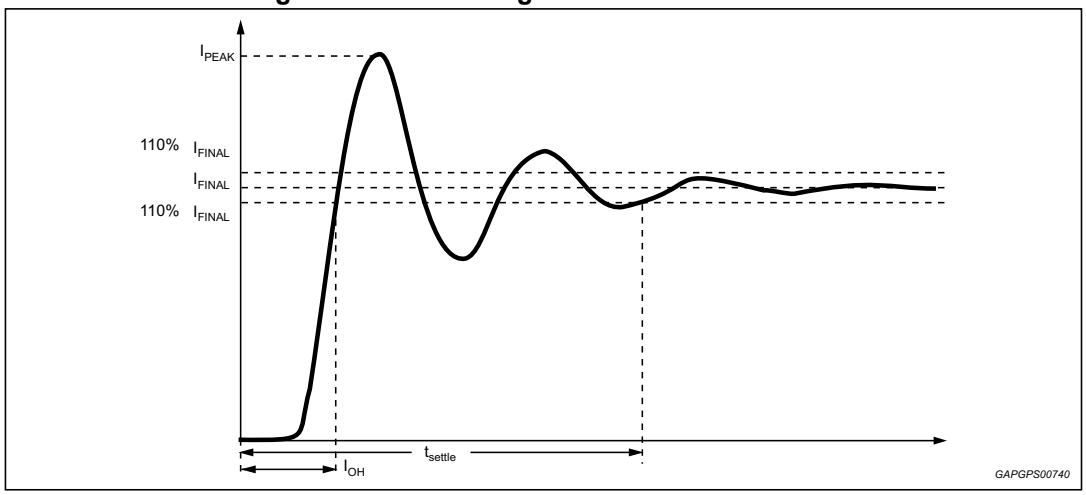
Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{isrcshtdwn}$	Time after voltage threshold crossed for squib pin to shutdown IISRC	Guaranteed by design	-	-	30	µs
$V_{LSDrsqb}$	Voltage threshold on squib pin to shutdown ISRC	-	0.8	-	2.2	V
t_{R_WAIT}	Rmeas wait time 6	Wait time before AOUT voltage is stable for ADC reading	-	-	300	µs
FENx Input pins						
$t_{FENfilter}$	Minimum pulse width	-	12	-	16	µs
I_{FENPD}	Internal pull-down current	VIN = VIL to VDD	20	-	50	µA
V_{FENLO}	Input low voltage threshold	-	0.8	-		V
V_{FENHI}	Input high voltage threshold	-	-	-	2.0	V
$T_{FENLATCH}$	FEN Latch timer	-	0	-	512	ms
t_{FLACC}	FEN latch timer accuracy	-	- 20%	-	20	%
Deployment drivers						
$T_{RESOLUTION}$	Diagnostic timing / resolution	Guaranteed by design, $I_{HS} \geq I_{MEAS}$, $0s \leq T_{MEASURE\_TIME} \leq 3.7$ ms $C_{SQUIB\_HI} = 0.12$ µF $C_{SQUIB\_LO} = 0.12$ µF	22.5	25	27.5	µs
$T_{ACCURACY}$	Diagnostic timing accuracy		-	-	2	LSB
I_{MEAS}	High side driver current limit detect threshold	Guaranteed by design	I_{HSX} x 0.90	-	I_{HSX} x 0.99	A
$V_{breakdown}$	HS or LS breakdown voltage	Voltage across driver = 40 V	-	-	50	µA
$R_{DSonTOTAL}$	Total high and low side MOS on resistance	High side MOS + low side MOS D9:D8="11"; V_{RES} = 7 V; I = 1.6A @95 °C	-	-	2.0	Ω
R_{DSonHS}	High side MOS on resistance	D9:D8="11"; VRES = 7 V; IVRES = 1.6 A;	-	0.3	0.8	Ω
R_{DSonLS}	Low side MOS on resistance		-	0.6	1.2	Ω

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{HS_12A}	High side deployment current limit	Configuration mode 1 bits D9:D8=”00” SQHx shorted to ground; V_{RES} = 7 to 37 V	1.21	-	1.47	A
I_{HS_15A}		Configuration Mode 1 bits D9:D8=”01” SQHx shorted to ground; V_{RES} = 7 to 25 V	1.51	-	1.85	A
I_{HS_175A}		Configuration Mode 1 bits D9:D8=”11” SQHx shorted to ground; V_{RES} = 7 to 37 V	1.76	-	2.14	A
t_{ILIM}	Low side MOS shutdown under short to battery	V_{sqblo}=18 V	90	-	110	µs
I_{LS}	Low side MOS current limit		2.2	-	4.0	A
t_{settle}	Firing current settling time	Time from fire command CS_D rising edge to where firing current remains within specified limits C_{SQUIB_HI} = 0 to 0.12 µF C_{SQUIB_LO} = 0 to 0.12 µF	-	-	150	µs
$t_{DEPLOY-2ms}$	Deployment time	V_{RES} = 7 to 37 V@ I_{HS_12A} V_{RES} = 7 to 25 V@ I_{HS_15A} For I_{HS_12A} and I_{HS_15A} Firing Measured from CS_D rising edge	2.15	-	2.5	ms
$t_{DEPLOY-1ms}$		V_{RES} = 7 to 37 V For I_{HS_175A} Firing Measured from CS_D rising edge	1.15	-	1.40	ms
$t_{DEPLOY-0.65ms}$		V_{RES} = 7 to 37 V For I_{HS_175A} Firing current Measured from CS_D rising edge	0.65	-	0.85	ms

Figure 2. MOS settling time and turn-on time 2



2.4.3 Electrical characteristics - Satellite interface

4.9 V ≤ V_{DD} ≤ 5.1 V; 7 V ≤ V_{RESX} ≤ 37V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5V) ≤ V_{SYNC} ≤ 25 V; 5 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 8. Satellite interface - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{ICHx\_IDLELim}$	Current limit per channel during communication voltage level	High side short to -0.3 V	-75	-	-150	mA
I_{ICHx_HVLim}	Current limit per channel during sync voltage level	High side short to -0.3 V	-100	-	-280	mA
I_{VSATS_max}	VSATS supply current excluding ICHx current	All channels with High side short to -0.3V	-	-	10	mA
$I_{VSATSLIM1}$	VSATS supply current with one channel in current limit during Sync Pulse	High side short to -0.3 V	-	-	-40	mA
$I_{VSYNCLIM1}$	VSYNC supply current per channel with channel in current limit	High side short to -0.3 V	100	-	375	mA
$I_{ICHx\_SB\_OFF}$	Short to battery current when driver is OFF.	ICHx short to battery V(ICHX)-VSATS > 50 mV 50 mV is the maximum threshold to switch OFF driver, TYP is 30 mV	-	-	5	mA
$I_{ICHx\_SB\_ON}$	Max short to battery current when driver is ON.	Guaranteed by design	-	-	25	mA
$I_{ICHxVSATS\_LK\ OFF}$	V_{SATS} leakage current per channel	V_{SATS} =18 V V_{cc} = V_{SYNC} = 0 V measured @ V_{SATS}	-	-	-1	mA

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{ICHxVSYNC\_LK\ OFF}$	VSYNC leakage current per channel	V_{SYNC} = 25 V V_{cc} = V_{SATS} = 0 V measured @ V_{SYNC}	-	-	-1	mA
$I_{OUTLEAK}$	Output Leakage Current ICHX	V_{SATS} = 18 V measured @ pin under test V_{SYNC} = 25 V Analog interface OFF	-	-	1	µA
Vhdp	High side voltage drop (VSATS-VICHX) Per Channel	I = -150 mA; V_{SATS} = 7 V to 14V guaranteed by design	-	-	3.0	V
		I = -70 mA; V_{SATS} = 7 V to 14 V	-	-	1.5	V
		I = -50 mA; V_{SATS} = 7 V to 14 V	-	-	1.0	V
		I = -25 mA; V_{SATS} = 7 V to 14 V	-	-	0.5	V
IFr	IF/I_{out} CH3 & CH4	I_{out} = -5 0 mA	460	-	540	µA
		I_{out} = -5 mA	46	-	54	µA
Itr	Low to high transition current threshold	SPI channel configuration bit <2:0>=111	35.10	-	42.90	mA
		bit <2:0>=110	28.80	-	34.20	mA
		bit <2:0>=101	24.85	-	29.15	mA
		bit <2:0>=100	20.25	-	24.75	mA
		bit <2:0>=011	17.10	-	20.90	mA
		bit <2:0>=010	14.85	-	18.15	mA
		bit <2:0>=001	8.0	-	11.0	mA
		bit <2:0>=000	1.0	-	4.0	mA
V_{CLAMP}	IF/Vx CH3 & CH4 clamp voltage	R_{ext} = 33.0k, 1%; CHx is shorted to GND	0.95* Vdd	-	1.05* Vdd	V
I_{hyst}	Current Threshold hysteresis	Sink current = Ithr at the output (ICHX). Ihyst = trip point high – trip point low	0.05*Itr	-	0.15*Itr	mA
Mdf	De-glitch filter as a function of protocol speed	Manchester Protocol Excluding Osc tolerance; bit<8:7>= 00, 01, 10, 11. bit Time = the smallest bit time allowed in the selected range.	11.7% *bit-Time	-	23.5% *bit-Time	µs

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Bitr	Minimum frequency operating range (Incoming messages fall within this operating range is guaranteed to be accepted by the IC)	Channel configurations bit<8:7> = 00 Test at frq. = 52.33 kHz Test at frq. =13.32 kHz	13.32	-	52.33	kHz
		bit<8:7> =01Test at frq =110.74 kHz Test at frq. = 26.32 kHz	26.32	-	110.74	kHz
		bit<8:7> =10 Test at frq =164.20 kHz Test at frq = 43.50 kHz	43.50	-	164.20	kHz
		bit<8:7>=11 Test at frq. = 250.63 kHz Test at frq. = 62.66 kHz	62.66	-	250.63	kHz
Bitr	Maximum frequency operating range (Incoming messages fall outside this operating range is guaranteed to be rejected by the IC)	Channel configurations bit<8:7> = 00 Test at frq. > 59.14 kHz Test at frq. <11.99 kHz	11.99	-	59.14	kHz
		bit<8:7> =01 Test at frq > 128.37 kHz Test at frq < 23.57 kHz	23.57	-	128.37	kHz
		bit<8:7> =10 Test at frq >194.93 kHz Test at frq < 38.71 kHz	38.71	-	194.93	kHz
		bit<8:7>=11 Test at frq > 309.6 kHz Test at frq < 55.37 kHz	55.37	-	309.6	kHz
Idle	Idle time	CRC disabled: The idle bit time is based on the bit time calculated using the start bits based on the last edge of previous message to 1st rising edge (start bit) of new message If an error is detected then the device shall default to 1.5 times the maximum frequency (minimum bit time). No idle time required after enabling channel	1.5*Tbit	-	-	µs
		CRC enabled:	1.5*Tbit +4µs	-	-	
Tdl & Tdh	IFx/Vx delay	Test with 10K 1% Iref resistor check response from changing between the following current levels. High = 0 to 15 mA, Low = 66 to 15 0mA	-	1	-	µs
Tdl - Tdh	IFx/Vx delay time differential	ICHX outputs with a 500 µs symmetrical pulse in and 500us out.	-	-	0.3	µs

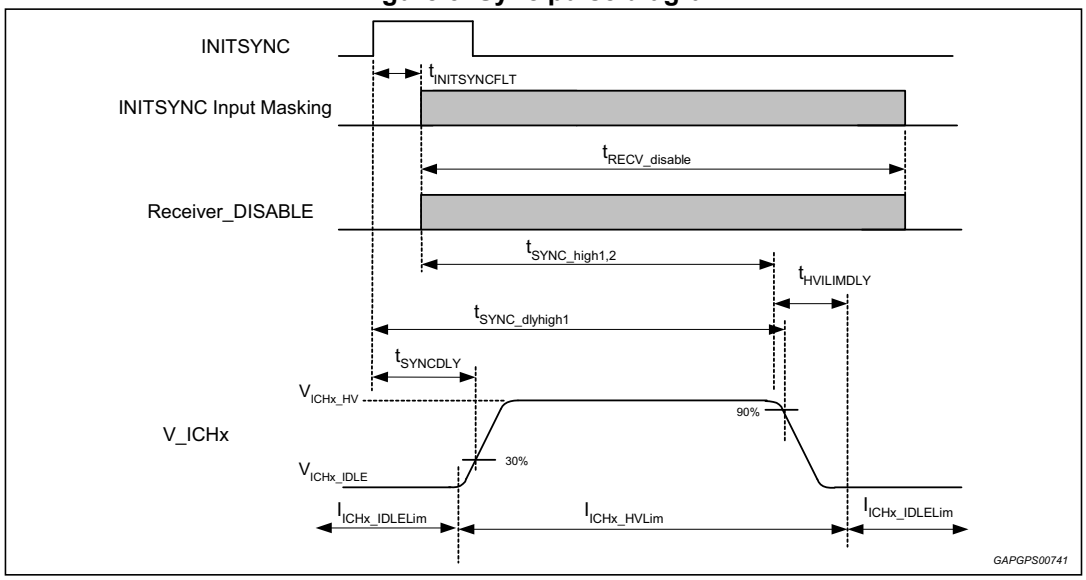
Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{Flt_BATT}	Output fault filter for short to battery	V(ICHX)-VSATS>50mV	12	-	16	µs
t_{Flt_GND}	Output fault filter for short to ground	I_sensor>I_lim	300	-	360	µs
Receive Mode						
V_{ICHx}	Output voltage on pin ICHx (x = 1…4)	I_{ICHx}= [0…50mA]; 7V ≤ V_{SATS} ≤ 14V	VSAT-1	-	VSAT	V
SYNC Mode and High Voltage mode						
V_{ICHx_HV}	Output voltage during High Voltage Mode and SYNC Mode High time	7V ≤ V_{SATS} ≤ 14V (V_{SATS}+6V) ≤ VSYNC ≤ 25V I_{ICHx} = 50mA	V_{ICHx} +4	-	V_{ICHx} +8	V
V_{REG_DO}	Regulator Drop Out voltage	I_{ICHx} = 50mA	-	-	2.5	V
$t_{SYNCDLY}$	Delay time from rising edge of INITSYNC pin to sync pulse voltage active	Measured from INITSYNC pin rising edge to 5% of V_{HV} All Channels	2.7	-	6.6	µs
t_{SYNC_high1}	SYNC pulse high time	-	-7%	20	+ 7%	µs
$t_{SYNC\_dlyhigh1}$	Total delay time from INITSYNC to sync pulse falling edge	MCR D9:D8="00" Measured from INITSYNC pin rising edge to 90% of sync pulse falling edge (V ICHx_HV - V ICHx idle) All Channels using default slew rate	20.3	-	28	µs
t_{SYNC_high2}	SYNC pulse high time	-	-7%	30	+ 7%	µs
t_{SYNC_high3}	SYNC pulse high time data "0" pulse width (High voltage mode)	-	-7%	40	+ 7%	µs
t_{SYNC_high4}	SYNC pulse high time data "1" pulse width (High voltage mode)	-	-7%	80	+ 7%	µs
$t_{RECV\_disable}$	Receiver disable time	MCR bit D2=0	-7%	62	+ 7%	µs
		MCR bit D2=1	-7%	t_{SYNC_highx} typ + 20µs	+ 7%	µs
$t_{riseslewrate}$	High Voltage rise slew rate for ICHx	MCR bit D3=0	0.9	-	2	V/µs
		MCR bit D3=1	0.43	-	1.5	
$t_{fallslewrate}$	High Voltage fall slew rate for ICHx	MCR bit D3=0	0.9	-	2	V/µs
		MCR bit D3=1	0.43	-	1.5	

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{HVILIMDLY}$	HV current limit active time following t_{SYNC_highx}	Guaranteed by design	-	-	12	µs
C_{ICHX}	Capacitance on satellite output for stability (per pin)	ICHx pin to $C_{ICHX} \leq$ 70nH;	10	-	47	nF
INITSYNC input						
$V_{INITSYNCLO}$	Input low voltage threshold	-	0	-	0.8	V
$V_{INITSYNCHI}$	Input high voltage threshold	-	2.0	-	1.0 x VDD	V
I_{ISPD}	Input pulldown current INITSYNC	VIN = VIL to VDD	10	-	50	µA
$T_{INITSYNCFLT}$	Minimum pulse width	-	1.7	-	2.1	µs

Figure 3. Sync pulse diagram



2.4.4 SPI timing

All SPI timing is performed with a 150 pF load on MISO unless otherwise noted

$4.9V \le V_{DD} \le 5.1V$; $7V \le V_{RESX} \le 37V$; $7V \le V_{SDIAG} \le 37V$; $(V_{SATS} + 6V) \le V_{SYNC} \le 25V$; $5V \le V_{SATS} \le 14V$; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10KΩ, ±1%, 100PPM; $-40°C \le T_A \le +95°C$; unless other specified.

Table 9. SPI timing - DC electrical characteristics

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
-	fop	Transfer frequency	dc	-	5.50	MHz
1	tSCK	SCLK, SCLK_S period	181	-	-	ns
2	tLEAD	Enable lead time	65	-	-	ns
3	tLAG	Enable lag time	50	-	-	ns
4	tSCLKHS	SCLK, SCLK_S high time	65	-	-	ns
5	tSCLKLS	SCLK, SCLK_S low time	65	-	-	ns
6	tSUS	MOSI, MOSI_S input setup time	20	-	-	ns
7	tHS	MOSI, MOSI_S input hold time	20	-	-	ns
8	tA	MISO, MISO_S access time	-	-	60	ns
9	tDIS (1)	MISO, MISO_S disable time	-	-	100	ns
10	tVS	MISO, MISO_S output valid time	-	-	60	ns
11	tHO (1)	MISO, MISO_S output hold time	0	-	-	ns
12	tRO	Rise Time (design information)	-	-	30	ns
13	tFO	Fall Time (design information)	-	-	30	ns
14	tCSN	CS_D, CS_S negated time	640	-	-	ns
15	tCLKN	Time between CS rising edge and first transition of SCLK must be higher than tCLKN. It happens when multiple L9662 are connected to the same SCLK and MOSI but with different chip select.	500	-	-	ns

1. Parameters t_{DIS} and t_{HO} shall be measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 4. SPI timing diagram

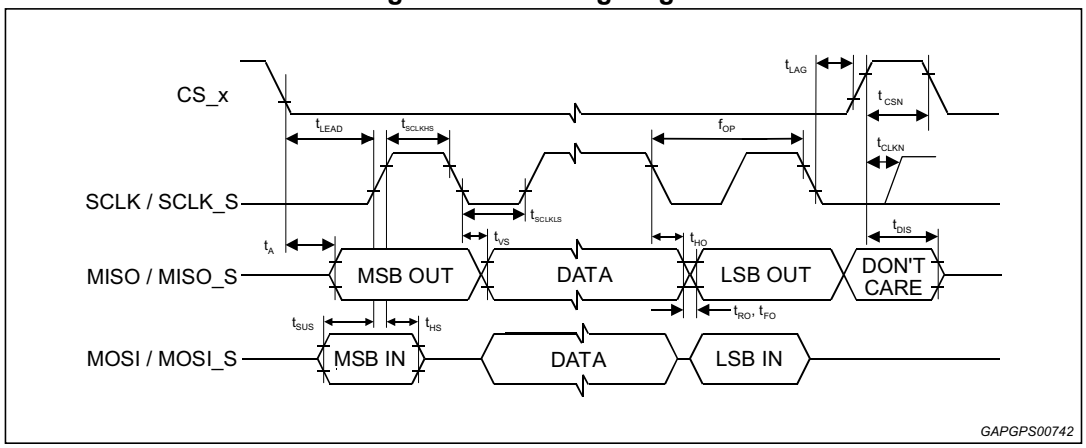


Figure 5. MISO Loading for Disable Time Measurement