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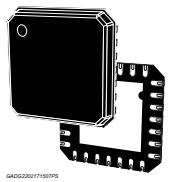
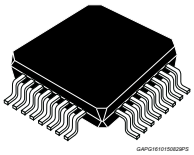
L9663

Automotive PSI5 transceiver IC

Datasheet - production data



VFQFPN28



TQFP32
(Exposed pad down)

Features

- AEC-Q100 qualified
- 2-channel PSI5 transceiver compatible with rev. 1.3 and rev. 2.x
- Manchester coded digital data transmission
- High data transmission speed of 125 kbps (optional 83.3 kbps and 189 kbps)
- High EMC robustness and low emission
- Bootstrap circuits for sync pulses
- Current limitation and voltage clamp on interface pins
- Integrated charge pump stage for pre-regulation with spread spectrum approach
- Integrated FLL module for high accuracy timing control
- Reverse voltage protection structure
- Short to ground tolerant with ±1.5 V ground shift
- 32-bit SPI interface with address multiplexing
- Operating voltage: V_B = 4.8 V (5.2 V for sync pulses with 3.5 V step) to 35 V
- Ambient temperature range: -40°C to 140 °C
- Package: VFQFPN28 or TQFP32EP

Description

The Peripheral Sensor Interface (PSI5) is an interface for automotive sensor applications. PSI5 is an open standard based on existing sensor interfaces for peripheral sensors and offers a universal and flexible solution for multiple sensor applications.

The PSI5 interface allows asynchronous or synchronous operations and different bus modes. The device is compatible with both v1.3 and v2.x PSI5 revisions (limitations are specified inside this document). It operates with a wide range of sensor supply current and variable data word length (8 to 28 bit).

The sensors are connected to the ECU using the same line for power supply and data transmission. The transceiver IC provides a pre-regulated voltage to the sensors and reads in the transmitted sensor data.

The PSI5 interface allows either point to point connection or bussed mode.

Table 1. Device summary

Order code	Package	Packing
L9663	TQFP32 (Exposed pad)	Tray
L9663-TR		Tape & Reel
L9663-1	VFQFPN28	Tray
L9663-TR-1		Tape & Reel

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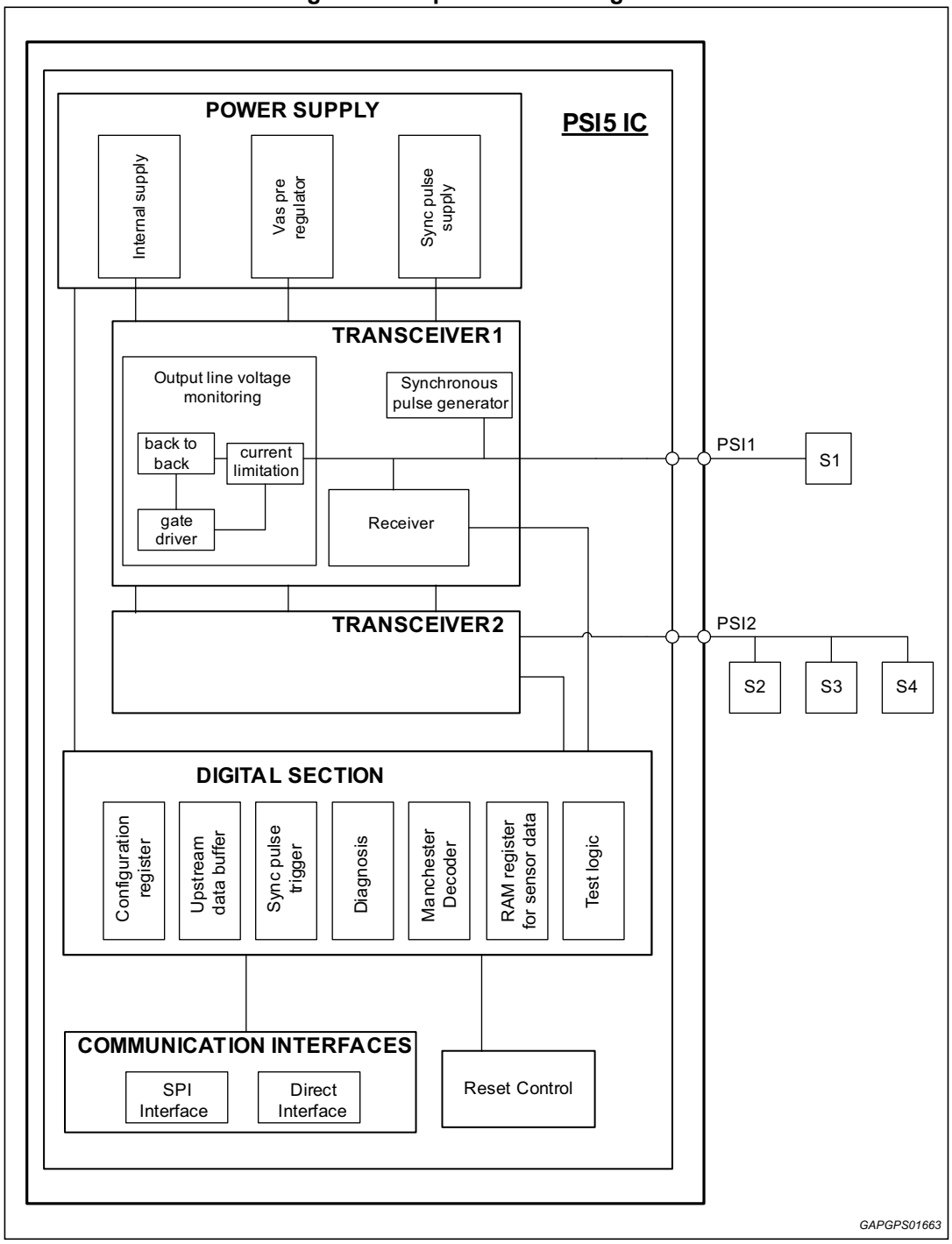
1 Overall description

1.1 Simplified block diagram

Figure 1. Simplified block diagram



1.2 Main functionality

The transceiver IC can be used in two different modes (Mode 1 or Mode 2)[a] . The system configuration called Mode 1 performs the decoding effort of sensor signals in the IC. The system configuration called Mode 2 is a frontend to a PSI5 decoder contained in an external device (typically a µC with a dedicated module).

The transceiver IC can monitor all internally generated relevant voltages, such as V_{SYNCx} V_{AS} and V_PSIx.

The PSI5 interfaces inside the IC are supplied by a separate input pin VAS. If only asynchronous mode is required, the VAS voltage is sufficient for the sensor power supply. When synchronous mode is required, a higher voltage than VAS is needed in order to generate the synchronous pulses. This voltage VSYNCx is generated by a dedicated bootstrap circuit for each channel.

For direct supply from battery, the transceiver IC includes a V_{AS} pre-regulator supplied by VASSUP-pin: the pre-regulator can drive an external FET to regulate the VAS voltage to 7.6 V or 5.3 V. In case of low voltage level at VASSUP, an integrated charge pump is implemented, with supply from VASSUP.

The internal analog and digital circuits are supplied by VB. The external voltage on VDD pin is used to supply the digital output pins; VDD pin can be used to switch the digital outputs from 5 V output level (default) to 3.3 V output level.

The PSI5 transceiver is functional in the whole V_{DD}, VB, VASSUP and V_{AS} power supply range.

The internal voltage supplies (V_{SYNCx}) are automatically activated by the transceiver IC depending on the operating mode whenever they are needed.

Each transceiver interface can be activated and deactivated by an SPI command. At start-up, the interfaces are off by default.

The communication interface block includes two different interfaces. In mode 1, SPI is used for data transfer. In mode 2, the direct interface is used. The data from and to the sensors will be transmitted bit-wise between the transceiver IC and the µC. The data evaluation and error handling for frame errors will be done in the PSI5 controller which is integrated in the µC.

Transceiver 1 and 2 supply the sensors and generate the synchronous pulses for synchronous data transfer (if required) from the sensors to the transceiver and for data transfer from the ECU to the sensors.

A data transfer from the ECU to the sensors can be performed:

- by using sync pulses with different duration (PSI5 2.x standard)
- by masking of sync pulses (PSI5 1.3 and 2.x standard)

The sync pulse trigger can be generated by an SPI command, by a dedicated pin (for connection to the Synchronous Pulse Output Block included in the microcontroller) or by an integrated automatic timer.

a. Mode 1 and Mode 2 are two system architectures which relate on the way L9663 communicates with the microcontroller. Depending on the chosen architecture, the µC must configure the IC with the correct setup.

The Transceivers 1 and 2 limit the current and the PSIx voltage (PSI5-requirement when VAS is too high because of failure in the VAS power supply, less than 11 V in data transmission or less than 16.5 V in sync pulse).

The current modulated signal received from sensor is detected and digitally converted. This sensor data will then either be:

- First Manchester decoded by the Manchester Decoder block with mark space error correction and then transferred to the "receive data buffer" module (Mode 1). The data from the new sensor frames will be saved in a buffer and then will be transferred to the µC via SPI.
- Transferred directly to the µC (Mode 2). In this case the output of the transceiver is a Manchester-coded signal without error correction that falls under microcontroller responsibility.

1.3 VQFPN28 pins description

Figure 2. VQFPN28 pins connection diagram (top view)

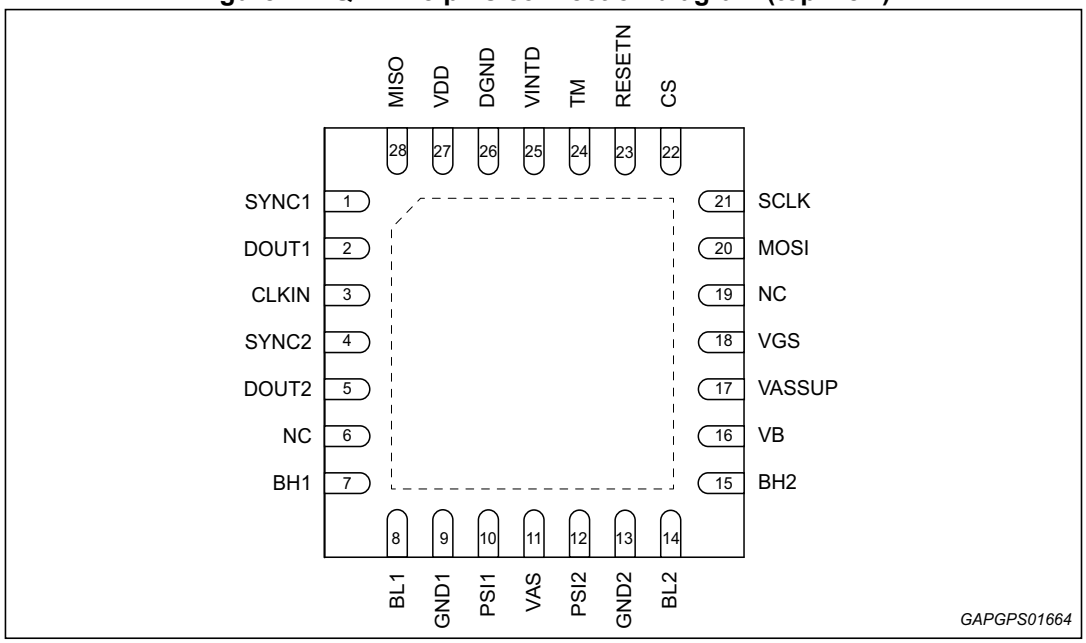


Table 2. VQFPN28 pin-out

Pin	Name	Description	Pin type	
1	SYNC1	Direct interface sync pulse trigger 1	I	local
2	DOUT1	Direct interface 1/Interrupt 1	O	local
3	CLKIN	External clock input	I	local
4	SYNC2	Direct Interface sync pulse trigger 2	I	local
5	DOUT2	Direct interface 2/Interrupt 2	O	local
6	NC(1)	-	-	-
7	BH1	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 1	I/O	local
8	BL1	Bootstrap capacitor pin 2, transceiver 1	I/O	local
9	GND1	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
10	PSI1	PSI5 Interface 1	I/O	global
11	V_{AS}	PSI5 Interface pre-regulated voltage supply	supply	local
12	PSI2	PSI5 Interface 2	I/O	global
13	GND2	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
14	BL2	Bootstrap capacitor pin 2, transceiver 2	I/O	local
15	BH2	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 2	I/O	local

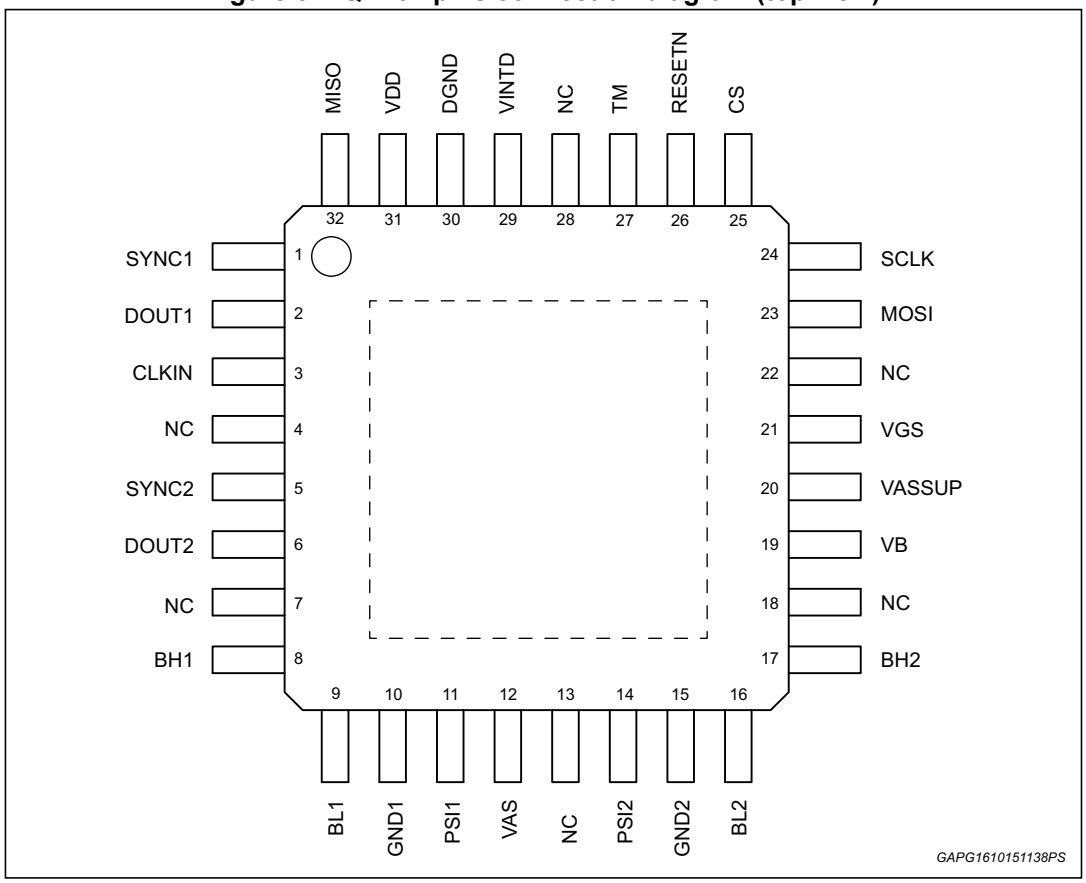
Table 2. VQFPN28 pin-out (continued)

Pin	Name	Description	Pin type	
16	V_B	Input voltage supply	supply	global
17	V_{ASSUP}	VAS pre-regulator and charge pump voltage supply	supply	global
18	V_{GS}	Gate driver for V_{AS} pre-regulator	I/O	local
19	NC(2)	-	-	-
20	MOSI	SPI input	I	local
21	SCLK	SPI Clock	I	local
22	CS	SPI Chip Select	I	local
23	RESETN	Reset	I	local
24	TM	Test-mode pin(3)	I	local
25	V_{INTD}	Internal digital supply voltage	supply	local
26	DGND	Digital ground	supply	local
27	V_{DD}	Digital I/O supply	supply	local
28	MISO	SPI output	O	local

1. Not connected internally, must be left open.
2. Not connected internally, it can be connected to GND externally.
3. It must be connected to GND, for safety reasons.

1.4 TQFP32 pins description

Figure 3. TQFP32 pins connection diagram (top view)



Note: The exposed pad is electrically shorted to the substrate and to pins GND1 and GND2. These three nodes have to be kept shorted on the application.

Table 3. TQFP32 pin-out

Pin	Name	Description	Pin type	
1	SYNC1	Direct interface sync pulse trigger 1	I	local
2	DOUT1	Direct interface 1/Interrupt 1	O	local
3	CLKIN	External clock input	I	local
4	NC[2]	-	-	-
5	SYNC2	Direct Interface sync pulse trigger 2	I	local
6	DOUT2	Direct interface 2/Interrupt 2	O	local
7	NC[(1)]	-	-	-
8	BH1	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 1	I/O	local
9	BL1	Bootstrap capacitor pin 2, transceiver 1	I/O	local

Table 3. TQFP32 pin-out (continued)

Pin	Name	Description	Pin type	
10	GND1	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
11	PSI1	PSI5 Interface 1	I/O	global
12	V_{AS}	PSI5 Interface pre-regulated voltage supply	supply	local
13	NC(2)	-	-	-
14	PSI2	PSI5 Interface 2	I/O	global
15	GND2	Ground return for PSI5 interface (analog ground and substrate ground)	supply	local
16	BL2	Bootstrap capacitor pin 2, transceiver 2	I/O	local
17	BH2	Bootstrap capacitor pin 1 or SYNC voltage supply (from ECU), transceiver 2	I/O	local
18	NC(1)	-	-	-
19	V_B	Input voltage supply	supply	global
20	V_{ASSUP}	VAS pre-regulator and charge pump voltage supply	supply	global
21	V_{GS}	Gate driver for V_{AS} pre-regulator	I/O	local
22	NC2	-	-	-
23	MOSI	SPI input	I	local
24	SCLK	SPI Clock	I	local
25	CS	SPI Chip Select	I	local
26	RESETN	Reset	I	local
27	TM	Test-mode pin(3)	I	local
28	NC(2)	-	-	-
29	V_{INTD}	Internal digital supply voltage	supply	local
30	DGND	Digital ground	supply	local
31	V_{DD}	Digital I/O supply	supply	local
32	MISO	SPI output	O	local

1. Not connected internally, must be left open.
2. Not connected internally, it can be left open or connected to GND externally.
3. It must be connected to GND, for safety reasons.

1.5 Maximum ratings

Within the maximum ratings, no damage to the component shall occur. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

All maximum ratings can occur at the same time.

All analog voltages are related to the potential at substrate ground (GND1 and GND2, internally shorted), all digital voltages are related to DGND.

Operative voltage conditions are specified in *Section 6*.

Table 4. Pin maximum ratings

Symbol	Description	Min	Max	Unit
Power supply				
V_B, V_{ASSUP}	Input voltage range	-0.3	40	V
V_{AS}	Pre-regulated voltage range	-0.3	40	V
V_{DD}	Supply voltage range for digital I/O pins	-0.3	6.5	V
V_{INTD}	Internal digital supply voltage	-0.3	4.6	V
BHx, BLx	Voltage range of bootstrap capacitor or SYNC voltage supply (from ECU)	-0.3	40	V
Other pins				
PSI1, PSI2	Voltage of sensor interface	-1.5	40	V
V_{GS}	Pre-regulator gate voltage range	-0.3	40	V
RESETN	Reset input pin range	-0.3	6.5	V
TM	Test mode input pin range	-0.3	6.5	V
CLKIN	Clock input pin range	-0.3	6.5	V
CS, SCLK, MOSI	SPI communication pin range	-0.3	6.5	V
MISO	SPI communication pin range	-0.3	V_{DD}+0.3≤6.5	V
D_{OUT1}, D_{OUT2}	Direct interface pin range	-0.3	V_{DD}+0.3≤6.5	V
SYNC1, SYNC2	Sync pulse trigger input range	-0.3	6.5	V
ESD robustness				
-	ESD according to Human Body Model (HBM), Q100-002 for pins PSIx, VB, VASSUP; (100 pF/1.5 kΩ)	±4000	-	V
-	ESD according to Human Body Model (HBM), Q100-002 for all other pins; (100 pF/1,5 kΩ)	±2000	-	V
-	ESD according to Charged Device Model (CDM), Q100-011 Corner pins	±750	-	V
-	ESD according to Charged Device Model (CDM), Q100-011 Non-corner pins	±500	-	V

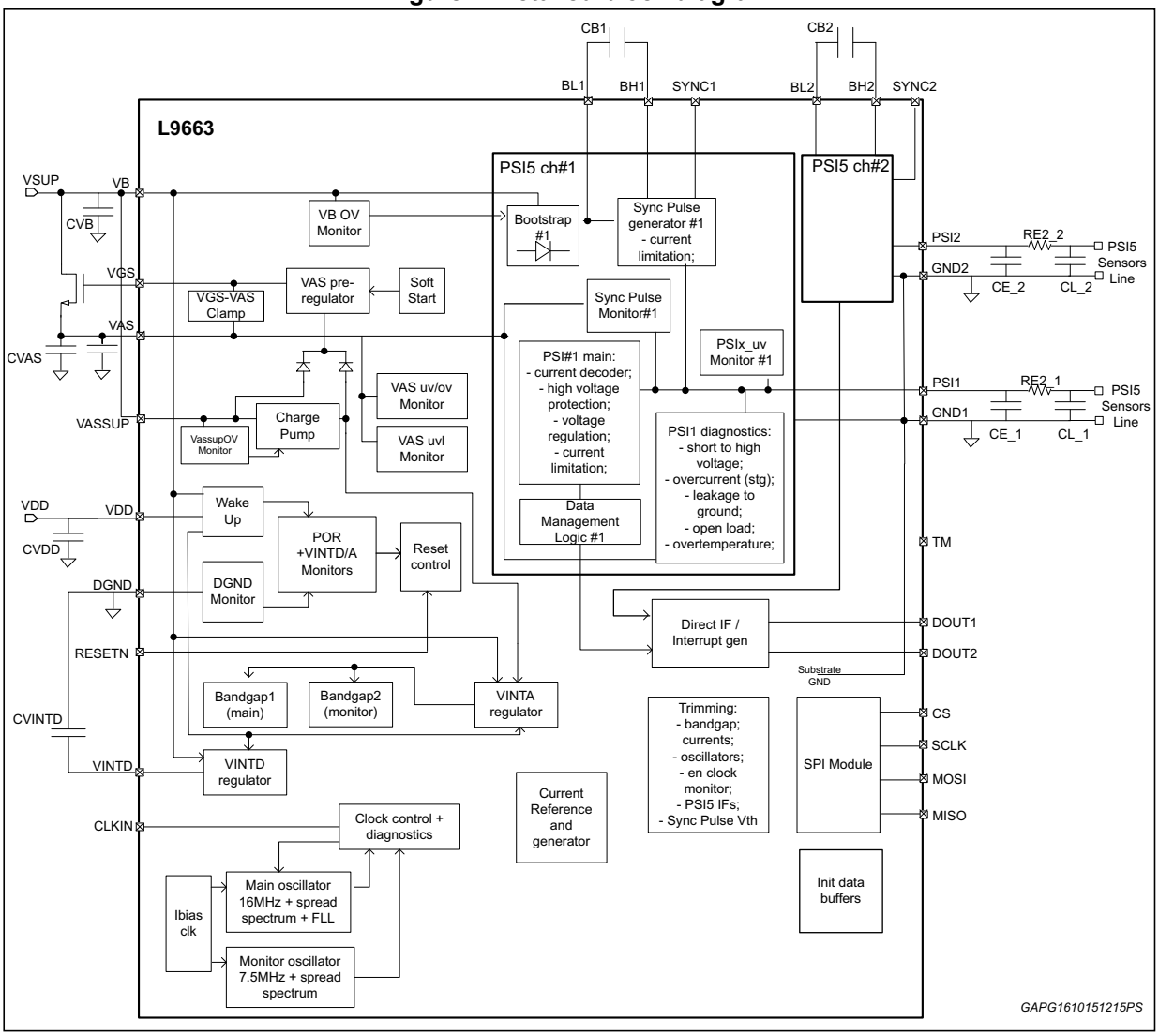
Table 4. Pin maximum ratings (continued)

Symbol	Description	Min	Max	Unit
Temperature				
T_a	Ambient operating temperature range	-40	140	°C
T_j	Junction operating temperature range	-40	175	°C
Rthja	Package thermal resistance (on PCB JEDEC 2s2p)		45	°C/W

The device offers a high level of flexibility on power supply configuration. The calculated maximum power dissipation can reach 1.6 W considering the worst case configuration.

1.6 Detailed block diagram

Figure 4. Detailed block diagram



The high supply voltage of the IC can be a battery or a regulated voltage provided by the ECU.

To reduce disturbances on the voltage supply which might have a negative influence on the PSIx interface and therefore lead to bit errors, a PI filter can be employed in the supply line.

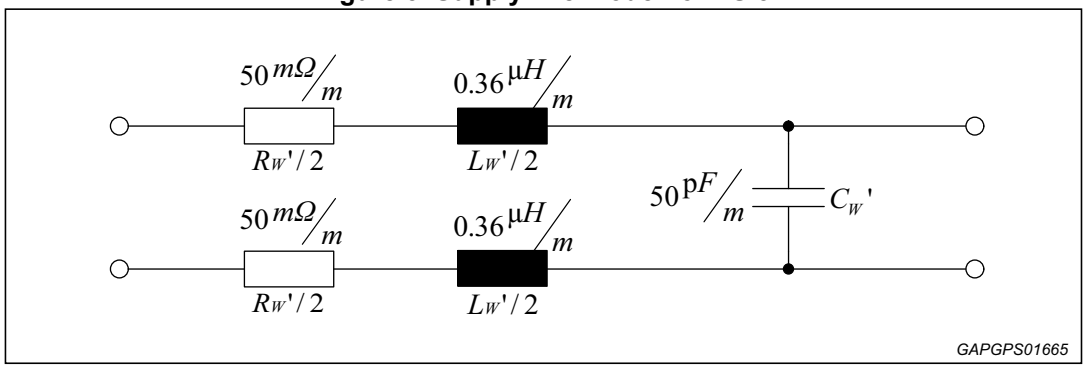
Possible power supply configurations[b] are:

- VB, VASSUP connected to VSUP, VAS and V_{SYNCx} generated by the IC with external components (as in the above figure);
- VAS, VB, VASSUP connected to VSUP, V_{SYNCx} generated by bootstrap, no external MOS, VGS pin open;
- VB, VASSUP, BH1, BH2 connected to VSUP, no external capacitors CBx, VAS generated by IC pre-regulator and external MOS;
- VB connected to VSUP, VASSUP connected to 0V (charge pump off), VAS supplied by an external source and VSYNCx generated by the IC with external components.

The values of the external components RE2_x, CE_x and CL_x are specified in PSI5 standard.

The assumed line model for the PSI5 interface on which the transceiver IC operates is as follows:

Figure 5. Supply line model for PSI5



b. The high supply voltage VSUP must be in the correct operative range of connected pins.

1.7 Power up sequence

When VDD is higher than the startup threshold and VB is available the IC is switched on.

To reduce disturbances on its voltage supply, the transceiver IC does a staggered startup of its internal voltage supplies.

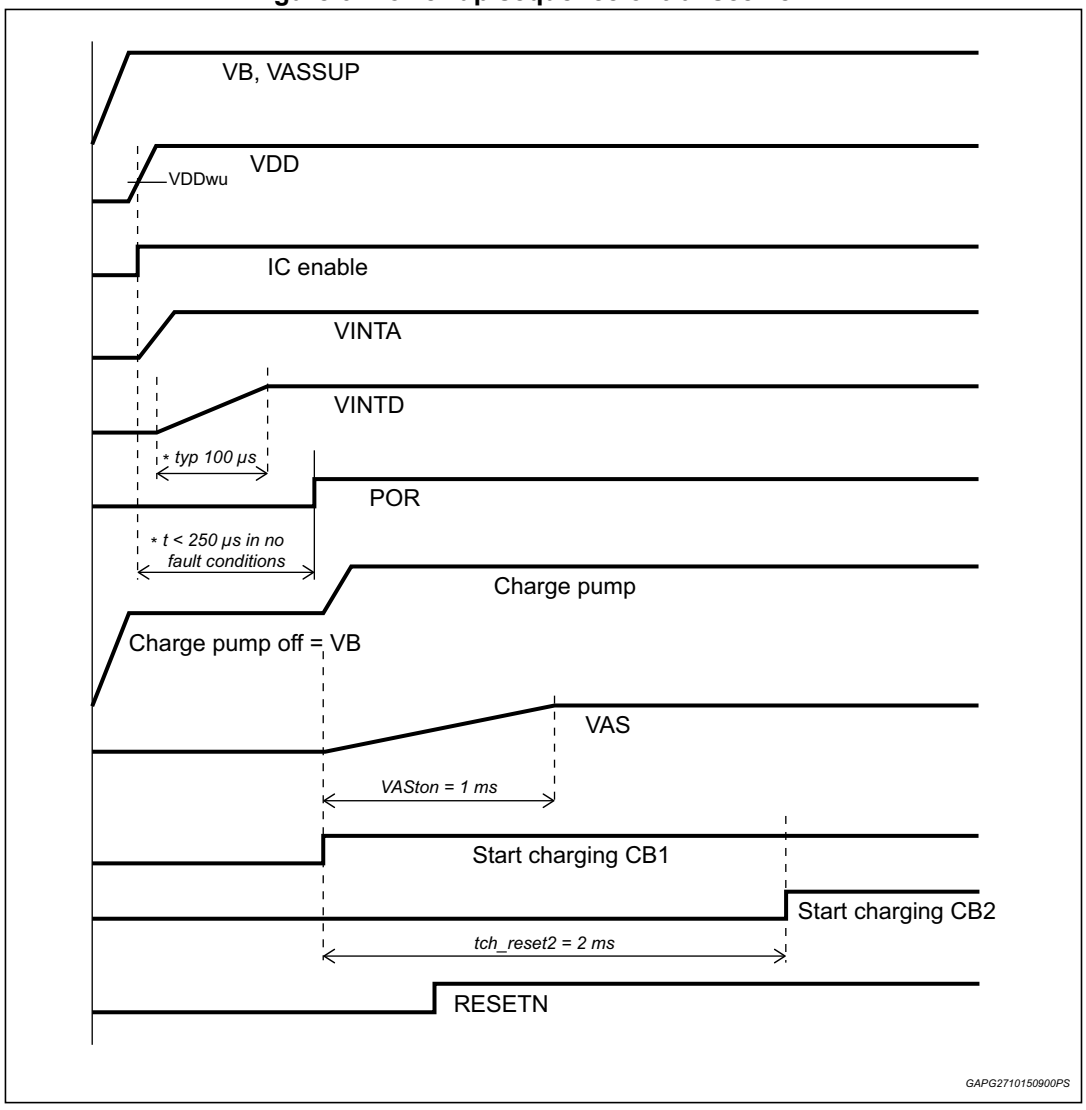
While RESETN is low, the PSIx lines are deactivated to reduce power consumption and to increase system safety.

The transceiver IC can be configured to operate in the standard current mode (4 mA up to 19 mA) or in the extended current mode (4 mA up to 35 mA). Moreover, both channels can be configured to allow the extension to a maximum quiescent current of 45 mA, only in case of asynchronous mode.

The synchronous sensors send data only after a synchronous pulse is triggered via the dedicated pin or by SPI.

The following figure shows a power-up example.

Figure 6. Power-up sequence of transceiver IC

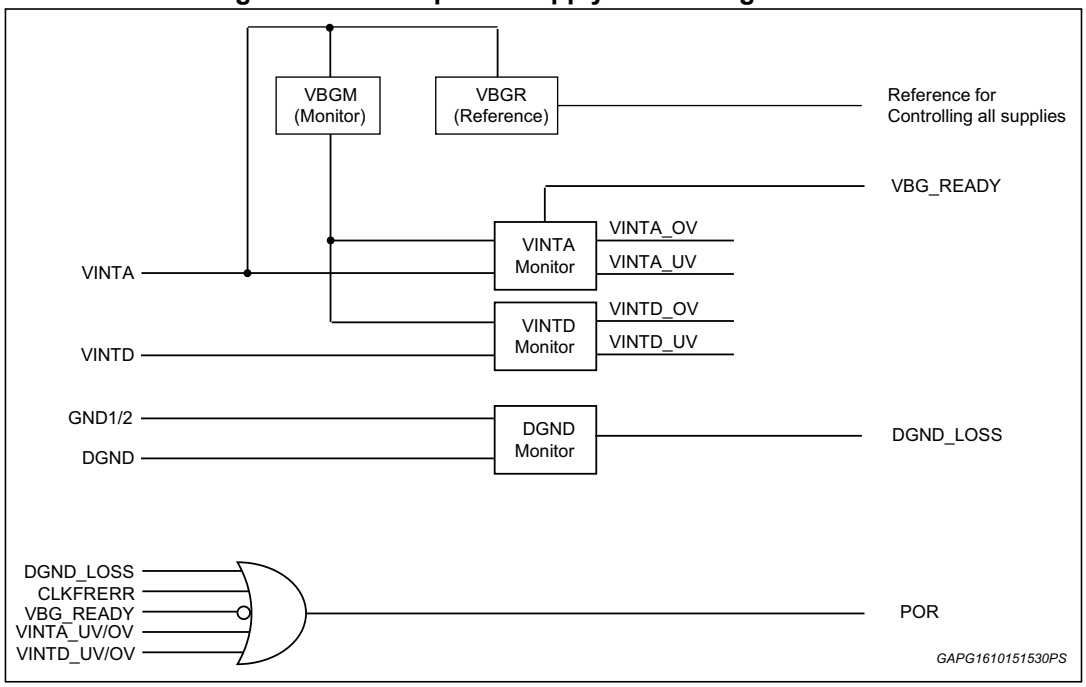


2 Power supply

2.1 Internal supply

The internal analog and digital part is supplied by the supply voltage VB. The necessary power supply for the internal digital and analog parts is generated internally by the transceiver IC. The generated voltage is monitored. In case of under/over voltage, the transceiver IC performs a power on reset (POR).

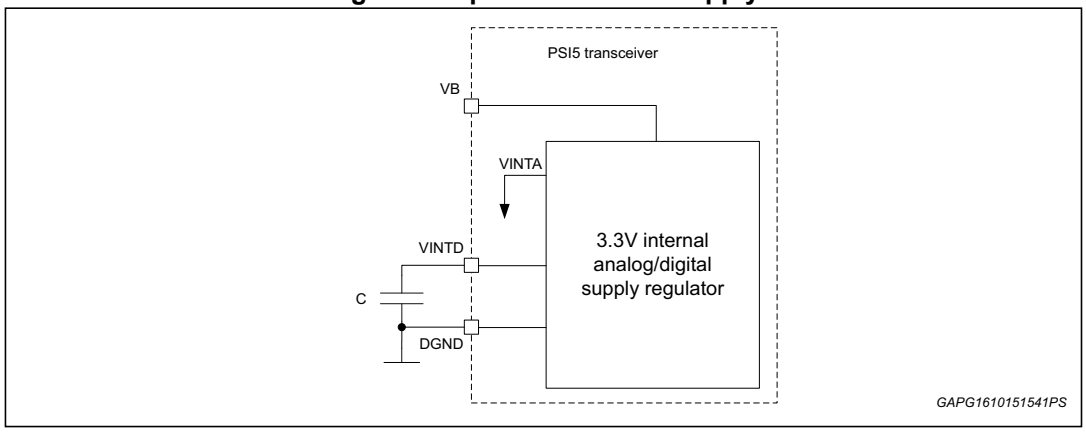
Figure 7. Internal power supply and reset generation



Basic features:

- Voltage regulator
- Under / Over voltage monitoring
- Reset generation of the IC in case of under / over voltage

Figure 8. Input structure of supply



A ceramic capacitor with a typical capacitance of 100 nF is required as a blocking capacitor close to the pins V_{DD} and VB.

The internal supply voltages V_{INTD} (supply voltage for digital part) and V_{INTA} (supply voltage for analog part) are monitored for under voltage and over voltage to prevent the transceiver IC from malfunction. The reference for the voltage monitoring is a bandgap voltage, supplied by V_{INTA}. The device integrates two separated instances of bandgap voltage regulators; one of these bandgaps is used as voltage reference for the internal regulators, while the other one is used for monitoring the voltage levels. In case of under or over voltage, the transceiver IC is set into reset: outside reset thresholds full functionality is granted.

The functionality of the digital part only depends on the voltages on V_{INTD}. In order to improve noise emissions and stability of the regulator, the digital supply line needs an external decoupling 100 nF ceramic capacitor to be connected between V_{INTD} and DGND and close to them.

DGND ground line is protected against ground loss scenarios. In case DGND line would be at least $DGND_{OPEN}$ above the reference ground lines GND1/2, a POR is asserted.

The transceiver IC returns to normal operation with full functionality as soon as the POR is released.

2.2 V_{AS} supply and pre-regulator

The V_{AS} pre-regulator sets the V_{AS} voltage if no regulated voltage with the necessary value is available in the ECU.

The pre-regulator is designed for two different regulated voltages at V_{AS}: 5.3 V or 7.6 V, selectable by a SPI command. The supply of external FET can be chosen at application level according to the required voltage at VAS pin.

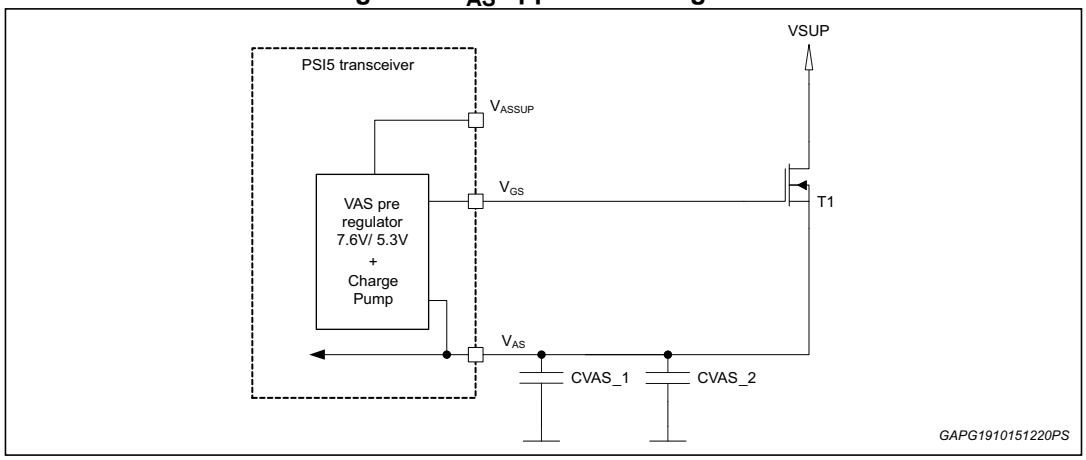
Two possible applications are:

- V_{AS} typical of 5.3 V; external FET supplied by ECU internal voltage, typically 6 V .
- V_{AS} typical of 7.6 V; external FET directly supplied from battery, from 8 V to 35 V.

Basic features:

- Gate control for an external n-ch FET transistor with integrated charge pump stage
- Gate control is switched on if no power on reset condition is present
- Configurable output voltage: either 5.3 V or 7.6 V.

Figure 9. V_{AS} application diagram



When POR is active, the V_{GS} output pin is driven low to keep external N-ch switched off. The V_{AS} pre-regulator is automatically activated with a soft start at POR and automatically switched off, after a filter time, if V_{AS} falls below V_{VASU_off}. It can be later controlled off or on by means of a dedicated VAS_EN bit. To protect the external component from exceeding maximum allowed gate to source voltage if VAS is shorted to ground by a fault, an internal passive clamp is implemented on V_{GS}.

The integrated charge pump, supplied by VASSUP, assures proper voltage regulation in case of low voltage conditions. It is automatically switched off in case the voltage on V_{ASSUP} is high enough to allow proper regulation.

If the pre-regulator is not needed, the VAS_EN bit can be set to '0' to switch off the pre-regulator itself. The pin V_{GS} can be left open, and the V_{AS} pin directly connected to the regulated voltage in the ECU.

The pre-regulator is active independently of RESETN input pin if the supply voltage of the internal analog/digital circuits is available.

2.3 Voltage supply for synchronous pulse generation V_{SYNCx}

To use synchronous PSI5 sensors and for ECU-to-sensor communication, the transceiver IC needs to generate synchronization pulses. These require a voltage which is higher than V_{AS}.

This module generates the necessary voltage V_{SYNCx} by two bootstrap circuits. Two capacitors with two transceiver IC pins each are used as external components of this module.

The bootstrap blocks start pre-charging the external capacitors after POR (with a 2 ms time gap between the first and second block).

The bootstrap circuits are enabled by default, activated by internal logic with timing sync pulses dependent, and can be disabled later on through a dedicated SPI command. The bootstrap block can recharge the capacitor so that subsequent sync pulses are allowed with a minimum period of 200 µs.

A useful option is the possibility to connect the BHx pin directly to a high voltage rail. In this configuration, VB has also to be connected to the same high voltage rail and the bootstrap

circuit can be bypassed by disabling it through the dedicated SPI command (bit 12 of CH1_CR2, CH2_CR2, writable during PROG phase).

The bootstrap blocks are automatically switched off in case the voltage on VB is high enough to allow proper regulation. In this case both CBx capacitors should be omitted.

The V_{SYNCx} voltage can supply a 2.5 V minimum sync pulse as per PSI5 v2.x low power mode down to V_B = 4.8 V and a 3.5 V minimum sync pulse down to V_B = 5.2 V, with a maximum quiescent current level of 35mA and down to minimum 200 µs period between sync pulses. The block is protected against reverse feeding to V_B.

The bootstrap module is fully functional while V_B and V_{DD} are all inside their specified voltage ranges.

2.4 Power supply for PSI5 sensor line

Basic features:

- Reverse voltage protection structure
- Voltage limitation and current limitation for PSIx input/output
- Protection against negative voltages on PSIx transceiver pin due to ground shifts
- Disconnection of PSIx from V_{AS} in failure cases

The PSI5 transceiver IC is supplied directly from the pin V_{AS}. It includes blocks with the following functionalities:

- Reverse voltage protection structure and gate driver block for
  - Voltage clamp on PSIx in case of V_{AS} fault
  - Backward voltage supply blocking mechanism from PSIx to V_{AS}
  - Sensor supply by switching V_{AS} to the PSIx pin
  - Disconnection of PSIx from the VAS if required or in failure cases
- Under voltage detection block to implement cross coupling test between the two channels (see *Section 3.7.5* and *4.2*)
- Receiver block for Sensor Data receive (see *Section 3.1* for details).

The reverse voltage protection structure is also used to switch off the PSIx transceiver channel, if:

- the local junction temperature exceeds its maximum rating and the channel is in overcurrent
- an overcurrent condition on PSIx is detected (STG)
- a short to battery is detected
- it is requested via SPI or RESETN pin.

In case of short to battery on the PSIx lines, there is no interference to any other IC pin/supply including SPI.

The two interfaces can be enabled by SPI command, and the enable has effect only if VAS under voltage signals are not asserted.

If an over temperature condition (OT) occurs, the interface that is also in overcurrent condition is switched off and a failure bit is set. The fault bit is latched and cleared only when a SPI switch off command is sent for confirmation on the line that was automatically switched off. The shutoff of one interface does not affect the second interface.

If an overcurrent condition on PSIx is detected, the current limitation is active and after a filter time t_{filt} a fault bit is set and the interface is shut off. In order to switch on again, the interface must be first switched off by SPI and then switched on, as for over temperature.

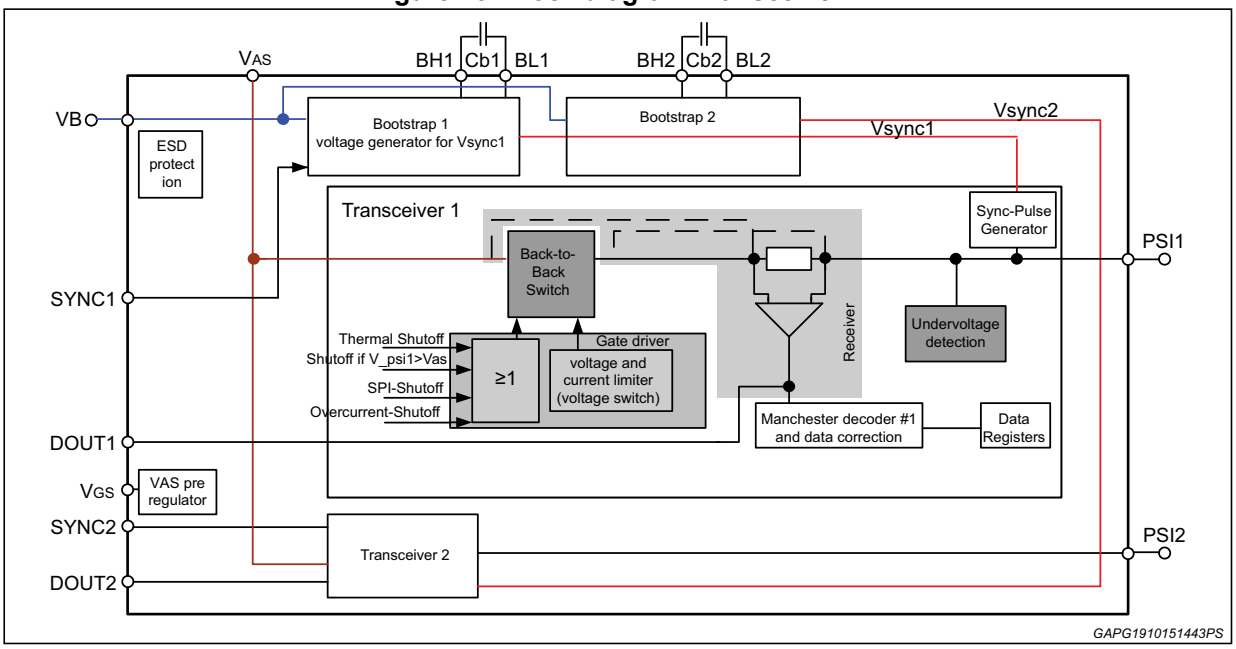
The channels' switch off by overcurrent can be disabled if the corresponding bits STG_MASK for every channel are set in the SPI registers.

During start up, a configurable blanking time is implemented (128 µs/5 ms/10 ms, see BLANKING_SEL bits in SPI register); during this time current limitation is active, even though the interface will not shut off for overcurrent, thermal shutdown is always active, the PSI5 receiver is disabled, and some fault flags are masked (short to battery, under voltage, leakage to ground).

The quiescent current is monitored for minimum and maximum value, depending on the range selected by SPI (CH1_CR1, QC_SEL bits). In failure case the corresponding bit in the diagnostic register is set (SR2).

The voltage at PSIx is compared with VAS to monitor short to battery condition: if an over voltage occurs PSIx is disconnected from VAS and the corresponding bit in diagnostic register is set (STBx in SR2), In over voltage condition also low quiescent current bit is set (OLx in SR2) after a transient time.

Figure 10. Block diagram Transceiver 1



2.5 Frequency references

The device comes with an integrated accurate oscillator, used for any of the internal circuitry, with no need of external connections or components. The nominal clock frequency is 16 MHz with a ±5% accuracy.

Should the application need some more accurate timing reference, a discrete pin CLKIN is provided. An external clock reference can be connected to this pin. The PSI5 transceiver IC offers an integrated FLL module that tracks this input to provide a high accurate clock reference (±1%). This feature can be used especially if accurate timeslot control needs to be achieved.

External signal on CLKIN can be configured as follows (see CLKIN_CFG bits in GCR1 SPI register):

- 1 MHz square signal
- 4 MHz square signal
- No signal (Not connected pin)

Pin CLKIN can be grounded when not used. The pin input circuit implements a pull-down structure.

The FLL module tracking the CLKIN signal is off by default.

The PSI5 transceiver IC implements a safety function for monitoring the device clock reference, both in case it is derived from the CLKIN signal through the FLL module or internally generated. In the first condition the monitoring is always activated, while in the second condition it can be enabled by programming in ST (storing a '1' in a dedicated OTP[c] bit) and another oscillator generator is used for monitoring.[d]

When the CLKIN_CFG is set, the FLL tries to close the LOOP and a mask counter of T_CKMSK (16 ms MAX) is used to count the maximum transient time.

During this time, regardless the CLK frequency the CKER_DETECT is masked, i.e the device doesn't detect a clock error.

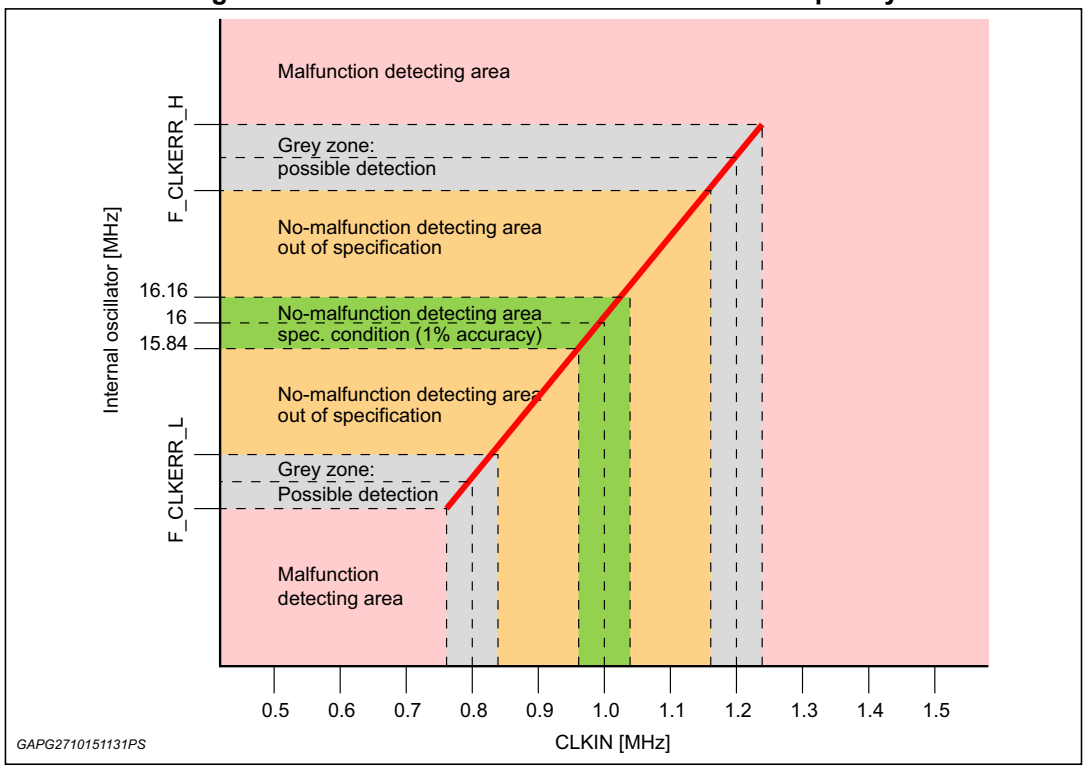
After this time, if the CLKIN frequency is in the correct range, the loop is closed and the CLK frequency is inside the 1% tolerance; if the CLKIN frequency is outside the malfunction detecting range, a clock error is detected after a detection time T_CKERD, the device is reset and the CLK_FLT is set so that the µC can read the reset source.

The T_CKERD and the transient during detection time depend on the CLKIN frequency behavior; the figure below shows the behavior of the internal oscillator as function of the external one.

c. One Time Programmable bit: it can be programmed by ST only.

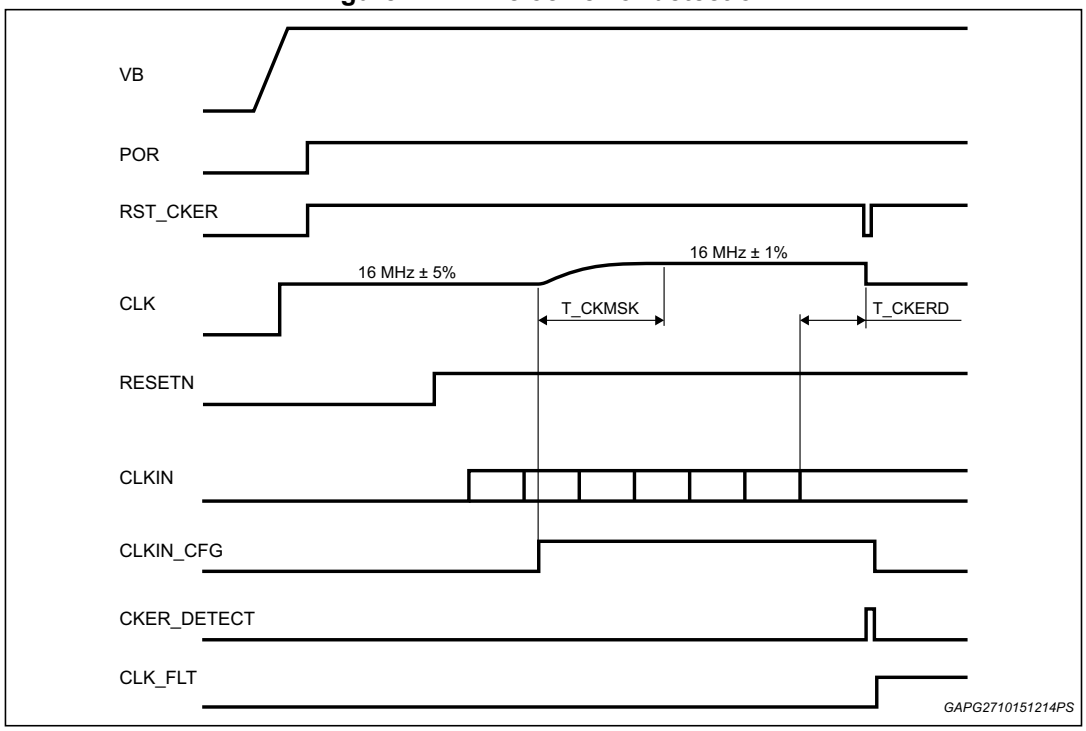
d. For clock error detection by internal monitor oscillator see errata n.3367, *Section 7: Errata*.

Figure 11. Internal oscillator vs external clock frequency



If the CLKIN is stuck the device behavior is shown in the figure below: in this case during the detection time the tolerance is still inside the 1% tolerance until the device enters reset (T_CKERD max 260 µs).

Figure 12. FLL clock error detection



2.6 Reset handling

Four different sources are considered in resetting the IC:

- POR (Power On Reset, see *Section 2.1*)
- RESETN pin
- SW_RESET
- CKER_DETECT

All these sources of reset, when asserted, will switch off the PSIx lines and reset to default value the device registers (including those registers for configuration).

Additionally to the hardware resets (by pin/POR), a reset can also be initiated by software (SW_RESET).

The command SW_RESET initiates a soft reset-sequence if all of the following conditions are fulfilled (see also the DCR register in SPI section):

- unlocked state: it means that if the UNLOCK command is not received the command SW_RESET has no effect;
- The command SW_RESET is sent in next SPI communication of the unlock command.

A SW_RESET initiates soft reset-sequence and resets all digital parts of the device, except POR and RST flag that is set in SR3 register.

3 Satellite interface

3.1 Receiver with digital sampling and filtering

This module has the following features:

- The output current signal is mirrored and converted to the digital domain
- Automatic synchronization on entire PSI5 frames
- Fast DAC digital conversion of sensed currents with digital filtering
- Static DC current set point tracking of PSI5 quiescent current.
- Tracking of modulated PSI5 current signal

The quiescent current tracking can be configured to work in two ways (reg. ADVSET1, ADVSET3, bits FREEZE_DIS): continuous mode tracking or tracking between consecutive frames till the first edge of a new frame is recognized. In the second case, the quiescent current is frozen till the end of the frame.

To recognize the PSI5 current signal level the receiver compares the digitally converted and filtered current with a threshold. This threshold can be fixed or dynamic, depending on the configuration selected by SPI (reg. ADVSET).

In fixed threshold mode the user must program the right delta current threshold, according to the application requirements. The threshold is obtained as tracked quiescent current plus the programmed threshold.

In dynamic threshold mode, the threshold is dynamically adapted considering the PSI5 current input signal.

For detailed explanation on all the possible configurations refer to ADVSET registers section.

Depending on the selected configuration, the threshold for the sensor signal can be permanently tracked, separately for each PSI5 interface. The IC is designed to compensate erratic changes of the quiescent current in the bus according to PSI5 standard requirements.

The v2.x standard low power mode is not supported with dynamic threshold mode.

Micro cuts up to 10µs do not affect the DC current tracking in a way that more than one frame will be lost.

The PSI5 Receiver is designed to operate at:

- 83.3 Kbps typical (slow mode)
- 125 Kbps typical (standard mode)
- 189 Kbps typical (fast mode).