



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

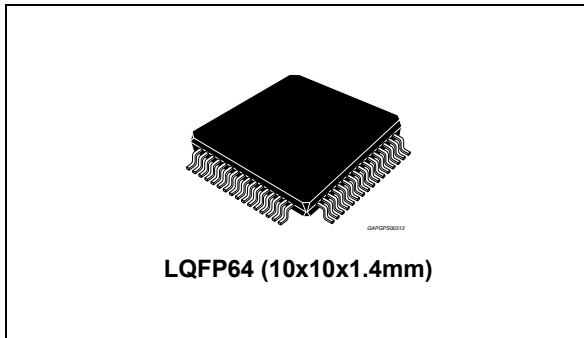
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Automotive user configurable airbag IC

Datasheet - production data



Features



- AEC-Q100 qualified
- Energy reserve voltage power supply
 - High frequency boost regulator, 1.882 MHz
 - Output voltage user selectable, 23 V or 33 V $\pm 5\%$
- User configurable linear power supplies
 - 5.0 V and 7.2 V $\pm 4\%$ output voltages
 - External pass transistor
- Fully integrated 3.3 V $\pm 4\%$ linear regulator
- Battery voltage monitor and shutdown control with wake-up control
- System voltage diagnostics with integrated ADC
- Crossover switch
 - Crossover performance, max 3 Ω , 600 mA max.
- Squib deployment drivers
 - 4 channel HSD/LSD
 - 25 V maximum deployment voltage
 - 1.2 A @ 2 ms and 1.75 A @ 0.5/0.7 ms deployment profiles
 - Integrated safing FET linear regulator, 20 V/25 V nominal
 - Current monitoring
 - Rmeasure, STB, STG and leakage diagnostics
 - High and low side driver FET tests
 - Safing FET test
- User customizable safing logic
- Two channel PSI-5 remote sensor interface (asynchronous mode), [only for L9678P-S version]
- Four channel hall-effect, resistive or switch sensor interface
- ISO9141 transceiver
- Dual channel configurable high-side/low-side LED driver
- Watchdog timer
- Two integrated oscillators: 7.5/16 MHz
- Temperature sensor
- 32 bit SPI communications
- Minimum operating voltage = 6 V
- Operating temperature, -40 °C to 95 °C
- Packaging - 64 pin

Table 1. Device summary

Order code	Package	Packing	Remote sensor interface
L9678P	LQFP64 (10 x 10 x 1.4 mm)	Tray	No
L9678PTR		Tape & Reel	No
L9678P-S	LQFP64 (10 x 10 x 1.4 mm)	Tray	Yes
L9678PTR-S		Tape & Reel	Yes

Contents

- 1 Description 11**
- 2 Absolute and operative maximum ratings 12**
 - 2.1 Absolute maximum ratings 12
 - 2.2 Operative maximum ratings 14
 - 2.3 Pin-out description 16
- 3 Overview and block diagram 17**
- 4 Start-up power control 19**
 - 4.1 Power supply overview 19
 - 4.2 Power mode control 20
 - 4.2.1 Power_off mode 21
 - 4.2.2 Sleep mode 21
 - 4.2.3 Active mode 21
 - 4.2.4 Passive mode 21
 - 4.2.5 Power-up and power-down sequence 23
 - 4.2.6 Operating states 26
 - 4.3 Configurable system power control 28
 - 4.3.1 ERBOOST switching regulator 28
 - 4.3.2 Energy reserve capacitor charging circuit 29
 - 4.3.3 ER switch and COVRACT pin 30
 - 4.3.4 VDD5 linear regulator 31
 - 4.3.5 VDD3V3 linear regulator 32
 - 4.3.6 VSUP linear regulator (optional) 33
 - 4.3.7 VSF linear regulator 33
 - 4.4 Reset functions 34
- 5 SPI interface 36**
 - 5.1 Global SPI register 49
 - Read/write register. 51
 - 5.1.1 Fault status register (FLTSR) 51
 - 5.1.2 System configuration register (SYS_CFG) 53
 - 5.1.3 System control register (SYS_CTL) 55

5.1.4	SPI Sleep command register (SPI_SLEEP)	56
5.1.5	System status register (SYS_STATE)	57
5.1.6	Power state register (POWER_STATE)	58
5.1.7	Deployment configuration registers (DCR_x)	61
5.1.8	Deployment command (DEPCOM)	63
5.1.9	Deployment configuration registers (DSR_x)	64
5.1.10	Deployment current monitor status registers (DCMTSxy)	65
5.1.11	Deploy enable register (SPIDEPEN)	66
5.1.12	Squib ground loss register (LP_GNDLOSS)	66
5.1.13	Device version register (VERSION_ID)	67
5.1.14	Watchdog retry configuration register (WD_RETRY_CONF)	67
5.1.15	Watchdog timer configuration register (WDTCR)	68
5.1.16	WD1 timer control register (WD1T)	69
5.1.17	WD1 state register (WDSTATE)	69
5.1.18	Clock configuration register (CLK_CONF)	70
5.1.19	Scrap state entry command register (SCRAP_STATE)	71
5.1.20	Safing state entry command register (SAFING_STATE)	71
5.1.21	WD1 test command register (WD1_TEST)	72
5.1.22	System diagnostic register (SYSDIAGREQ)	72
5.1.23	Diagnostic result register for deployment loops (LPDIAGSTAT)	74
5.1.24	Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)	77
5.1.25	Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)	79
5.1.26	DC sensor diagnostic configuration command register (SWCTRL)	81
5.1.27	ADC request and data registers (DIAGCTRL_x)	82
5.1.28	GPO configuration register (GPOCR)	85
5.1.29	GPO configuration register (GPOCTRLx)	86
5.1.30	GPO fault status register (GPOFLTSR)	87
5.1.31	ISO fault status register (ISOFLTSR)	88
5.1.32	Remote sensor configuration register (RSCRx)	89
5.1.33	Remote sensor control register (RSCTRL)	90
5.1.34	Remote sensor data/fault registers w/o fault (RSDRx)	91
5.1.35	Safing algorithm configuration register (SAF_ALGO_CONF)	95
5.1.36	Arming signals register (ARM_STATE)	96
5.1.37	ARMx assignment registers (LOOP_MATRIX_ARMx)	97
5.1.38	ARMx pulse stretch registers (AEPSTS_ARMx)	98
5.1.39	Safing records enable register (SAF_ENABLE)	99

5.1.40	Safing records request mask registers (SAF_REQ_MASK_x)	100
5.1.41	Safing records request target registers (SAF_REQ_TARGET_x)	101
5.1.42	Safing records response mask registers (SAF_RESP_MASK_x)	102
5.1.43	Safing records response target registers (SAF_RESP_TARGET_x)	103
5.1.44	Safing records data mask registers (SAF_DATA_MASK_x)	104
5.1.45	Safing records threshold registers (SAF_THRESHOLD_x)	105
5.1.46	Safing control registers (SAF_CONTROL_x)	106
5.1.47	Safing record compare complete register (SAF_CC)	109
6	Deployment drivers	110
6.1	Control logic	110
6.1.1	Deployment current selection	112
6.1.2	Deploy command expiration timer	112
6.1.3	Deployment control flow	113
6.1.4	Deployment success	114
6.2	Energy reserve - deployment voltage	114
6.3	Deployment ground return	114
6.4	Deployment driver protections	114
6.4.1	Delayed low-side deactivation	114
6.4.2	Low-side voltage clamp	114
6.4.3	Short to battery	114
6.4.4	Short to ground	114
6.4.5	Intermittent open squib	115
6.5	Diagnostics	115
6.5.1	Low level diagnostic approach	116
6.5.2	High level diagnostic approach	121
7	Remote sensor interface	124
7.1	PSI-5 protocol	125
7.1.1	Functional description - remote sensor modes	126
7.1.2	RSU data fields and CRC	127
7.1.3	Detailed description	127
7.2	Remote sensor interface fault protection	130
7.2.1	Short to ground, current limit	130
7.2.2	Short to battery	130
7.2.3	Cross link	130
7.2.4	Leakage to battery, open condition	131

	7.2.5	Leakage to ground	131
	7.2.6	Thermal shutdown	131
8		Watchdog timer	132
	8.1	Temporal watchdog	132
		8.1.1 Watchdog timer configuration	134
		8.1.2 Watchdog timer operation	134
	8.2	Watchdog reset assertion timer	135
	8.3	Watchdog timer disable input (WDT/TM)	135
9		DC sensor interface	136
10		Safing logic	139
	10.1	Safing logic overview	139
	10.2	SPI sensor data decoding	140
	10.3	In-frame and out-of-frame responses	148
	10.4	Safing state machine operation	148
		10.4.1 Simple threshold comparison operation	148
	10.5	Safing engine output logic (ARMxINT)	149
	10.6	Arming pulse stretch	152
	10.7	Additional communication line	152
11		General purpose output (GPO) drivers	154
12		ISO9141 transceiver	157
13		System voltage diagnostics	158
	13.1	Analog to digital algorithmic converter	162
14		Temperature sensor	164
15		Electrical characteristics	165
	15.1	Configuration and control	165
	15.2	Internal analog reference	167
	15.3	Internal regulators	168
	15.4	Oscillators	168
	15.5	Watchdog	169

15.6	Reset	169
15.7	SPI interface	170
15.8	ER boost	172
15.9	ER charge	174
15.10	ER switch	174
15.11	COVRACT	175
15.12	VDD5 regulator	175
15.13	VDD3V3 regulator	177
15.14	VSUP regulator	178
15.15	VSF regulator	179
15.16	Deployment drivers	180
15.17	Squib diagnostic	183
15.17.1	Squib resistance measurement	183
15.17.2	Squib leakage test (VRCM)	184
15.17.3	High/low side FET test	185
15.17.4	Deployment timer test	185
15.18	Remote sensor interface	186
15.19	DC sensor interface	188
15.20	Safing engine	189
15.21	General purpose output drivers	191
15.22	ISO9141 interface (K-LINE)	193
15.22.1	Analog to digital converter	195
15.23	Voltage diagnostics (analog Mux)	196
15.24	Temperature sensor	196
16	Quality information	197
16.1	OTP trim bits	197
17	Package information	198
17.1	LQFP64 (10x10x1.4 mm) package information	198
17.2	LQFP64 (10x10x1.4) marking information	200
18	Errata sheet	201
19	Revision history	202

List of tables

Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	12
Table 3.	Operative maximum ratings	14
Table 4.	Functions disabling by state	22
Table 5.	SPI register R/W	36
Table 6.	Global SPI register map	38
Table 7.	Global status word (GSW)	49
Table 8.	Short between loops diagnostics decoding	118
Table 9.	Watchdog timer status description	133
Table 10.	Records results comparison against two threshold	147
Table 11.	Diagnostics control register (DIAGCTRLx)	159
Table 12.	Diagnostics divider ratios	161
Table 13.	Configuration and control DC specifications	165
Table 14.	Configuration and control AC specifications	167
Table 15.	Open ground detection DC specifications	167
Table 16.	Open ground detection AC specifications	167
Table 17.	Internal analog reference	167
Table 18.	Internal regulators DC specifications	168
Table 19.	Internal regulators AC specifications	168
Table 20.	Oscillators AC specifications	168
Table 21.	Temporal watchdog timer AC specifications	169
Table 22.	Reset DC specifications	169
Table 23.	Reset AC specifications	169
Table 24.	SPI DC specifications	170
Table 25.	SPI AC specifications	171
Table 26.	ER Boost converter DC specifications	172
Table 27.	ER boost converter AC specifications	173
Table 28.	ER boost converter external components (Design Info)	173
Table 29.	ER current generator DC specifications	174
Table 30.	ER current generator AC specifications	174
Table 31.	ER switch DC specifications	174
Table 32.	ER switch AC specifications	174
Table 33.	COVRACT DC Specifications	175
Table 34.	COVRACT AC specifications	175
Table 35.	VDD5 regulator DC specifications	175
Table 36.	VDD5 regulator AC specifications	176
Table 37.	VDD5 regulator external components (Design Info)	176
Table 38.	VDD3V3 regulator DC specifications	177
Table 39.	VDD3V3 regulator AC specifications	177
Table 40.	VDD3V3 regulator external components (design info)	177
Table 41.	VSUP regulator DC specifications	178
Table 42.	VSUP AC specifications	178
Table 43.	VSUP regulator external components (Design Info)	178
Table 44.	VSF regulator DC specifications	179
Table 45.	VSF regulator AC specifications	179
Table 46.	Deployment drivers - DC specifications	180
Table 47.	Deployment drivers - AC specifications	182
Table 48.	Deployment drivers diagnostics (Squib resistance)	183

Table 49.	Squib leakage test (VRCM)	184
Table 50.	High/low side FET test	185
Table 51.	Deployment timer test	185
Table 52.	Remote sensor I/F DC parameters	186
Table 53.	PSI-5 remote sensor transceiver - AC specifications	187
Table 54.	DC sensor interface specifications	188
Table 55.	Arming interface - DC specifications	189
Table 56.	Arming interface - AC specifications	190
Table 57.	GPO interface DC specifications	191
Table 58.	GPO Driver Interface - AC specifications	192
Table 59.	ISO9141 interface DC specifications	193
Table 60.	ISO9141 interface transceiver AC specifications	194
Table 61.	Analog to digital converter	195
Table 62.	Voltage diagnostics (Analog MUX) DC specifications	196
Table 63.	Temperature sensor specifications	196
Table 64.	LQFP64 (10x10x1.4 mm) package mechanical data	199
Table 65.	Errata sheet	201
Table 66.	Document revision history	202

List of figures

Figure 1.	Pin-out description	16
Figure 2.	Functional block diagram	18
Figure 3.	Power control state flow diagram	20
Figure 4.	Wake-up input signal behaviour	22
Figure 5.	Normal power-up sequence - WAKEUP controlled	23
Figure 6.	Normal power-up sequence - VIN controlled	24
Figure 7.	Normal power down sequence - WAKEUP and SPI controlled	25
Figure 8.	Normal power down sequence - VIN controlled	26
Figure 9.	System operating state diagram	27
Figure 10.	ERBOOST block diagram	28
Figure 11.	ERBOOST control behaviour	29
Figure 12.	ER cap charging circuit	29
Figure 13.	ER switch control behaviour	30
Figure 14.	VDD5 control behavior	31
Figure 15.	VDD3V3 control behaviour	32
Figure 16.	VSUP control behavior	33
Figure 17.	VSF control logic	34
Figure 18.	Internal voltage errors	34
Figure 19.	Reset control diagram	35
Figure 20.	Deployment driver control blocks	110
Figure 21.	Deployment driver control logic - Enable signal	111
Figure 22.	Deployment driver control logic - Turn-on signals	111
Figure 23.	Deployment driver block	112
Figure 24.	Global SPI deployment enable state diagram	113
Figure 25.	Deployment loop diagnostics	116
Figure 26.	SRx pull-down enable logic	117
Figure 27.	Deployment timer diagnostic sequence	121
Figure 28.	High level loop diagnostic flow1	122
Figure 29.	High level loop diagnostic flow2	123
Figure 30.	Remote sensor interface logic blocks	124
Figure 31.	Remote sensor interface block diagram	125
Figure 32.	PSI-5 remote sensor protocol (10-bit, 1-bit parity)	126
Figure 33.	Manchester bit encoding	126
Figure 34.	Manchester decoder state diagram	128
Figure 35.	Remote sensor current sensing auto adjust	129
Figure 36.	Watchdog state diagram	132
Figure 37.	Watchdog timer refresh diagram	135
Figure 38.	Switch sensor interface block diagram	136
Figure 39.	Top level safing engine flow chart	139
Figure 40.	Safing engine - 16-bit message decoding flow chart	140
Figure 41.	Safing engine - 32-bit message decoding flow chart	141
Figure 42.	Safing engine - validate data flow chart	142
Figure 43.	Safing engine - combine function flow chart	143
Figure 44.	Safing engine threshold comparison	144
Figure 45.	Safing engine - compare complete	145
Figure 46.	In-frame example	148
Figure 47.	Out of frame example	148
Figure 48.	Safing Engine Arming flow diagram	150

Figure 49.	Safing engine diagnostic logic	151
Figure 50.	ARM output control logic.....	151
Figure 51.	Pulse stretch timer example	152
Figure 52.	Scrap ACL state diagram	153
Figure 53.	Disposal PWM signal	153
Figure 54.	GPO driver block diagram - LS configuration	154
Figure 55.	GPO driver block diagram - HS configuration.....	155
Figure 56.	ISO9141 block diagram	157
Figure 57.	ADC conversion time	163
Figure 58.	SPI timing diagram	171
Figure 59.	Deployment drivers diagram	182
Figure 60.	LQFP64 (10x10x1.4 mm) package outline	198
Figure 61.	LQFP64 (10x10x1.4) marking information	200

1 Description

The L9678P IC is a system chip solution targeted for emerging market applications. Base system designs can be completed with the L9678P, SPC560Px microcontroller and an on-board acceleration sensor or PSI5 sensor.

Energy reserve voltage is derived through a cost effective high frequency boost regulator. High frequency operation allows the user to pick up low value and cheap inductance. The voltage is programmable to 23 V or 33 V nominal.

Battery voltage is sensed through the VBATMON pin providing start-up and shutdown control for the system. Once battery voltage drops below the minimum operating voltage, the device enables the integrated crossover switch to permit orderly shutdown.

L9678P offers two linear regulators (5 V with external pass transistor and fully integrated 3.3 V). User can use one of these regulators to supply μ C. Input/output pins are compatible with both ranges by dedicated supply pin VDDQ. External pass transistor gives the flexibility to easily address different current loads in case of different micro-controllers.

One optional 7.2 V linear regulator with external pass transistor can be used to supply remote sensor interface.

External acceleration data is received through the PSI-5 remote sensor interface. Both channels have independent decoders. Sensor data and diagnostics are available via SPI.

The safing logic monitors inertial sensors (remote sensors via PSI-5 or on-board sensors via SPI) to determine if a crash event is in progress, thereby enabling deployment to occur. Parameters for sensor configuration and thresholds are user programmable.

Squib deployment uses four independent high and low side drivers, capable of deploying at 25 V max. Diagnostic data control is provided through the SPI interface.

The Hall-effect, resistive or switch sensor interface can be used to determine the state of external switch devices, such as buckle switches, seat track position sensors, weight sensors, deactivation switches.

The integrated clock module provides a fixed clock signal for the microcontroller. The clock module provides the user the option of deleting the commonly used resonator or crystal.

2 Absolute and operative maximum ratings

2.1 Absolute maximum ratings

Warning: This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

Table 2. Absolute maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.3	$V_{DDQ}+0.3 \leq 6.5$	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.3	$V_{DDQ}+0.3 \leq 6.5$	V
3	SPI_MOSI	SPI interface data in	-0.3	$V_{DDQ}+0.3 \leq 6.5$	V
4	SPI_SCK	SPI interface clock	-0.3	$V_{DDQ}+0.3 \leq 6.5$	V
5	SPI_CS	SPI interface chip select	-0.3	$V_{DDQ}+0.3 \leq 6.5$	V
6	WDT/TM	Watchdog disable (Not for application)	-0.3	20	V
7	VDD3V3	3.3 V regulator output	-0.3	4.6	V
8	NC	Not connected ⁽¹⁾	-	-	-
9	CVDD	Internal 3.3 V regulator output	-0.3	4.6	V
10	GNDD	Digital ground	-0.3	0.3	V
11	SR0	Squib 0 low-side pin	-0.3	40	V
12	SF0	Squib 0 high-side pin	-1.0	40	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.3	0.3	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
15	SF1	Squib 1 high-side pin	-1.0	40	V
16	SR1	Squib 1 low-side pin	-0.3	40	V
17	DCS3	Sensor switch interface channel 3	-1.0	40	V
18	DCS2	Sensor switch interface channel 2	-1.0	40	V
19	DCS1	Sensor switch interface channel 1	-1.0	40	V
20	DCS0	Sensor switch interface channel 0	-1.0	40	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.3	40	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678P-S), NC on L9678P	-1.0	40	V
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678P-S), NC on L9678P	-1.0	40	V
24	VSUP/NC	Remote sensor power supply (only L9678P-S), NC ⁽¹⁾ on L9678P	-0.3	40	V

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
25	BVSUP/NC	VSUP external transistor control (only L9678P-S), NC ⁽¹⁾ on L9678P	-0.3	40	V
26	GPOD0	GPO driver 1 drain output pin	-1.0	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	40	V
28	GPOS1	GPO driver 0 source output pin	-1.0	40	V
29	GPOD1	GPO driver 0 drain output pin	-1.0	40	V
30	NC	Not connected ⁽¹⁾	-	-	-
31	ISOK	ISO9141 bus pin (K-LINE)	-18.0	40	V
32	GNDSUB1	Substrate ground	-0.3	0.3	V
33	SR3	Squib 3 low-side pin	-0.3	40	V
34	SF3	Squib 3 high-side pin	-1.0	40	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.3	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.3	0.3	V
37	SF2	Squib 2 high-side pin	-1.0	40	V
38	SR2	Squib 2 low-side pin	-0.3	40	V
39	GND A	Analog ground	-0.3	0.3	V
40	ISORX	ISO9141 receiver pin	-0.3	VDDQ+0.3 ≤6.5	V
41	ISOTX	ISO9141 transmit pin	-0.3	VDDQ+0.3 ≤6.5	V
42	FENL	LS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
43	FENH	HS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
46	NC	Not connected ⁽¹⁾	-	-	-
47	WAKEUP	Wake-up control input	-0.3	40	V
48	VBATMON	Battery line voltage monitor	-18	40	V
49	VSF	Safing regulator supply output	-0.3	ERBOOST+0.3 ≤40	V
50	VIN	Battery connection	-0.3	40	V
51	VER	Reserve voltage	-0.3	40	V
52	ERBOOST	Energy reserve regulator output	-0.3	40	V
53	ERBSTSW	Boost switching output	-0.3	40	V
54	NC	Not connected ⁽¹⁾	-	-	-
55	BSTGND	Boost regulator ground	-0.3	0.3	V
56	ACL	EOL disposal control input	-0.3	40	V
57	BVDD5	VDD5 external transistor control	-0.3	40	V
58	NC	Not connected	-	-	-
59	VDD5	5V regulator output	-0.3	6.5	V
60	NC	Not connected ⁽¹⁾	-	-	-

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
61	COVRACT	External crossover switch control	-0.3	VDDQ+0.3 ≤6.5	V
62	VDDQ	I/O supply	-0.3	6.5	V
63	ARM	Arming Output	-0.3	VDDQ+0.3 ≤6.5	V
64	GNDSUB2	Substrate ground	-0.3	0.3	V

1. Not connected internally, should be connected to GND externally.

2.2 Operative maximum ratings

Within the operative ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply-voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.1	VDDQ+0.1 ≤5.5	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.1	VDDQ+0.1 ≤5.5	V
3	SPI_MOSI	SPI interface data in	-0.1	VDDQ+0.1 ≤5.5	V
4	SPI_SCK	SPI interface clock	-0.1	VDDQ+0.1 ≤5.5	V
5	SPI_CS	SPI interface chip select	-0.1	VDDQ+0.1 ≤5.5	V
6	WDT/TM	Watchdog disable	-0.1	20	V
7	VDD3V3	3.3V regulator output	-0.1	3.6	V
8	NC	Not connected ⁽¹⁾	-	-	-
9	CVDD	Internal 3.3V regulator output	-0.1	3.6	V
10	GNDD	Digital ground	-0.1	0.1	V
11	SR0	Squib 0 low-side pin	-0.1	VER	V
12	SF0	Squib 0 high-side pin	-1.0	VER	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.1	0.1	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.1	40	V
15	SF1	Squib 1 high-side pin	-1.0	VER	V
16	SR1	Squib 1 low-side pin	-0.1	VER	V
17	DCS3	Sensor switch interface channel 3	-1.0	V _{DCS_L}	V
18	DCS2	Sensor switch interface channel 2	-1.0	V _{DCS_L}	V
19	DCS1	Sensor switch interface channel 1	-1.0	V _{DCS_L}	V
20	DCS0	Sensor switch interface channel 0	-1.0	V _{DCS_L}	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.1	35	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678P-S), NC on L9678P	-1.0	VSUP	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678P-S), NC on L9678P	-1.0	VSUP	V
24	VSUP/NC	Remote sensor power supply (only L9678P-S, NC ⁽¹⁾ on L9678P)	-0.1	VIN	V
25	BVSUP/NC	VSUP external transistor control (only L9678P-S, NC ⁽¹⁾ on L9678P)	-0.1	VIN	V
26	GPOD0	GPO driver 1 drain output pin	-0.1	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	VIN	V
28	GPOS1	GPO driver 0 source output pin	-1.0	VIN	V
29	GPOD1	GPO driver 0 drain output pin	-0.1	40	V
30	NC	Not connected ⁽¹⁾	-	-	-
31	ISOK	ISO9141 bus pin	-1.0	40	V
32	GNDSUB1	Substrate ground	-0.1	0.1	V
33	SR3	Squib 3 low-side pin	-0.1	VER	V
34	SF3	Squib 3 high-side pin	-1.0	VER	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.1	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.1	0.1	V
37	SF2	Squib 2 high-side pin	-1.0	VER	V
38	SR2	Squib 2 low-side pin	-0.1	VER	V
39	GND A	Analog ground	-0.1	0.1	V
40	ISORX	ISO9141 receiver pin	-0.1	VDDQ+0.1 ≤ 5.5	V
41	ISOTX	ISO9141 transmit pin	-0.1	VDDQ+0.1 ≤ 5.5	V
42	FENL	LS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
43	FENH	HS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
46	NC	Not connected ⁽¹⁾	-	-	-
47	WAKEUP	Wake-up control input	-0.1	VIN	V
48	VBATMON	Battery line voltage monitor	-0.1	18	V
49	VSF	Safing regulator supply output	-0.1	27	V
50	VIN	Battery connection	-0.1	35	V
51	VER	Reserve voltage	-0.1	35	V
52	ERBOOST	Energy reserve regulator output	-0.1	35	V
53	ERBSTSW	Boost switching output	-0.1	ERBOOST+1	V
54	NC	Not connected ⁽¹⁾	-	-	-
55	BSTGND	Boost regulator ground	-0.1	0.1	V
56	ACL	EOL disposal control input	-0.1	40	V
57	BVDD5	VDD5 external transistor control	-0.1	VIN	V

Table 3. Operative maximum ratings (continued)

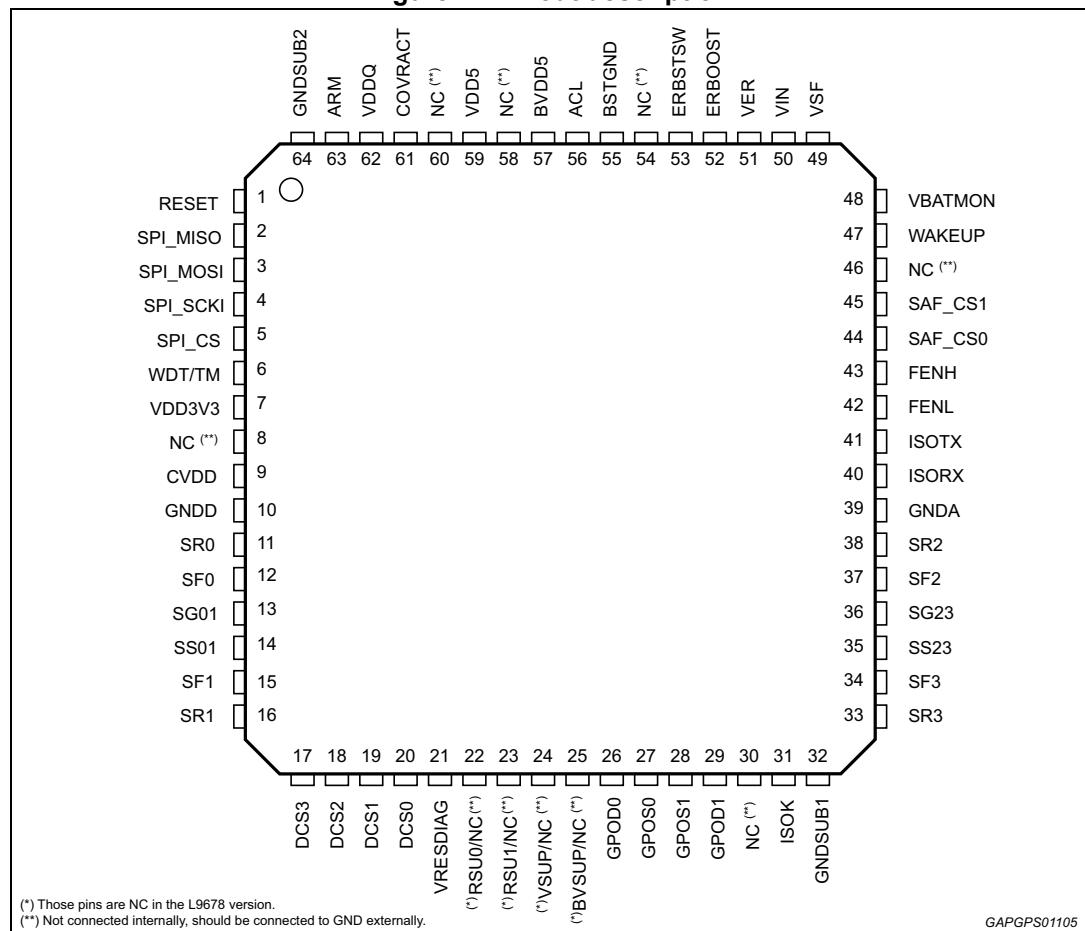
Pin #	Pin name	Pin function	Min.	Max.	Unit
58	NC	Not connected ⁽¹⁾	-	-	-
59	VDD5	5V regulator output	-0.1	5.5	V
60	NC	Not connected ⁽¹⁾	-	-	-
61	COVRACT	External crossover switch control	-0.1	VDDQ+0.1 ≤ 5.5	V
62	VDDQ	I/O supply	-0.1	5.5	V
63	ARM	Arming Output	-0.1	VDDQ+0.1 ≤ 5.5	V
64	GNDSUB2	Substrate ground	-0.1	0.1	V

1. Not connected internally, should be connected to GND externally.

2.3 Pin-out description

The L9678P-S/L9678P pin-out is shown below. The package is a LQFP 64-pin full plastic package.

Figure 1. Pin-out description

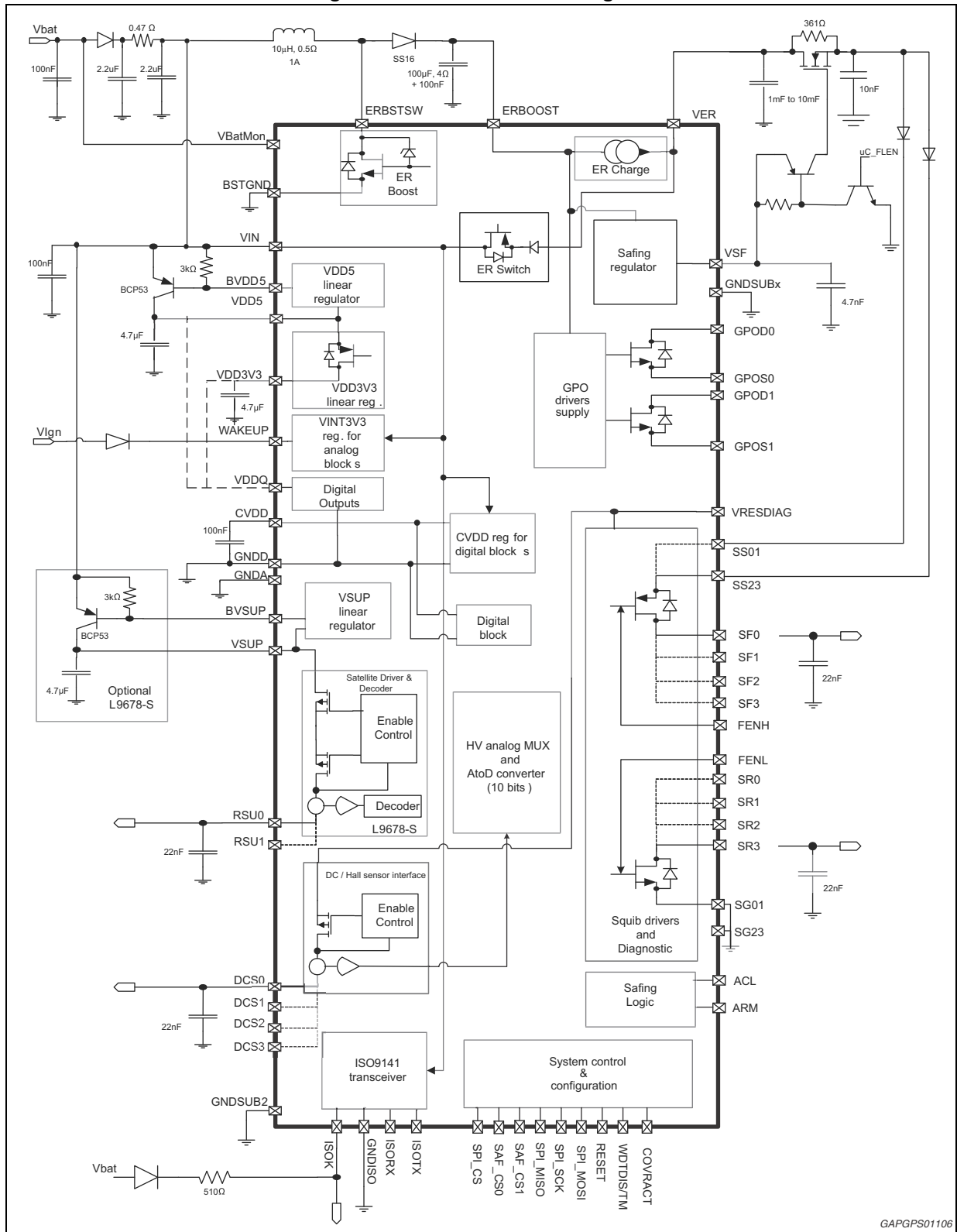


3 Overview and block diagram

The L9678P is a unique solution specifically targeted for entry level airbag systems while permitting the system designer significant flexibility in configuring the system power and management block. The configurable methodology allows cost versus performance trade-off without changing devices or circuit board designs. The L9678P contains the base functionality required for entry level systems and can complete a system design with a microcontroller and acceleration sensor. The high level block diagram is shown below [Figure 2](#).

Basic features include a configurable power supply & management block, 4 channel squib drivers, 2 channel HS/LS GPO drivers, 4 channel sensor interface, safing logic, watchdog timer, ISO9141 communications and temperature sensor. The L9678P-S device is pin compatible to the L9678P and includes two PSI-5 remote sensor interface channels and a dedicated regulator for remote sensor.

Figure 2. Functional block diagram



GAPGPS01106

4 Start-up power control

4.1 Power supply overview

The L9678P IC contains a complete power management system able to provide all necessary voltages for an entry level airbag application. Moreover L9678P power supply is user configurable allowing the design engineer to balance cost and performance as per their particular application. The power supply block contains the following features:

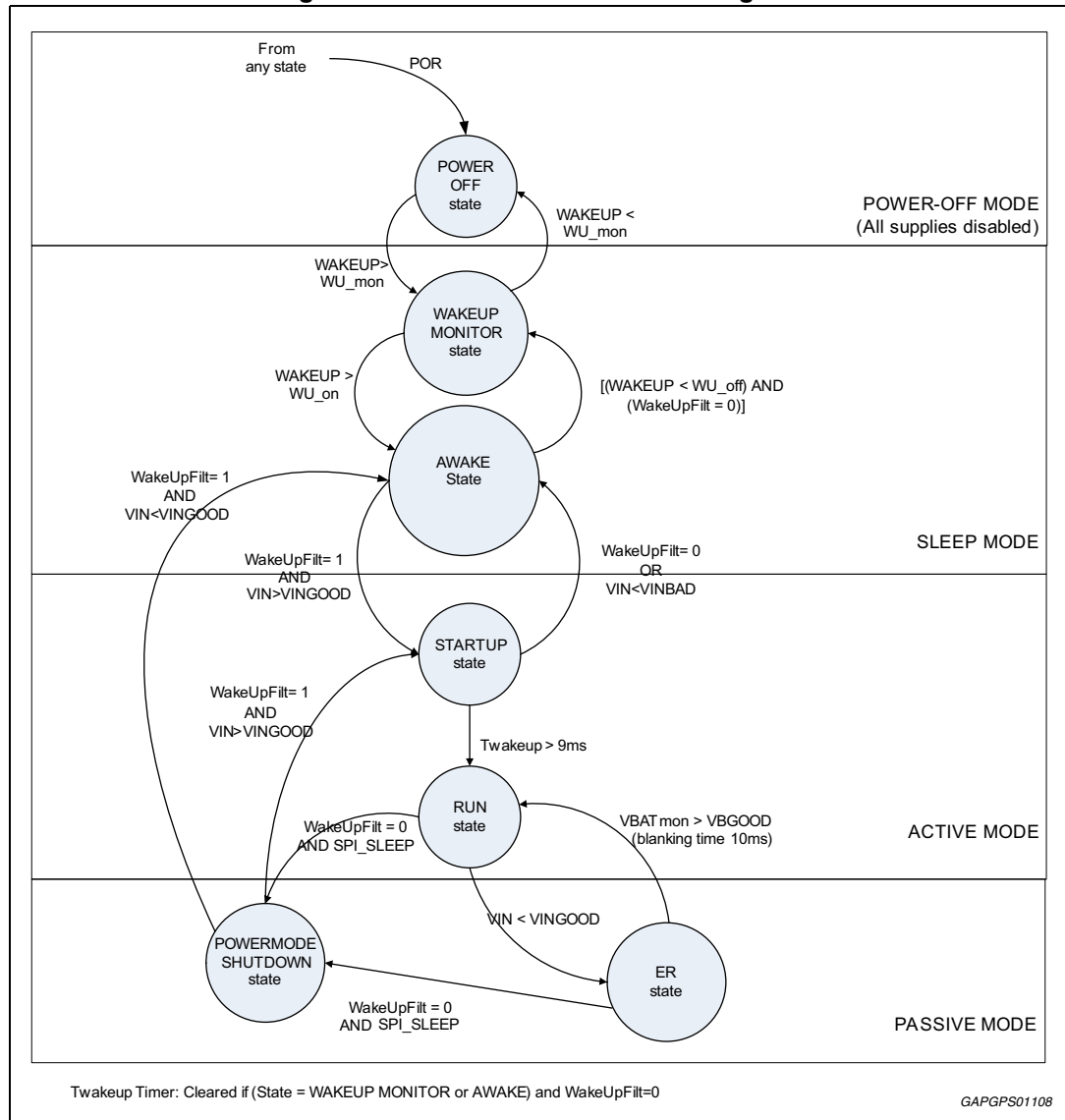
- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail.
- Energy reserve supply (ERBOOST) achieved through an integrated switching boost regulator. The design of this boost regulator is intended to be a cost effective solution with respect to traditional boost regulators because it makes use of a low value inductor with an operative frequency of 1.882 MHz. Switching output is ERBSTSW pin, while voltage feedback input pin is ERBOOST. The output voltage could be set to either 23 V \pm 5% or 33 V \pm 5%.
- Energy reserve capacitor connected to VER pin. To control in-rush current, a dedicated current generator is implemented between ERBOOST pin and VER pin.
- Capability to drive an external safing FET (n-ch type) by means of an internal voltage regulator on VSF pin, where a 20 V level is given (configurable to 25V via SPI command).
- The integrated current limited ER switch requires no external components. This switch is controlled through the integrated power control state machine and is enabled either once a loss of battery is detected or a shutdown command is received. Under the same conditions also the discrete digital pin COVRACT is activated allowing the control of an external optional cross-over switch.
- One linear regulator VDD5 (5 V nominal, \pm 4% tolerance) requiring external power transistor and capacitors. VDD5 is used as micro-controller supply (in case of 5 V family controllers) and, in any case, as supply for VDD3V3 rail.
- One integrated linear regulator VDD3V3 (3.3 V nominal, \pm 4% tolerance) requiring external capacitors. VDD3V3 is used as micro-controller supply (in case of 3.3 V family controllers).
- VDDQ pin to provide output voltage rail reference. VDDQ could be connected to either VDD5 or VDD3V3 to enable 5 V or 3.3 V digital communication between device and micro-controller.
- Capability to drive an external power transistor connected to VIN to provide a 7.2 V rail on VSUP pin. This voltage rail could be used to supply PSI-5 remote sensor.
- Battery voltage sense input comparator with hysteresis connected to VBATMON pin. Power-up and operation states are carefully handled with respect to the battery level to provide the most effective power supply configuration.
- All voltage rails (VIN, ERBOOST, VER, VRESDIAG, VDD5, VDD3V3, VSUP and VSF) can be monitored through internal ADC diagnostics.

4.2 Power mode control

Start-up and power down of the L9678P are controlled by the WAKEUP pin, VBATMON pin, VIN pin device status and the SPI interface. There are four main power modes: power-off, sleep, active and passive mode.

Each power mode is described below and represented in the state flow diagram shown in [Figure 3](#). The descriptions include references to conditions and sometimes nominal values. The absolute values for each condition are listed in the electrical specifications section.

Figure 3. Power control state flow diagram



4.2.1 Power_off mode

During the Power-off mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as WAKEUP > WU_mon the IC will move to Sleep mode.

4.2.2 Sleep mode

During the Sleep mode the VINT3V3 and CVDD internal regulators are turned on and the IC is ready for full activation of all the other supplies. As soon as battery voltage is over a minimum threshold, all the other supplies are turned on and the IC enters the Active mode.

4.2.3 Active mode

This is the normal operating mode for the system.

All power supplies are enabled and the energy reserve boost converter starts to increase the voltage at ERBOOST. Likewise, the VDD5 regulator is turned on. Once the VDD5 has reached a good value, the VDD3V3 regulator starts up. Once the VDD3V3 regulator is in regulation, RESET is released allowing the system microcontroller and other components to begin their power-on sequence. Among these, also the ER charge current generator can be enabled by the microcontroller via a dedicated SPI command.

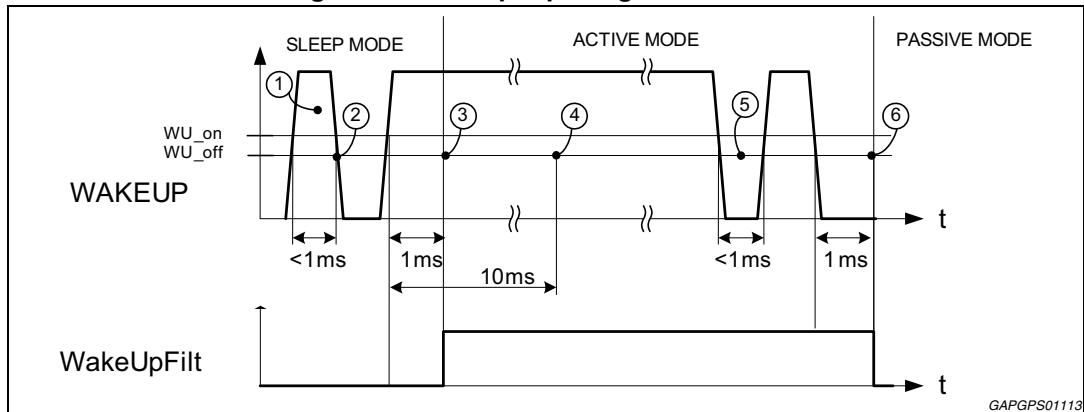
The active mode can be left when either WAKEUP pin or VIN voltage drop down. For the very first 9 ms after having entered the active mode, the WAKEUP pin low would immediately cause the IC to switch back to sleep mode. After that time, WAKEUP pin low must be first confirmed by a MCUSPI_SLEEP command prior to cause the system to switch to passive mode. Passive mode is also entered in case of VIN voltage low.

4.2.4 Passive mode

In this state, the energy reserve charge current is disabled and the ERBOOST boost converter is disabled only if the SYS_CFG(KEEP_ERBST_ON)=0. When in passive mode the device automatically activates both the COVRACT output pin and the integrated ER switch to allow VIN to be connected to the ER capacitor. In this time, VIN is supposed to be increased up to almost VER level and the system operation relies on energy from the ER capacitor. Two scenarios are possible: high or low battery. If VIN < VINGOOD, the device moved from RUN state in ACTIVE mode to the ER state. Here, the ER capacitor is depleted while supplying all the regulators until the POR on internal regulator occurs. The threshold to decide the ER switch activation is based on VIN, because VIN is the supply voltage rail for all regulators. If the device has still a good battery level, it entered the POWERMODE SHUTDOWN thanks to WAKEUP pin and MCU command to switch off. In this case, the VER node will be discharged down to approximately VIN level, which then will be supplied out of the battery line. System will continue to run up to a dedicated SPI command which will lead the device to enter the POWEROFF state.

The wake-up pin is filtered to suppress undesired state changes resulting from transients or glitches. Typical conditions are shown in the chart below and summarized by state.

Figure 4. Wake-up input signal behaviour



Condition summary:

1. No change of sleep mode state but current consumption may exceed specification for sleep mode.
2. The sleep mode current returns within the specified limits.
3. Power supply exits sleep mode. Switchers start operating if applicable voltages exceed under voltage lockouts. As T_{wakeup} time-out is not elapsed, a low level at WAKEUP instantaneously sends the system back to sleep.
4. Sleep Reset is released and the entire system starts operating. A SPI command to enter sleep state would be ignored.
5. No change in system status, a SPI command to enter sleep state would be ignored.
6. No change in system status, but a SPI command to turn off switchers would be accepted and turn the system off.

With the below table, all the functionalities of the device are shown with respect to the power states. When one function is flagged, the related circuitry cannot be activated on that state.

Table 4. Functions disabling by state

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Wakeup detector	X	-	-	-	-	-	-
Internal regulator	X	X	-	-	-	-	-
ERBOOST regulator	X	X	X	-	-	X	X
VSUP regulator (L9678P-S only)	X	X	X	-	-	-	-
ER CAP charge current source	X	X	X	-	-	X	X
ER switch	X	X	X	X	X	-	-
COVRACT Output	X	X	X	X	X	-	-
VDD5 regulator	X	X	X	-	-	-	-
VDD3V3 regulator	X	X	X	-	-	-	-
Deployment drivers	X	X	X	-	-	-	-
VSF safing FET regulator	X	X	X	-	-	-	-
Remote sensor interfaces (L9678P-S only)	X	X	X	-	-	-	-

Table 4. Functions disabling by state (continued)

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Watchdog	X	X	X	-	-	-	-
Diagnostics	X	X	X	-	-	-	-
DC sensor interface	X	X	X	-	-	-	-
GPO drivers	X	X	X	-	-	-	-
Safing logic	X	X	X	-	-	-	-
ISO9141	X	X	X	-	-	-	-

4.2.5 Power-up and power-down sequence

The behavior of the IC during normal power-up and power-down is shown from [Figure 5](#) to [Figure 8](#). The following sequences represent just a subset of all possible power-up and power-down scenarios.

In [Figure 5](#) a normal IC power-up controlled by the state of the WAKEUP pin is shown.

Figure 5. Normal power-up sequence - WAKEUP controlled

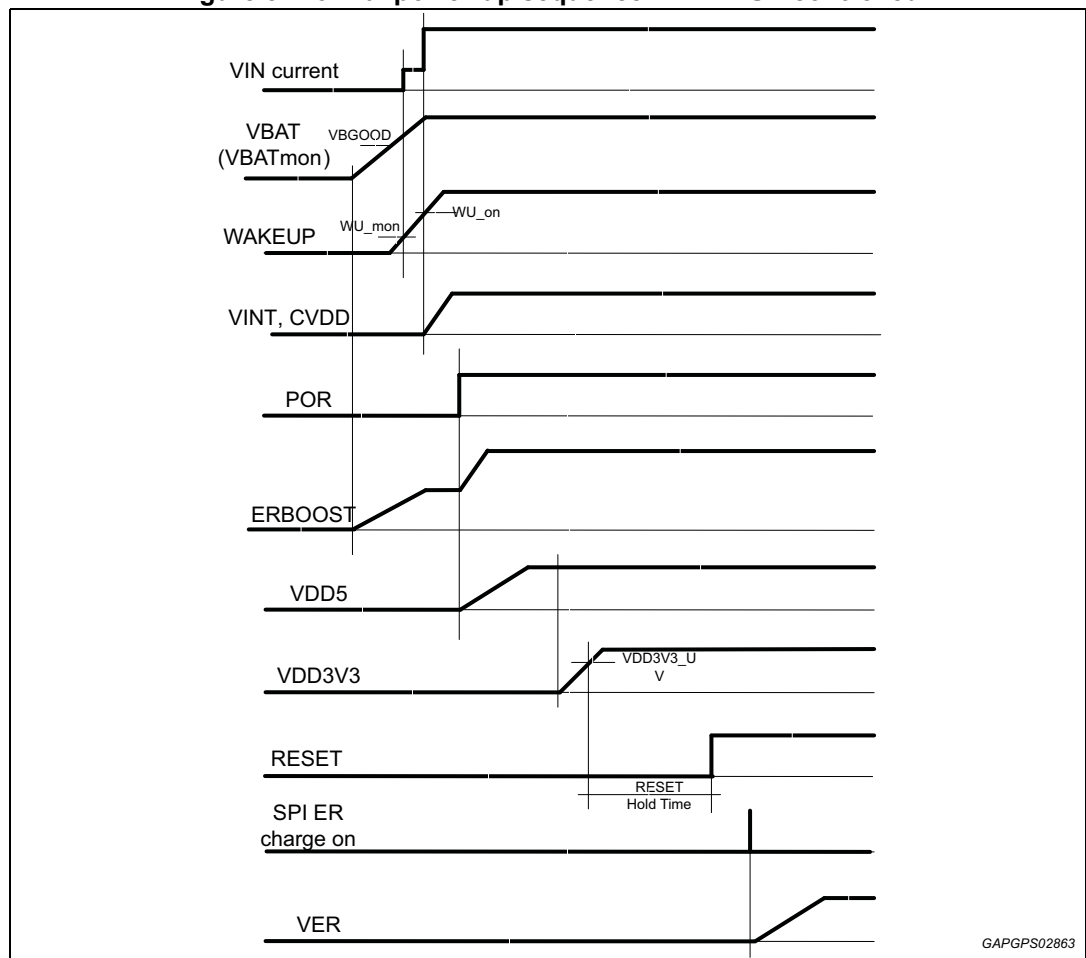
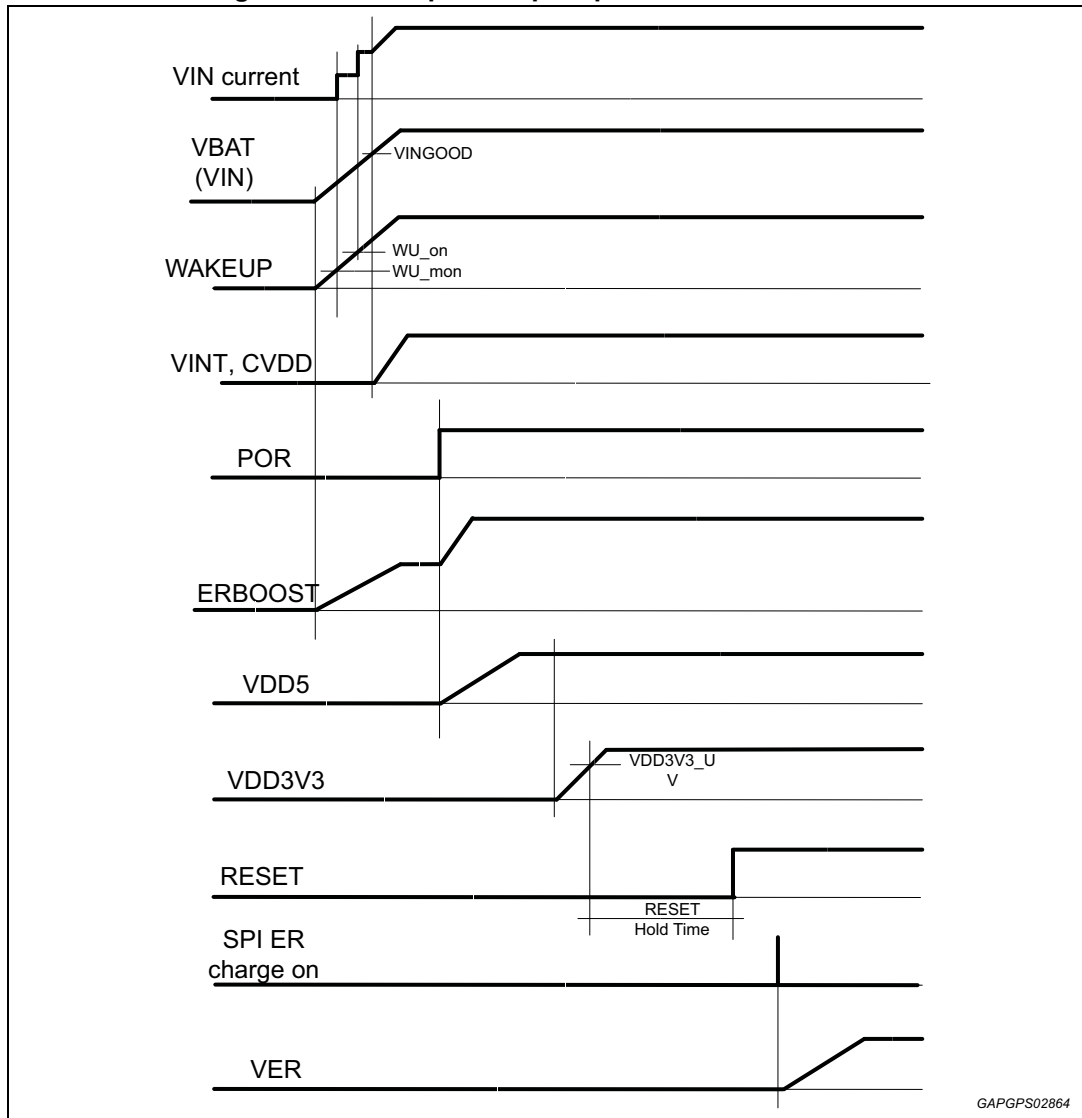


Figure 6. Normal power-up sequence - VIN controlled



Two different scenarios for power-down of the IC are shown here below. [Figure 7](#) describes the powering down for the case when WAKEUP pin is released. As soon as a SPI_SLEEP command is received by the MCU the System will immediately move to the energy reserve (PASSIVE mode). In [Figure 8](#), VIN release begins the shutdown process.

Figure 7. Normal power down sequence - WAKEUP and SPI controlled

