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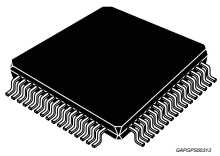
L9678
L9678-S

User configurable airbag IC

Datasheet - production data



LQFP64 (10x10x1.4mm)

Features

- Energy reserve voltage power supply
  - High frequency boost regulator, 1.882 MHz
  - Output voltage user selectable, 23 V or 33 V ±5%
- User configurable linear power supplies
  - 5.0 V and 7.2 V ±4% output voltages
  - External pass transistor
- Fully integrated 3.3 V ±4% linear regulator
- Battery voltage monitor and shutdown control with wake-up control
- System voltage diagnostics with integrated ADC
- Crossover switch
  - Crossover performance, max 3 Ω, 600 mA max.
- Squib deployment drivers
  - 4 channel HSD/LSD
  - 25 V maximum deployment voltage
  - 1.2 A @ 2 ms and 1.75 A @ 0.5/0.7 ms deployment profiles
  - Integrated safing FET linear regulator, 20 V/25 V nominal
  - Current monitoring
  - Rmeasure, STB, STG and leakage diagnostics
  - High and low side driver FET tests
  - Safing FET test
- User customizable safing logic
- Two channel PSI-5 remote sensor interface (asynchronous mode), [only for L9678-S version]
- Four channel hall-effect, resistive or switch sensor interface
- ISO9141 transceiver
- Dual channel configurable high-side/low-side LED driver
- Watchdog timer
- Two integrated oscillators: 7.5/16 MHz
- Temperature sensor
- 32 bit SPI communications
- Minimum operating voltage = 6 V
- Operating temperature, -40 °C to 95 °C
- Packaging - 64 pin

Table 1. Device summary

Order code	Package	Packing	Remote sensor interface
L9678	LQFP64 (10 x 10 x 1.4 mm)	Tray	No
L9678-S	LQFP64 (10 x 10 x 1.4 mm)	Tray	Yes

This is information on a product in full production. www.st.com

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1 Description

The L9678 IC is a system chip solution targeted for emerging market applications. Base system designs can be completed with the L9678, SPC560Px microcontroller and an on-board acceleration sensor or PSI5 sensor.

Energy reserve voltage is derived through a cost effective high frequency boost regulator. High frequency operation allows the user to pick up low value and cheap inductance. The voltage is programmable to 23 V or 33 V nominal.

Battery voltage is sensed through the VBATMON pin providing start-up and shutdown control for the system. Once battery voltage drops below the minimum operating voltage, the device enables the integrated crossover switch to permit orderly shutdown.

L9678 offers two linear regulators (5 V with external pass transistor and fully integrated 3.3 V). User can use one of these regulators to supply µC. Input/output pins are compatible with both ranges by dedicated supply pin VDDQ. External pass transistor gives the flexibility to easily address different current loads in case of different micro-controllers.

One optional 7.2 V linear regulator with external pass transistor can be used to supply remote sensor interface.

External acceleration data is received through the PSI-5 remote sensor interface. Both channels have independent decoders. Sensor data and diagnostics are available via SPI.

The safing logic monitors inertial sensors (remote sensors via PSI-5 or on-board sensors via SPI) to determine if a crash event is in progress, thereby enabling deployment to occur. Parameters for sensor configuration and thresholds are user programmable.

Squib deployment uses four independent high and low side drivers, capable of deploying at 25 V max. Diagnostic data control is provided through the SPI interface.

The Hall-effect, resistive or switch sensor interface can be used to determine the state of external switch devices, such as buckle switches, seat track position sensors, weight sensors, deactivation switches.

The integrated clock module provides a fixed clock signal for the microcontroller. The clock module provides the user the option of deleting the commonly used resonator or crystal.

2 Absolute and operative maximum ratings

2.1 Absolute maximum ratings

Warning: **This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.**

Table 2. Absolute maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.3	VDDQ+0.3 ≤6.5	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.3	VDDQ+0.3 ≤6.5	V
3	SPI_MOSI	SPI interface data in	-0.3	VDDQ+0.3 ≤6.5	V
4	SPI_SCK	SPI interface clock	-0.3	VDDQ+0.3 ≤6.5	V
5	SPI_CS	SPI interface chip select	-0.3	VDDQ+0.3 ≤6.5	V
6	WDT/TM	Watchdog disable (Not for application)	-0.3	20	V
7	VDD3V3	3.3 V regulator output	-0.3	4.6	V
8	NC	Not connected (1)	-	-	-
9	CVDD	Internal 3.3 V regulator output	-0.3	4.6	V
10	GNDD	Digital ground	-0.3	0.3	V
11	SR0	Squib 0 low-side pin	-0.3	40	V
12	SF0	Squib 0 high-side pin	-1.0	40	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.3	0.3	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
15	SF1	Squib 1 high-side pin	-1.0	40	V
16	SR1	Squib 1 low-side pin	-0.3	40	V
17	DCS3	Sensor switch interface channel 3	-1.0	40	V
18	DCS2	Sensor switch interface channel 2	-1.0	40	V
19	DCS1	Sensor switch interface channel 1	-1.0	40	V
20	DCS0	Sensor switch interface channel 0	-1.0	40	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.3	40	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678-S), NC on L9678	-1.0	40	V
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678-S), NC on L9678	-1.0	40	V
24	VSUP/NC	Remote sensor power supply (only L9678-S), NC(1) on L9678	-0.3	40	V

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
25	BVSUP/NC	VSUP external transistor control (only L9678-S), NC(1) on L9678	-0.3	40	V
26	GPOD0	GPO driver 1 drain output pin	-1.0	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	40	V
28	GPOS1	GPO driver 0 source output pin	-1.0	40	V
29	GPOD1	GPO driver 0 drain output pin	-1.0	40	V
30	NC	Not connected (1)	-	-	-
31	ISOK	ISO9141 bus pin (K-LINE)	-18.0	40	V
32	GNDSUB1	Substrate ground	-0.3	0.3	V
33	SR3	Squib 3 low-side pin	-0.3	40	V
34	SF3	Squib 3 high-side pin	-1.0	40	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.3	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.3	0.3	V
37	SF2	Squib 2 high-side pin	-1.0	40	V
38	SR2	Squib 2 low-side pin	-0.3	40	V
39	GNDA	Analog ground	-0.3	0.3	V
40	ISORX	ISO9141 receiver pin	-0.3	VDDQ+0.3 ≤6.5	V
41	ISOTX	ISO9141 transmit pin	-0.3	VDDQ+0.3 ≤6.5	V
42	FENL	LS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
43	FENH	HS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
46	NC	Not connected (1)	-	-	-
47	WAKEUP	Wake-up control input	-0.3	40	V
48	VBATMON	Battery line voltage monitor	-18	40	V
49	VSF	Safing regulator supply output	-0.3	ERBOOST+0.3 ≤40	V
50	VIN	Battery connection	-0.3	40	V
51	VER	Reserve voltage	-0.3	40	V
52	ERBOOST	Energy reserve regulator output	-0.3	40	V
53	ERBSTSW	Boost switching output	-0.3	40	V
54	NC	Not connected (1)	-	-	-
55	BSTGND	Boost regulator ground	-0.3	0.3	V
56	ACL	EOL disposal control input	-0.3	40	V
57	BVDD5	VDD5 external transistor control	-0.3	40	V
58	NC	Not connected	-	-	-
59	VDD5	5V regulator output	-0.3	6.5	V
60	NC	Not connected (1)	-	-	-

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
61	COVRACT	External crossover switch control	-0.3	VDDQ+0.3 ≤6.5	V
62	VDDQ	I/O supply	-0.3	6.5	V
63	ARM	Arming Output	-0.3	VDDQ+0.3 ≤6.5	V
64	GNDSUB2	Substrate ground	-0.3	0.3	V

1. Not connected internally, should be connected to GND externally.

2.2 Operative maximum ratings

Within the operative ratings the part operates as specified and without parameter deviations Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply-voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.1	VDDQ+0.1 ≤5.5	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.1	VDDQ+0.1 ≤5.5	V
3	SPI_MOSI	SPI interface data in	-0.1	VDDQ+0.1 ≤5.5	V
4	SPI_SCK	SPI interface clock	-0.1	VDDQ+0.1 ≤5.5	V
5	SPI_CS	SPI interface chip select	-0.1	VDDQ+0.1 ≤5.5	V
6	WDT/TM	Watchdog disable	-0.1	20	V
7	VDD3V3	3.3V regulator output	-0.1	3.6	V
8	NC	Not connected(1)	-	-	-
9	CVDD	Internal 3.3V regulator output	-0.1	3.6	V
10	GNDD	Digital ground	-0.1	0.1	V
11	SR0	Squib 0 low-side pin	-0.1	VER	V
12	SF0	Squib 0 high-side pin	-1.0	VER	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.1	0.1	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.1	40	V
15	SF1	Squib 1 high-side pin	-1.0	VER	V
16	SR1	Squib 1 low-side pin	-0.1	VER	V
17	DCS3	Sensor switch interface channel 3	-1.0	V_{DCS_L}	V
18	DCS2	Sensor switch interface channel 2	-1.0	V_{DCS_L}	V
19	DCS1	Sensor switch interface channel 1	-1.0	V_{DCS_L}	V
20	DCS0	Sensor switch interface channel 0	-1.0	V_{DCS_L}	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.1	35	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678-S), NC on L9678	-1.0	VSUP	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678-S), NC on L9678	-1.0	VSUP	V
24	VSUP/NC	Remote sensor power supply (only L9678-S, NC(1) on L9678)	-0.1	VIN	V
25	BVSUP/NC	VSUP external transistor control (only L9678-S, NC(1) on L9678)	-0.1	VIN	V
26	GPOD0	GPO driver 1 drain output pin	-0.1	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	VIN	V
28	GPOS1	GPO driver 0 source output pin	-1.0	VIN	V
29	GPOD1	GPO driver 0 drain output pin	-0.1	40	V
30	NC	Not connected (1)	-	-	-
31	ISOK	ISO9141 bus pin	-1.0	40	V
32	GNDSUB1	Substrate ground	-0.1	0.1	V
33	SR3	Squib 3 low-side pin	-0.1	VER	V
34	SF3	Squib 3 high-side pin	-1.0	VER	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.1	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.1	0.1	V
37	SF2	Squib 2 high-side pin	-1.0	VER	V
38	SR2	Squib 2 low-side pin	-0.1	VER	V
39	GNDA	Analog ground	-0.1	0.1	V
40	ISORX	ISO9141 receiver pin	-0.1	VDDQ+0.1 ≤ 5.5	V
41	ISOTX	ISO9141 transmit pin	-0.1	VDDQ+0.1 ≤ 5.5	V
42	FENL	LS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
43	FENH	HS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
46	NC	Not connected (1)	-	-	-
47	WAKEUP	Wake-up control input	-0.1	VIN	V
48	VBATMON	Battery line voltage monitor	-0.1	18	V
49	VSF	Safing regulator supply output	-0.1	27	V
50	VIN	Battery connection	-0.1	35	V
51	VER	Reserve voltage	-0.1	35	V
52	ERBOOST	Energy reserve regulator output	-0.1	35	V
53	ERBSTSW	Boost switching output	-0.1	ERBOOST+1	V
54	NC	Not connected (1)	-	-	-
55	BSTGND	Boost regulator ground	-0.1	0.1	V
56	ACL	EOL disposal control input	--0.1	40	V
57	BVDD5	VDD5 external transistor control	-0.1	VIN	V

Table 3. Operative maximum ratings (continued)

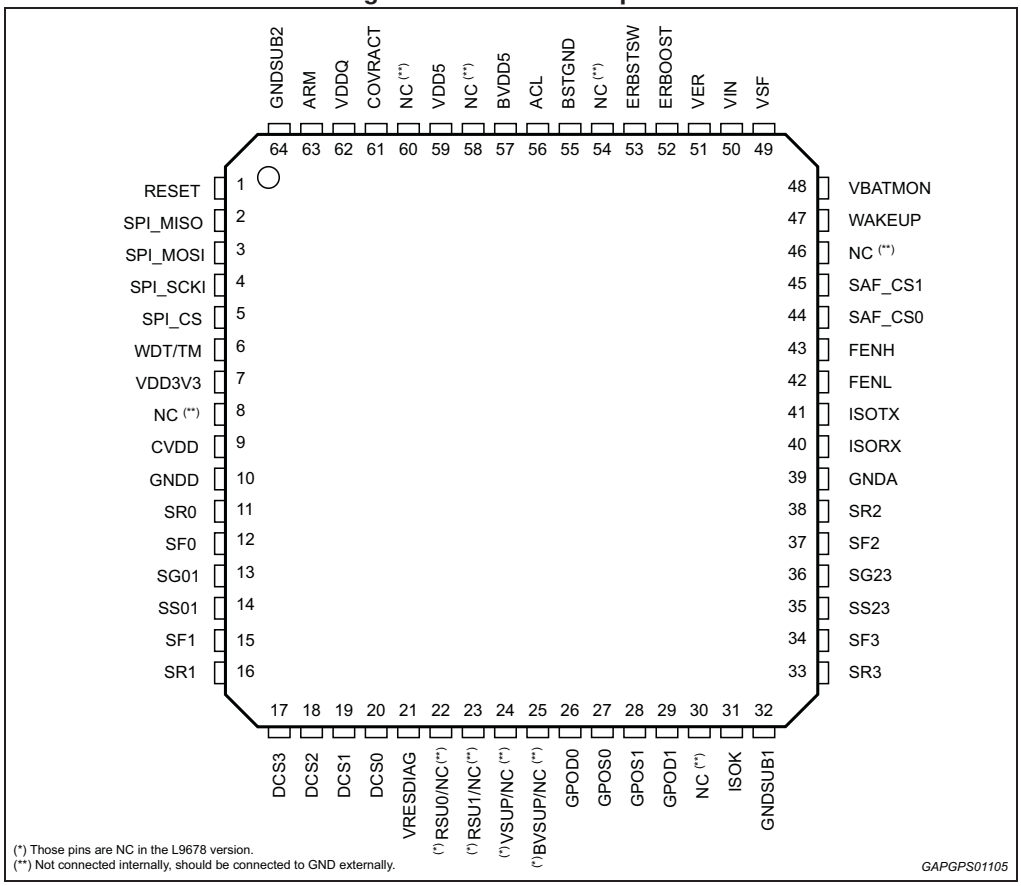
Pin #	Pin name	Pin function	Min.	Max.	Unit
58	NC	Not connected (1)	-	-	-
59	VDD5	5V regulator output	-0.1	5.5	V
60	NC	Not connected (1)	-	-	-
61	COVRACT	External crossover switch control	-0.1	VDDQ+0.1 ≤ 5.5	V
62	VDDQ	I/O supply	-0.1	5.5	V
63	ARM	Arming Output	-0.1	VDDQ+0.1 ≤ 5.5	V
64	GNDSUB2	Substrate ground	-0.1	0.1	V

1. Not connected internally, should be connected to GND externally.

2.3 Pin-out description

The L9678-S/L9678 pin-out is shown below. The package is a LQFP 64-pin full plastic package.

Figure 1. Pin-out description

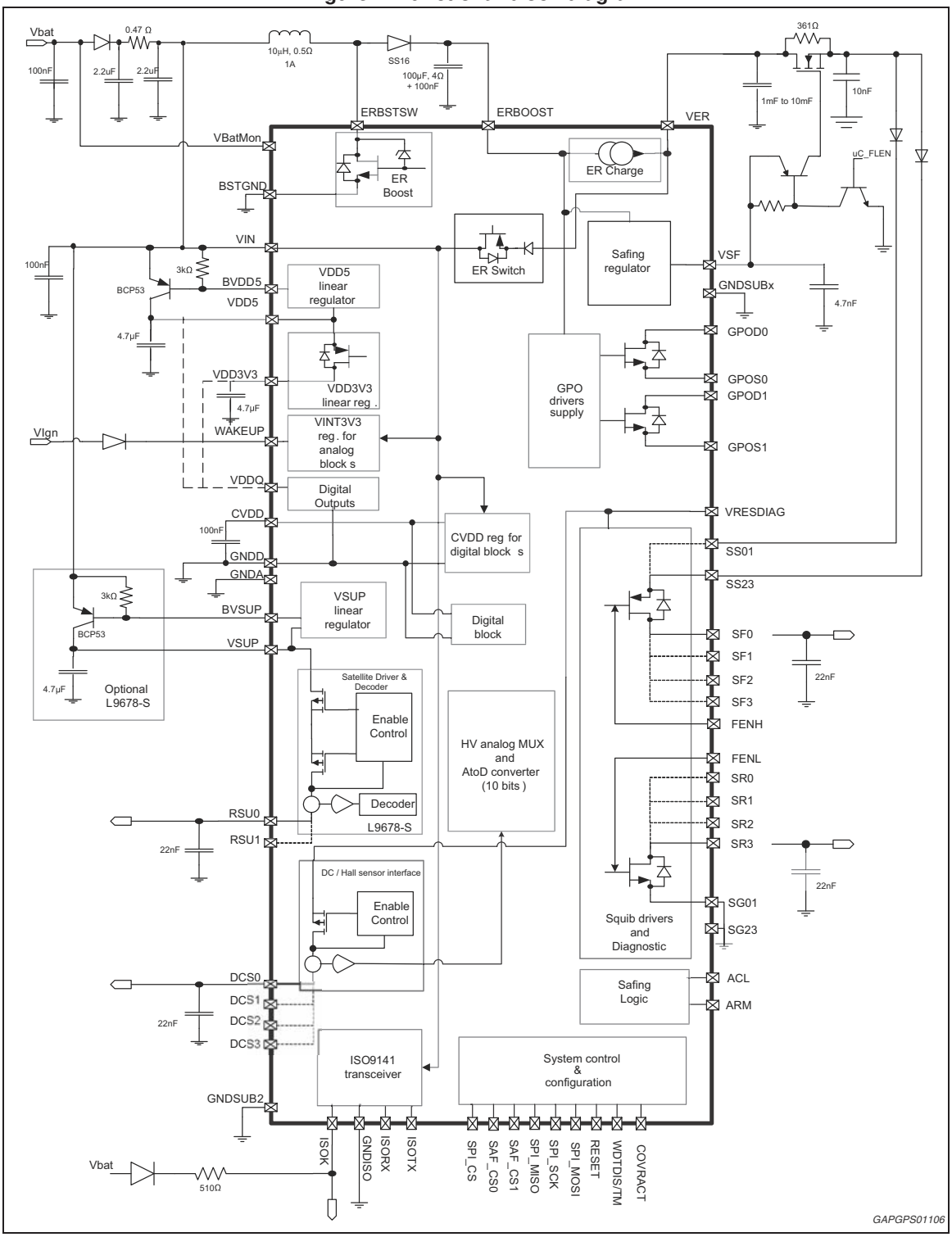


3 Overview and block diagram

The L9678 is a unique solution specifically targeted for entry level airbag systems while permitting the system designer significant flexibility in configuring the system power and management block. The configurable methodology allows cost versus performance trade-off without changing devices or circuit board designs. The L9678 contains the base functionality required for entry level systems and can complete a system design with a microcontroller and acceleration sensor. The high level block diagram is shown below *Figure 2*.

Basic features include a configurable power supply & management block, 4 channel squib drivers, 2 channel HS/LS GPO drivers, 4 channel sensor interface, safing logic, watchdog timer, ISO9141 communications and temperature sensor. The L9678-S device is pin compatible to the L9678 and includes two PSI-5 remote sensor interface channels and a dedicated regulator for remote sensor.

Figure 2. Functional block diagram



4 Start-up power control

4.1 Power supply overview

The L9678 IC contains a complete power management system able to provide all necessary voltages for an entry level airbag application. Moreover L9678 power supply is user configurable allowing the design engineer to balance cost and performance per their particular application. The power supply block contains the following features:

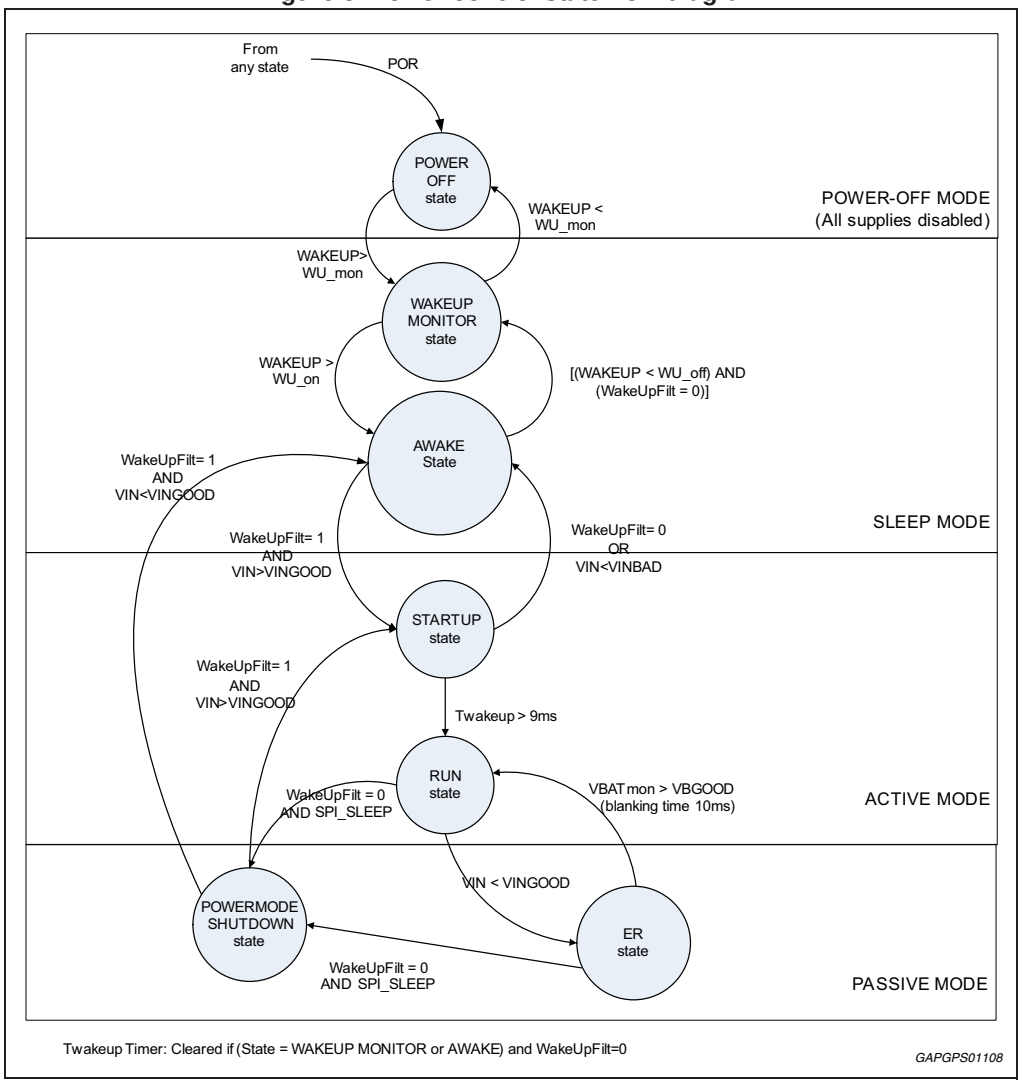
- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail.
- Energy reserve supply (ERBOOST) achieved through an integrated switching boost regulator. The design of this boost regulator is intended to be a cost effective solution with respect to traditional boost regulators because it makes use of a low value inductor with an operative frequency of 1.882 MHz. Switching output is ERBSTSW pin, while voltage feedback input pin is ERBOOST. The output voltage could be set to either 23 V±5% or 33 V±5%.
- Energy reserve capacitor connected to VER pin. To control in-rush current, a dedicated current generator is implemented between ERBOOST pin and VER pin.
- Capability to drive an external safing FET (n-ch type) by means of an internal voltage regulator on VSF pin, where a 20 V level is given (configurable to 25V via SPI command).
- The integrated current limited ER switch requires no external components. This switch is controlled through the integrated power control state machine and is enabled either once a loss of battery is detected or a shutdown command is received. Under the same conditions also the discrete digital pin COVRACT is activated allowing the control of an external optional cross-over switch.
- One linear regulator VDD5 (5 V nominal, ±4% tolerance) requiring external power transistor and capacitors. VDD5 is used as micro-controller supply (in case of 5 V family controllers) and, in any case, as supply for VDD3V3 rail.
- One integrated linear regulator VDD3V3 (3.3 V nominal, ±4% tolerance) requiring external capacitors. VDD3V3 is used as micro-controller supply (in case of 3.3 V family controllers).
- VDDQ pin to provide output voltage rail reference. VDDQ could be connected to either VDD5 or VDD3V3 to enable 5 V or 3.3 V digital communication between device and micro-controller.
- Capability to drive an external power transistor connected to VIN to provide a 7.2 V rail on VSUP pin. This voltage rail could be used to supply PSI-5 remote sensor.
- Battery voltage sense input comparator with hysteresis connected to VBATMON pin. Power-up and operation states are carefully handled with respect to the battery level to provide the most effective power supply configuration.
- All voltage rails (VIN, ERBOOST, VER, VRESDIAG, VDD5, VDD3V3, VSUP and VSF) can be monitored through internal ADC diagnostics.

4.2 Power mode control

Start-up and power down of the L9678 are controlled by the WAKEUP pin, VBATMON pin, VIN pin device status and the SPI interface. There are four main power modes: power-off, sleep, active and passive mode.

Each power mode is described below and represented in the state flow diagram shown in *Figure 3*. The descriptions include references to conditions and sometimes nominal values. The absolute values for each condition are listed in the electrical specifications section.

Figure 3. Power control state flow diagram



4.2.1 Power_off mode

During the Power-off mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as WAKEUP > WU_mon the IC will move to Sleep mode.

4.2.2 Sleep mode

During the Sleep mode the VINT3V3 and CVDD internal regulators are turned on and the IC is ready for full activation of all the other supplies. As soon as battery voltage is over a minimum threshold, all the other supplies are turned on and the IC enters the Active mode.

4.2.3 Active mode

This is the normal operating mode for the system.

All power supplies are enabled and the energy reserve boost converter starts to increase the voltage at ERBOOST. Likewise, the VDD5 regulator is turned on. Once the VDD5 has reached a good value, the VDD3V3 regulator starts up. Once the VDD3V3 regulator is in regulation, RESET is released allowing the system microcontroller and other components to begin their power-on sequence. Among these, also the ER charge current generator can be enabled by the microcontroller via a dedicated SPI command.

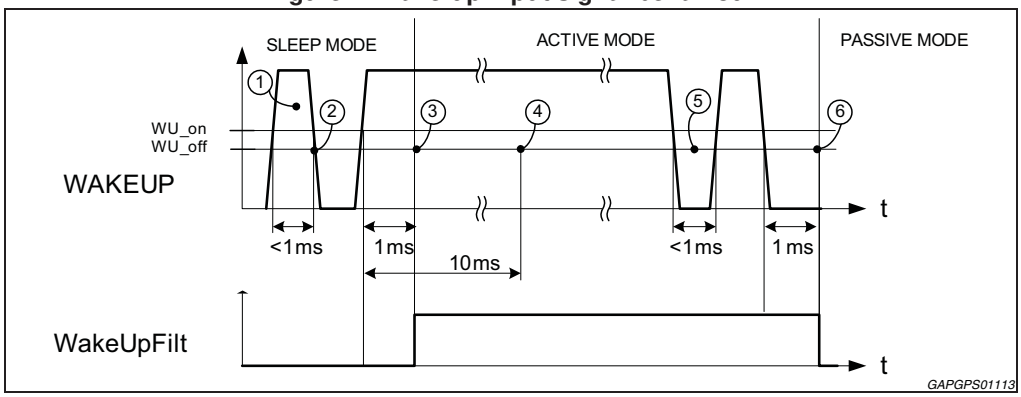
The active mode can be left when either WAKEUP pin or VIN voltage drop down. For the very first 9 ms after having entered the active mode, the WAKEUP pin low would immediately cause the IC to switch back to sleep mode. After that time, WAKEUP pin low must be first confirmed by a MCUSPI_SLEEP command prior to cause the system to switch to passive mode. Passive mode is also entered in case of VIN voltage low.

4.2.4 Passive mode

In this state, the energy reserve charge current is disabled and the ERBOOST boost converter is disabled only if the SYS_CFG(KEEP_ERBST_ON)=0. When in passive mode the device automatically activates both the COVRACT output pin and the integrated ER switch to allow VIN to be connected to the ER capacitor. In this time, VIN is supposed to be increased up to almost VER level and the system operation relies on energy from the ER capacitor. Two scenarios are possible: high or low battery. If VIN < VINGOOD, the device moved from RUN state in ACTIVE mode to the ER state. Here, the ER capacitor is depleted while supplying all the regulators until the POR on internal regulator occurs. The threshold to decide the ER switch activation is based on VIN, because VIN is the supply voltage rail for all regulators. If the device has still a good battery level, it entered the POWERMODE SHUTDOWN thanks to WAKEUP pin and MCU command to switch off. In this case, the VER node will be discharged down to approximately VIN level, which then will be supplied out of the battery line. System will continue to run up to a dedicated SPI command which will lead the device to enter the POWEROFF state.

The wake-up pin is filtered to suppress undesired state changes resulting from transients or glitches. Typical conditions are shown in the chart below and summarized by state.

Figure 4. Wake-up input signal behaviour



Condition summary:

1. No change of sleep mode state but current consumption may exceed specification for sleep mode.
2. The sleep mode current returns within the specified limits.
3. Power supply exits sleep mode. Switchers start operating if applicable voltages exceed under voltage lockouts. As T_{wakeup} time-out is not elapsed, a low level at WAKEUP instantaneously sends the system back to sleep.
4. Sleep Reset is released and the entire system starts operating. A SPI command to enter sleep state would be ignored.
5. No change in system status, a SPI command to enter sleep state would be ignored.
6. No change in system status, but a SPI command to turn off switchers would be accepted and turn the system off.

With the below table, all the functionalities of the device are shown with respect of the power states. When one function is flagged, the related circuitry cannot be activated on that state.

Table 4. Functions disabling by state

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Wakeup detector	X	-	-	-	-	-	-
Internal regulator	X	X	-	-	-	-	-
ERBOOST regulator	X	X	X	-	-	X	X
VSUP regulator (L9678-S only)	X	X	X	-	-	-	-
ER CAP charge current source	X	X	X	-	-	X	X
ER switch	X	X	X	X	X	-	-
COVRACT Output	X	X	X	X	X	-	-
VDD5 regulator	X	X	X	-	-	-	-
VDD3V3 regulator	X	X	X	-	-	-	-
Deployment drivers	X	X	X	-	-	-	-
VSF safing FET regulator	X	X	X	-	-	-	-
Remote sensor interfaces (L9678-S only)	X	X	X	-	-	-	-

Table 4. Functions disabling by state (continued)

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Watchdog	X	X	X	-	-	-	-
Diagnostics	X	X	X	-	-	-	-
DC sensor interface	X	X	X	-	-	-	-
GPO drivers	X	X	X	-	-	-	-
Safing logic	X	X	X	-	-	-	-
ISO9141	X	X	X	-	-	-	-

4.2.5 Power-up and power-down sequence

The behavior of the IC during normal power-up and power-down is shown in *Figure 5* to *Figure 8*. The following sequences represent just a subset of all possible power-up and power-down scenarios.

In *Figure 5* a normal IC power-up controlled by the state of the WAKEUP pin is shown.

Figure 5. Normal power-up sequence - WAKEUP controlled

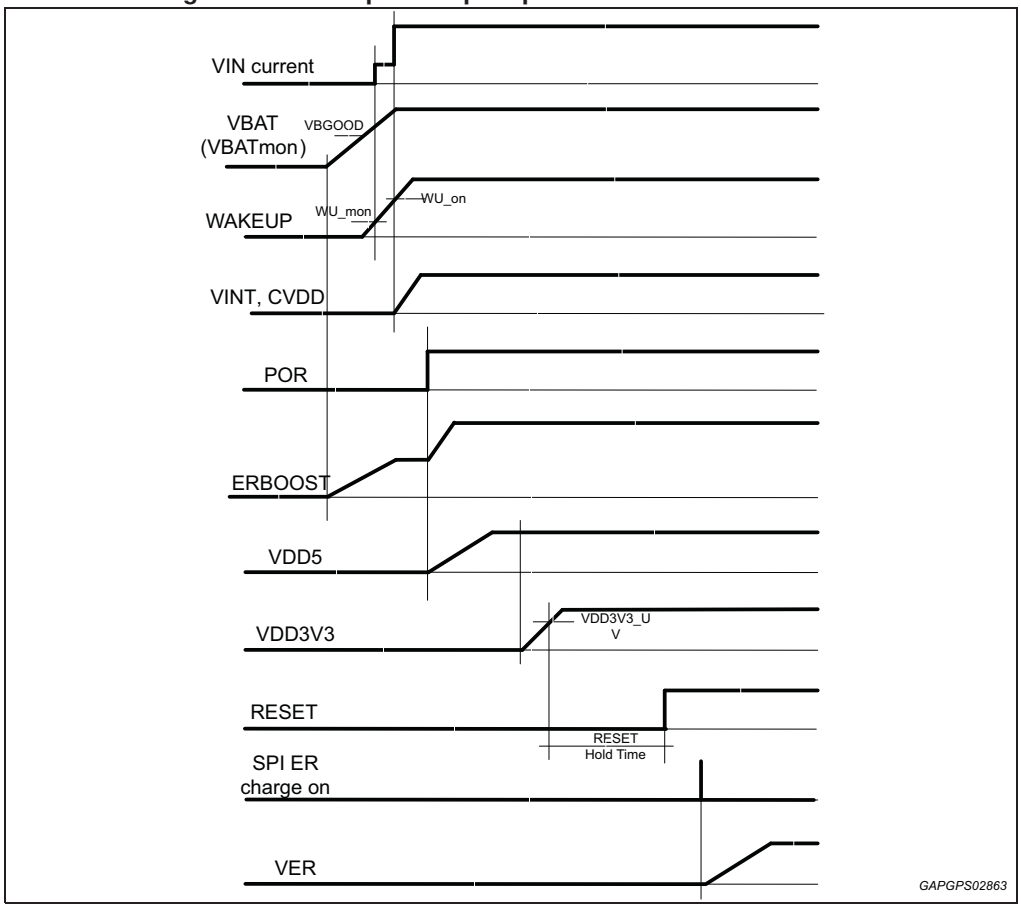
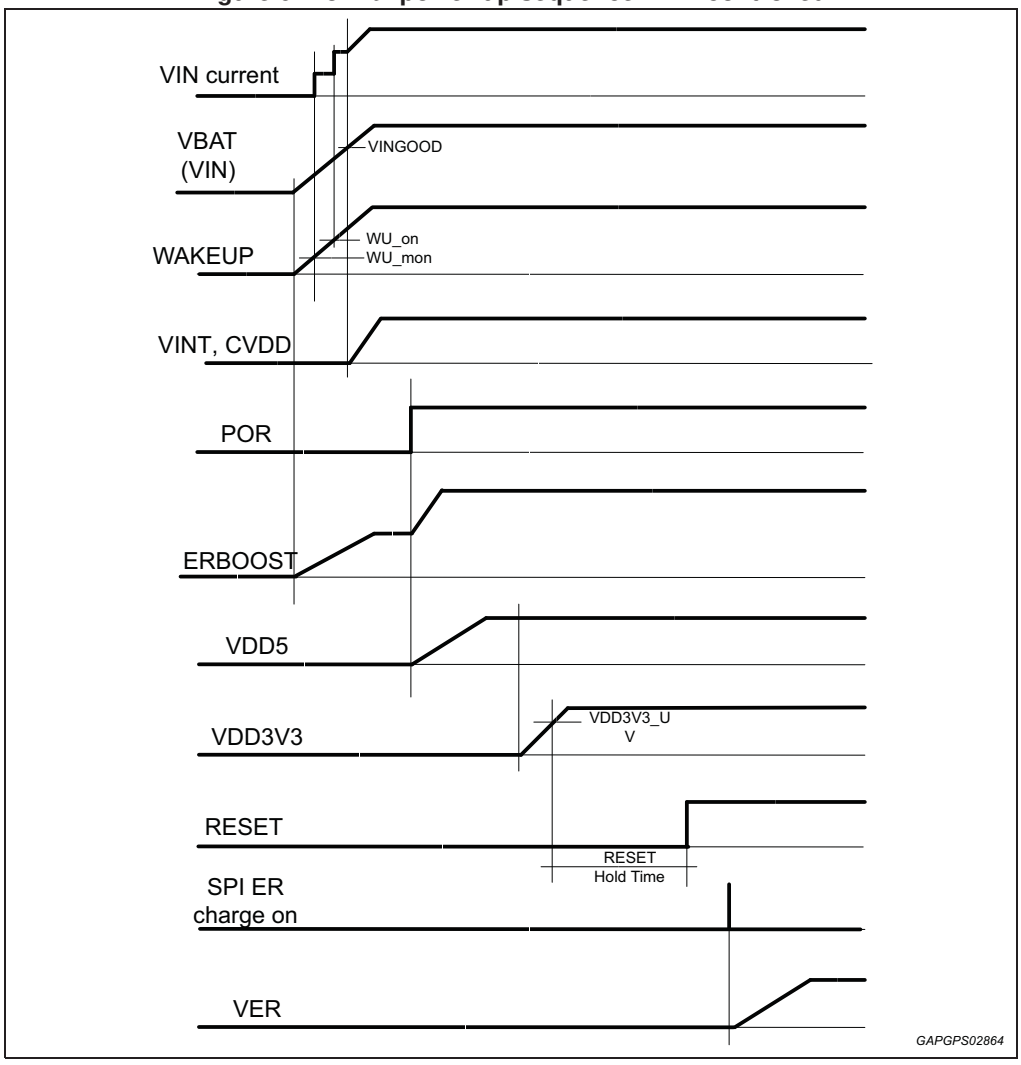


Figure 6. Normal power-up sequence - VIN controlled



Two different scenarios for power-down of the IC are here below shown. *Figure 7* describes the powering down for the case when WAKEUP pin is released. As soon as a SPI_SLEEP command is received by the MCU the System will immediately move to the energy reserve (PASSIVE mode). In *Figure 8*, VIN release begins the shutdown process.

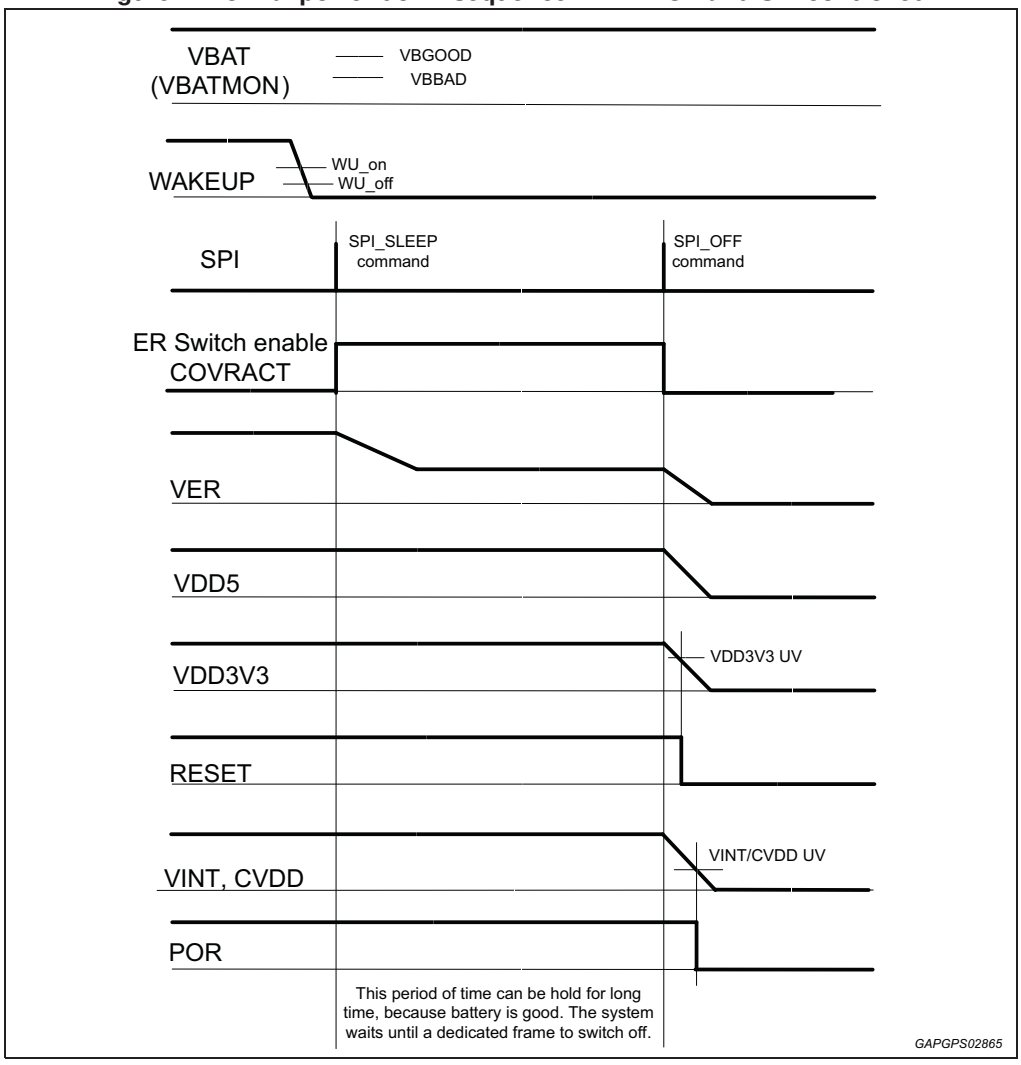



Figure 7. Normal power down sequence - WAKEUP and SPI controlled