



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

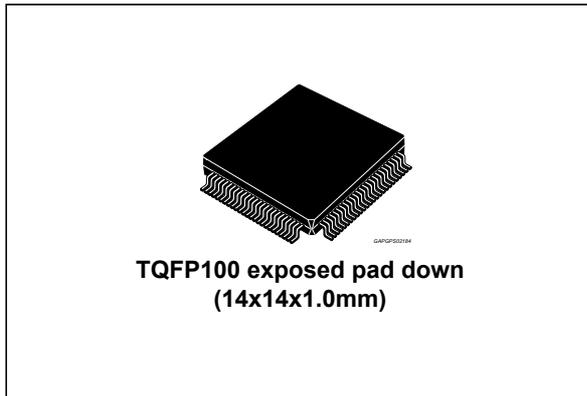
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Automotive advanced airbag IC for mid/high end applications

Datasheet - production data



Features



- AEC-Q100 qualified
- Boost regulator for energy reserve
 - 1.882 MHz operation, $I_{load} = 55$ mA max
 - Output voltage user selectable, 23 V/ 33 V $\pm 5\%$
 - Capacitor value & ESR diagnostics
- Boost regulator for PSI-5 SYNC pulse
 - 1.882 MHz operation,
 - Output voltage, 12 V/14.75 V, user configurable
- Buck regulator for remote sensor
 - 1.882 MHz operation
 - Output voltage, 7.2 V/9 V $\pm 4\%$, user configurable
- Buck regulator for micro controller unit
 - 1.882 MHz operation
 - Output voltage user selectable, 3.3 V or 5.0 V $\pm 3\%$
- Integrated energy reserve crossover switch
 - 3 Ω - 912 mA max
 - Switch active output indicator
- Battery voltage monitor & shutdown control with Wake-up control
- System voltage diagnostics with integrated ADC
- Squib deployment drivers
 - 8 channel HSD/LSD
 - 25 V max deployment voltage
 - Various deployment profiles
 - Current monitoring
 - $R_{measure}$, STB, STG & Leakage diagnostics
 - High & low side driver FET tests
- High side safing switch regulator and enable control
- Two channel remote sensor interface
 - PSI-5 satellite sensors
- Three channel GPO, HSD or LSD configurable, with PWM 0-100% control
- Nine channel hall-effect, resistive or switch sensor interface
- User customizable safing logic
- Specific disarm signal for passenger airbag
- Temporal and algorithmic Watchdog timers
- End of life disposal interface
- Temperature sensor
- 32 bit SPI communications
- 5.5 V minimum operating voltage at device battery pin
- Operating temperature, -40 to 95 °C
- Packaging - 100 pin

Table 1. Device summary

Order code	Package	Pacing
L9679P	TQFP100	Tray
L9679PTR		Tape & Reel

Contents

- 1 Description 13**
- 2 Absolute maximum ratings 14**
- 3 Operative maximum ratings 18**
- 4 Pin out 22**
- 5 Overview and block diagram 23**
 - 5.1 Power supply 24
 - 5.2 Deployment drivers 24
 - 5.3 Remote sensor interfaces 25
 - 5.4 DC sensor interfaces 25
 - 5.5 General purpose outputs 25
 - 5.6 Arming logic 25
 - 5.7 Other features 26
- 6 Start-up and power control 27**
 - 6.1 Power supply overview 27
 - 6.2 Power mode control 29
 - 6.2.1 POWER OFF mode 30
 - 6.2.2 SLEEP mode 30
 - 6.2.3 ACTIVE mode 30
 - 6.2.4 PASSIVE mode 30
 - 6.2.5 Power-up and power-down sequences 33
 - 6.2.6 IC operating states 37
 - 6.3 ERBOOST switching regulator 38
 - 6.4 Energy reserve capacitor charging and discharging circuits 40
 - 6.5 ER CAP diagnostic 41
 - 6.5.1 ER CAP measurement 41
 - 6.5.2 ER CAP ESR measurement 43
 - 6.6 ER switch and COVRACT pin 44
 - 6.7 SYNCBOOST boost regulator 45

6.8	SATBUCK regulator	47
6.9	VCC buck regulator	47
6.10	VSF regulator and control	49
6.11	Oscillators	49
6.12	Reset control	49
7	SPI interfaces	52
7.1	SPI protocol	52
7.2	Global SPI register map	53
7.3	Global SPI tables	65
	Global SPI read/write register	67
7.3.1	Fault status register (FLTSR)	67
7.3.2	System configuration register (SYS_CFG)	69
7.3.3	System control register (SYS_CTL)	72
7.3.4	SPI Sleep command register (SPI_SLEEP)	74
7.3.5	System state register (SYS_STATE)	75
7.3.6	Power state register (POWER_STATE)	76
7.3.7	Deployment configuration registers (DCR_x)	79
7.3.8	Deployment command (DEPCOM)	82
7.3.9	Deployment status registers (DSR_x)	83
7.3.10	Deployment current monitor registers (DCMTSxy)	85
7.3.11	Deploy enable register (SPIDEPEN)	86
7.3.12	Deployment ground loss register (LP_GNDLOSS)	86
7.3.13	Device version register (VERSION_ID)	87
7.3.14	Watchdog retry configuration register (WD_RETRY_CONF)	88
7.3.15	Watchdog timer configuration register (WDTCR)	88
7.3.16	WD1 timer control register (WD1T)	89
7.3.17	WD state register (WDSTATE)	90
7.3.18	Clock configuration register (CLK_CONF)	91
7.3.19	Scrap seed read command register (SCRAP_SEED)	92
7.3.20	Scrap key write command register (SCRAP_KEY)	93
7.3.21	Scrap state entry command register (SCRAP_STATE)	93
7.3.22	Safing state entry command register (SAFING_STATE)	94
7.3.23	WD2 recover write command register (WD2_RECOVER)	94
7.3.24	WD2 seed read command register (WD2_SEED)	95
7.3.25	WD2 key write command register (WD2_KEY)	95

7.3.26	WD test command register (WD_TEST)	96
7.3.27	System diagnostic register (SYSDIAGREQ)	97
7.3.28	Diagnostic result register for deployment loops (LPDIAGSTAT)	98
7.3.29	Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)	101
7.3.30	Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)	104
7.3.31	DC sensor diagnostic configuration command register (SWCTRL)	105
7.3.32	ADC request and data registers (DIAGCTRL_x)	107
7.3.33	Configuration register for switching regulators (SW_REGS_CONF)	110
7.3.34	Global configuration register for GPO driver function (GPOCR)	112
7.3.35	GPOx control register (GPOCTRLx)	113
7.3.36	GPO fault status register (GPOFLTSR)	114
7.3.37	ISOK fault status register (ISOFLTSR)	117
7.3.38	Wheel speed sensor test request register (WSS_TEST)	118
7.3.39	PSI5 configuration register for channel x (RSCRx)	119
7.3.40	Remote sensor control register (RSCTRL)	122
7.3.41	Safing algorithm configuration register (SAF_ALGO_CONF)	123
7.3.42	Arming signals register (ARM_STATE)	124
7.3.43	ARMx assignment registers to specific Loops (LOOP_MATRIX_ARMx)	125
7.3.44	ARMx enable pulse stretch timer status (AEPSTS_ARMx)	126
7.3.45	Passenger inhibit upper threshold for DC sensor 0 (PADTHRESH_HI)	127
7.3.46	Passenger inhibit lower threshold for DC sensor 0 (PADTHRESH_LO)	127
7.3.47	Assignment of PSINH signal to specific Loop(s) (LOOP_MATRIX_PSINH)	128
7.3.48	Safing records enable register (SAF_ENABLE)	128
7.3.49	Safing records request mask registers (SAF_REQ_MASK_x)	129
7.3.50	Safing records request target registers (SAF_REQ_TARGET_x)	131
7.3.51	Safing records response mask registers (SAF_RESP_MASK_x)	133
7.3.52	Safing records response mask registers (SAF_RESP_TARGET_x)	135
7.3.53	Safing records data mask registers (SAF_DATA_MASK_x)	137
7.3.54	Safing record threshold registers (SAF_THRESHOLD_x)	139
7.3.55	Safing control x registers (SAF_CONTROL_x)	141
7.3.56	Safing record compare complete register (SAF_CC)	144
7.4	Remote sensor SPI register map	145
7.5	Remote sensor SPI tables	146
7.5.1	Remote sensor SPI global status word	146
7.6	Remote sensor SPI read/write registers	147

7.6.1	Remote sensor data/fault registers (RSDRx @FLT = 0)	147
7.6.2	Remote sensor data/fault registers (RSDRx @ FLT=1)	149
7.6.3	Remote sensor x current registers y (RSTHRx_y)	152
7.6.4	Arming signals status register (ARM_STATE)	153
7.6.5	Safing record compare complete register (SAF_CC)	154
8	Deployment drivers	155
8.1	Control logic	155
8.1.1	Deployment current selection	157
8.1.2	Deploy command expiration timer	157
8.1.3	Deployment control flow	158
8.1.4	Deployment current monitoring	159
8.1.5	Deployment success	159
8.2	Energy reserve - deployment voltage	159
8.3	Deployment ground return	159
8.4	Deployment driver protections	160
8.4.1	Delayed low-side deactivation	160
8.4.2	Low-side voltage clamp	160
8.4.3	Short to battery	160
8.4.4	Short to ground	160
8.4.5	Intermittent open squib	160
8.5	Diagnostics	161
8.5.1	Low level diagnostic approach	162
8.5.2	High level diagnostic approach	169
9	Remote sensor interface	171
9.1	PSI5 mode	172
9.1.1	Functional description	172
9.1.2	Sensor data integrity: LCID and CRC	175
9.1.3	Detailed description	175
9.2	Test mode	178
9.3	Remote sensor interface fault protection	178
9.3.1	Short to ground, current limit	178
9.3.2	Short to battery	178
9.3.3	Cross link	178
9.3.4	Leakage to battery, sensor open	179

9.3.5	Leakage to ground	179
9.3.6	Thermal shutdown	179
10	Watchdog timers	180
10.1	Temporal watchdog (WD1)	180
10.1.1	Watchdog timer configuration	181
10.1.2	Watchdog timer operation	182
10.2	Algorithmic watchdog (WD2)	183
10.3	Watchdog reset assertion timer	185
10.4	Watchdog timer disable input (WDT/TM)	185
11	DC sensor interface	186
11.1	Passenger inhibit interface	188
12	Safing logic	190
12.1	Safing logic overview	190
12.2	SPI sensor data decoding	191
12.3	In-frame and out-of-frame responses	198
12.4	Safing state machine operation	199
12.4.1	Simple threshold comparison operation	199
12.5	Safing engine output logic (ARMxINT)	200
12.5.1	Arming pulse stretch	203
12.6	Additional communication line	204
13	General purpose output (GPO) drivers	207
14	ISO9141 Transceiver (K-Line)	210
15	System voltage diagnostics	211
15.1	Analog to digital algorithmic converter	217
16	Temperature sensor	218
17	Electrical characteristics	219
17.1	Configuration and control	219
17.2	Internal analog reference	223

17.3	Internal regulators	224
17.4	Watchdog	225
17.5	Oscillators	226
17.6	Reset	227
17.7	SPI interface	227
17.8	ERBoost regulator	229
17.9	ER CAP current generators and diagnostic	232
17.10	ER switch	233
17.11	COVRACT	234
17.12	SYNCBOOST converter	234
17.13	SATBUCK converter	237
17.14	VCC regulator	239
17.15	VSF regulator	241
17.16	Deployment drivers	242
17.17	Deployment driver diagnostic	247
17.17.1	Squib resistance measurement	247
17.17.2	Squib leakage test (VRCM)	248
17.17.3	High/low side FET test	250
17.17.4	Deployment timer test	250
17.18	Remote sensor interface	251
17.18.1	PSI-5 interface	251
17.19	DC sensor interface	256
17.20	Safing engine	257
17.21	General purpose output drivers	260
17.22	ISO9141 Interface (K-LINE)	262
17.23	Analog to digital converter	264
17.24	Voltage diagnostics (Analog MUX)	265
17.25	Temperature sensor	266
18	Quality information	267
18.1	OTP memory	267
19	Errata sheet	268
20	Package information	269

20.1 TQFP100 (14x14x1.4 mm exp. pad down) package information 269

21 Revision history 271

List of tables

Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	14
Table 3.	Operative maximum ratings	18
Table 4.	Functions disabling by state	31
Table 5.	SPI MOSI and MISO frames layout	52
Table 6.	Global SPI register map	54
Table 7.	Global SPI Global Status Word.	65
Table 8.	Remote sensor SPI register map	145
Table 9.	GSW - Remote sensor SPI global status word.	146
Table 10.	Short between loops diagnostics decoding.	164
Table 11.	HS FET TEST	166
Table 12.	LS FET TEST	166
Table 13.	Watchdog timer status description	181
Table 14.	WD2 states and signals	184
Table 15.	Example of combine function operation	198
Table 16.	Short to ground fault in LS mode	208
Table 17.	Short to battery fault in HS mode	209
Table 18.	Diagnostics control register (DIAGCTRLx).	213
Table 19.	Diagnostics divider ratios	215
Table 20.	Configuration and control DC specifications.	219
Table 21.	Configuration and control AC specifications.	222
Table 22.	Open ground detection DC specifications.	223
Table 23.	GND_OPEN_AC - Open ground detection DC specifications	223
Table 24.	Internal analog reference	223
Table 25.	Internal regulator DC specifications	224
Table 26.	Internal regulators AC specifications	224
Table 27.	Temporal watchdog timer AC specifications (WD1)	225
Table 28.	Algorithmic watchdog timer DC specifications (WD2).	225
Table 29.	Algorithmic watchdog timer AC specifications (WD2).	225
Table 30.	Oscillators specifications.	226
Table 31.	Reset DC specifications	227
Table 32.	Reset AC specifications	227
Table 33.	Global and remote sensor SPI DC specifications.	227
Table 34.	SPI AC specifications	228
Table 35.	ERBoost regulator DC specifications	229
Table 36.	ERBoost regulator AC specifications	231
Table 37.	ERBOOST Converter external components design info.	231
Table 38.	ER CAP current generators and diagnostic DC specifications	232
Table 39.	ER CAP current generators and diagnostic AC specifications	233
Table 40.	ER Switch DC specifications.	233
Table 41.	ER Switch AC specifications.	233
Table 42.	COVRACT DC specifications	234
Table 43.	COVRACT AC specifications	234
Table 44.	SYNCBOOST converter DC specifications.	234
Table 45.	SYNCBOOST converter AC specifications.	236
Table 46.	SYNCBOOST converter external components design info.	236
Table 47.	SATBUCK converter DC specifications	237
Table 48.	SATBUCK converter AC specifications	238

Table 49.	SATBUCK converter external components design info	238
Table 50.	VCC converter DC specifications	239
Table 51.	VCC converter AC specifications	240
Table 52.	VCC converter external components design info	240
Table 53.	VSF regulator DC specifications	241
Table 54.	VSF regulator AC specifications	241
Table 55.	Deployment drivers – DC specifications	242
Table 56.	Deployment drivers – AC specifications	246
Table 57.	Deployment drivers diagnostics - Squib resistance measurement	247
Table 58.	Squib Leakage Test (VRCM)	248
Table 59.	High/low side FET test	250
Table 60.	Deployment timer test - AC specifications	250
Table 61.	PSI-5 satellite transceiver - DC specifications	251
Table 62.	PSI-5 satellite transceiver - AC specifications	252
Table 63.	DC Sensor interface specifications	256
Table 64.	Arming Interface – DC specifications	257
Table 65.	Arming interface – AC specifications	258
Table 66.	GPO interface DC specifications	260
Table 67.	GPO driver interface – AC specifications	261
Table 68.	ISO9141 interface DC specifications	262
Table 69.	ISO9141 interface transceiver AC specifications	263
Table 70.	Analog to digital converter	264
Table 71.	Voltage diagnostics (Analog MUX)	265
Table 72.	Temperature sensor specifications	266
Table 73.	Errata sheet	268
Table 74.	TQFP100 (14x14x1.4 mm exp. pad down) package mechanical data	270
Table 75.	Document revision history	271

List of figures

Figure 1.	Pin connection diagram (top view)	22
Figure 2.	Device function block diagram	23
Figure 3.	Power supply block diagram	28
Figure 4.	Power control state flow diagram	29
Figure 5.	Wake-up input signal behaviour	31
Figure 6.	Normal power-up sequence	33
Figure 7.	Normal power down sequence through POWERMODE SHUTDOWN state - no ER cap active discharge	34
Figure 8.	Normal power down sequence through Powermode Shutdown state - ER cap active discharge	35
Figure 9.	Normal power down sequence through ER state	36
Figure 10.	IC operating state diagram	38
Figure 11.	ERBOOST regulator block diagram	39
Figure 12.	ERBOOST regulator state diagram	40
Figure 13.	ER charge state diagram	40
Figure 14.	ER discharge state diagram	41
Figure 15.	ER CAP measurement block diagram	41
Figure 16.	ER CAP measurement timing diagram	42
Figure 17.	ER ESR measurement block diagram	43
Figure 18.	ER ESR measurement timing diagram	44
Figure 19.	ER switch state diagram	45
Figure 20.	SYNCBOOST regulator block diagram	46
Figure 21.	SYNCBOOST regulator state diagram	46
Figure 22.	SATBUCK regulator state diagram	47
Figure 23.	VCC regulator state diagram	48
Figure 24.	VSF control logic	49
Figure 25.	Internal voltage monitors	50
Figure 26.	Reset control logic	51
Figure 27.	Deployment driver control blocks	155
Figure 28.	Deployment driver control logic - Enable signal	156
Figure 29.	Deployment driver control logic - Turn-on signals	156
Figure 30.	Deployment driver block	157
Figure 31.	Global SPI deployment enable state diagram	158
Figure 32.	Current monitor counter behavior	159
Figure 33.	Deployment loop diagnostics	162
Figure 34.	SRx pull-down enable logic	163
Figure 35.	Deployment timer diagnostic sequence	168
Figure 36.	High level loop diagnostic flow1	169
Figure 37.	High level loop diagnostic flow2	170
Figure 38.	Remote sensor interface logic blocks	171
Figure 39.	PSI-5 remote sensor protocol (10-bit, 1-bit parity)	172
Figure 40.	Manchester bit encoding	173
Figure 41.	Remote sensor synchronization pulses	174
Figure 42.	PSI5 slot timing control	174
Figure 43.	Manchester decoder state diagram	176
Figure 44.	WD1 Temporal watchdog state diagram	180
Figure 45.	Watchdog timer refresh diagram	182
Figure 46.	Algorithmic watchdog timer flow diagram	183

Figure 47.	DC sensor interface block diagram	186
Figure 48.	Passenger inhibit logic diagram	188
Figure 49.	Top level safing engine flow chart	190
Figure 50.	Safing engine – 32-bit message decoding flow chart	191
Figure 51.	Safing engine – 16-bit Message decoding flow chart	192
Figure 52.	Safing engine - Validate data flow chart	193
Figure 53.	Safing engine - Combine function flow chart	194
Figure 54.	Safing engine threshold comparison.	195
Figure 55.	Safing engine - Compare complete	196
Figure 56.	In-frame example	199
Figure 57.	Out-of-frame example.	199
Figure 58.	Safing engine arming flow diagram.	201
Figure 59.	Safing engine diagnostic logic	202
Figure 60.	ARMx input/output control logic	203
Figure 61.	Pulse stretch timer example	204
Figure 62.	Scrap SEED-KEY state diagram.	205
Figure 63.	Scrap ACL state diagram	205
Figure 64.	Disposal PWM signal	206
Figure 65.	GPO driver and diagnostic block diagram	207
Figure 66.	GPO Over temperature logic	208
Figure 67.	ISO9141 block diagram	210
Figure 68.	ADC MUX	211
Figure 69.	ADC conversion time	217
Figure 70.	SPI timing diagram	229
Figure 71.	Deployment drivers diagram	245
Figure 72.	TQFP100 (14x14x1.4 mm exp. pad down) package outline.	269

1 Description

The L9679P is an advanced airbag system chip solution targeted for mature airbag market and integrated safety markets. This device is family compatible with the L9678 and L9680 devices. Safety system integration is enabled through higher power supply currents and integrated PSI-5 satellite interface.

High frequency power supply design allows further cost reduction by using smaller and less expensive external components. All switching regulators operate at 1.882 MHz while buck converters have integrated synchronous rectifiers.

Additional attention is given to system integrity and diagnostics. The reserve capacitor is electrically isolated from the boost regulator by a 50 mA nominal fixed current source, controlling in-rush an additional capacitor discharge fixed current source is integrated to diagnose the reserve capacitor value and ESR. The same current sources can be used to discharge the capacitor at shutdown.

Thanks to low quiescent current, the device can be directly connected to battery. In this way, the device start-up and shutdown are controlled through the wake-up input function. The power supply and crossover function are controlled automatically through the internal state machine.

The user can select both ECU logic voltage (V_{CC} at 3.3 V or 5.0 V) and energy reserve output voltage (at either 23 V or 33 V). Deployment voltage is set to a maximum of 25 V for all profiles and can be controlled through external safing switch circuit using the high side safing switch reference enabled through the system SPI interface or the arming logic.

2 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

The operating junction temperature range is -40 °C to +150 °C. The maximum junction temperature must not be exceeded except when in deployment and within the deploy power stages. Deployment is possible starting with a junction temperature of 150 °C. A power dissipation calculation has to be performed for the final application limiting the available functionality to a subset of it in order to respect to the power dissipation capability.

Table 2. Absolute maximum ratings

Pin#	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.3	$VCC+0.3 \leq 6.5$	V
2	SCLK_RS	Remote SPI interface clock	-0.3	$VCC+0.3 \leq 6.5$	V
3	MOSI_RS	Remote SPI interface data in	-0.3	$VCC+0.3 \leq 6.5$	V
4	MISO_RS	Remote SPI interface data out	-0.3	$VCC+0.3 \leq 6.5$	V
5	RESET	Reset output	-0.3	$VCC+0.3 \leq 6.5$	V
6	MISO_G	Global SPI interface data out	-0.3	$VCC+0.3 \leq 6.5$	V
7	MOSI_G	Global SPI interface data in	-0.3	$VCC+0.3 \leq 6.5$	V
8	SCLK_G	Global SPI interface clock	-0.3	$VCC+0.3 \leq 6.5$	V
9	CS_G	Global SPI interface chip select	-0.3	$VCC+0.3 \leq 6.5$	V
10	WDT/TM	Watchdog disable	-0.3	20	V
11	SR4	Squib 4 low-side pin	-0.3	40	V
12	SF4	Squib 4 high-side pin	-1.0	40	V
13	SS45	Squib 4 & 5 deployment supply pin	-0.3	40	V
14	SF5	Squib 5 high-side pin	-1.0	40	V
15	SR5	Squib 5 low-side pin	-0.3	40	V
16	SR0	Squib 0 low-side pin	-0.3	40	V
17	SF0	Squib 0 high-side pin	-1.0	40	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
19	SF1	Squib 1 high-side pin	-1.0	40	V
20	SR1	Squib 1 low-side pin	-0.3	40	V
21	NC	Not connected			
22	NC	Not connected			
23	NC	Not connected			
24	NC	Not connected			
25	NC	Not connected			
26	DCS8	DC Sensor interface channel 8	-2	40	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
27	DCS7	DC Sensor interface channel 7	-2	40	V
28	DCS6	DC Sensor interface channel 6	-2	40	V
29	DCS5	DC Sensor interface channel 5	-2	40	V
30	DCS4	DC Sensor interface channel 4	-2	40	V
31	DCS3	DC Sensor interface channel 3	-2	40	V
32	DCS2	DC Sensor interface channel 2	-2	40	V
33	DCS1	DC Sensor interface channel 1	-2	40	V
34	DCS0	DC Sensor interface channel 0	-2	40	V
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	40	V
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	40	V
37	NC	Not connected			
38	NC	Not connected			
39	GPOD0	GPO driver 0 drain output pin	-1	40	V
40	GPOS0	GPO driver 0 source output pin	-1	40	V
41	GPOS1	GPO driver 1 source output pin	-1	40	V
42	GPOD1	GPO driver 1 drain output pin	-1	40	V
43	GPOD2	GPO driver 2 drain output pin	-1	40	V
44	GPOS2	GPO driver 2 source output pin	-1	40	V
45	COVRACT	External Crossover Switch Driver	-0.3	40	V
46	ISOK	ISO9141 bus pin (K-LINE)	-18	40	V
47	NC	Not connected			
48	SATSYNC	Initiate Satellite Sensor Sync Pulse	-0.3	$VCC+0.3 \leq 6.5$	V
49	PSINHB	Active Low Passenger Airbag Inhibit Control	-0.3	$VCC+0.3 \leq 6.5$	V
50	GNDSUB1	Substrate ground / Squib ground	-0.3	0.3	V
51	NC	Not connected			
52	NC	Not connected			
53	NC	Not connected			
54	NC	Not connected			
55	NC	Not connected			
56	SR3	Squib 3 low-side pin	-0.3	40	V
57	SF3	Squib 3 high-side pin	-1.0	40	V
58	SS23	Squib 2 & 3 deployment supply pin	-0.3	40	V
59	SF2	Squib 2 high-side pin	-1.0	40	V
60	SR2	Squib 2 low-side pin	-0.3	40	V
61	SR7	Squib 7 low-side pin	-0.3	40	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
62	SF7	Squib 7 high-side pin	-1.0	40	V
63	SS67	Squib 6 & 7 deployment supply pin	-0.3	40	V
64	SF6	Squib 6 high-side pin	-1.0	40	V
65	SR6	Squib 6 low-side pin	-0.3	40	V
66	GND A	Analog ground	-0.3	0.3	V
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.3	$VCC+0.3 \leq 6.5$	V
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.3	$VCC+0.3 \leq 6.5$	V
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.3	$VCC+0.3 \leq 6.5$	V
70	ISOTX	ISO9141 transmit pin	-0.3	$VCC+0.3 \leq 6.5$	V
71	WD2_LockOut	WD2 fault output	-0.3	$VCC+0.3 \leq 6.5$	V
72	NC	Not connected			
73	ISORX	ISO9141 receiver pin	-0.3	$VCC+0.3 \leq 6.5$	V
74	WS1	Wheel speed output Ch1	-0.3	$VCC+0.3 \leq 6.5$	V
75	WS0	Wheel speed output Ch0	-0.3	$VCC+0.3 \leq 6.5$	V
76	VCCSEL	VCC select	-0.3	40	V
77	ACL	EOL disposal control input	-0.3	40	V
78	WAKEUP	Wake-up control input	-0.3	40	V
79	VBATMON	Battery line voltage monitor	-18 ⁽¹⁾	40	V
80	VSF	Safing regulator supply output	-0.3	40	V
81	VIN	Battery connection	-0.3	40	V
82	VER	Reserve voltage	-0.3	40	V
83	ERBOOST	Energy reserve regulator output	-0.3	40	V
84	ERBSTSW	ER Boost switching output	-0.3	40	V
85	BSTGND	Boost regulators ground	-0.3	0.3	V
86	SYNCBSTSW	SYNC Boost switching output	-0.3	40	V
87	SYNCBOOST	SYNC boost output voltage	-0.3	40	V
88	SATBCKSW	SAT Buck switching output	-0.3	40	V
89	SATGND	SAT Buck regulator ground	-0.3	0.3	V
90	SATBUCK	SAT Buck output voltage	-0.3	40	-
91	VCCBCKSW	VCC Buck switch output	-0.3	40	V
92	VCCGND	VCC Buck Ground	-0.3	0.3	V
93	CVDD	Internal 3.3V regulator output	-0.3	4.6	V
94	GNDD	Digital ground	-0.3	0.3	-
95	VCC	VCC Buck voltage	-0.3	6.5	V
96	ARM1	Arming output 1	-0.3	$VCC+0.3 \leq 6.5$	V

Table 2. Absolute maximum ratings (continued)

Pin#	Pin name	Pin function	Min	Max	Unit
97	ARM2	Arming output 2	-0.3	$V_{CC}+0.3 \leq 6.5$	V
98	NC	Not connected			
99	FENL	LS driver FET control input	-0.3	$V_{CC}+0.3 \leq 6.5$	V
100	GND SUB2	Substrate ground / Squib ground	-0.3	0.3	V
-	Exposed pad down	Substrate ground / Squib ground	-0.3	0.3	V

1. VBATMON negative AMR is -18 V or -20 mA.

3 Operative maximum ratings

Within the operating ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min	Max	Unit
1	CS_RS	Remote SPI interface chip select	-0.1	$VCC+0.1 \leq 5.5$	V
2	SCLK_RS	Remote SPI interface clock	-0.1	$VCC+0.1 \leq 5.5$	V
3	MOSI_RS	Remote SPI interface data in	-0.1	$VCC+0.1 \leq 5.5$	V
4	MISO_RS	Remote SPI interface data out	-0.1	$VCC+0.1 \leq 5.5$	V
5	RESET	Reset output	-0.1	$VCC+0.1 \leq 5.5$	V
6	MISO_G	Global SPI interface data out	-0.1	$VCC+0.1 \leq 5.5$	V
7	MOSI_G	Global SPI interface data in	-0.1	$VCC+0.1 \leq 5.5$	V
8	SCLK_G	Global SPI interface clock	-0.1	$VCC+0.1 \leq 5.5$	V
9	CS_G	Global SPI interface chip select	-0.1	$VCC+0.1 \leq 5.5$	V
10	WDT/TM	Watchdog disable	-0.1	15	V
11	SR4	Squib 4 low-side pin	-0.1	SS45	V
12	SF4	Squib 4 high-side pin	-1.0	SS45	V
13	SS45	Squib 4 & 5 deployment supply pin	-0.1	VER	V
14	SF5	Squib 5 high-side pin	-1.0	SS45	V
15	SR5	Squib 5 low-side pin	-0.1	SS45	V
16	SR0	Squib 0 low-side pin	-0.1	SS01	V
17	SF0	Squib 0 high-side pin	-1.0	SS01	V
18	SS01	Squib 0 & 1 deployment supply pin	-0.1	VER	V
19	SF1	Squib 1 high-side pin	-1.0	SS01	V
20	SR1	Squib 1 low-side pin	-0.1	SS01	V
21	NC	Not connected			
22	NC	Not connected			
23	NC	Not connected			
24	NC	Not connected			
25	NC	Not connected			
26	DCS8	DC sensor interface channel 8	-1	18	V
27	DCS7	DC sensor interface channel 7	-1	18	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
28	DCS6	DC sensor interface channel 6	-1	18	V
29	DCS5	DC sensor interface channel 5	-1	18	V
30	DCS4	DC sensor interface channel 4	-1	18	V
31	DCS3	DC sensor interface channel 3	-1	18	V
32	DCS2	DC sensor interface channel 2	-1	18	V
33	DCS1	DC sensor interface channel 1	-1	18	V
34	DCS0	DC Sensor interface channel 0	-1	18	V
35	RSU0	PSI-5/WSS ch. 0 remote sensor output	-1	$V_{RSU_SYNC_MAX}$	V
36	RSU1	PSI-5/WSS ch. 1 remote sensor output	-1	$V_{RSU_SYNC_MAX}$	V
37	NC	Not connected			
38	NC	Not connected			
39	GPOD0	GPO driver 0 drain output pin	-0.1	40	V
40	GPOS0	GPO driver 0 source output pin	-1	40	V
41	GPOS1	GPO driver 1 source output pin	-1	40	V
42	GPOD1	GPO driver 1 drain output pin	-0.1	40	V
43	GPOD2	GPO driver 2 drain output pin	-0.1	40	V
44	GPOS2	GPO driver 2 source output pin	-1	40	V
45	COVRACT	External crossover switch driver	-0.1	40	V
46	ISOK	ISO9141 bus pin (K-LINE)	-0.1	$VCC+0.1 \leq 5.5$	V
47	NC	Not connected			
48	SATSYNC	Initiate satellite sensor sync pulse	-0.1	$VCC+0.1 \leq 5.5$	V
49	PSINHB	Active low passenger airbag inhibit control	-1	18	V
50	GNDSUB1	Substrate ground / Squib ground	-0.1	0.1	V
51	NC	Not connected			
52	NC	Not connected			
53	NC	Not connected			
54	NC	Not connected			
55	NC	Not connected			
56	SR3	Squib 3 low-side pin	-0.1	SS23	V
57	SF3	Squib 3 high-side pin	-1.0	SS23	V
58	SS23	Squib 2 & 3 deployment supply pin	-0.1	VER	V
59	SF2	Squib 2 high-side pin	-1.0	SS23	V
60	SR2	Squib 2 low-side pin	-0.1	SS23	V
61	SR7	Squib 7 low-side pin	-0.1	SS67	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
62	SF7	Squib 7 high-side pin	-1.0	SS67	V
63	SS67	Squib 6 & 7 deployment supply pin	-0.1	VER	V
64	SF6	Squib 6 high-side pin	-1.0	SS67	V
65	SR6	Squib 6 low-side pin	-0.1	SS67	V
66	GND A	Analog ground	-0.1	0.1	V
67	SAF_CS0	SPI interface safing sensor chip select 0	-0.1	VCC+0.1 <= 5.5	V
68	SAF_CS1	SPI interface safing sensor chip select 1	-0.1	VCC+0.1 <= 5.5	V
69	SAF_CS2	SPI interface safing sensor chip select 2	-0.1	VCC+0.1 <= 5.5	V
70	ISOTX	ISO9141 transmit pin	-0.1	VCC+0.1 <= 5.5	V
71	WD2_LockOut	WD2 Fault Output	-0.1	VCC+0.1 <= 5.5	V
72	NC	Not connected			
73	ISORX	ISO9141 receiver pin	-0.1	VCC+0.1 <= 5.5	V
74	WS1	Wheel Speed Output Ch1	-0.1	VCC+0.1 <= 5.5	V
75	WS0	Wheel Speed Output Ch0	-0.1	VCC+0.1 <= 5.5	V
76	VCCSEL	VCC select	-0.1	35	V
77	ACL	EOL disposal control input	-0.1	35	V
78	WAKEUP	Wake-up control input	-0.1	VIN	V
79	VBATMON	Battery line voltage monitor	-1	18	V
80	VSF	Safing regulator supply output	-0.1	27	V
81	VIN	Battery connection	-0.1	35	V
82	VER	Reserve voltage	-0.1	35	V
83	ERBOOST	Energy reserve regulator output	-0.1	35	V
84	ERBSTSW	ER Boost switching output	-0.1	35	V
85	BSTGND	Boost regulators ground	-0.1	0.1	V
86	SYNCBSTSW	SYNC Boost switching output	-0.1	35	V
87	SYNCBOOST	SYNC boost output voltage	-0.1	35	V
88	SATBCKSW	SAT Buck switching output	-0.1	35	V
89	SATGND	SAT Buck regulator ground	-0.1	0.1	V
90	SATBUCK	SAT Buck output voltage	-0.1	10	-
91	VCCBCKSW	VCC Buck switch Output	-0.1	10	V
92	VCCGND	VCC Buck Ground	-0.1	0.1	V
93	CVDD	Internal 3.3V regulator output	-0.1	3.6	V
94	GNDD	Digital ground	-0.1	0.1	-
95	VCC	VCC Buck Voltage	-0.1	5.5	V

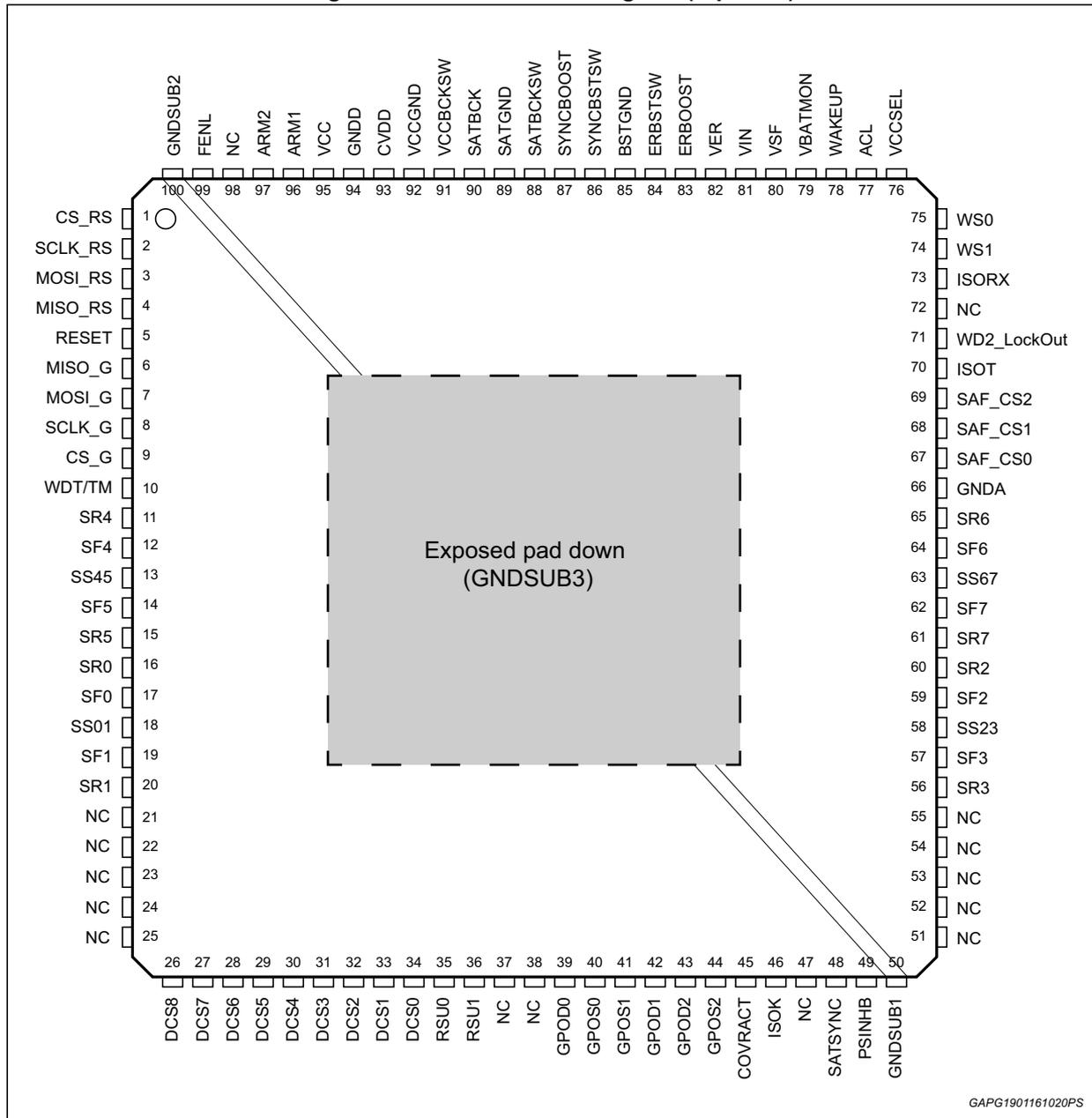
Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min	Max	Unit
96	ARM1	Arming Output 1	-0.1	VCC+0.1 <= 5.5	V
97	ARM2	Arming Output 2	-0.1	VCC+0.1 <= 5.5	V
98	NC	Not connected			
99	FENL	LS Driver FET control input	-0.1	VCC+0.1 <= 5.5	V
100	GNDSUB2	Substrate ground / Squib ground	-0.1	0.1	V
-	Exposed Pad Down	Substrate ground / Squib ground	-0.1	0.1	V

4 Pin out

The L9679P pin out is shown below. The IC is housed in a 100 pin package (14 x 14 x 1.0mm) with a 7.6 x 7.6 mm exposed pad down.

Figure 1. Pin connection diagram (top view)

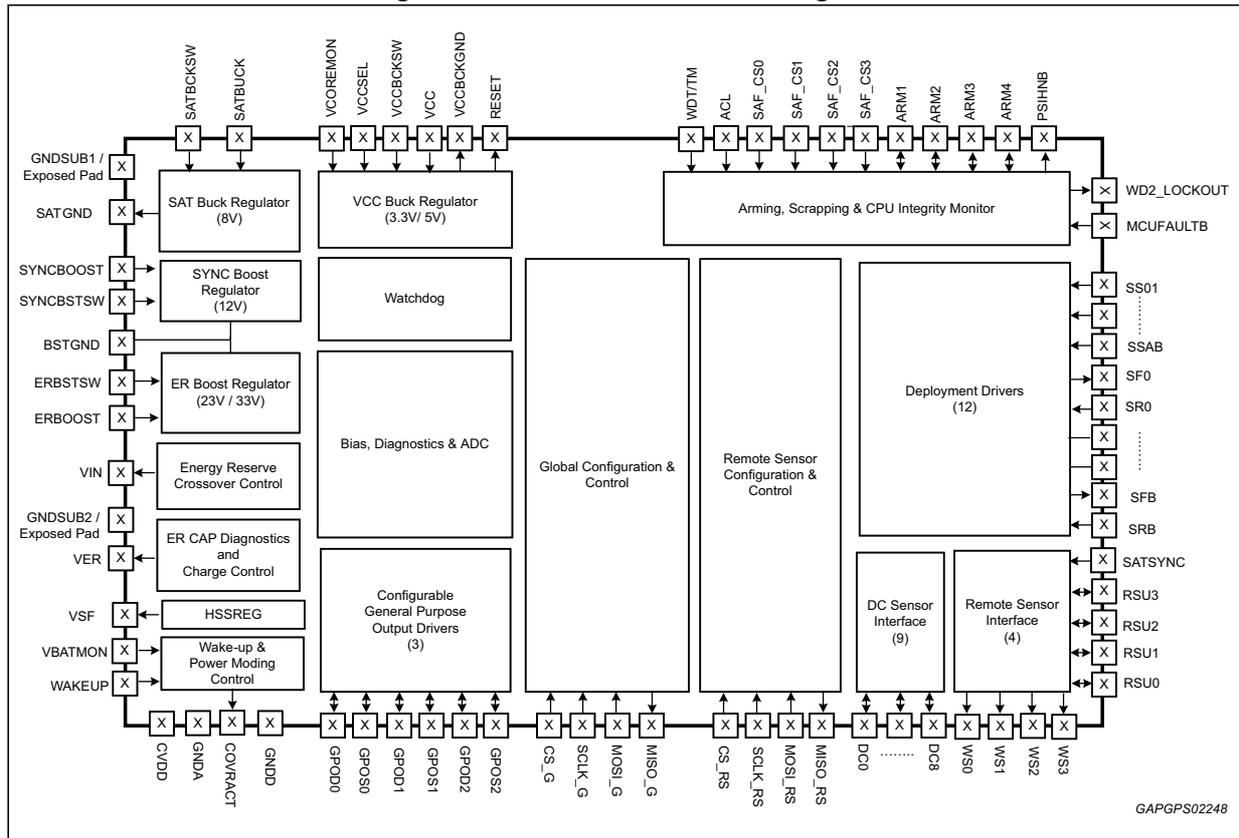


The exposed pad is electrically shorted to the substrate pins GNDSUB1 and GNDSUB2. These three connection nodes are to be kept shorted on the application.

5 Overview and block diagram

The L9679P IC is an application specific standard component air bag system chip. Its main functions include, power management, deployment drivers, remote sensor interfaces (PSI-5 satellite sensors), diagnostics, deployment arming, hall-effect sensor interface, general purpose output drivers, watchdog timer and a dedicated passenger airbag disarm signal. A block diagram for this IC is shown in *Figure 2*.

Figure 2. Device function block diagram



5.1 Power supply

- Integrated 1.882 MHz boost regulator, 33 V \pm 5% or 23 V \pm 5% nominal output
- Integrated 1.882 MHz boost regulator, 12 V/14.75 V nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 7.2 V/9 V \pm 4% nominal output, user selectable via SPI command
- Integrated 1.882 MHz synchronous buck regulator, 5 V \pm 3% or 3.3 V \pm 3% nominal output, user selectable via VCCSEL pin
- Over and under voltage detection and shutdown for all regulators
- Under-voltage lockout to guarantee buck regulator outputs disabled and discharged
- Integrated energy reserve capacitor fixed constant current source (50 mA, nominal) switch for controlled inrush and charge characteristics
- Integrated energy reserve diagnostics, capacitor value and ESR
- Integrated energy reserve crossover switch with current limit and battery input voltage monitoring
- Crossover switch 'active' output signal
- Integrated 25 V/20 V SPI selectable linear regulator for high side safing FET gate supply enabled via SPI or arming logic
- Reset output

5.2 Deployment drivers

- 8 high side deployment drivers, 8 low side deployment drivers
- User programmable deployment options
 - 1.20 A or 1.75 A minimum
 - programmable time in 0.1ms increments
- Capability to deploy a squib with a minimum current of 1.2 / 1.75 A and the low side FET shorted to ground up to 25 V on SSxy
- Independently-controlled high-side and low-side FETs
- Squib resistance measurement
- Firing current monitor feature
- High and low side FET tests
- Open & shorts diagnostics, including between loop drivers
- Independent fire enable logic, SPI and discrete digital input

5.3 Remote sensor interfaces

- Two channel receiver
 - standard PSI-5 v1.3 compatible with sync pulse
- Current limit with short circuit protection diagnostics
- PSI-5 satellite sensor mode
 - Auto-adjusting current trip points for each satellite channel
 - Even parity, 8 or 10 bit messages, 125k or 189kbps
 - Satellite message error detection

5.4 DC sensor interfaces

- Nine integrated switch interfaces with current sense capability
- Compatible with Hall-effect, resistive and switch sensors
- Current limit protected
- System dedicated path to disable the passenger airbag with input from DC sensor interface

5.5 General purpose outputs

- Three configurable high-side or low-side drivers
- ON-OFF mode and PWM 0-100% fine control
- Diagnostics for short circuit protection and open load detection
- Current limit and reverse battery protected

5.6 Arming logic

- User configurable safing algorithms with 12 safing records
- Four digital sensor interfaces through SPI
- Independent user programmable thresholds
- Independent user programmable latch timers
- Two discrete and independent arming logic outputs
- Two discrete and independent internal arming signals
- End-of-life interface