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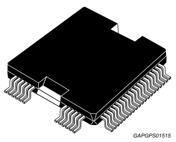
# L9779WD

## Multifunction IC for engine management system

**Datasheet - production data**



**HiQUAD-64**

## Features

- 5 V logic regulator
- 3.3 V logic regulator
- 5 V tracking sensor supply
- Smart reset function
- Power latch with Secure Engine Off (SEO) functionality, to safely complete driver switch off procedure
- Flying wheel interface function (VRS) with adaptive time and amplitude control
- Protected low-side relay driver
  - OUT13 to 18, MRD
- Protected low-side (injector drivers)
  - OUT1 to 4
- Protected low-side (high current)
  - OUT5, 6, 7
- Protected low-side (low current)
  - OUT19, 20
- IGBT pre-drivers (IGN1 to 4)
- External MOS pre-drivers (OUT8 to 9)
- Configurable power stages CPS
  - Stepper motor driver/ high-side - low-side (OUT21 to 28)
- Thermal warning and shutdown
- Serial interface
  - Micro Second Channel interface (MSC)
  - ISO9141 interface (K-Line)
- High speed CAN transceiver
- Dedicated pin VDDIO to select the voltage level of digital output used for serial communication
- VDA 2.0 compliance with 3 level Watchdog
- Package: HiQUAD-64

## Description

The L9779WD is an integrated circuit designed for automotive environment and implemented in BCD6S technology.

It is conceived to provide all basic functions for standard engine management control units.

It is assembled in the HiQUAD-64 power package.

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| L9779WD | HiQUAD-64 | Tray |
| L9779WD-TR | HiQUAD-64 | Tape and Reel |

# Contents

# List of tables

# List of figures

# 1 Detailed features description

- Package
  - HiQUAD-64
- 5 V logic regulator
  - 5 V precision voltage regulator (± 2%) with external NMOS
  - Max current regulated: 400 mA
  - Charge pump capacitor at pin CP is used to drive the gate of the external NMOS transistor
- 3.3 V logic regulator
  - 3.3 V precision voltage regulator (± 2%) with over-current protection
  - Max current regulated: 100 mA
- 5 V tracking sensor supply
  - 2 x 5 V tracking sensor supply with protection and diagnosis on MSC
  - Short-circuit to Vbat/GND fully protected
  - Max current regulated: 2 x 100 mA
- VDD_IO supply
  - All the digital output is supplied by external VDD_IO through VDD_IO pin
- Smart reset
  - Main Reset monitoring VB_UV Logic voltage management and safety control
- Watch dog
  - Main reset management 5 V voltage monitoring safety output disable
  - MicroSecond Channel activity watch dog
  - MSC controllable query and answer watch dog compliant with VDA2.0 level 3 (enabled by default)
- Power latch
  - L9779WD is switched on by KEY_ON signal and switched off by logic OR of KEY_ON signal and MicroSecond Channel bit
- Secure engine off mode (default) switches off the drivers in the following order:
  - OUT1 through to OUT4 in 225 ms (typical)
  - OUT13 and OUT14 in 600 ms (typical)
- Flying wheel interface function (VRS)
  - The VRS is the interface between the microprocessor and the magnetic pick-up or variable reluctance sensor that collects the information coming from the flying wheel
  - Adaptive filtering on amplitude and timing adapts better the device response to VRS input switching
- Protected low-side driver
  - LSa (OUT1 to 5)

    4 Ch. serial IN via MicroSecond Channel, $R_{dson}$ = 0.72 Ohm @150 °C, $V_{cl}$ = 58 V ±5, $I_{max}$ = 2.2 A;

    1 Ch. serial IN via MicroSecond Channel, $R_{dson}$ = 0.72 Ohm @150 °C, $V_{cl}$ = 58 V ±5, $I_{max}$ = 3 A;

- LSb (OUT6, 7)

  2 Ch. serial IN via MicroSecond Channel, $R_{dson}$ = 0.47 Ohm @150°C, $V_{cl}$ = 45 V ±5, $I_{max}$ = 5 A
- LSc (OUT19, 20)

  2 Ch serial IN via MicroSecond Channel, $I_{max}$ = 50 mA

Full diagnosis on MicroSecond Channel (2 bit for each channel) and voltage slew rate control.

When an over current fault occurs, the driver switch off with faster slew rate in order to reduce the power dissipation.

- Protected low side relay driver (OUT13 to 18, MRD)
  - LSD

    6 Ch. serial IN via MicroSecond Channel, $R_{dson}$ = 1.5 Ohm @150 °C, $V_{cl}$ = 48 V, $I_{max}$ = 600 mA (2 of them with low battery voltage function);

    1 main relay driver $R_{dson}$ = 2.4 Ohm @150 °C, $V_{cl}$ = 48 V, $I_{max}$ = 600 mA

  With full diagnosis on MicroSecond Channel (2 bit for each channel) and voltage slew-rate control.

  When an over current fault occurs, the driver switch off with faster slew rate in order to reduce the power dissipation.
- Ignition pre-drivers (IGN1 to 4)
  - 4 x ignition pre-drivers with full diagnostic.
- External MOS pre-drivers (OUT8 to 9)
  - 2 x MOS pre-drivers with sense of the external drain voltage to perform the diagnostic:

    Open load in OFF state

    Shorted load in ON state with programmable threshold voltage and programmable filter time via MSC
- Configurable power stages CPS: stepper motor driver/ high-side - low-side (OUT21 to 28)

  1 x Stepper motor driver designed for a double winding coil motor, used for engine idle speed control.

  The bridge driver is made by 4 independent high-side drivers and 4 independent low-side drivers:
  - 4 high-side driver, $R_{dson}$ =1.5 Ohm, $I_{max}$ = 600 mA
  - 4 low-side driver, $R_{dson}$ = 1.5 Ohm, $I_{max}$ = 600mA

  The 4 high-side drivers and the 4 low-side drivers can be controlled independently

  The low-side drivers could be connected in parallel (in pairs): OUT22 with OUT24 and OUT27 with OUT28.

  Low-side and high-side drivers implement voltage SR control to minimize emission.

  Two high-side drivers have the low battery voltage function.
- Thermal shutdown
  - 1 x Thermal shutdown ($T_j$ > 175 °C = Tsd) if $T_j$ > Tsd: VTRK1, 2 are turned off.
  - 1 x Thermal shutdown ($T_j$ > 175 °C = Tsd) if Tj > Tsd: OUT1 to 10, OUT13 to 20, OUT21 to 28, IGN1 to 4 are turned off.
  - 1 x Thermal shutdown ($T_j$ > 175 °C = Tsd) if $T_j$ > Tsd: MRD is turned off (if battery present).

  - 1 x Thermal Shutdown ($T_j$ > 175 °C = Tsd) if $T_j$ > Tsd: V3V3 is turned off.

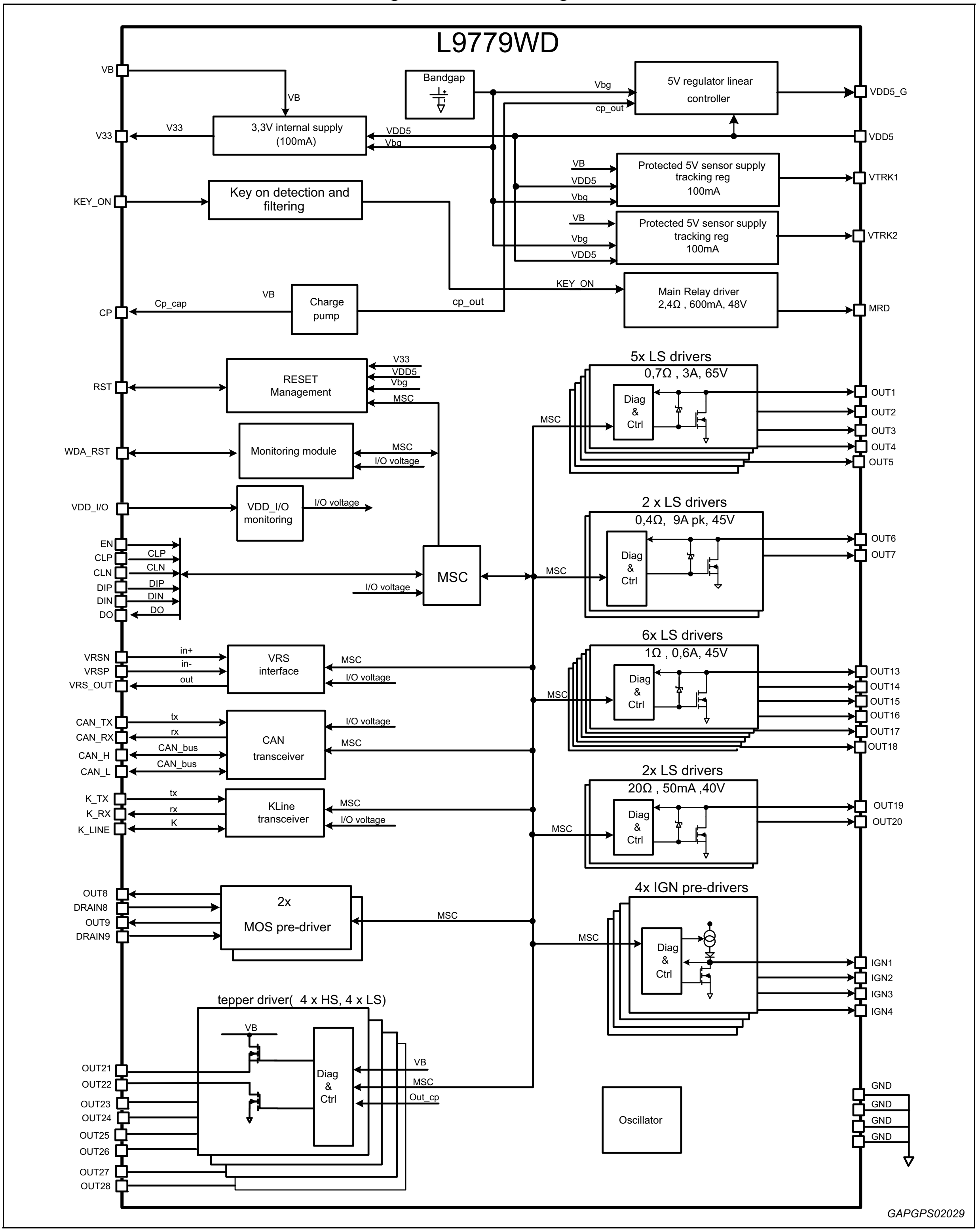
There are 5 temperature sensors for OT2 (OUT1..10, OUT13…20, OUT21…28, IGN1…4 are turned off) in different Layout position, they are logically “AND” in case of thermal shutdown.

- ISO9141 interface
  - ISO9141 serial interface (K-Line)
- CAN transceiver

  The CAN bus transceiver allows the connection of the microcontroller, with CAN controller unit, to a high speed CAN bus with transmission rates up to 1Mbit/s for exchange of data with other ECUs.

# 2 Block diagram

**Figure 1. Block diagram**



# 3 Pins description

**Figure 2. Pins connection diagram (top view)**

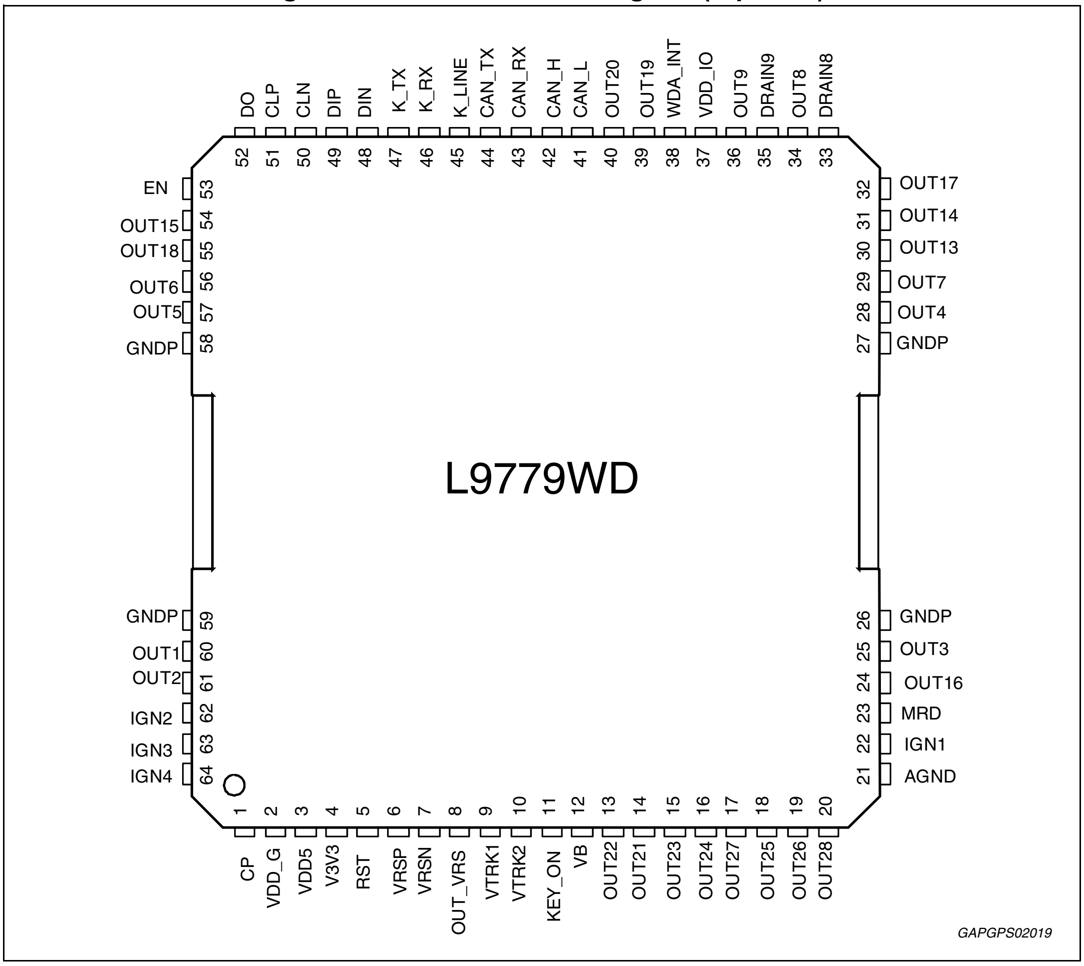



**Table 2. Pins description**

| Pin# | Name | Function | Type | Polarization/note |
|---|---|---|---|---|
| **Supply block** | | | | |
| 12 | VB | Battery supply | Power supply polarization | - |
| 3 | VDD5 | 5 V output voltage regulator | Power logic output supply | - |
| 2 | VDD_G | 5 V regulator ext MOS gate | Analog output | - |
| 11 | KEY_ON | Key signal | Analog Input | Internal pull down resistor |
| 4 | V3V3 | 3.3 V output voltage regulator | Power logic output supply | - |
| 1 | CP | Charge pump | Analog Input | - |
| 9 | VTRK1 | Sensor1 tracking supply 5V | Sensor supply output | - |

Table 2. Pins description (continued)

| Pin# | Name | Function | Type | Polarization/note |
|---|---|---|---|---|
| 10 | VTRK2 | Sensor1 tracking supply 5V | Sensor supply output | - |
| 5 | RST | Reset input/output for µP | Output: push-pull<br>DGT input | Open drain |
| 37 | VDD_IO | External supply | Power input | - |
| 38 | WDA_INT | WDA Interrupt Signal | Output: open drain DGT input | - |
| **VRS** | | | | |
| 7 | VRSN | Negative VRS input | Analog input | 1.65 V internal polarization |
| 6 | VRSP | Positive VRS input | Analog input | 1.65 V internal polarization |
| 8 | OUT_VRS | Digital VRS output | DGT output | Push-pull |
| **CAN** | | | | |
| 44 | CAN_TX | Can transceiver input (from TX µP) | DGT input | - |
| 43 | CAN_RX | Can transceiver output (to RX µP) | DGT output | - |
| 42 | CAN_H | Bi-dir protected CAN_H wire | Analog input/output | - |
| 41 | CAN_L | Bi-dir protected CAN_L wire | Analog input/output | - |
| **ISO9141** | | | | |
| 47 | K_TX | ISO9141 logical input | DGT input | Internal pull-up resistor |
| 45 | K_LINE | Bi-dir protected K-line wire | Analog input/output | Open drain |
| 46 | K_RX | ISO9141logical output | DGT output | Push-pull |
| **Low side drivers** | | | | |
| 60 | OUT1 | Output low-side 1 for R, L load (Injector) | Power output | Open drain |
| 61 | OUT2 | Output low-side 2 for R, L load (Injector) | Power output | Open drain |
| 25 | OUT3 | Output low-side 3 for R, L load (Injector) | Power output | Open drain |
| 28 | OUT4 | Output low-side 4 for R, L load (Injector) | Power output | Open drain |
| 26 | PGND | Power GND | PGND | - |
| 27 | PGND | Power GND | PGND | - |
| 57 | OUT5 | Output low-side 5 for R, L load (high current) | Power output | Open drain |
| 56 | OUT6 | Output low-side 6 for R, L load (heater) | Power output | Open drain |
| 29 | OUT7 | Output low-side 7 for R, L load (heater) | Power output | Open drain |

Table 2. Pins description (continued)

| Pin# | Name | Function | Type | Polarization/note |
|---|---|---|---|---|
| 30 | OUT13 | Output low-side 13 for relay (low. bat.) | Power output | Open drain |
| 31 | OUT14 | Output low-side 14 for relay (low. bat.) | Power output | Open drain |
| 54 | OUT15 | output low-side 15 for relay | Power output | Open drain |
| 24 | OUT16 | Output low-side 16 for relay | Power output | Open drain |
| 32 | OUT17 | Output low-side 17 for relay | Power output | Open drain |
| 55 | OUT18 | Output low-side 18 for relay | Power output | Open drain |
| 58 | PGND | Power GND | PGND | - |
| 59 | PGND | Power GND | PGND | - |
| **Ignition pre-driver** | | | | |
| 22 | IGN1 | Output ignition driver 1 | Power output | - |
| 62 | IGN2 | Output ignition driver 2 | Power output | - |
| 63 | IGN3 | Output ignition driver 3 | Power output | - |
| 64 | IGN4 | Output ignition driver 4 | Power output | - |
| 21 | GND_STEP | Analog GND | AGND | - |
| **Main relay driver** | | | | |
| 23 | MRD | Main relay driver | Power output | Open drain |
| **Low current drivers (50 mA)** | | | | |
| 39 | OUT19 | Output low-side 19 | Power Output | Open drain |
| 40 | OUT20 | Output low-side 20 | Power Output | Open drain |
| **Ext MOS pre-driver** | | | | |
| 33 | DRAIN8 | Ext. drain voltage sense for OUT8 | Input | - |
| 34 | OUT8 | Gate driver for ext MOS OUT8 | Power output | - |
| 35 | DRAIN9 | Ext. Drain voltage sense for OUT9 | Input | - |
| 36 | OUT9 | Gate driver for ext MOS OUT9 | Power output | - |
| **MSC interface** | | | | |
| 51 | CLP | Clock positive for differential interface | DGT Input | - |
| 50 | CLN | Clock negative for differential interface | DGT Input | - |
| 49 | DIP | Downstream data positive for differential interface | DGT Input | - |
| 48 | DIN | Downstream data negative for differential interface | DGT Input | - |
| 53 | EN | Enable pin | DGT Input | - |

**Table 2. Pins description (continued)**

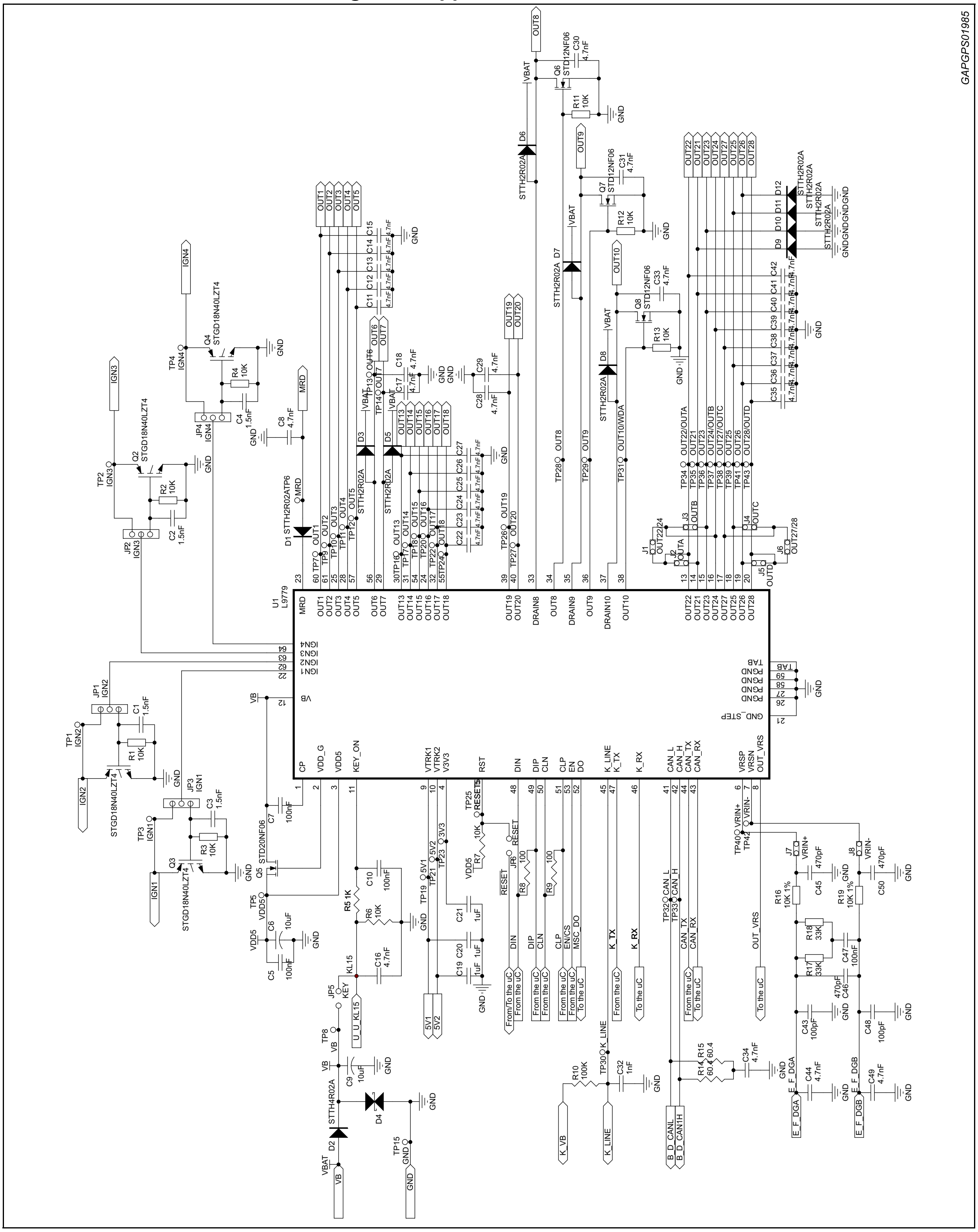
| Pin# | Name | Function | Type | Polarization/note |
|---|---|---|---|---|
| 52 | DO | Upstream data push-pull output | DGT Output | - |
| **Configurable power stage: Stepper motor driver / low-side, high-side drivers** | | | | |
| 14 | OUT21 | Output high-side 21 / stepper (low. bat.) | Power output | Open drain |
| 13 | OUT22 | Output low-side 22/ stepper | Power output | Open drain |
| 15 | OUT23 | Output high-side 23 / stepper | Power output | Open drain |
| 16 | OUT24 | Output low-side 24 / stepper | Power output | Open drain |
| 18 | OUT25 | Output high-side 25 / stepper (low. bat.) | Power output | Open drain |
| 19 | OUT26 | Output high-side 26 / stepper | Power output | Open drain |
| 17 | OUT27 | Output low-side 27/ stepper | Power output | Open drain |
| 20 | OUT28 | Output low-side 28 / stepper | Power output | Open drain |

*Note: OUT11 and OUT12 are not valid.*

*All the powers GND are connected to the package slug, so it is mandatory to connect the slug to GND.*

# 4 Application schematic

**Figure 3. Application schematic**



# 5 Absolute maximum ratings

**Warning: Maximum ratings are absolute ratings: exceeding any of these values may cause permanent damage to the integrated circuit**

**Table 3. Absolute maximum ratings**

| Pin | Parameter | Condition | Value | Unit |
|---|---|---|---|---|
| VB | DC supply battery power voltage (Vb) | Also without external components | -0.3 to +40 | V |
| V3V3 | DC logic supply voltage | - | -0.3 to VDD5, when V3V3 = VDD5 = max+19V | V |
| VTRK1,2 | DC sensors supply voltage | - | -2 to +40 | V |
| VDD_G | - | - | -0.3 to VDD5, when VDDG = VDD5 = max+19 | V |
| VDD5 | Voltage pin | - | -0.3 to 19 | V |
| CP | - | - | -0.3 to 40<br>Max ABS = +40 V when VB = 40 V | V |
| KEY_ON | - | Protected with external component (R = 1 kΩ plus a diode, refer to *Figure 4*) for negative pulse (isopulse 1) | -1.2 to +40 | V |
| RST | - | - | -0.3 to +19 | V |
| VRSP | - | Max current to be limited with external resistors (see *Section 6.16.3: Application circuits on page 106*) | -20 to +20 | mA |
| VRSM | - | Max current to be limited with external resistors (see *Section 6.16.3: Application circuits on page 106*) | -20 to +20 | mA |
| MRD | - | - | -0.3 to +40 | V |
| OUT1-5 | Low-side output | - | -1 to +53 | V |
| OUT6-7 | Low-side output | - | -1 to +40 | V |
| OUT8-9 | - | - | -0.3 to 40 | V |
| VDD_IO | DC logic output supply voltage | - | -0.3 to 19 | V |
| DRAIN8-9 | - | - | -1 to 60 | V |
| WDA_INT | - | - | -0.3 to 19 | V |

**Table 3. Absolute maximum ratings (continued)**

| Pin | Parameter | Condition | Value | Unit |
|---|---|---|---|---|
| OUT13-18 | Low-side output | - | -1 to +40 | V |
| OUT19-20 | Low-side output | - | -1 to +40 | |
| IGNx | - | - | -1 to 19 | V |
| OUT21, 23, 25, 26 | High-side output | With external diode vs ground for negative voltage | -1.0 to VB (–2.0 dynamically for a short time) | V |
| OUT22, 24, 27 28 | Low-side output | - | -1 to 41 | V |
| DIP,DIN | - | - | -0.3 to +19 | V |
| DO, CAN_RX,K_RX, OUT_VRS | - | - | -0.3 to VDD_IO, when DO = VDD_IO = max+19V | V |
| EN | - | - | -0.3 to +19 | V |
| CLP,CLN | - | - | -0.3 to +19 | V |
| CAN_TX | - | - | -0.3 to +19 | V |
| CAN_H, CAN_L | - | - | -18 to 40 (1) | V |
| K_TX | - | - | -0.3 to +19 | V |
| K_LINE | - | - | -18 to 40 | V |

1. In case of negative voltage is applied on CAN_H or CAN_L the voltage slew rate must be <10 V/µs.

## 5.1 ESD protection

**Table 4. ESD protection**

| Item | Condition | Min | Max | Unit |
|---|---|---|---|---|
| All pins | Electro static discharge voltage “Charged-device-model – CDM” all pin(1) | -500 | +500 | V |
| All pins | Electro static discharge voltage “Charged-device-model – CDM” corner pin (1,20,21,32,33,52,53,64) | -750 | +750 | V |
| All pins | ESD voltage HBM respect to GND | -1.5 | +1.5 | KV |
| Pins to connector(2) | ESD voltage HBM respect to GND | -4 | +4 | KV |

1. All pins are OK at ±500 V except VTRK1, VTRK2, VB, CP, HIGHSIDE21-23-25-26. [1, 9, 10, 12, 14, 15, 18 e 19]. Pins 1, 9, 10, 12, 14, 15, 18 e 19 passed ±350 V
2. Pins to connector are: LSa, LSb, LSc, LSd, DRAIN1-3, IGNx,VTRK1-2, CAN_H, CAN_L, K_LINE, OUT22, 24, 27, 28. (60, 61, 24, 25, 28, 29, 30, 31, 32, 39, 40, 54, 55, 56, 57, 22, 62, 63, 64, 9, 10, 42, 41, 45, 13, 16, 17, 20, 33, 35).

Test circuit according to HBM (EIA/JESD22-A114-B) and CDM (EIA/JESD22-C101-C).

## 5.2 Latch-up test

According to JEDEC 78 class 2 level A.

## 5.3 Temperature ranges and thermal data

**Table 5. Temperature ranges and thermal data**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{amb}$ | Operating temperature | -40 | 125 | °C |
| $T_j$ | Continuative operative junction temperature | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature | -40 | 150 | °C |
| $R_{thj\text{-}case}$ | Thermal resistance junction-to-case | - | 1 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-to-ambient(1) | - | 16 | °C/W |
| $T_s$ | Lead temperature during soldering (for a time = 10 s max) | - | 260 | °C |

1. With 2S2P+vias PCB.

## 5.4 Operating range

**Table 6. Operating range**

| Pins symbol | Battery voltage range | Junction temperature condition | Note |
|---|---|---|---|
| VB | 4.15 V < Vb < 6 V | -40 < Tj < 40 | Low battery |
| | 6 V < Vb = 18 V | -40 < Tj < 150 | Normal battery |
| | 18 V < Vb = 28 V | -40 < Tj < 40 | High battery |
| | 28 < Vb = 40 V, $t_{rise}$ = 10ms, $T_{pulse}$= 400 ms. | -40 < Tj < 40 | Load dump |

### 5.4.1 Low battery

All the functions are guaranteed with degraded parameters. The voltage regulators follow VB in RDSon mode with drop-out depending on load current.
V3V3 regulator works as expected assuming VDD5 > 4 V.

### 5.4.2 Normal battery

All the functions and the parameters are guaranteed by testing coverage.

### 5.4.3 High battery

All the functions are guaranteed with degraded parameters.

### 5.4.4 Load dump

The device is switched-off if load dump exceeds battery overvoltage threshold for a time longer than filter time.

# 6 Functional description

## 6.1 Ignition switch, main relay, battery pin

The system has an ignition switch pin KEY_ON and a pin VB for battery behind the main relay connected at pin MRD.

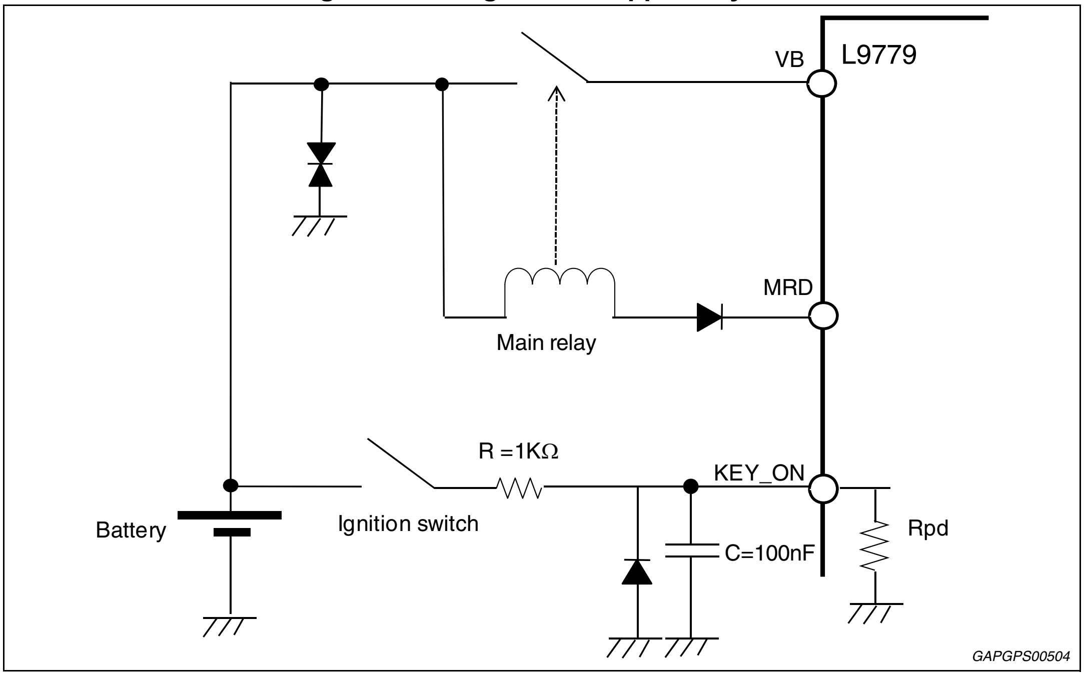
L9779WD can also support the configuration where it is permanently supplied by VB; in this case the MRD output can be used to connect the loads to VB.

At pin KEY_ON there is an external diode for reverse battery protection. An internal Pull-down resistor is provided on the KEY_ON pin. The external components to be connected to KEY pin are shown in the below schematic.

Internal functions and regulators are supplied by VB; only some basic functions required for startup are supplied from KEY_ON as described below. Reverse protection for pin VB is done by the main relay. Transient negative voltage at VB may be limited by an external diode if necessary. There is no integrated reverse protection at pin VB.

The pin connected to the battery line can bear the ISO 7637/1 noise pulses without any damage. The VB voltage must be externally limited to +40 V and -0.3 V (with external components as in *Figure 4*). It is suggested the use of a transil.

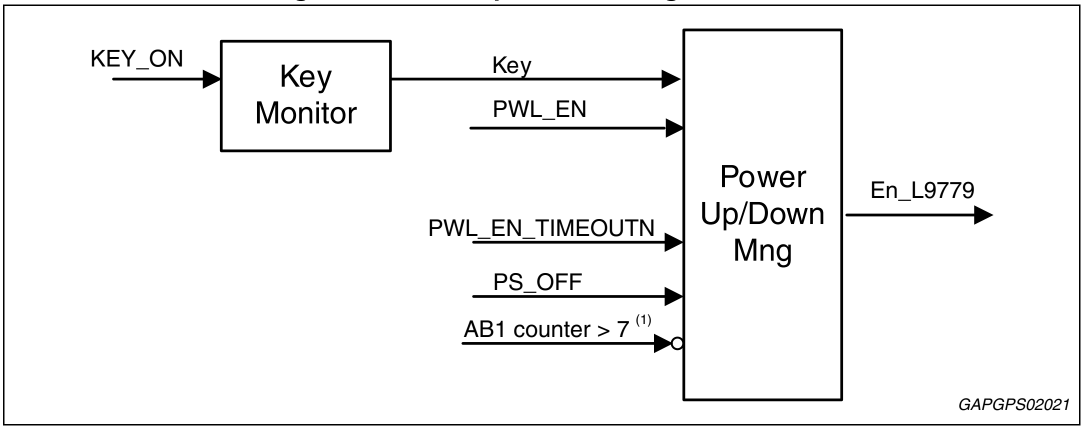
**Figure 4. Configuration supplied by VB**




1. The external components connected to KEY_ON pin are mandatory in order to protect the device from ISO 7637 pulses.

## 6.2 Power-up/down management unit

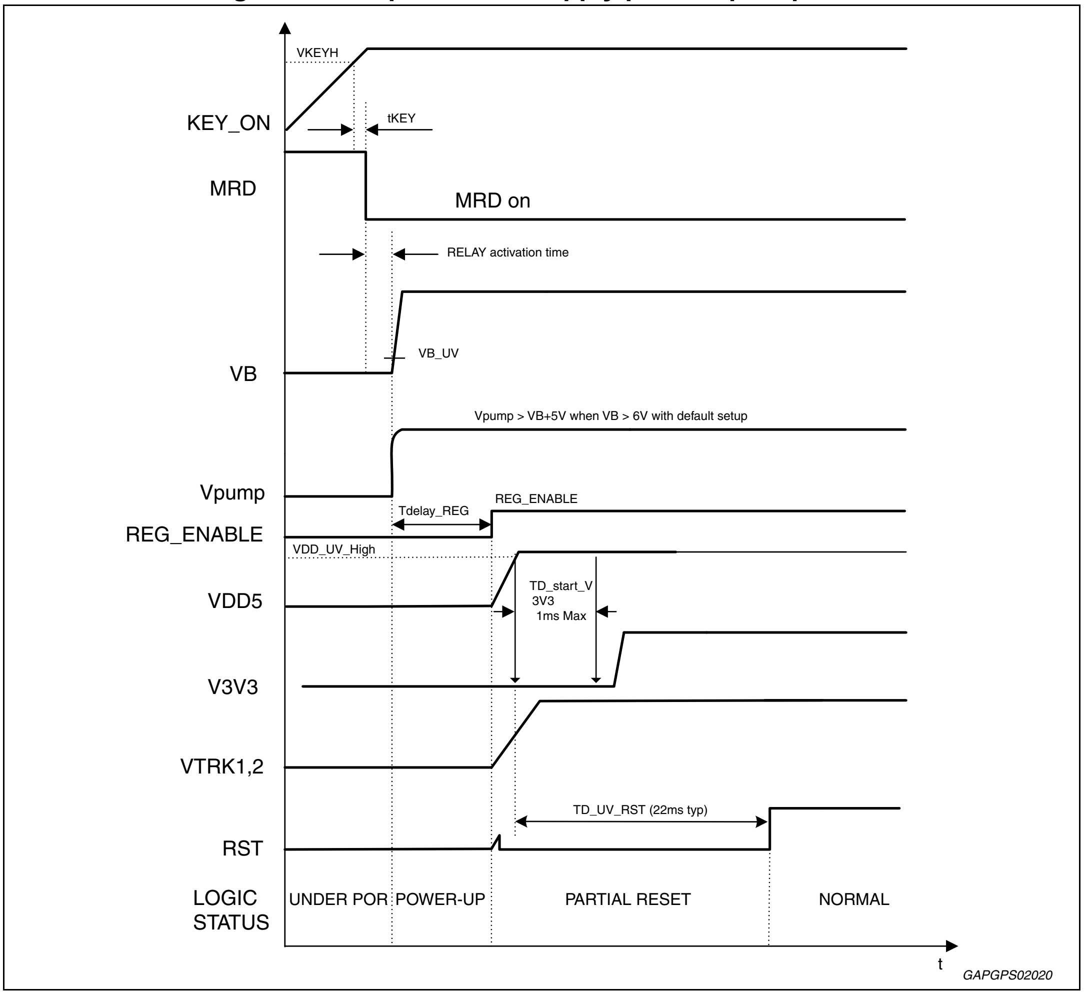
**Figure 5. Power-up/down management unit**




1. AB1 counter function defined at WDA *Section 6.17.1*.

### 6.2.1 Power-up sequence

**Figure 6. Non-permanent supply power-up sequence**



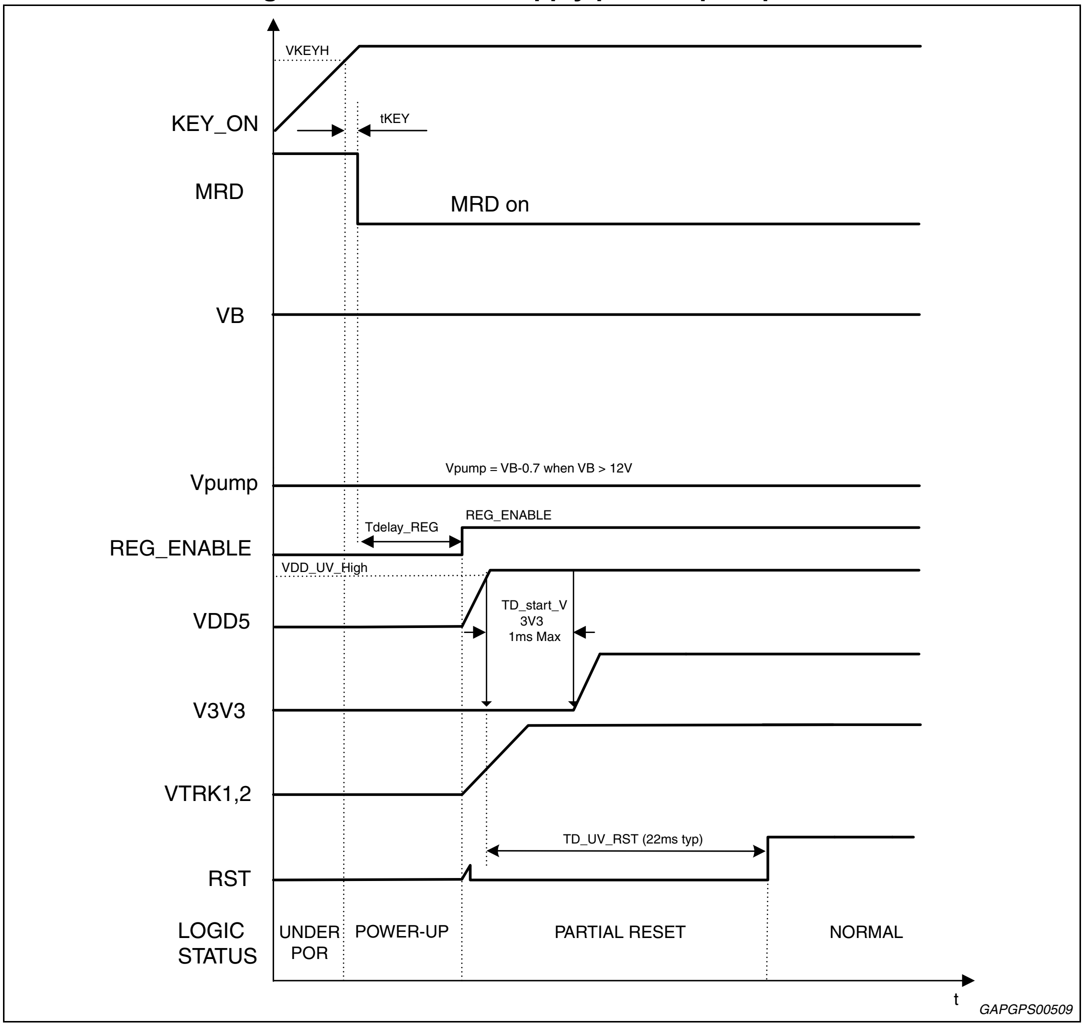
When the KEY_ON reaches a sufficient high voltage VKEYH, after a minimum deglitch filter time T_KEY the system is switched on. First of all the main relay driver is switched on, so the main relay connects VB pin to battery.

Control current into pin KEY_ON is sufficient for basic functions such as filtering time, control the main relay output stage, internal oscillator and internal bias currents.

When the voltage at VB exceeds the under voltage-detection threshold for VB (VB_UV_H) the internal biasing circuits are activated.

VDD5 regulator is activated Tdelay_REG seconds later. After VDD5 exceeds the VDD_UV threshold and with typ. 1.0 ms delay, the V3V3 is activated also. The sensor supplies VTRK1, 2 are turned on together with VDD5.

**Figure 7. Permanent supply power-up sequence**




In case VB is always connected, when the KEY_ON voltage exceeds VKEYH the internal biasing circuits are activated.

VDD5 regulator is activated Tdelay_REG seconds after the tKEY filter time has expired.

VDD5 regulator is activated Tdelay_REG seconds later. After VDD5 exceeds the VDD_UV threshold and with typ. 1.0 ms delay, the V3V3 is activated also. The sensor supplies VTRK1, 2 are turned on together with VDD5.

### 6.2.2 Power-down sequence

The system is switched off according to the status of KEY_ON, VB and power latch mode bit PWL_EN_N set by the µC, according to:

En_L9779 = [(!PWL_EN_N AND PWL_EN_TIMEOUTN) OR KEY_ON] AND VB_UVN.

The KEY_ON is the status of KEY_ON pin after deglitch filter time.

En_L9779 represents the enable signals used by different blocks.

The system will be switched off after a minimum deglitch filter time if the voltage at pin KEY_ON is below VKEYL and if power latch mode is not active i.e. PWL_EN_N =1.

Otherwise, if the power latch mode is active PWL_EN_N=0, nothing happens until the power latch mode has finished by the µC writing PWL_EN_N=1.

However L9779WD will wait for a maximum time-out time PWL_TIMEOUT for PWL_EN_N de-assertion after which the system will be forced to switch off. PWL_TIMEOUT can be enabled and configured by 3 bit PWL_TIMEOUT_CONF.

For TNL description see Smart reset circuit description.

The status of KEY_ON can be read through the bit KEY_ON_STATUS. After tKEY filter time the status of KEY_ON can be read through the bit KEY_ON_FLT also.

All the supply outputs shall be switched-off simultaneously. If the supplied devices have particular sequencing requirements, external diodes or clamping devices will be used.

During power down, whether the regulators are switched off at the same time as the main relay output or not is decided via the <PSOFF> bit.

- <PSOFF>='0' (default): simultaneous switching-off the regulators with the main-relay driver MRD
- <PSOFF>='1': regulators remain active when the main relay driver MRD will be switched off

With this function it is possible to detect a stuck main relay. If conditions to switch off are satisfied when <PSOFF>='1', the MRD is switched off while the voltage regulators continue to operate as long as no under voltage is detected at VB. The RST pin is not asserted till VDD_UV. The µC measures the time passed since shutdown. If a certain time is exceeded, then a stuck main relay is detected and this fault is stored in the µC (not in the L9779WD). After this the µC turns off the voltage regulators by setting the bit <PSOFF> to '0' (reset state). With a stuck main relay the voltage at pin VB remains present at battery level with a current consumption of $I_{Leak}$.

Secure Engine Off function is that the engine can be directly switched off by the key-switch via a hardware path and without the help or interference of software or µC.

Whenever the KEY_ON signal goes low the output stages mentioned in the following pages are disabled.

In no power latch/no SEO mode the key-switch has direct shut-off access to the injector stages (OUT1-4 in L9779) and to the starter relay drivers (OUT13 and OUT14).

An additional feature for the starter delay drivers is that the starters are only shut-off after the time delay THOLD if the SEO condition is still active. To satisfy the Secure Engine Switch off THOLD time, we need to activate the drivers OUT1-4 at least for 225 ms and the OUT 13/14 at least for 600 ms when the Key is ON, the Watch DOG Algorithm [Watchdog influence *Section 6.17.2*] is served and the PWL is enabled after the power on.

The KEY_ON, WDA and “OUT 13/ 14 Switch ON” events for 13 and 14 channels or the KEY_ON, WDA [Watchdog influence *Section 6.17.2*] and "OUT_1-4 Switch ON" events for 1 to 4 channels are “anded” by the internal SEO filter in order to guarantee the THOLD switch off time after the KEY OFF. Example: If the Key is not maintained in ON state for at least 225 ms for driver 1 to 4 and 600 ms for drivers 13/14, the SEO hold time will not be granted and the drivers are switched off immediately at next Key turn OFF. The same behaviour will happen if the WDA [Watchdog influence *Section 6.17.2*] is not served ($EC \geq 4$) for 225 ms and 600ms when Key is in ON state after the POWER ON.

The ignition stages are not affected by the SEO signal. This is different from the WDA signal which additionally switches off the ignition stages.

To avoid misunderstandings one must be aware that the SEO function has nothing to do with the WDA function and is not a part of the WDA module. The SEO function is related to the key switch, not to the WDA function. The SEO function adds an additional safety procedure for switching off.

Other functions than the injector stages and the starter relay drivers are not affected or influenced by the SEO signal.

With the falling edge of KEY_ON a timer is started which disables the mentioned power stages after 200 ms to 250 ms (typ. 225 ms). The timer is clocked by an internal oscillator. The timer does not depend on any µC clock or function. The µC still has control on switching on/off drivers during SEO time. This function is configured by CONFIG_REG6 register. After a SEO event, KEY should be stay ON for at least 600ms so to allow a further SEO event delay.