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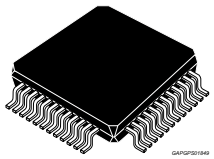
L9780

Wide range air fuel sensor control interface

Datasheet - production data



LQFP48

Features

- Voltage controlled current source (VCCS) pump cell driver with selectable voltage clamp, offset compensation, diagnostic (short to battery) and 2 output channels
- Impedance measurement of reference cell
- 10-bit multiplexed A/D converter
- Scaling amplifier with sample & hold and offset compensation
- Control voltage amplifier with sample & hold and offset compensation
- Synchronous or asynchronous functionality selectable via SPI
- Heater FET driver with diagnostic (short to battery, short to ground, open circuit)
- 4 possible levels for clean current
- SPI with fault detection
- Digital input and outputs compatible with 5 V or 3.3 V voltage supply
- 2 channels available to connect compensation networks
- Short to battery diagnostic on functional ground (pin SR)
- Short to battery/ground diagnostic on voltage from reference cell (pin INRC)
- -5 V internal supply
- 4 MHz internal oscillator
- Package: 48 pin LQFP
- Technology: BCD5s_70 V

Description

L9780 is an IC designed to interface a variety of wide range air fuel sensors.

The device manages the oxygen pump of the wide range air fuel sensor by means of a voltage controlled current source (VCCS). The reference for the VCCS is generated by a PI controller with external compensation network in order to adapt the device to different sensors. The user can choose between two different networks using the SPI interface. L9780 is fully compatible with most sensors on the market.

The internal timing state machine automatically manages all the operations needed for a right sequencing of the measurement process. All the main time values can be configured by SPI.

L9780 drives also an external FET used to control the sensor heater. The device protects the sensor and all the I/O against shorts and provides the diagnosis by SPI.

Table 1. Device summary

Order code	Package	Packing
L9780	LQFP48	Tray
L9780TR	LQFP48	Tape and reel

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1 Pin description

Figure 1. Pin connection diagram (top view)

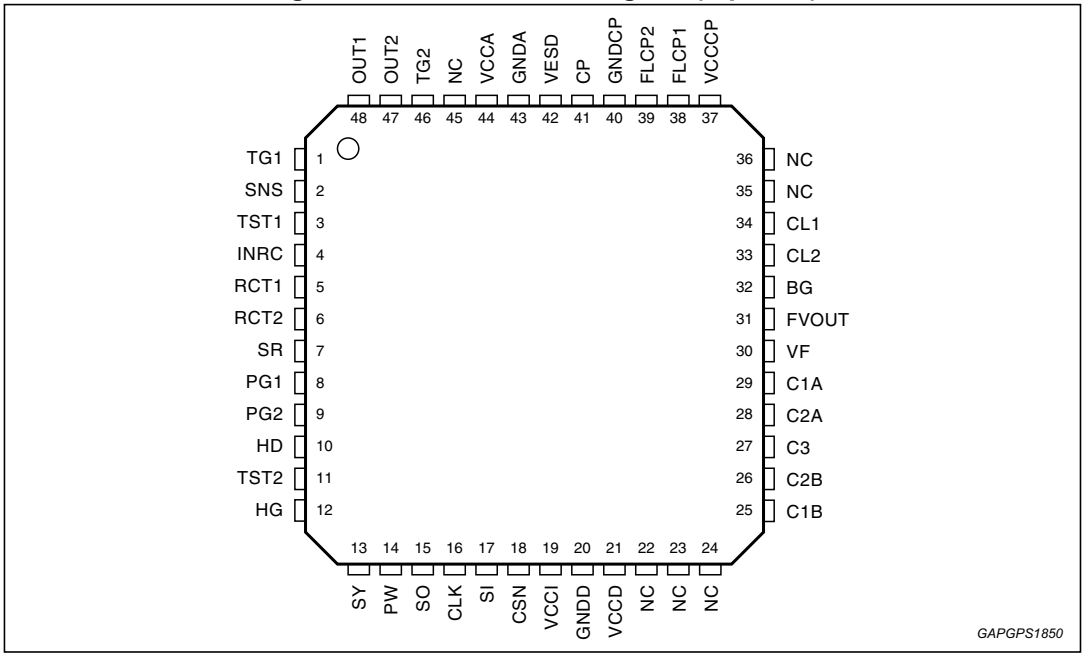


Table 2. Pin function

Pin number	Pin name	Pin description
1	TG1	Switching TAG resistor pin channel 1
2	SNS	VCCS sense pin
3	TST1	Test mode pin 1
4	INRC	Reference cell input
5	RCT1	Impedance test pin 1
6	RCT2	Impedance test amplifier input
7	SR	Sensor return
8	PG1	Protection fet gate channel 1
9	PG2	Protection fet gate channel 2
10	HD	Heater fet drain
11	TST2	Test mode pin 2
12	HG	Heater fet gate
13	SY	Synchronous mode pin
14	PW	Heater PWM input pin
15	SO	Serial data output
16	CLK	SPI clock
17	SI	Serial data input

Table 2. Pin function (continued)

Pin number	Pin name	Pin description
18	CSN	SPI chip select
19	VCCI	Digital transfer level supply
20	GNDD	Digital ground
21	VCCD	Digital supply
22	n.c.	Not connected pin
23	n.c.	Not connected pin
24	n.c.	Not connected pin
25	C1B	Compensation network pin1, side B
26	C2B	Compensation network pin2, side B
27	C3	Compensation network common pin
28	C2A	Compensation network pin2, side A
29	C1A	Compensation network pin1, side A
30	FV	VCCS filtered control voltage pin
31	FVOUT	Analog output
32	BG	Bandgap voltage
33	CL2	VCCS voltage clamp channel 2
34	CL1	VCCS voltage clamp channel 1
35	n.c.	Not connected pin
36	n.c.	Not connected pin
37	VCCCP	Charge pump supply
38	FLCP1	Charge pump floating pin 1
39	FLCP2	Charge pump floating pin 2
40	GNDCP	Charge pump analog ground
41	CP	-5V charge pump output
42	VESD	ESD reference voltage
43	GNDA	Analog ground
44	VCCA	Analog supply
45	n.c.	Not connected pin
46	TG2	Switching TAG resistor pin channel 2
47	OUT2	Pump cell output pin channel 2
48	OUT1	Pump cell output pin channel 1

2 Operating conditions

2.1 Maximum ratings

L9780 may not operate out of the maximum rating ranges. Once the correct situation is restored after one of the following conditions is not respected (but not exceeding the absolute maximum rating range) the part is still able to work with no damage.

Table 3. Maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage: VCCA, VCCD, VCCCP VCCI	 4.9 to 5.1 3.14 to 5.1	V
V_{ESD}	ESD reference	40	V
V_{in}	Input voltage HD, RCT1, RCT2, INRC SR, SNS CSN, SI, CLK, PW, SY	 0 to 40 -VCCA to VCCA 0 to VCCA	V
I_{in}	Input current VESD SR, RCT1, RCT2, SNS INRC HD OUT1, OUT2, TG1, TG2 (leakage for maximum short to battery voltage) SR, RCT1, RCT2, SNS, INRC, HD, OUT1, OUT2, TG1, TG2 (when the voltage is driven below the normal operating range) CSN, SI, CLK, PW, SY	 -20 10 50 150 350 -275 ±275	 mA µA µA µA µA µA µA
T_j	Junction temperature	-40 to 150	°C

2.2 Absolute maximum ratings

The part can be irreparably damaged if the voltages out of the absolute maximum ratings ranges are applied to the pins. The part at these ratings could not work properly.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage: VCCA, VCCD, VCCCP, VCCI	 -0.3 to +6.5	V
V_{ESD}	ESD reference	+53	V

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{in}	Input voltage:		V
	HD	-0.3 to 53(1)	
	RCT1, RCT2, INRC	-0.3 to +40(1)	
	SR, SNS, TGx, OUTx	-VCCA to +40(1)	
	CSN, SI, CLK, PW, SY, SO	-0.3 to VCCI+0.3	
	C1B, C2B, C3, C2A, C1A, BG, CL2, CL1, FV, FVOUT, PG1, PG2, HG	-0.3 to VCCA+0.3	
	CP	-6.5 to +0.3	
	FLCP1	-0.3 to VCCCP+0.3	
	FLCP2	CP-0.3 to +0.3	
	TST1, TST2	-0.3 to 40(1)	
	|TGx – OUTx|	+16	
I_{in}	Input current:		
	VESD	-20	mA
	SR, RCT1, RCT2, SNS	10	µA
	INRC	50	µA
	HD	150	µA
	OUT1, OUT2, TG1, TG2 (leakage for maximum short to battery voltage)	500	µA
	SR, RCT1, RCT2, SNS, INRC, HD, OUT1, OUT2, TG1, TG2 (when the voltage is driven below the normal operating range)	-500	µA
	CSN, SI, CLK, PW, SY	±500	µA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C

1. Voltage at the pin cannot exceed V_{ESD}+0.3 V.

2.3 Operating temperature range

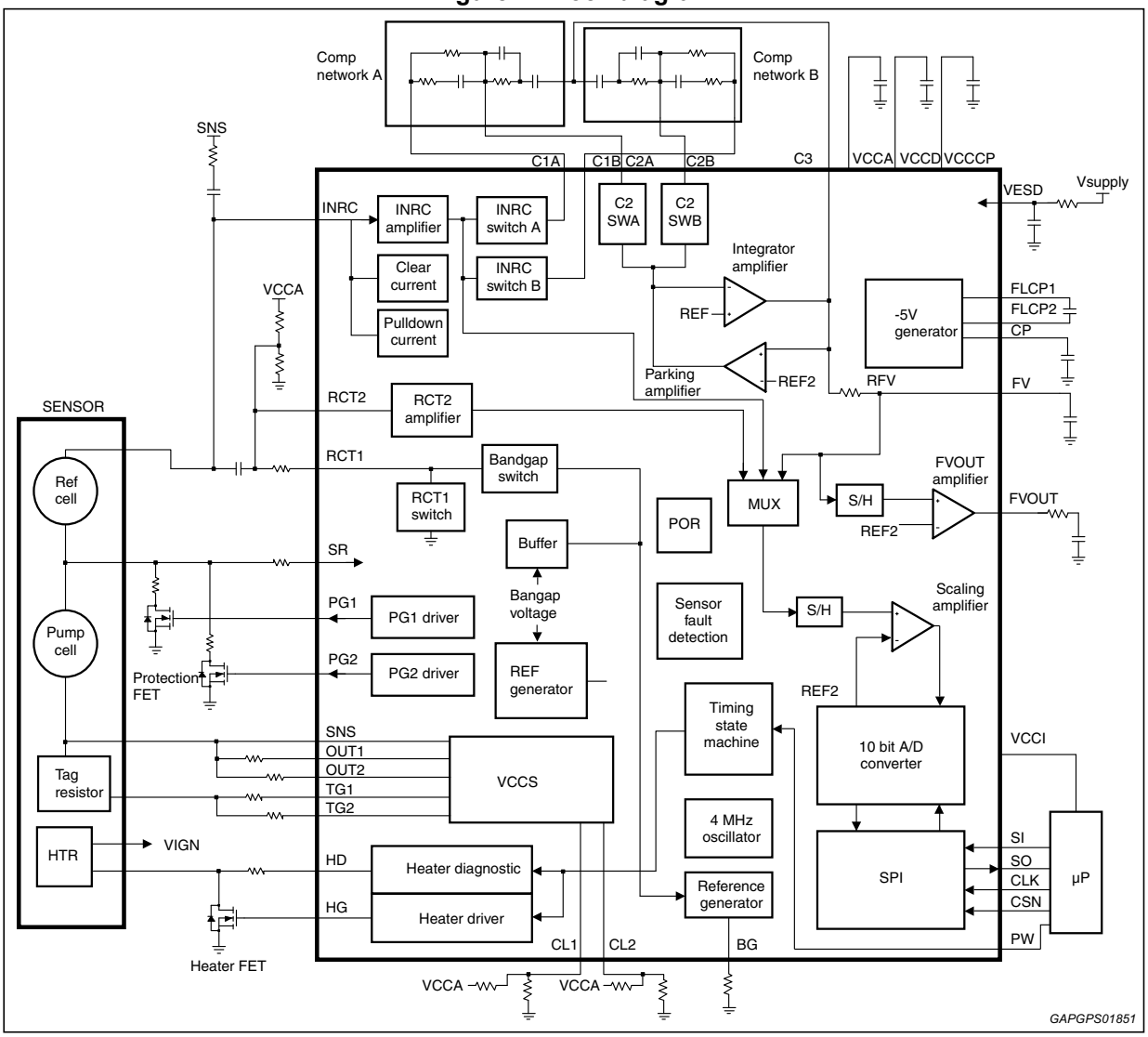
Table 5. Operating temperature range

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range	-40 to 125	°C

3 Block diagram

The following is L9780 block diagram; the description of each block and the definition of external components can be found in the next sections.

Figure 2. Block diagram



4 Main functionalities

4.1 Power supplies

4 different power supplies are present in the device: VCCA, VCCD, VCCCP, VCCI, respectively for analog part, digital part, charge pump, digital interfaces. Digital inputs are compatible with 2 different logic levels (5 V or 3.3 V, the possible levels for VCCI), and are converted to the range 0V-VCCD using internal level shifters connected to VCCD and VCCI. In the device a negative charge pump is also present and it is used to generate -5 V voltage level (on CP pin), to bias the substrate and to allow the excursion to the negative range to the output pins of VCCS. Charge pump clock frequency is 2 MHz.

3 different ground pins are also present in the device: GNDA, GNDD, GNDCP, respectively for analog, digital and charge pump circuitry.

Possible ranges for power supplies, currents consumption and input/output logic levels are specified in *Table 9*, *Table 12* and *Table 13*. External component values are specified in *Table 19*.

4.2 Pin protection

On the device a high ESD reference voltage pin (VESD) is available and is used as a protection for the pins externally connected to the sensor and for HD pin; this voltage must be the highest in the application and has to be always connected to the device, through the RC low pass filter shown in *Figure 12* (external component values are specified in *Table 19*). For pins compatible to negative voltages, the negative ESD reference voltage is the substrate (internally connected to CP pin, -5 V). All the other pins have a 5V positive ESD protection voltage level and GND as negative ESD protection voltage level.

4.3 Internal references

Into the device the following voltage references are present:

- a band-gap voltage (typical value 1.215 V) with 3 trimming bits dedicated;
- REF voltage; obtained as the band-gap multiplied by a factor of 1.555; typical value for this voltage is 1.89 V (possible range for this parameter is specified in *Table 10*.
- REF2 voltage; typical value is about VCCA/2 (possible range for this parameter is specified in *Table 11*).

All internal currents are generated from a reference current obtained by the band-gap (buffered on BG pin) applied on an external resistance; the possible BG pin voltage range is specified in *Table 9*, the value of external resistance is defined in *Table 19*.

All timing references are calculated as multiples of the period of the internal oscillator (TOSC); the typical oscillation frequency is 4 MHz, the possible range is specified in *Table 15*. Internal oscillator has 4 trimming bits dedicated.

4.4 Power on reset

A power on reset (POR) circuit is present into the device; this circuit monitors VCCA, VCCCP, VCCD, GNDA, GNDCP, GNDD voltage levels. If one of the supplies falls below (or one of the grounds exceeds) the defined POR threshold (defined in *Table 10*) all the outputs are driven in inactive state, all the registers are set at their default state and the time state machine and all the timers are fixed in the reset state. All these actions are applied after a typical filter time of 15 µs (possible range is defined in *Table 15*). When the supply that has caused POR condition reaches POR value plus hysteresis (or the ground decreases under POR threshold) all the outputs are re-enabled.

During reset condition an internal switch connects the charge pump output voltage (CP pin) to GNDA.

4.5 Pin INRC functionalities: INRC amplifier, clean currents, pull-down current

Pin INRC in the application is connected to the sensor reference cell; the voltage generated by this cell and applied on L9780 INRC pin is a function of the λ parameter of the sensor and gives information about how much the λ parameter is far from the target value. The final purpose is to obtain λ =1, that in terms of electrical parameters means to have 450 mV as output of the reference cell (and applied on INRC pin). In the device this pin is the input of an amplifier (INRC amplifier) with gain selectable via SPI (using bit INRCGAIN). The output of this amplifier is one of the multiplexed inputs of the A/D converter (in order to give the µP the estimation of the λ parameter of the sensor via SPI) and is also internally connected by a switch (INRC switch) to C1A or C1B pin and the external compensation network. The selection of channel A or B is possible using bit COMPSEL. Electrical parameters of INRC amplifier and INRC switches are specified in *Table 10*.

On INRC pin is present a diagnostic circuitry able to detect short to battery/ground conditions and communicate it via SPI (bits STBS2 and STGRC of SPI output register); short to battery detection is always enabled, while the short to ground detection is disabled by default; it can be enabled using bit STGINRC. INRC short to battery/ground thresholds typical values are 3.2 V and 200 mV (possible ranges are defined in *Table 13*). The consequences of the detection of each one of these faults are described in *Section 5.1* and *5.2*.

The INRC pin is connected to the clean current generator: it is a pull-up current source used to clean the air reference of the sensor; the generated current value is selectable via SPI (using bits CCS[3..0]). Possible clean current values are specified in *Table 10*.

On the same pin a 500 µA pull-down current source is also available, used in order to prevent the presence of false short to battery detection due to capacitive commutations. The activation of this current is selectable via SPI (bit INRCPD); pull-down current range is specified in *Table 10*.

A detailed bit description is present in *Section 6.3* and *6.4*.

4.6 Pin RCT1 – RCT2 functionalities: RCT2 amplifier, RCT1 switch, RCT1 band-gap switch

RCT2 pin is the input of an amplifier with typical gain 4.2 (electrical characteristics of RCT2 amplifier are specified in *Table 10*). The output of this amplifier is evaluated during the impedance test and converted in order to communicate its value via SPI to the µP: the value of RCT2 amplifier output, measured in 2 different conditions (with RCT1 switch open and closed), can in fact give a feedback about the impedance of the reference cell, and consequently about the temperature of the sensor.

RCT1 pin is connected through a switch (RCT1 switch) to ground and through another switch (RCT1 band-gap switch) to the band-gap voltage; both these functions are used during the reference cell impedance test, in particular the second one is used to restore the correct charge of the reference cell after the impedance test (charge balance mechanism). RCT1 switches resistance range and RCT1 voltage during charge balance are specified in *Table 10*. For the time diagram of the sequence and the related description see *Section 4.12*. Values of external components connected to pins RCT1 and RCT2 are specified in *Table 19*.

4.7 Pin C1A, C2A, C1B, C2B, C3 functionalities: compensation network connection

These pins are used to connect externally the compensation network to the device; via SPI (using COMPSEL bit) it is possible to select the desired channel (A or B) and connect the external network to the pins C1(A or B), C2(A or B) and C3. The pins of the non selected channel are in high impedance state. C1 is internally connected to the output of INRC amplifier through the INRC switch (driven by the logic during the impedance test, for details see *Section 4.12*), while C2 and C3 are internally connected to the inverting input and the output of an integrator amplifier (C3 is also the VCCS control voltage pin). The non inverting input of the amplifier is connected to REF voltage (typ 1.89 V). The integrator amplifier and the VCCS create a loop (with the external compensation network) of a PI controller. When the loop reaches a stable condition ($\lambda = 1$), on INRC pin there are 450 mV (if 4.2 gain for INRC amplifier is selected), while the inputs of integrator amplifier are both to 1.89 V (450 mV * 4.2). In this condition there is no output current from the VCCS cell (2.5 V on C3 pin).

The values of the external components that must be used in compensation network depend on the sensor that will be driven by the device.

Two examples of possible compensation networks (with defined external components values) are shown below.

Figure 3. Typical sensor D compensation network

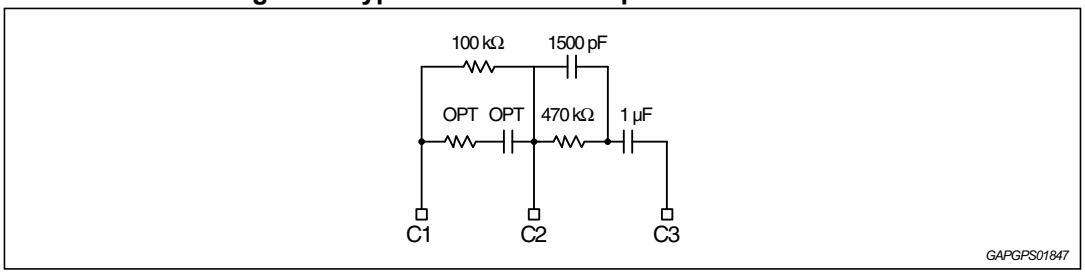


Figure 4. Typical sensor N compensation network

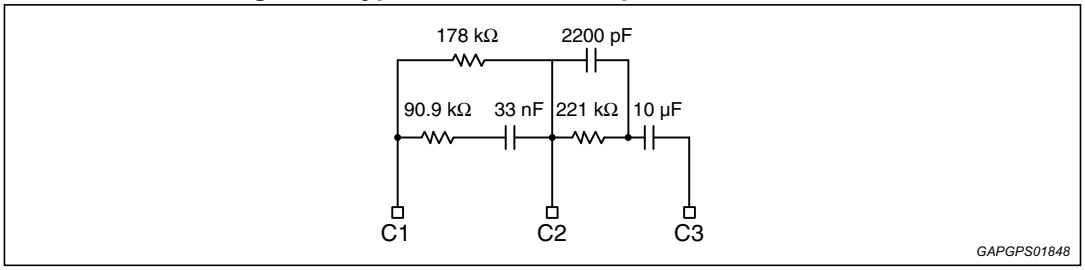
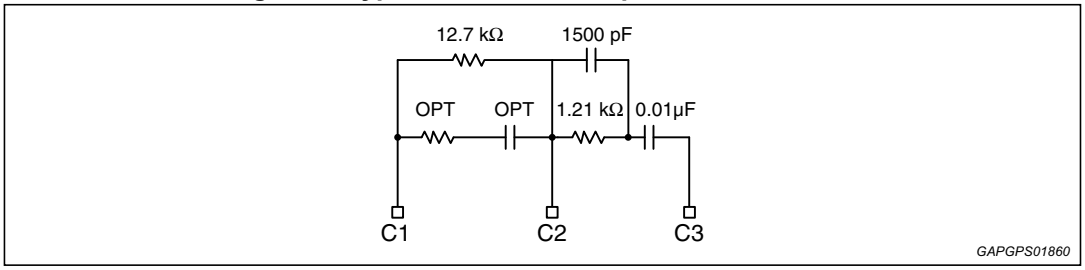


Figure 5. Typical sensor B compensation network



Typical ranges for integrator amplifier electrical parameters are specified in *Table 15*.

4.8 Pin FV, FVOUT functionalities: FVOUT amplifier

C3 pin voltage is the VCCS direct input control voltage. Thanks to the presence of the external capacitor on FV pin (CFV, specified in *Table 19*) and the internal resistance RFV (typical value 5 kΩ and possible range specified in *Table 11*), on FV pin the low pass filtered C3 voltage can be measured. FV voltage is the input of the FVOUT amplifier used to provide on FVOUT pin a signal range compatible with an external A/D converter, as follows:

$$FVOUT = REF2 + G * (FV – REF2)$$

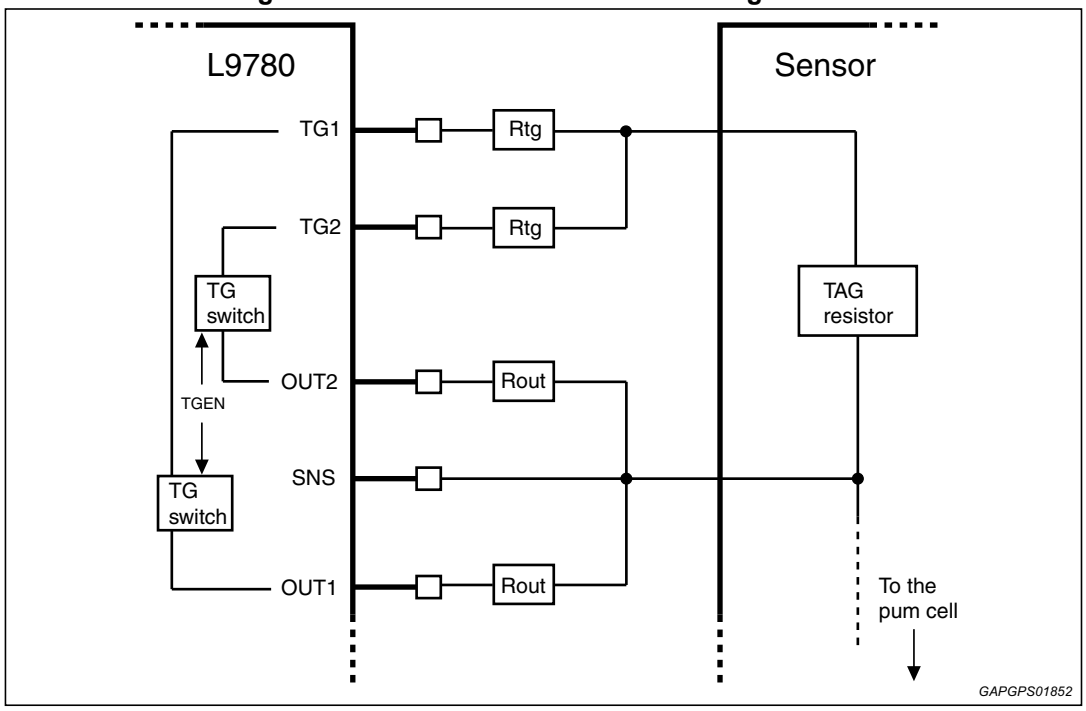
Where G is the gain of VOUT amplifier selectable via SPI (using bits SAMP[2..0]) among the following values: 1 - 1.5 - 2 - 3 - 4 - 6 - 8 – 12. A sample and hold circuitry and the offset compensation technique are used in the architecture of FVOUT amplifier; for this cell all the electrical parameters are specified in *Table 10* and *Table 15*.

4.9 Pin TG1, TG2, OUT1, OUT2, SNS functionalities: the VCCS

TG1, TG2, OUT1, OUT2, SNS are the interface pins between VCCS structure and the external pump cell. The pump cell allows to control the oxygen concentration by forcing an electric current through the cell itself; in other words it is possible to control the direction and the intensity of oxygen transport, because it is directly related to the direction and the intensity of the current. By controlling the amount of current through the pump cell, it is possible to control the amount of oxygen and consequently the λ parameter of the sensor; closing this mechanism into a loop, like in L9780, it is possible to regulate the pump cell current in order to obtain the target λ = 1. The best working condition for the sensor is the high temperature; in this condition the AC impedance of the pump cell can be assumed to be a large capacitance in series to with a resistor of about 20-30 Ω. When cold, the pump cell can be assumed to be an open circuit.

VCCS is a voltage controlled current source and is able to sink or source current from the pump cell, depending on its control voltage, that is the voltage present on C3 pin. Through TG and OUT pins there is the VCCS output current flow, while SNS is a sense pin. VCCS present in L9780 has 2 output channels (1 and 2), selectable via SPI (using bit VCCSOUT); TG and OUT pins of the non selected channel are in high impedance condition. In VCCS architecture there are 2 internal switches (TG switches) able to short OUT and TG pins of the selected channel (see *Figure 6*); the actuation of these switches can be selected via SPI (using bit TGEN).

Figure 6. VCCS external resistance configuration



If the switch is in off condition the TG pin of the selected channel is in high impedance state. If the TG switch is in on state the output current of VCCS structure can flow both through TG and OUT pins and can be described with the following expression:

$$I_{out} = - (C3 – REF2)/R_{tot}$$

where R_{tot} is the external total resistance, that can be obtained as a combination of all the external resistances connected to the VCCS pins. Referring to *Figure 6*, R_{tot} can be calculated as follows:

$$R_{tot} = R_{out} // (R_{tg} + \text{TAG resistor})$$

where R_{tg} and R_{out} are the series resistances of the VCCS pins related to the selected channel.

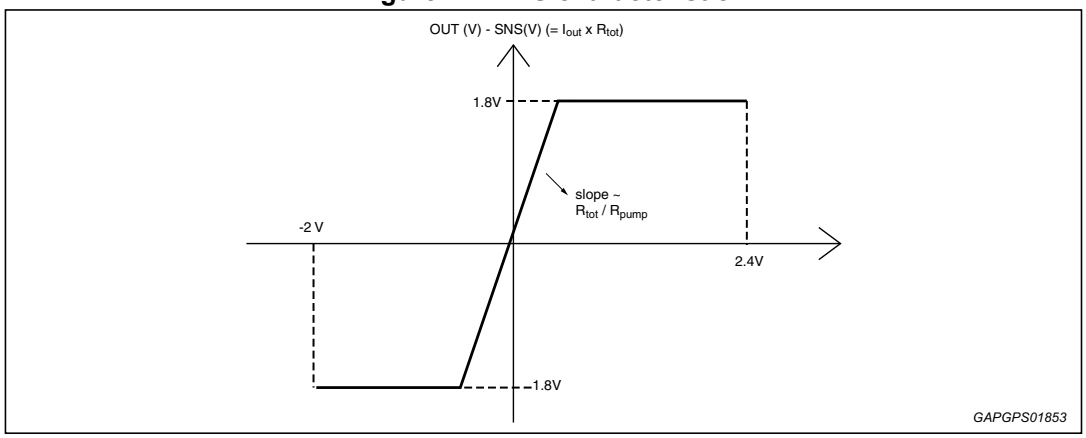
Otherwise, if TG switch is in off state, $R_{tot} = R_{out}$ and consequently the VCCS output current can be described with the following expression:

$$I_{out} = - (C3 – REF2)/R_{out}$$

The VCCS characteristic is shown in *Figure 7*. In this figure the relationship between SNS voltage and the voltage on R_{tot} resistance (that is equal to the difference between OUT voltage and SNS voltage) is defined; these two quantities are in agreement in sign as both

depend on the VCCS output current multiplied by a resistance value (the resistance of the pump cell in SNS voltage case and the R_{tot} resistance in the voltage drop case); from the same figure it is evident that the maximum SNS voltage dynamic range compatible with L9780 VCCS architecture is -2 V < SNS < 2.4 V and the maximum drop allowed on R_{tot} (or Rout if TG switch is off) is 1.8 V.

Figure 7. VCCS characteristic



At the startup of the device, VCCS structure is disabled by default, that means that all its pins are in high impedance condition and the “parking functionality” is active; in other words, the parking amplifier is switched on and a voltage similar to REF2 is present on C3 pin (see block diagram in *Figure 2*). Besides, a pull-down resistor is internally connected by default from OUT1 pin to GNDA; this is done to avoid that a leakage current can increase the voltage value of VCCS pins until the short to battery condition. When VCCS is enabled or a sensor short to battery condition is detected, the pull-down resistor is automatically disconnected from OUT1 pin; when VCCS is disabled and no fault conditions are present, VCCS pull-down resistor can be re enabled via SPI (using bit VCCSPD).

If no sensor short to battery condition is present, VCCS structure can be enabled and the output channel selected with an SPI frame (using bits VCCSEN and VCCSOUT); in this case the “parking functionality” is disabled. When VCCS is enabled, it is also possible to activate/deactivate clamp functionality via SPI (using bit CLAMPEN), in order to protect the sensor; when the clamp functionality is activated, a voltage control is enabled on SNS pin and, if its value is going to exceed the voltage range defined by the user, the clamp circuit intervenes in order to modify the VCCS output current and make SNS pin reenter the clamp limits. The clamp limit range can be symmetric or asymmetric; the desired kind of range can be defined via SPI (bit CLAMPSIM). In case of symmetric range, if VCL is the clamp voltage defined by the user, the consequent range allowed for SNS voltage is:

$$-VCL < SNS < +VCL, \text{ with } 0.75V<VCL<2V$$

In case of asymmetric range, if VCL is the clamp voltage defined by the user, the consequent range for SNS voltage is:

$$-0.8333*VCL < SNS < +VCL, \text{ with } 0.75\ V < VCL < 2.4\ V$$

If the clamp circuit is activated and intervenes while VCCS is working, it is visible also via SPI because CLAMP bit in SO register is kept = 1 until the clamp circuit is acting during VCCS activation. The clamp voltage VCL is defined by the user and is equal to the voltage applied on CL1 or CL2 pin; the input channel chosen to read the clamp voltage can be selected via SPI (bit CLAMPCL); the non selected pin can be left open.

On all VCCS pins a short to battery diagnostic is always active: a short to battery condition is detected if OUT or TG pins exceed VCCA voltage + 30 mV or if SNS pin exceed STBS3 threshold voltage (2.7 V typical value, possible range defined in). The consequences of a short to battery fault detection are specified in *Section 5.1*.

On SNS pin is also present a short to ground diagnostic circuitry, that is able to detect if SNS pin is into the range SNS_NTH < SNS < SNS_PTH (SNS_NTH and SNS_PTH are voltage thresholds specified in *Table 13*, their typical values are -200 mV and 200 mV). The consequences of a sensor short to ground detection are specified in *Section 5.3*.

VCCS is designed to respect specification of minimum bandwidth (100 kHz) for different R_{tot} values and is able to guarantee in all conditions a minimum phase margin of 60°. This is possible thanks to the programmability of the VCCS internal compensation capacitances (C_{int}). In SPI input frame, 6bit for capacitance configuration are present (VCCSCAP[5..0]); these bits allow to drive the connection of internal compensation capacitances, that in this way are selectable by the user. The higher is the value of capacitance selected and the higher is the phase margin of the structure, but the lower is the consequent bandwidth; with some simplifications the bandwidth of VCCS can be described with the following formula:

$$Ft = (Gm\_in * Gm\_outDC * R_{tot})/ (2\pi * C_{int})$$

where Gm_in * Gm_outDC is a constant parameter depending by on the structure used in the design; R_{tot} is the external total resistance and C_{int} the internal selectable capacitance.

In the following table it is shown that a wide range of possible R_{tot} can be driven obtaining the correct compromise between bandwidth and phase margin.

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
1	6	4
2	13	9
3	19	13
4	26	17
5	33	22
6	40	27
7	46	31
8	53	35
9	60	40
10	66	44
11	72	48
12	79	53
13	85	57
14	91	61
15	98	65
16	104	69
17	111	74

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth (continued)

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
18	117	78
19	123	82
20	129	86
21	135	90
22	141	94
23	148	99
24	154	103
25	160	107
26	166	111
27	172	115
28	178	119
29	184	123
30	190	127
31	196	131
32	202	135
33	208	139
34	214	143
35	220	147
36	226	151
37	231	154
38	237	158
39	243	162
40	249	166
41	255	170
42	261	174
43	267	178
44	272	181
45	278	185
46	284	189
47	290	193
48	295	197
49	301	201
50	306	204
51	312	208

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth (continued)

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
52	318	212
53	324	216
54	329	219
55	335	223
56	341	227
57	347	231
58	352	235
59	357	238
60	363	242
61	369	246
62	374	249
63	380	253
64	386	257

In the table above the list of selectable C_{int} is shown and for each C_{int} is specified maximum and minimum R_{tot} value that guarantee respectively a phase margin > 60° and a bandwidth > 100 kHz.

In order to avoid that during the activation of VCCS for a short time the output current can be out of control, the selection or the change of different functionalities of VCCS (like the change of output channel, of input clamp or of C_{int} capacitances) are possible only when VCCS is disabled. Well defined rules have to be respected in order to be able to drive correctly VCCS; these rules are specified in *Section 5.5.2*.

All VCCS electrical parameters ranges are specified in sections *Table 12* and *Table 15*. All the logic signals used to select VCCS functionalities are defined in detail in section 7.3.

4.10 Pin PG1, PG2, SR functionalities

The device is able to drive via SPI (through bits PG1EN, PG2EN) the gate of the external protection FET, that can be connected to PG1 or PG2 pin. This external FET acts as a switch that connects to ground the second terminal of the pump cell and completes the path for VCCS output current (see block diagram in *Figure 2*). In this condition SR pin voltage is expected to be low; if the voltage value exceeds STBS1 threshold (typical value of 200mV and possible range specified in *Table 13*), a sensor short to battery condition is detected. For the consequences of this detection see *Section 5.1*.

In order to avoid the possibility that the external FET switch on when the device is un-powered the FET driver has 100 kΩ (typ) pull down resistor permanently connected to PG1 and PG2 pins. Electrical parameters of PG driver are specified in *Table 12* and *Table 15*.

4.11 Analog to digital conversion

In the device a 10bit A/D converter is present. The analog voltages to be converted are multiplexed by the logic while the state machine is running and are: the output of RCT2 amplifier, the output of INRC amplifier and FV pin voltage (see block diagram in *Figure 2*). Between the analog inputs and the A/D converter a scaling amplifier is present; this cell is able to amplify the input signal according to the gain selected via SPI (using bit SAMP[2..0]) with the following relation:

$$OUTsa = REF2 + G * (Input\_voltage – REF2)$$

where G is the gain selectable via SPI among the following values: 1 - 1.5 - 2 - 3 - 4 - 6 - 8 – 12, and OUTsa is the output of the scaling amplifier (and the input of A/D converter). When the selected input of the scaling amplifier is the output of the INRC or RCT2 amplifier, G is fixed (=1), while when the input is FV voltage the gain G can be modified by the user. The multiplexing sequence at the input of the scaling amplifier when the state machine is running is shown in *Figure 8*.

The absolute conversion accuracy compared to an ideal transfer curve is ±2 counts. All the electrical parameters regarding the scaling amplifier and the A/D conversion are specified in *Table 11*.

The nominal conversion of the scaling amplifier output is defined in the following formula:

$$count\_SA = floor\left(\frac{OUTsa}{VCCA} \cdot 1024\right)$$

where:

count_SA is the result of the A/D conversion;

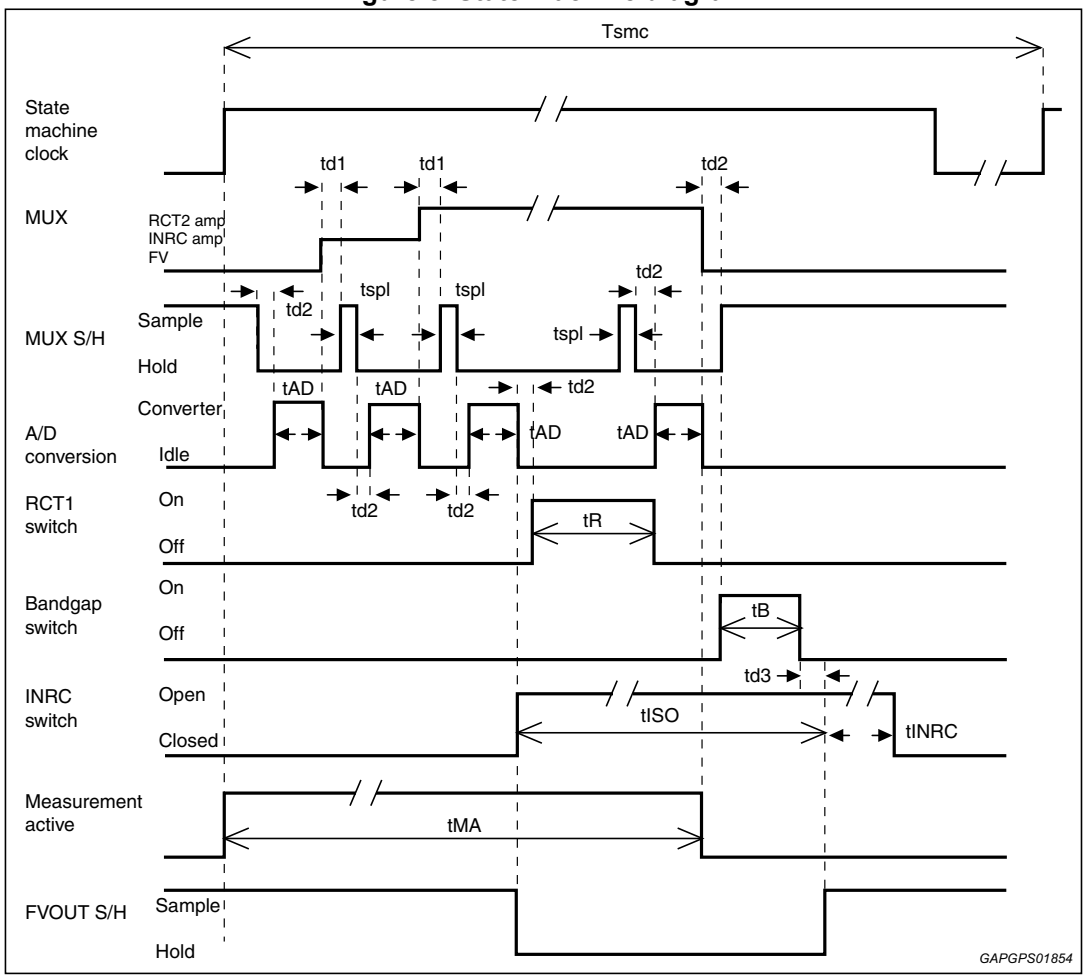
OUTsa is the output voltage of the scaling amplifier;

floor: a function that returns the greatest integer less than or equal to the argument.

4.12 Timing state machine

The internal temporization of A/D conversion and of the impedance test are defined by an internal state machine that acts as shown in *Figure 8*.

Figure 8. State machine diagram



The A/D conversion results give an indication about the λ parameter of the sensor (that is in relation with INRC pin voltage), about the VCCS output current (from FV voltage evaluation) and about the sensor temperature (from the double conversion of the output of RCT2 amplifier the external µP is able to evaluate the impedance of the reference cell and consequently the temperature).

All times are defined in *Table 16*; some of them (the state machine clock period (T_{smc}), the duration of RCT1 switch and band-gap switch pulses (t_R and t_B) and the second portion of INRC switch pulse (t_{INRC})) can be defined by SPI (using bits MCP[1..0], ITPT[6..0], CBT[6..0], ISPT[2..0]), while the first portion of INRC switch pulse is determined by the summation of different events. The SPI selectable variables can not change during the measurement; if any change occurs while a measurement is on going, the new values will be applied in the next measurement cycle.

In SO output frame, 3 bits are dedicated to the measurement cycle counter (COUNT[2..0]); the value measured by the counter is cleared after every power on reset, is automatically incremented by one at every falling edge of measurement clock and latched in SO output

register. When the counter reaches its maximum value, the count restarts from zero. The measurement is able to operate in free running or synchronized mode, according to SPI selection (bit SNC); if free running mode is selected, the timing state machine is continuously running, otherwise if synchronized mode is selected the measurement cycle starts for each rising edge on SY pin; if multiple rising edges are detected on SY pin during one measurement cycle, they will be ignored. For a more detailed description of the bits involved see *Section 6.3*.

When the INRC amplifier is selected by the MUX, the scaling amplifier gain is automatically set to 1, and the nominal transfer function from INRC pin to A/D output is:

$$count\_INRC = floor\left(Ginrc \cdot \frac{INRC}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$INRC = \frac{count\_INRC}{1024} \cdot \frac{1}{Ginrc} \cdot VCCA$$

where:

Ginrc is the gain of the INRC amplifier;

count_INRC is the result of the A/D conversion of INRC pin voltage;

INRC is the INRC pin voltage level.

INRC voltage resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±0.5%);

scaling amplifier offset (±300 µV);

INRC amplifier gain accuracy (±1%);

INRC amplifier output offset (±21 mV);

VCCA voltage precision.

When the RCT2 amplifier is selected by the MUX, the scaling amplifier gain is automatically set to 1, and the nominal transfer function from RCT2 pin to A/D output is:

$$count\_RCT2 = floor\left(Grtc2 \cdot \frac{RCT2}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$RCT2 = \frac{count\_RCT2}{1024} \cdot \frac{1}{Grtc2} \cdot VCCA$$

where:

Grct2 is the gain of the RCT2 amplifier;

count_RCT2 is the result of the A/D conversion of RCT2 pin voltage;

RCT2 is the RCT2 pin voltage level.

RCT2 voltage resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±.5%);

scaling amplifier offset (±300 µV);

RCT2 amplifier gain accuracy (±1%);

RCT2 amplifier output offset (±21 mV);

VCCA voltage precision.

When the VCCS filtered control voltage FV is selected by the MUX, the nominal transfer function from VCCS current (I_VCCS) to A/D output is:

$$count\_VCCS = floor\left(512 + \frac{Gsa \cdot (-I\_VCCS) \cdot Rtot}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$I\_VCCS = -\left(\frac{count\_VCCS}{1024} - \frac{1}{2}\right) \cdot \frac{1}{Gsa \cdot Rtot} \cdot VCCA$$

where:

Gsa is the scaling amplifier gain;

I_VCCS is the VCCS output current;

count_VCCS is the result of the A/D conversion of FV pin voltage;

Rtot is the VCCS external resistance as defined in *Section 4.9*.

I_VCCS current resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±0.5% if Gsa=1, ±1% if Gsa = 1.5-2-3-4, ±2% if Gsa=6-8-12);

scaling amplifier offset (±300 µV);

VCCS gain accuracy (±1.2%);

VCCS offset (±700 µV);

VCCA voltage precision;

Rtot precision.

4.13 Pin HD, HG functionalities: heater FET driver and diagnostic

As shown in the block diagram of *Figure 2*, HG pin is externally connected to the gate of the external heater FET (an NMOS in low-side configuration, with the drain directly connected to the heater element), while HD is connected to the drain through the external resistance RHD (possible range for this resistor is specified in *Table 19*).

The heater is necessary in order to make the sensor work at a correct temperature. The sensor can only operate in high temperature conditions, but as it is not able to reach the desired range of temperature passively, an active heater is usually incorporated into the sensor structure. This heater is normally composed by an ohmic resistor through which the heater FET current is forced. The µP is able to obtain information regarding the sensor temperature from the results of the impedance test performed into the device and communicated to the µP via SPI (the higher is the sensor temperature, the lower is its impedance); consequently, the µP can intervene on sensor temperature acting on PW pin. PW is a digital input pin of the device and can be driven with a PWM signal by the µP. PW pin signal is then internally inverted by the logic and the consequent signal is then applied on HG pin, conditioning the activation/deactivation of the external heater FET (and so the power consumption necessary to heat the sensor).

Capacitive coupling due to heater commutations can cause undesired signals on the reference cell; in order to avoid it, the logic freezes the current state of HG signal during the measurement cycle. HG status will be driven again by PW signal once the measurement cycle is completed.

In order to avoid that the external FET switches on when VIGN voltage is present but the device is un-powered, a 100 kΩ pull-down resistor is permanently connected to HG pin.

A diagnostic circuitry is also present into the heater driver, in order to detect open circuit, short to ground or short to battery fault conditions; the logic into the device can communicate via SPI to the µP the fault detection through OCH, STGH, STBH bit status. The actions related to the diagnostic fault detection are described in *Section 5.4*, while all the heater diagnostic thresholds are specified in *Table 13*. More details about the heater diagnostic bits can be found in *Section 6.4*.

The ranges of the electrical parameters of the heater FET driver are specified in *Table 12* and *Table 15*.