



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

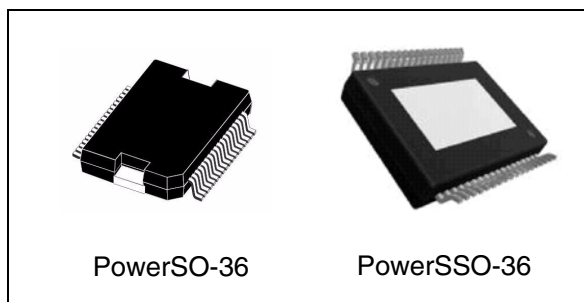
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Door actuator driver

Features

- One full bridge for 6A load ($R_{on}=150\text{ m}\Omega$)
- Two half bridges for 3A load ($R_{on}=300\text{ m}\Omega$)
- Two half bridges for 1.5A load ($R_{on}=800\text{ m}\Omega$)
- One highside driver for 6A load ($R_{on}=100\text{ m}\Omega$)
- Four highside drivers for 1.5 A load ($R_{on}=800\text{ m}\Omega$)
- Programmable softstart function to drive loads with higher inrush currents (i.e. current $>6\text{ A}, >3\text{ A}, >1.5\text{ A}$)
- Very low current consumption in standby mode ($I_S < 6\text{ }\mu\text{A typ}; I_{CC} < 25\text{ }\mu\text{A typ}; T_j \leq 85\text{ }^\circ\text{C}$)
- All outputs short circuit protected
- Current monitor output for 300 m Ω , 150 m Ω and 100 m highside drivers
- All outputs over temperature protected
- Open load diagnostic for all outputs
- Overload diagnostic for all outputs
- Separated half bridges for door lock motor
- PWM control of all outputs
- Charge pump output for reverse polarity protection



Applications

- Door actuator driver with bridges for door lock and safe lock, mirror axis control, mirror fold and highside driver for mirror defroster and four 10W-light bulbs.

Description

The L9950 and L9950XP are microcontroller driven multifunctional door actuator driver for automotive applications. Up to five DC motors and five grounded resistive loads can be driven with six half bridges and five highside drivers. The integrated standard serial peripheral interface (SPI) controls all operation modes (forward, reverse, brake and high impedance). All diagnostic informations are available via SPI.

Table 1. Device summary

Package	Order codes	
	Part number (tube)	Part number (tape and reel)
PowerSO-36	L9950	L9950TR
PowerSSO-36	L9950XP	L9950XPTR

4.7	Status register	25
4.8	Test mode	26
5	Packages thermal data	31
6	Package and packing information	32
6.1	ECOPACK®	32
6.2	PowerSO-36 package information	32
6.3	PowerSSO-36 package information	34
6.4	PowerSO-36 packing information	35
6.5	PowerSSO-36 packing information	37
7	Revision history	38

List of tables

Table 1.	Device summary	1
Table 2.	Pin definitions and functions	6
Table 3.	Absolute maximum ratings	9
Table 4.	ESD protection	9
Table 5.	Thermal data	9
Table 6.	Temperature warning and thermal shutdown	10
Table 7.	Supply	10
Table 8.	Overvoltage and under voltage detection	11
Table 9.	Current monitor output	11
Table 10.	Charge pump output	11
Table 11.	OUT1 - OUT11	12
Table 12.	Delay time from standby to active mode	14
Table 13.	Inputs: CSN, CLK, PWM1/2 and DI	14
Table 14.	DI timing	15
Table 15.	DO	15
Table 16.	DO timing	16
Table 17.	CSN timing	16
Table 18.	Test mode	26
Table 19.	SPI - input data and status registers 0	27
Table 20.	SPI - input data and status registers 1	29
Table 21.	PowerSO-36 mechanical data	33
Table 22.	PowerSSO-36 mechanical data	34
Table 23.	Document revision history	38

List of figures

Figure 1.	Block diagram	6
Figure 2.	Configuration diagram (top view)	8
Figure 3.	SPI - transfer timing diagram	16
Figure 4.	SPI - input timing	17
Figure 5.	SPI - DO valid data delay time and valid time	17
Figure 6.	SPI - DO enable and disable time	18
Figure 7.	SPI - driver turn-on/off timing, minimum csn hi time	18
Figure 8.	SPI - timing of status bit 0 (fault condition)	19
Figure 9.	Example of programmable soft start function for inductive loads	23
Figure 10.	Packages thermal data	31
Figure 11.	PowerSO-36 package dimensions	32
Figure 12.	PowerSSO-36 package dimensions	34
Figure 13.	PowerSO-36 tube shipment (no suffix)	35
Figure 14.	PowerSO-36 tape and reel shipment (suffix "TR")	36
Figure 15.	PowerSSO-36 tube shipment (no suffix)	37
Figure 16.	PowerSSO-36 tape and reel shipment (suffix "TR")	37

1 Block diagram and pin description

Figure 1. Block diagram

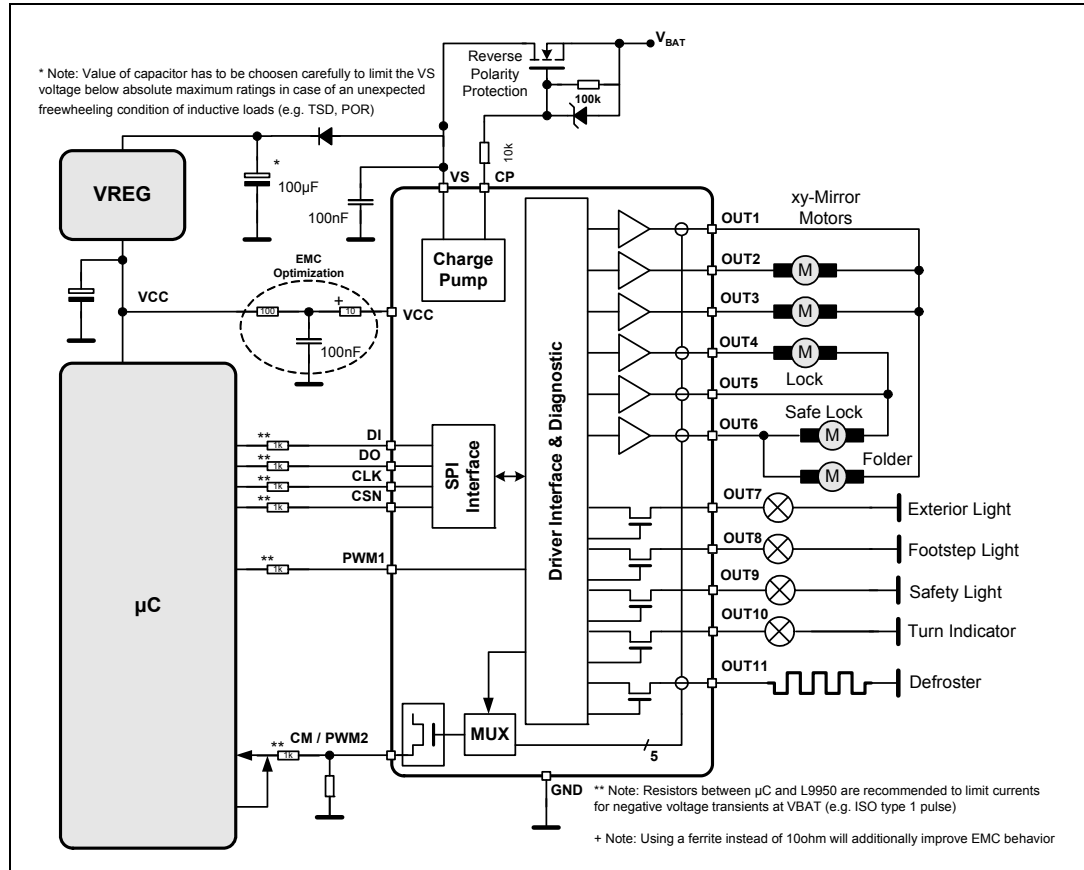


Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground. Reference potential. Important: for the capability of driving the full current at the outputs all pins of GND must be externally connected.
2, 35	OUT11	Highside driver output 11. The output is built by a highside switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The highside driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected. Important: for the capability of driving the full current at the outputs both pins of OUT11 must be externally connected.

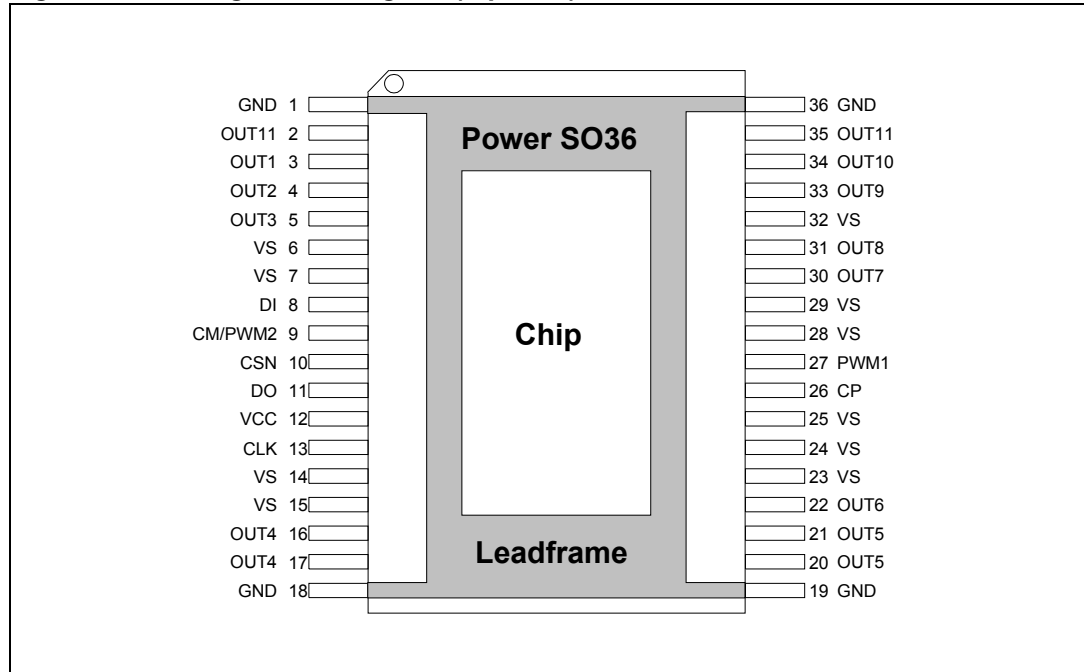
Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
3 4 5	OUT1 OUT2 OUT3	Hal bridge output 1,2,3. The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: highside driver from output to VS, lowside driver from GND to output). This output is over-current and open load protected.
6, 7, 14, 15, 23, 24, 25, 28, 29, 32	VS	Power supply voltage (external reverse protection required). For this input a ceramic capacitor as close as possible to GND is recommended. Important: for the capability of driving the full current at the outputs all pins of VS must be externally connected.
8	DI	Serial data input. The input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 24bit control word and the least significant bit (LSB, bit 0) is transferred first.
9	CM/PWM2	Current monitor output/PWM2 input. Depending on the selected multiplexer bits of Input Data Register this output sources an image of the instant current through the corresponding highside driver with a ratio of 1/10.000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the outputs OUT9 and OUT10.
10	CSN	Chip select not input/test mode. This input is low active and requires CMOS logic levels. The serial data transfer between L9950 and micro controller is enabled by pulling the input CSN to low level. If an input voltage of more than 7.5V is applied to CSN pin the L9950 will be switched into a test mode.
11	DO	Serial data output. The diagnosis data is available via the SPI and this tristate output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high).
12	VCC	Logic supply voltage. For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input. This input controls the internal shift register of the SPI and requires CMOS logic levels.
16,17, 20,21, 22	OUT4 OUT5 OUT6	Half bridge output 4,5,6: see OUT1 (pin 3). Important: for the capability of driving the full current at the outputs both pins of OUT4 (OUT5, respectively) must be externally connected.
26	CP	Charge pump output. This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
27	PWM1	PWM1 input. This input signal can be used to control the drivers OUT1-OUT8 and OUT11 by an external PWM signal.
30 31 33 34	OUT7, OUT8, OUT9, OUT10	Highside driver output 7,8,9,10. The output is built by a highside switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The highside driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected.

Figure 2. Configuration diagram (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
	Single pulse $t_{max} < 400$ ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
$V_{DI}, V_{DO}, V_{CLK},$ V_{CSN}, V_{pwm1}	Digital input/output voltage	-0.3 to $V_{CC} + 0.3$	V
V_{CM}	Current monitor output	-0.3 to $V_{CC} + 0.3$	V
V_{CP}	Charge pump output	-25 to $V_S + 11$	V
$I_{OUT1,2,3,6,7,8,9,10}$	Output current	± 5	A
$I_{OUT4,5,11}$	Output current	± 10	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	± 4 ⁽¹⁾	kV
Output pins: OUT1 - OUT11	± 8 ⁽²⁾	kV

1. HBM according to CDF-AEC-Q100-002.

2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

2.4 Temperature warning and thermal shutdown

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature			150	°C
$T_{jTW\ OFF}$	Temperature warning threshold junction temperature	130	-	-	°C
$T_{jTW\ HYS}$	Temperature warning hysteresis	-	5	-	°K
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature			170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	150	-	-	°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis	-	5	-	°K

2.5 Electrical characteristics

$V_S = 8$ to 16 V, $V_{CC} = 4.5$ to 5.3 V, $T_j = -40$ to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage range		7	-	28	V
I_S	VS DC supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V active mode OUT1 - OUT11 floating	-	7	20	mA
	VS quiescent supply current	$V_S = 16$ V, $V_{CC} = 0$ V standby mode OUT1 - OUT11 floating $T_{test} = -40$ °C, 25 °C	-	4	12	μA
I_{CC}	VCC DC supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V $CSN = V_{CC}$, active mode	-	1	3	mA
	VCC quiescent supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V $CSN = V_{CC}$ standby mode OUT1 - OUT11 floating $T_{test} = -40$ °C, 25 °C	-	25	50	μA
$I_S + I_{CC}$	Sum quiescent supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V $CSN = V_{CC}$ standby mode OUT1 - OUT11 floating $T_{test} = -40$ °C, 25 °C	-	31	75	μA

Table 8. Overvoltage and under voltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	VS UV-threshold voltage	V_S increasing	5.9	-	7.2	V
$V_{SUV\ OFF}$	VS UV-threshold voltage	V_S decreasing	5.5	-	6.5	V
$V_{SUV\ hyst}$	VS UV-hysteresis	$V_{SUV\ ON} - V_{SUV\ OFF}$	-	0.5	-	V
$V_{SOV\ OFF}$	VS OV-threshold voltage	V_S increasing	18	-	24.5	V
$V_{SOV\ ON}$	VS OV-threshold voltage	V_S decreasing	17.5	-	22	V
$V_{SOV\ hyst}$	VS OV-hysteresis	$V_{SOV\ OFF} - V_{SOV\ ON}$	-	1	-	V
$V_{POR\ OFF}$	Power-on-reset threshold	V_{CC} increasing	-	-	4.4	V
$V_{POR\ ON}$	Power-on-reset threshold	V_{CC} decreasing	3.1	-	-	V
$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF} - V_{POR\ ON}$	-	0.3	-	V

Table 9. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range	$V_{CC} = 5\text{ V}$	0		4	V
$I_{CM,r}$	Current monitor output ratio: $I_{CM} / I_{OUT1,4,5,6,11}$	$0\text{ V} \leq V_{CM} \leq 4\text{ V}$, $V_{CC}=5\text{ V}$	-	$\frac{1}{10.000}$	-	-
$I_{CM\ acc}$	Current monitor accuracy	$0\text{ V} \leq V_{CM} \leq 3.8\text{ V}$, $V_{CC} = 5\text{ V}$, $I_{Out,min}=500\text{ mA}$, $I_{Out4,5,11,max} = 5.9\text{ A}$ $I_{Out1,6,max} = 2.9\text{ A}$ (FS = full scale= 600 μA)	-	4% + 1%FS	8% + 2%FS	-

Table 10. Charge pump output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	$V_S = 8\text{ V}$, $I_{CP} = -60\ \mu\text{A}$	6	-	13	V
		$V_S = 10\text{ V}$, $I_{CP} = -80\ \mu\text{A}$	8	-	13	V
		$V_S \geq 12\text{ V}$, $I_{CP} = -100\ \mu\text{A}$	10	-	13	V
I_{CP}	Charge pump output current	$V_{CP} = V_S + 10\text{ V}$, $V_S = 13.5\text{ V}$	95	150	300	μA

Table 11. OUT1 - OUT11

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT1}$, $r_{ON\ OUT6}$	On-resistance to supply or GND	$V_S = 13.5\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT1,6} = \pm 1.5\text{ A}$	-	300	400	mΩ
		$V_S = 13.5\text{ V}$, $T_j = 125\text{ }^\circ\text{C}$, $I_{OUT1,6} = \pm 1.5\text{ A}$	-	450	600	mΩ
		$V_S = 8.0\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT1,6} = \pm 1.5\text{ A}$	-	300	400	mΩ
$r_{ON\ OUT2}$, $r_{ON\ OUT3}$	On-resistance to supply or GND	$V_S = 13.5\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT2,3} = \pm 0.8\text{ A}$	-	800	1100	mΩ
		$V_S = 13.5\text{ V}$, $T_j = 125\text{ }^\circ\text{C}$, $I_{OUT2,3} = \pm 0.8\text{ A}$	-	1250	1700	mΩ
		$V_S = 8.0\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT2,3} = \pm 0.8\text{ A}$	-	800	1100	mΩ
$r_{ON\ OUT4}$, $r_{ON\ OUT5}$	On-resistance to supply or GND	$V_S = 13.5\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT4,5} = \pm 3.0\text{ A}$	-	150	200	mΩ
		$V_S = 13.5\text{ V}$, $T_j = 125\text{ }^\circ\text{C}$, $I_{OUT4,5} = \pm 3.0\text{ A}$	-	225	300	mΩ
		$V_S = 8.0\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT4,5} = \pm 3.0\text{ A}$	-	150	200	mΩ
$r_{ON\ OUT7}$, $r_{ON\ OUT8}$, $r_{ON\ OUT9}$, $r_{ON\ OUT10}$	On-resistance to supply	$V_S = 13.5\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT7,8,9,10} = -0.8\text{ A}$	-	800	1100	mΩ
		$V_S = 13.5\text{ V}$, $T_j = 125\text{ }^\circ\text{C}$, $I_{OUT7,8,9,10} = -0.8\text{ A}$	-	1250	1700	mΩ
		$V_S = 8.0\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT7,8,9,10} = -0.8\text{ A}$	-	800	1100	mΩ
$r_{ON\ OUT11}$	On-resistance to supply	$V_S = 13.5\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT11} = -3.0\text{ A}$	-	100	150	mΩ
		$V_S = 13.5\text{ V}$, $T_j = 125\text{ }^\circ\text{C}$, $I_{OUT11} = -3.0\text{ A}$	-	150	200	mΩ
		$V_S = 8.0\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$, $I_{OUT11} = -3.0\text{ A}$	-	100	150	mΩ
I_{OUT1} , I_{OUT6}	Output current limitation to supply or GND	Sink and source, $V_S = 13.5\text{ V}$	3	-	5	A
I_{OUT2} , I_{OUT3}	Output current limitation to supply or GND	Sink and source, $V_S = 13.5\text{ V}$	1.5	-	2.5	A
I_{OUT4} , I_{OUT5}	Output current limitation to supply or GND	Sink and source, $V_S = 13.5\text{ V}$	6	-	10	A
I_{OUT7} , I_{OUT8} , I_{OUT9} , I_{OUT10}	Output current limitation to GND	Source, $V_S = 13.5\text{ V}$	1.5	-	2.5	A

Table 11. OUT1 - OUT11 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$ I_{OUT11} $	Output current limitation to GND	Source, $V_S = 13.5V$	6	-	10	A
$t_{d\ ON\ H}$	Output delay time, highside driver on	$V_S = 13.5\ V$, corresponding lowside driver is not active	20	40	80	μs
$t_{d\ OFF\ H}$	Output delay time, highside driver off	$V_S = 13.5\ V$	50	150	300	μs
$t_{d\ ON\ L}$	Output delay time, lowside driver on	$V_S = 13.5\ V$, corresponding highside driver is not active	15	30	70	μs
$t_{d\ OFF\ L}$	Output delay time, lowside driver off	$V_S = 13.5\ V$	80	150	300	μs
$t_{D\ HL}$	Cross current protection time, source to sink	$t_{d\ ON\ L} - t_{d\ OFF\ H}$,	-	200	400	μs
$t_{D\ LH}$	Cross current protection time, sink to source	$t_{d\ ON\ H} - t_{d\ OFF\ L}$	-	200	400	μs
I_{QLH}	Switched-off output current highside drivers of OUT1-11	$V_{OUT1-11}=0\ V$, standby mode	0	-2	-5	μA
		$V_{OUT1-11}=0\ V$, active mode	-40	-15	0	μA
I_{QLL}	Switched-off output current lowside drivers of OUT1-6	$V_{OUT1-6} = V_S$, standby mode	0	110	180	μA
		$V_{OUT1-6} = V_S$, active mode	-40	-15	0	μA
I_{OLD1}	Open load detection current of OUT1		5	30	80	mA
I_{OLD23}	Open load detection current of OUT2, OUT3		15	40	60	mA
I_{OLD45}	Open load detection current of OUT4 and OUT5		60	150	300	mA
I_{OLD6}	Open load detection current of OUT6		30	70	150	mA
$I_{OLD78910}$	Open load detection current of OUT7, OUT8, OUT9, OUT10		15	40	60	mA
I_{OLD11}	Open load detection current of OUT11		30	150	300	mA
t_{dOL}	Minimum duration of open load condition to set the status bit		500	-	3000	μs
t_{ISC}	Minimum duration of over-current condition to switch off the driver		10	-	100	μs

Table 11. OUT1 - OUT11 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
dV_{OUT16}/dt	Slew rate of OUT1,OUT6	$V_S = 13.5\text{ V}$ $I_{load} = \pm 1.5\text{ A}$	0.1	0.2	0.4	V/ μ s
dV_{OUT23}/dt , $dV_{OUT78910}/dt$	Slew rate of OUT2/3 and OUT7-OUT10	$V_S = 13.5\text{ V}$ $I_{load} = -0.8\text{ A}$	0.09	0.2	0.4	V/ μ s
dV_{OUT45}/dt	Slew rate of OUT4, OUT5	$V_S = 13.5\text{ V}$ $I_{load} = \pm 3.0\text{ A}$	0.1	0.2	0.4	V/ μ s
dV_{OUT11}/dt	Slew rate of OUT11	$V_S = 13.5\text{ V}$ $I_{load} = 3.0\text{ A}$	0.1	0.2	0.4	V/ μ s

2.6 SPI - electrical characteristics

$V_S = 8$ to 16 V , $V_{CC} = 4.5$ to 5.3 V , $T_j = -40$ to $150\text{ }^\circ\text{C}$, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 12. Delay time from standby to active mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.	-	160	300	μ s

Table 13. Inputs: CSN, CLK, PWM1/2 and DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{inL}	Input low level	$V_{CC} = 5\text{ V}$	1.5	2.0	-	V
V_{inH}	Input high level	$V_{CC} = 5\text{ V}$	-	3.0	3.5	V
V_{inHyst}	Input hysteresis	$V_{CC} = 5\text{ V}$	0.5	-	-	V
$I_{CSN\ in}$	Pull up current at input CSN	$V_{CSN} = 3.5\text{ V}$ $V_{CC} = 5\text{ V}$	-40	-20	-8	μ A
$I_{CLK\ in}$	Pull down current at input CLK	$V_{CLK} = 1.5\text{ V}$	10	25	50	μ A
$I_{DI\ in}$	Pull down current at input DI	$V_{DI} = 1.5\text{ V}$	10	25	50	μ A
$I_{PWM1\ in}$	Pull down current at input PWM1	$V_{PWM} = 1.5\text{ V}$	10	25	50	μ A
C_{in}	Input capacitance at input CSN, CLK, DI and PWM1/2	$V_{CC} = 0$ to 5.3 V	-	10	15	pF

Note: Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 14. DI timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	$V_{CC} = 5\text{ V}$	1000	-	-	ns
t_{CLKH}	Clock high time	$V_{CC} = 5\text{ V}$	400	-	-	ns
t_{CLKL}	Clock low time	$V_{CC} = 5\text{ V}$	400	-	-	ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	$V_{CC} = 5\text{ V}$	400	-	-	ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	$V_{CC} = 5\text{ V}$	400	-	-	ns
$t_{set\ DI}$	DI setup time	$V_{CC} = 5\text{ V}$	200	-	-	ns
$t_{hold\ time}$	DI hold time	$V_{CC} = 5\text{ V}$	200	-	-	ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	$V_{CC} = 5\text{ V}$	-	-	100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	$V_{CC} = 5\text{ V}$	-	-	100	ns

Note: DI timing parameters tested in production by a passed/failed test:
 $T_j = -40\text{ }^\circ\text{C}/+25\text{ }^\circ\text{C}$: SPI communication @ 2 MHz.
 $T_j = +125\text{ }^\circ\text{C}$: SPI communication @ 1.25 MHz.

Table 15. DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low level	$V_{CC} = 5\text{ V}$, $I_D = -2\text{ mA}$	-	0.2	0.4	V
V_{DOH}	Output high level	$V_{CC} = 5\text{ V}$, $I_D = 2\text{ mA}$	$V_{CC} - 0.4$	$V_{CC} - 0.2$	-	V
I_{DOLK}	Tristate leakage current	$V_{CSN} = V_{CC}$, $0\text{ V} < V_{DO} < V_{CC}$	-10	-	10	μA
$C_{DO}^{(1)}$	Tristate input capacitance	$V_{CSN} = V_{CC}$, $0\text{ V} < V_{CC} < 5.3\text{ V}$	-	10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 16. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r DO}$	DO rise time	$C_L = 100 \text{ pF}$, $I_{load} = -1 \text{ mA}$	-	80	140	ns
$t_{f DO}$	DO fall time	$C_L = 100 \text{ pF}$, $I_{load} = 1 \text{ mA}$	-	50	100	ns
$t_{en DO \text{ tri L}}$	DO enable time from tristate to low level	$C_L = 100 \text{ pF}$, $I_{load} = 1 \text{ mA}$ pull-up load to V_{CC}	-	100	250	ns
$t_{dis DO \text{ L tri}}$	DO disable time from low level to tristate	$C_L = 100 \text{ pF}$, $I_{load} = 4 \text{ mA}$ pull-up load to V_{CC}	-	380	450	ns
$t_{en DO \text{ tri H}}$	DO enable time from tristate to high level	$C_L = 100 \text{ pF}$, $I_{load} = -1 \text{ mA}$ pull-down load to GND	-	100	250	ns
$t_{dis DO \text{ H tri}}$	DO disable time from high level to tristate	$C_L = 100 \text{ pF}$, $I_{load} = -4 \text{ mA}$ pull-down load to GND	-	380	450	ns
$t_{d DO}$	DO delay time	$V_{DO} < 0.3 V_{CC}$, $V_{DO} > 0.7 V_{CC}$, $C_L = 100 \text{ pF}$	-	50	250	ns

Table 17. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN_HI, \text{stb}}$	Minimum CSN HI time, switching from standby mode	Transfer of SPI command to Input Register	-	20	50	μs
$t_{CSN_HI, \text{min}}$	Maximum CSN HI time, active mode	Transfer of SPI command to input register	-	2	4	μs

Figure 3. SPI - transfer timing diagram

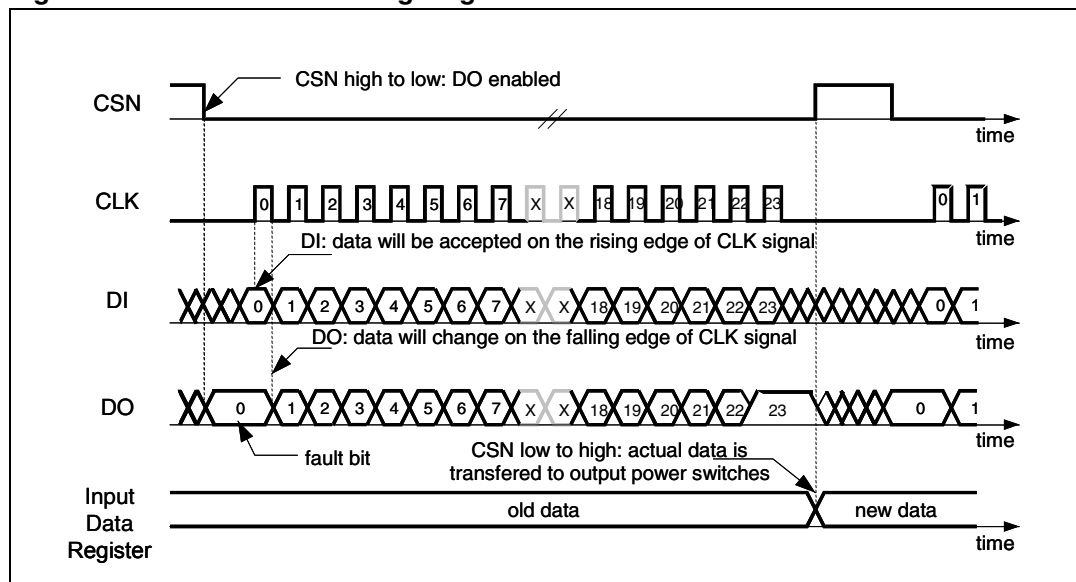


Figure 4. SPI - input timing

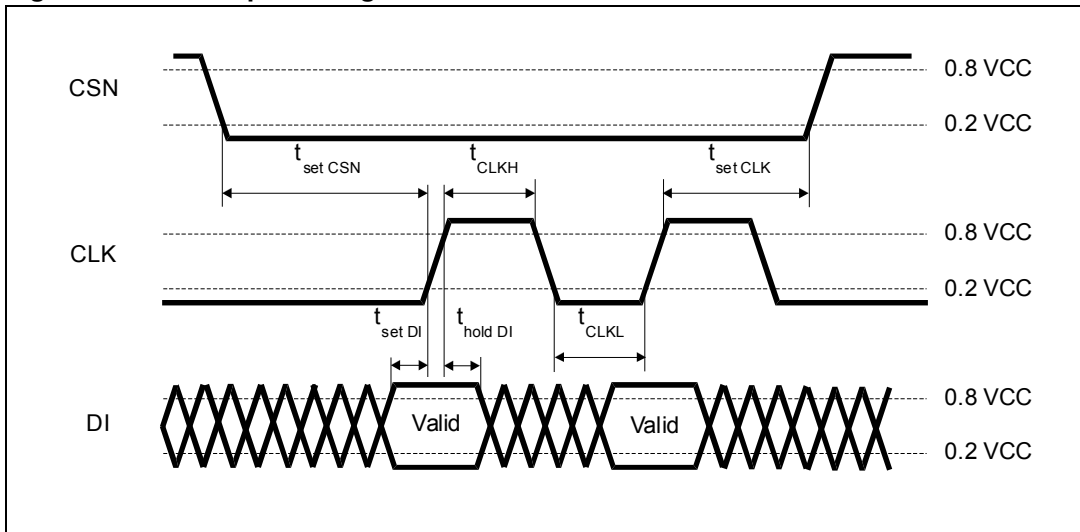


Figure 5. SPI - DO valid data delay time and valid time

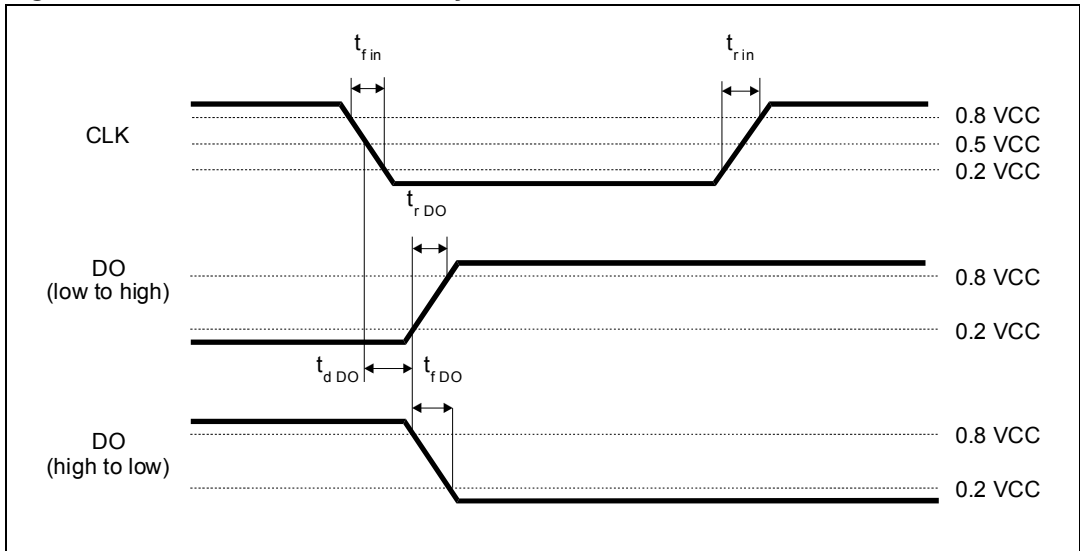


Figure 6. SPI - DO enable and disable time

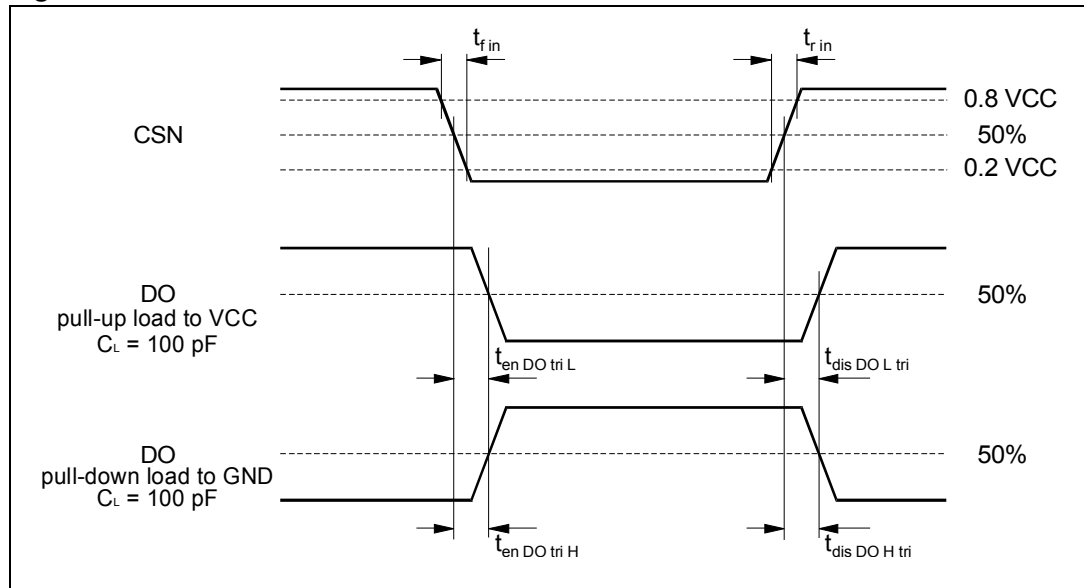


Figure 7. SPI - driver turn-on/off timing, minimum csn hi time

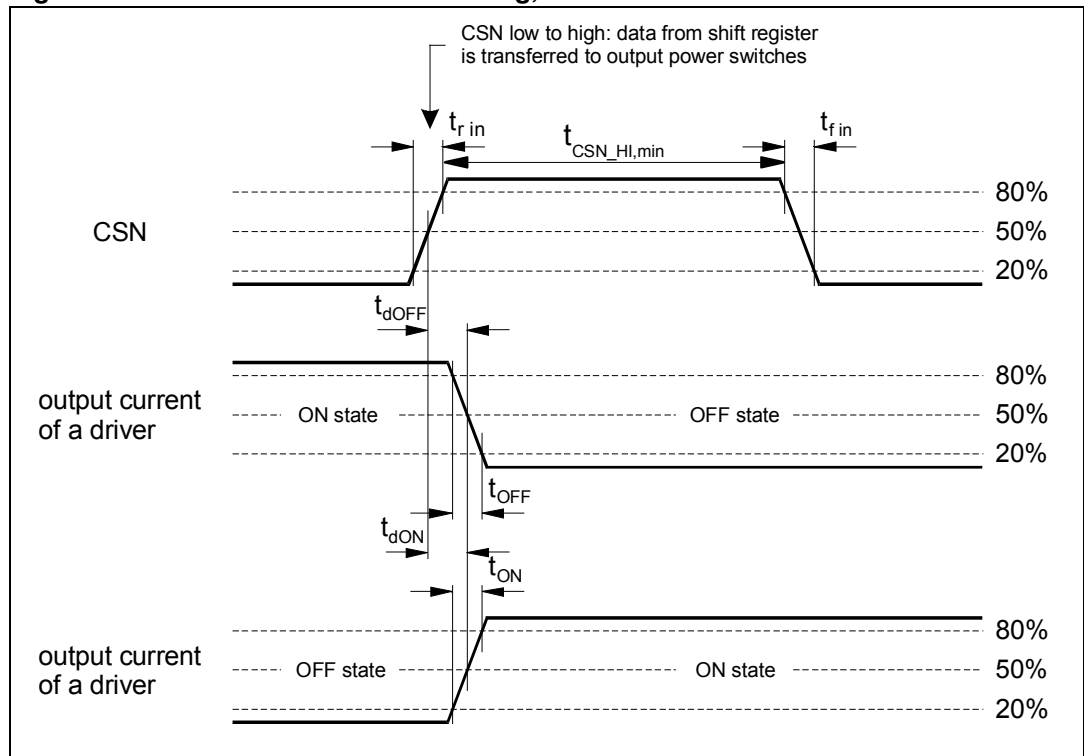
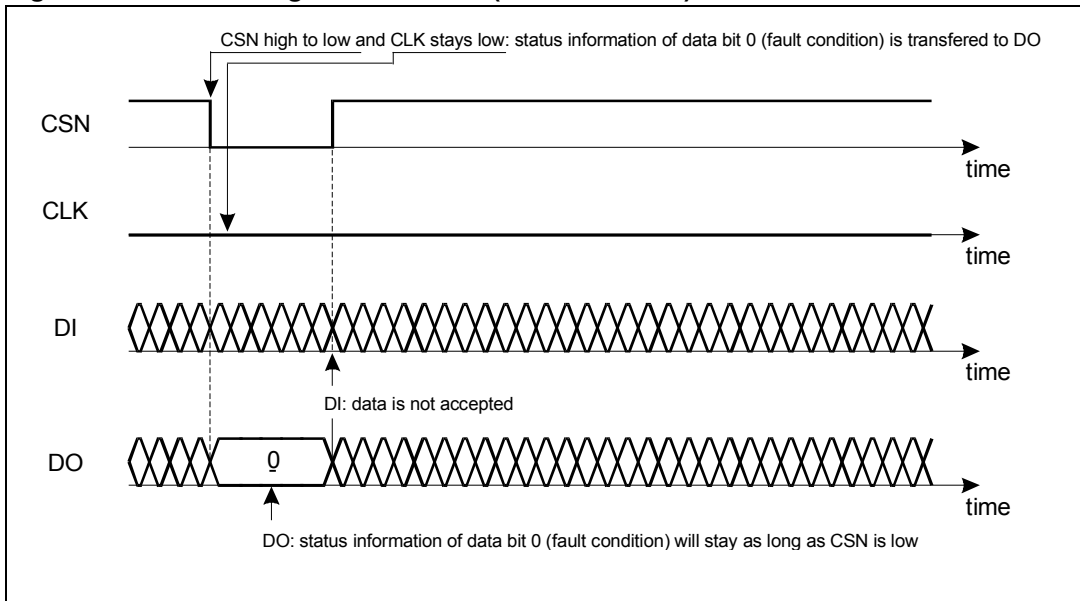


Figure 8. SPI - timing of status bit 0 (fault condition)



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the highside drivers. An internal charge-pump is used to drive the highside switches. The logic supply voltage V_{CC} (stabilized 5 V) is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from under voltage to $V_{POR\ OFF} = 4.2\text{ V}$) the circuit is initialized by an internally generated power on reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON} = 3.4\text{ V}$), the outputs are switched to tristate (high impedance) and the status registers are cleared.

3.2 Standby mode

The standby mode of the L9950 is activated by clearing the bit 23 of the Input Data Register 0. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at V_S (V_{CC}) is less than $6\ \mu\text{A}$ ($50\ \mu\text{A}$) for $CSN = \text{high}$ (DO in tristate). By switching the V_{CC} voltage a very low quiescent current can be achieved. If bit 23 is set, the device will be switched to active mode.

3.3 Inductive loads

Each half bridge is built by an internally connected highside and a lowside power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT6 without external free wheeling diodes. The highside drivers OUT7 to OUT11 are intended to drive resistive loads. Hence only a limited energy ($E < 1\text{ mJ}$) can be dissipated by the internal ESD diodes in freewheeling condition. For inductive loads ($L > 100\ \mu\text{H}$) an external free wheeling diode connected to GND and the corresponding output is needed.

3.4 Diagnostic functions

All diagnostic functions (over/open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least $32\ \mu\text{s}$ (open load: 1 ms , respectively) before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open load and temperature warning function are intended for information purpose and will not change the state of the output drivers. On contrary, the overload and thermal shutdown condition will disable the corresponding driver (overload) or all drivers (thermal shutdown), respectively. Without setting the over-current recovery bits in the Input Data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

3.5 Overvoltage and under voltage detection

If the power supply voltage V_S rises above the overvoltage threshold $V_{SOV\ OFF}$ (typical 21 V), the outputs OUT1 to OUT11 are switched to high impedance state to protect the load. When the voltage V_S drops below the under voltage threshold $V_{SUUV\ OFF}$ (UV switch OFF voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers to normal operating voltage the outputs stages return to the programmed state (input register 0: bit 20=0).

If the under voltage/overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers. It is recommended to set bit 20 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Temperature warning and thermal shutdown

If junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set and is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to protect the device. In order to reactivate the output stages the junction temperature must decrease below $T_{j\ SD} - T_{j\ SD\ HYS}$ and the thermal shutdown bit has to be cleared by the microcontroller.

3.7 Open-load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.8 Over load detection

In case of an over-current condition a flag is set in the status register in the same way as open load detection. If the over-current signal is valid for at least $t_{ISC} = 32\ \mu s$, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.9 Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/10000) of the instantaneous current of the selected highside driver. The bits 18 and 19 of the Input Data Register 0 control which of the outputs OUT1, OUT4, OUT5, OUT6 and OUT11 will be multiplexed to the current monitor output. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open or overload condition. For example this can be used to detect the motor state (starting, free running, stalled). Moreover, it is possible to regulate the power of the defroster more precisely by measuring the load current. The current monitor output is bidirectional (c.f. PWM inputs).

3.10 PWM inputs

Each driver has a corresponding PWM enable bit which can be programmed by the SPI interface. If the PWM enable bit is set, the output is controlled by the logically AND combination of the PWM signal and the output control bit in Input Data Register. The outputs OUT1-OUT8 and OUT11 are controlled by the PWM1 input and the outputs OUT9/10 are controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals.

3.11 Cross current protection

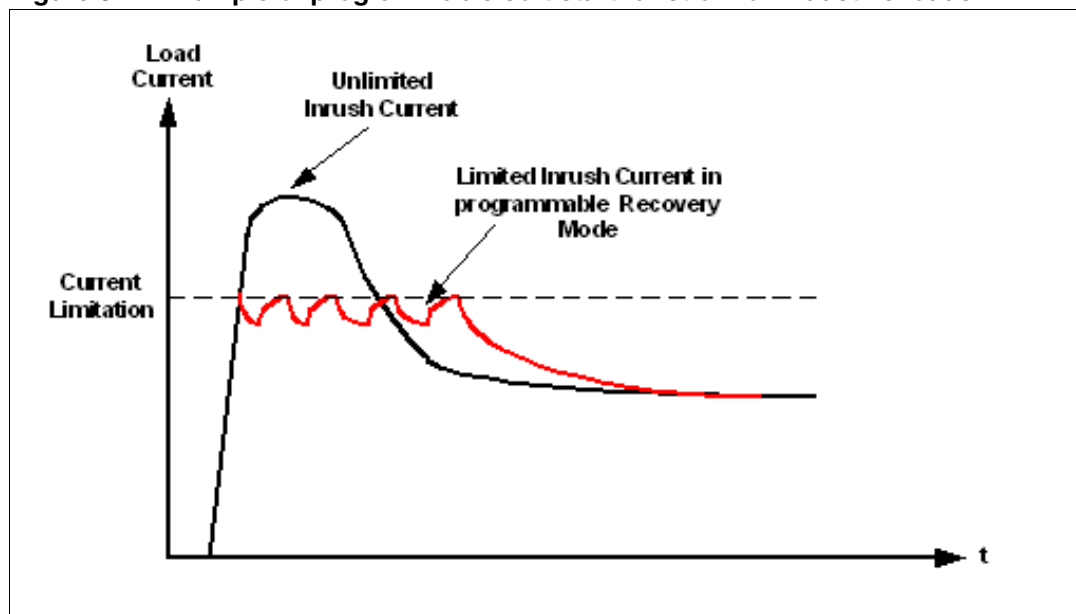
The six half bridges of the device are cross current protected by an internal delay time. If one driver (LS or HS) is turned off the activation of the other driver of the same half bridge will be automatically delayed by the cross current protection time. After the cross current protection time is expired the slew rate limited switch off phase of the driver will be changed to a fast turn-off phase and the opposite driver is turned on with slew rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned off before the opposite driver will start to conduct.

3.12 Programmable soft start function to drive loads with higher inrush current

Loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable soft start function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device will automatically switch-on the outputs again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to be about 12% or 25%. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition.

The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch on light bulbs by setting the over-current Recovery bit for the first 50ms. After clearing the recovery bit the output will be automatically disabled if the overload condition still exists.

Figure 9. Example of programmable soft start function for inductive loads



4 Functional description of the SPI

4.1 Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin will reflect the status bit 0 (fault condition) of the device which is a logical or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI communication cycle.

Note: In contrast to the SPI standard the least significant bit (LSB) will be transferred first (see [Figure 3](#)).

4.2 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN will be called a communication frame. If the CSN input pin is driven above 7.5V, the L9950 will go into a test mode. In the test mode the DO will go from tri state to active mode.

4.3 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

4.5 Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal.

4.6 Input data register

The device has two input registers. The first bit (bit 0) at the DI input is used to select one of the two Input Registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Input Data Register only if a frame of exact 24 data bits are detected. Depending on bit 0 the contents of the selected status register will be transferred to DO during the current communication frame. Bit 1-17 controls the behavior of the corresponding driver.

If bit 23 is zero, the device will go into the standby mode. The bits 18 and 19 are used to control the current monitor multiplexer. Bit 22 is used to reset all status bits in both status registers. The bits in the status registers will be cleared after the current communication frame (rising edge of CSN).

4.7 Status register

This device uses two status registers to store and to monitor the state of the device. Bit 0 is used as a fault bit and is a logical NOR combination of bits 1-22 in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI communication cycle. If one of the over-current bits is set, the corresponding driver will be disabled. If the over-current recovery bit of the output is not set the microcontroller has to clear the over-current bit to enable the driver. If the thermal shutdown bit is set, all drivers will go into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers.