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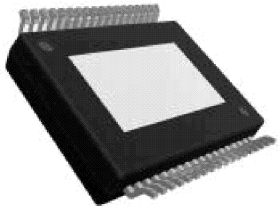
L9952GXP

Power management system IC

Features

- Two 5V low-drop voltage regulators (250mA, 100mA continuous mode
- Low stand-by current: V_{BAT} stby, 7µA; V_1 stby, 45µA, (75µA in cycl. sense)
- Window watchdog and fail-safe output
- Interrupt output
- Wake-up logic with cyclic contact monitoring
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- 24 bit SPI interface for mode control and diagnostic
- Output drivers
- 4 High side drivers for e.g. LED or HALL ($R_{DSon,typ}$ = 7 Ω)
- 1 High side driver Out_HS ($R_{DSon,typ}$ = 1 Ω)
- 2 Relay drivers ($R_{DSon,typ}$ = 2 Ω)
- Outputs are short circuit protected
- 2 Op amp's for current sensing in GND return lines
- Temperature warning and thermal shutdown



PowerSSO-36

Applications

- Automotive ECU' s such as door zone and body control modules.

Description

The L9952GXP is a power management system IC containing two low drop regulators with advanced contact monitoring and additional peripheral functions.

The integrated standard serial peripheral interface (SPI) controls all L9952GXP operation modes and provides driver diagnostic functions.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L9952GXP	L9952GXPTR

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1 Pin definitions and functions

Figure 1. Block diagram

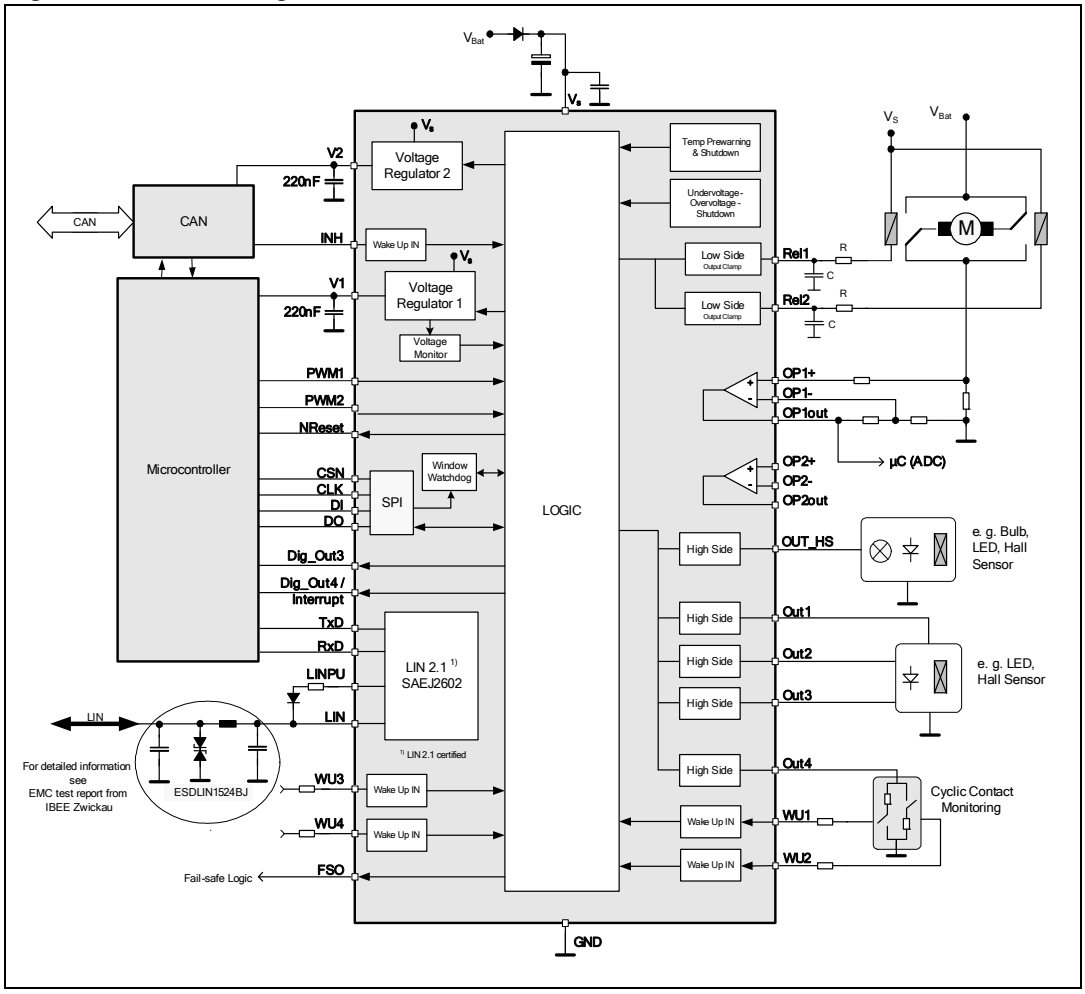


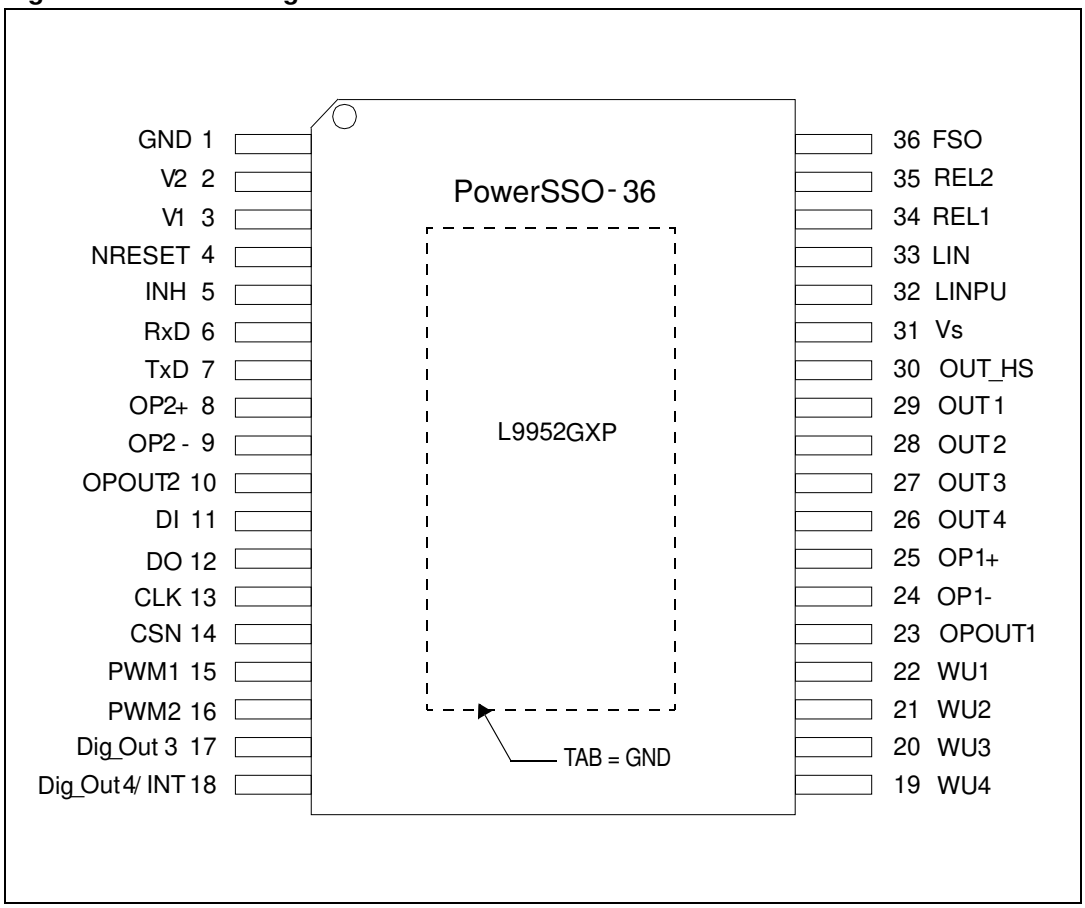
Table 2. Pins definitions and functions

Pin name	PowerSS0-36	Function
GND	1	Ground
V2	2	Voltage regulator 2 output : 5 V supply for external loads e.g. IR receiver, potentiometer
V1	3	Voltage regulator 1 output : 5 V supply e.g. micro controller, Can transceiver
NReset	4	NReset output to micro controller - Internal pull-up of typ. 100KΩ (reset state = low)
INH	5	Wake-up input e.g. from CAN transceiver
RxD	6	Receiver output of the LIN 2.1 transceiver

Table 2. Pins definitions and functions (continued)

Pin name	PowerSS0-36	Function
TxD	7	Transmitter input of the LIN 2.1 transceiver
OP2+	8	Non inverting input of operational sense amplifier
OP2-	9	Inverting input of operational sense amplifier
$OP2_{OUT}$	10	Output of operational sense amplifier
DI	11	SPI : serial data input
DO	12	SPI : serial data output
CLK	13	SPI : serial clock input
CSN	14	SPI : chip select not input
PWM1	15	Pulse width modulation input
PWM2	16	Pulse width modulation input
Dig_Out3	17	Digital output
Dig_Out4/INT	18	Digital output (configurable as Interrupt Output)
$Wu_{4..1}$	19 to 22	Wake-up input: input pins for static or cyclic monitoring of external contacts
$OP1_{OUT}$	23	Output of operational sense amplifier
OP1-	24	Inverting input of operational sense amplifier
OP1+	25	Non inverting input of operational sense amplifier
$Out_{4..1}$	26 to 29	High side driver (7 Ω, typ.) - to supply e.g. LED' s, HALL sensors or external contacts
Out_HS	30	High side drivers (1 Ω, typ.) - to supply e.g. LED' s, Bulbs, HALL sensors or external contacts
Vs	31	Power supply voltage
LINPU	32	LIN master pull up
LIN	33	LIN bus line
Rel1	34	Low side driver (2 Ω, typ.) - e.g. relay
Rel2	35	Low side driver (2 Ω, typ.) - e.g. relay
FSO	36	Fail safe output - used to supervise or control applications in case of watchdog and/or V1 under-voltage failure (e.g. to activate emergency lights)

Figure 2. Pins configuration



2 Description

2.1 Voltage regulator

The L9952GXP contains 2 independent and fully protected low drop voltage regulators, which are designed for very fast transient response.

The output voltage is stable with loads capacitors $\geq$ 220nF.

2.1.1 Voltage regulator: V1

The voltage regulator V1 provides 5V supply voltage and up to 250mA continuous load current for the external digital logic (micro controller, CAN transceiver ...). In addition the regulator V1 drives the L9952GXP internal 5V loads. The voltage regulator is protected against overload and over-temperature. An external reverse current protection has to be provided by the application circuitry to prevent the output capacitor from being discharged by negative transients or low input voltage. The output voltage precision is better than +/-2% (incl. temperature drift and line-/load regulation) for operating mode; respectively +/-3% during low current mode. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors $\geq$ 220nF.

If device Temperature exceeds TSD1 threshold, all outputs (Hsx, Lsx, V2, LIN) will be deactivated except V1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2>TSD1), also V1 will be deactivated (see state chart Fig. 3.1: “Protection and diagnosis”). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1sec. During this time, all other wakeup sources (CAN, LIN, and WU1...4) are disabled. After 1 sec, the voltage regulator will try to restart automatically. If TSD2 occurs within one minute and for 8 consecutive times, the L9952GXP enters the V_{BAT} - standby mode.

In case of short to GND at “V1” after initial turn on (V1 < 2V for at least 4ms) the L9952GXP enters the V_{BAT} - standby mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..4, SPI.

2.1.2 Voltage regulator: V2

The voltage regulator V2 supplies additional 5V loads (e.g. Logic components, external sensors, external potentiometers). The continuous load current is 50mA. The regulator provides accuracy better than $\pm$ 3% @ 50mA (4% @ 100mA) load current.

In case of short to GND at “V2” after initial turn on (V2 < 2V for at least 4ms) the V2 regulator is switched off. Micro processor has to send a clear command to reactivate the V2 regulator.

V2 is protected against:

- Overload
- Over temperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.2 Power control in operating modes

The L9952GXP can be operated in 4 different operating modes:

- Active
- Flash
- V_1- standby
- V_{BAT} - standby

A cyclic monitoring of wake-up inputs is available in stand-by modes.

2.2.1 Active mode

All functions are available.

2.2.2 Flash mode

To disable the watchdog feature a FLASH program mode is available.

The mode can be entered by $V_{PWM2} \geq 9V$

In this case all other functions are the same as in active mode

Watchdog can be disabled as well as soon as L9952GXP enters the V1 standby mode (see section 2.9 for details)

Note: "High" level for flash mode selection is $V_{PWM2} \geq 9V$. For all other operation modes, standard 5V logic signals are required. For proper operation PWM1 must not be set to a voltage level above standard 5V logic.

2.2.3 V_1 standby mode

Outputs and internal loads are switched off. To supply the micro controller in a low power mode, the voltage regulator1 (V1) remains active. The intention of the V1 standby mode is to preserve the RAM contents. A cyclic contact supply and wake-up input sense feature (for cyclic monitoring of external contacts) can be activated by SPI.

2.2.4 V_{BAT} standby mode

To achieve minimum current consumption during V_{BAT} standby mode, all L9952GXP functions (except the ones for wake up functionality) are switched off.

In V_{BAT} - standby mode the current consumption of the L9952GXP is reduced to 7µA, typical (without cyclic sense feature selected).

The transitions from active mode to either V_1-standby or V_{BAT} - standby are controlled by SPI.

V_{BAT} - standby mode is dominant; i.e. if both bits, V_1 - standby and V_{BAT} - standby are set to "1", the L9952GXP will enter V_{BAT} - standby mode.

2.3 Wake up events

A wake-up from standby mode will switch the device to active mode. This can be initiated by one or more of the following sources:

- Change of the LIN state at LIN bus interfaces
- A current at the INH pin (I ≥200uA) controlled by the CAN-transceiver (the CAN transceiver is not a part of the IC).
- Positive/negative edge at wake up pins WU1...WU4 -> change of level after going into stand-by
- Change of open-load state at OUT1 to 4
- SPI access in V1-standby mode (CSN is low and first rising edge on CLK)

Table 3. Wake up events

Wake up source	Description
LIN	Always active
INH	Always active
WU1...4	Can be individually disabled via SPI
Open Load at HS outputs	Can be individually disabled via SPI
SPI Access	Always active (except in V_{BAT} - standby mode)
High level at PWM2 input	VPWM2 > 9V (1)

1. Only if internal oscillator is running (e. g. in cyclic sense configuration or after wake-up request).

All wake-up events (except wake-up by LIN, INH or SPI from V1standby mode) generate a Reset pulse (NReset low for 2ms).

Wake-up events from V1standby by LIN, INH or SPI do not cause a Reset and the Reset generation is blocked for 2ms, i. e. a watchdog failure during this timeframe will not cause a reset.

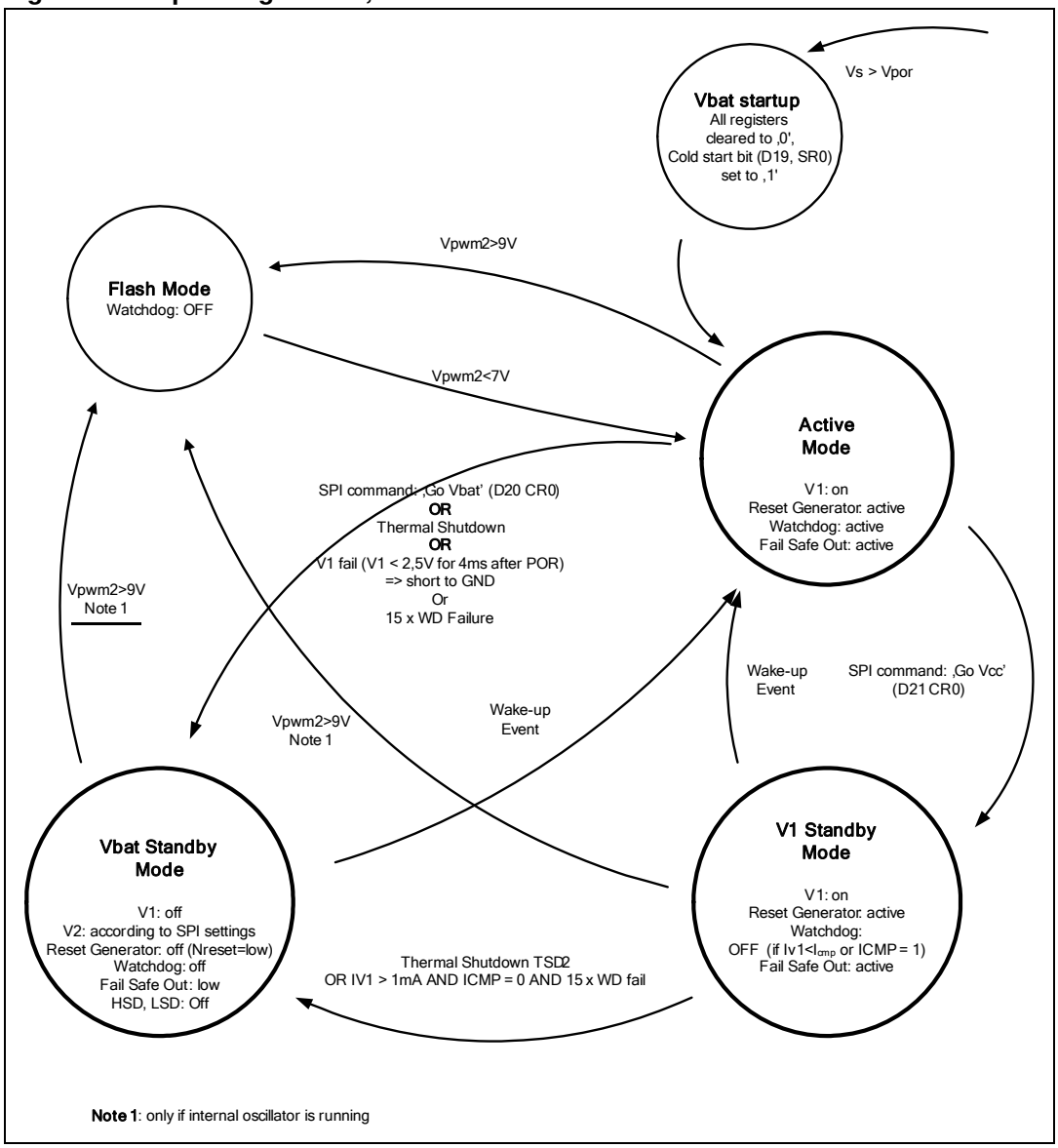
2.4 Functional overview (truth table)

Table 4. Functional overview (truth table)

	Function	Comments	Operating modes		
			Active mode	V_1-standby static mode (cyclic sense)	V_{BAT}-standby static mode (cyclic sense)
2.3.1	Voltage-regulator, V1	VOUT= 5V	On	On (1)	Off
2.3.2	Voltage-regulator, V2	VOUT= 5V	On / Off (2)	On (2) / Off	On (2) / Off
2.3.3	Reset-generator		On	On	Off
2.3.4	Window watchdog	V_1 monitor	On	Off if (I_V1 < I_{CMP} and I_{CMP}=0) or I_{CMP} = 1	Off
2.3.5	Wake up		Off (3)	Active (4)	Active (4)
2.3.6	HS-cyclic supply	Oscillator timebase	On / Off	On (2) / Off	On (2) / Off
2.3.7	Relay driver		On	Off	Off
2.3.8	Operational amplifiers		On	Off	Off
2.3.9	LIN line driver	LIN 2.1	On	Off	Off
2.3.10	LIN line receiver		On	On	On
2.3.11	FSO	Fail-safe output	Hi – no error Lo – WD or V1 fail	Hi – no error Lo – WD or V1 fail (5)	Lo -> because V1= off
2.3.12	Oscillator		On	(6)	(6)
2.3.13	Vs-Monitor		On	(7)	(7)

1. Supply the processor in low current mode
2. Only active when selected via SPI
3. Input Status can be read by SPI (Status Register 0); Inputs should be configured for static sense (Control Register 2)
4. Unless disabled by SPI
5. Watchdog is active in V1 standby mode, until I(V1) is below I_{CMP} current threshold
6. Activation = ON if cyclic sense is selected
7. Cyclic activation = pulsed ON during cyclic sense

Figure 3. Operating modes, main states



2.5 Wake up inputs

The de-bounced digital inputs WU1...WU4 can be used to wake up the L9952GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 µs is implemented at WU1-4. The filter is started when the input voltage passes the specified threshold. At Vin > 1V and Vin < (Vs – 2V), a Wake-up request is processed. During Wake-up request, the internal oscillator and other circuit blocks are activated in order to allow more accurate monitoring of the inputs.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic wake up feature is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer 1 (0.5sec to 4.0sec in 0.5sec steps) or Timer 2 (50ms). The input signal is filtered with a filter time of 16us after a programmable delay (80us or 800us). A Wake-up will be processed if the status has changed versus the previous cycle.

The Outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timing according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode (Icxx in control register 2), the same input filter timing (Timer1 or Timer2) and the corresponding input filter delay (control register 2) must be used for the HS Outputs (Hsxx in control register 0) which supply the external contact switches.

In Standby mode, the inputs WU1-4 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external contacts (pull-up for active low contacts, pull-down for active high contacts). In active mode the inputs have a pull down resistor of 100 kOhm (typ).

In Active mode, the input status can be read by SPI (Status Register 0). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

2.6 Hall sensor ports: WU3,4, Dig_Out 3,4

Applications like Hall sensor outputs need high processing speed. The 12V signals connected to the wakeup inputs WU3 and WU4 can be looped through to the digital outputs Dig_Out 3 and Dig_Out 4 (5V) in order to avoid read out of the input state by SPI.

The setup is programmable by SPI.

The open load states of the High Side Drivers OUT1 and OUT2 can be looped through the digital outputs Dig_Out3 and Dig_Out4 without delay. In addition, the status of OUT1 and OUT2 can be accessed through the SPI interface. This feature is intended for 2-pin HALL sensors. Open Load information is only valid during ON state.

The Open Load threshold at pins OUT1...4 can be switched from I_{OLD1} = 2mA to

I_{OLD2} = 8 mA via SPI .

2.7 Interrupt

Dig_Out4 can be configured via SPI as Interrupt output (INT) by setting Bit 20 / CR1:INT_enable='1'.

This configuration will enable the following behaviour:

- INT pin is pulled high for 2ms in case of any wake-up from V1 standby mode (WU inputs, LIN, INH, SPI, open load HS, Iv1 > I_{CMP}_ris)
- Wake-up events from V1 standby do not generate a reset (i.e. NRESET is not pulled low)
- The Dig_Out4 settings in CR1 (Bits 12..14) will be ignored

2.8 Cyclic contact supply

In V1 and V_{BAT} standby mode, any high side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X sec, the on-time is 10ms resp. 20ms

With X ∈ {0.5, 1.0, 1.5, ... 4 }

Timer 2: period is 50ms, the on- time is 100us resp. 1ms:

Note: Cyclic sense setup: if cyclic sense feature is used for wake-up inputs (Icxx in control register 2), same input filter timing (Timer1 or Timer2) must be used for HS Outputs (Hsxx in control register 0).

2.9 Window – watchdog

During normal operation the watchdog monitors the micro controller within a nominal trigger cycle of 10ms.

In V_{BAT} -standby , V1-standby and Flash program modes, the watchdog circuit is automatically disabled. However, the watchdog will remain enabled in V1-standby mode until the current at V1 decreases below I_{CMP}_fall. The V1 current monitoring can be disabled, if the I_{CMP} bit (CR2, D20) is set to '1'.

After 'power-on', 'standby mode' or reset, the window watchdog starts with a long open window (65ms). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is finally accepted when the CSN input becomes HIGH after the transmission of the SPI word.

A correct watchdog trigger will start the window watchdog with a closed window (< 6ms) followed by an open window (< 10ms), see timing diagrams. Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit (CR0, D19). The "negative" or "positive" edge has to meet the open window time. A correct watchdog trigger signal will immediately start the next closed window.

After 8 watchdog failures in sequence, the V1 regulator is switched off for 200ms. In case of 7 further watchdog failures, the V1 regulator is completely turned off and the device goes into V_{BAT} standby mode until a wakeup occurs. (e.g. via LIN, CAN/INH).

The watchdog is triggered by toggling the trigger bit (CR0, D19).

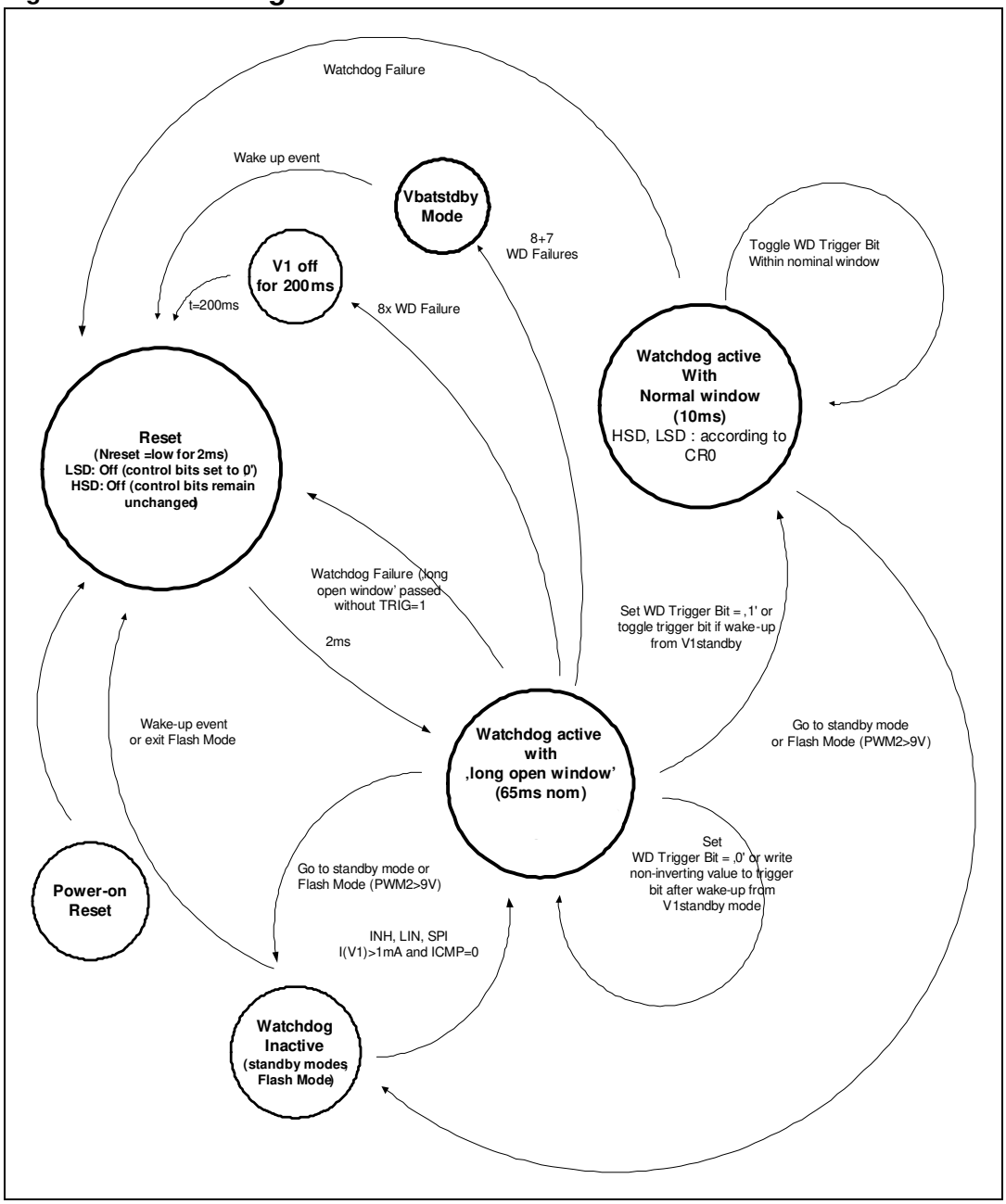
Note: The active trigger window will be reset after each correct trigger write operation.

In case of reset (NReset low for 2ms) the trigger bit is set to "0".

In case of a WD failure, the outputs (Lsx, Hsx, V2) are switched off and NReset is pulled low for 2ms.

Writing to control register 0 without inverting the WD trigger bit is possible at any time.

Figure 4. Watchdog



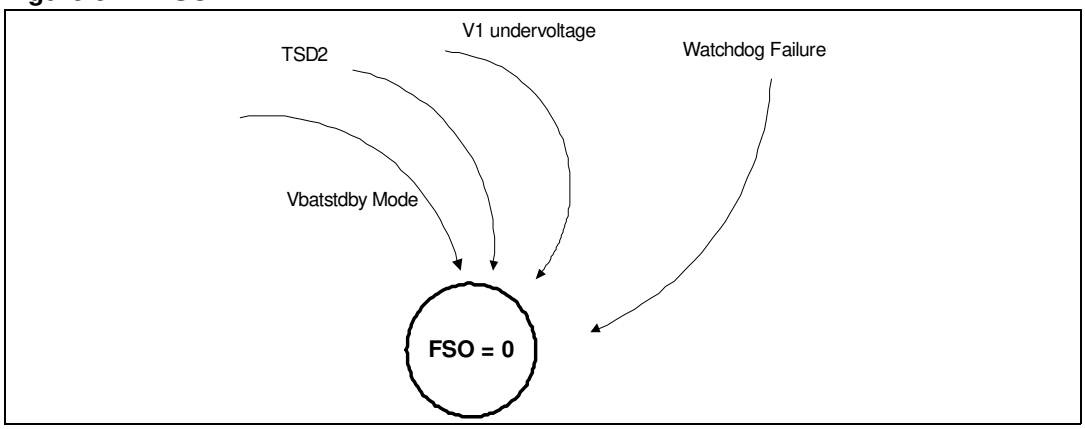
2.10 Fail safe output

After power-on (Vs > V_{POR}) or wakeup from V_{BAT} -standby mode, the output FSO is set to “HIGH”, if V1 is above the V1 threshold. FSO is set to “LOW” in case of V1 under voltage or watchdog failure.

During V1-standby mode, FSO is HIGH unless a V1 under-voltage or watchdog reset occurs. WD remains enabled in V1 standby mode until I_{V1} drops below 150uA. In V_{BAT} - standby mode, FSO is low. At exit from V_{BAT} - standby mode, it goes to high as soon as V1 is stable.

At wakeup FSO remains high, provided that the watchdog is triggered successfully. It is set low if the watchdog is not served during the long open window of if a V1 under-voltage occurs.

Figure 5. FSO

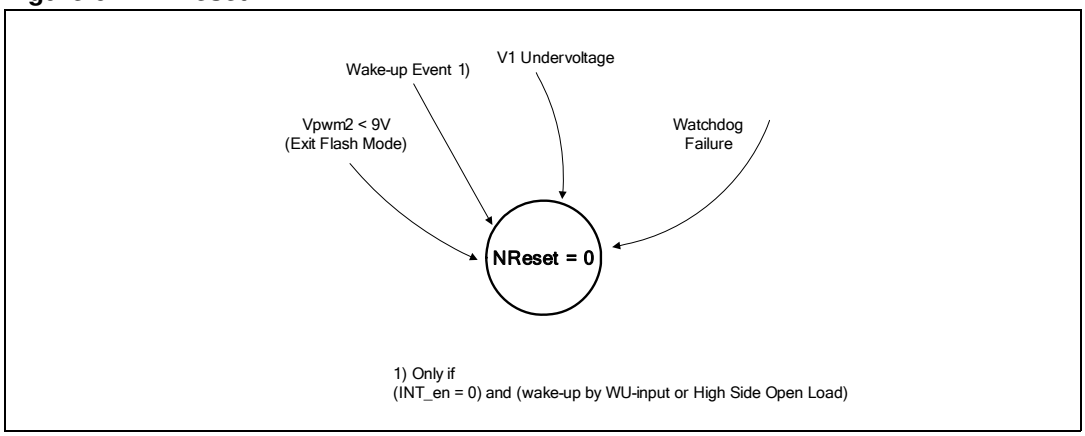


2.11 Reset – generator

IF V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output “NRESET” is switched to “HIGH” after a 2ms reset delay time. This is necessary for a defined start of the micro controller when the application is switched on.

As soon as an under voltage condition of the output voltage (V1 < VRT) for more than 8us appears, the reset output is switched low again.

Figure 6. NReset



2.12 V1, V2 fail

The $V_{1,}$ and V_2 regulator output voltages are monitored.

In case of a drop below the $V_{1,}$ V_2 – fail thresholds ($V_{1,2}$ < 2V,typ for t > 2us), the $V_{1,2}$ - fail bits are latched. The fail bits are cleared by a dedicated SPI command.

If 4ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for V1,2), the L9952GXP will identify a short circuit condition at the related regulator output and the regulator will be switched off.

In case of a V1 failure the device enters V_{BAT} - standby mode automatically.

In case of a V2 failure the SHT5V2 bit (SR0 Bit12) is set.

2.13 Low side driver outputs Rel1, Rel2

The outputs Rel1, Rel2 (R_{DSon} = 2 Ω typ. @25 °C) are specially designed to drive relay loads.

Typical relays used have the following characteristics:

Relay type 1:

- closed armature: R = 160 Ω ±10%, L= 300mH
- open armature: R = 160 Ω ±10%, L= 240mH

Relay type 2:

- closed armature: R= 220 Ω ±10%, L= 420mH
- open armature: R= 220 Ω ±10%, L= 330mH

The outputs provide an active output zener clamping (40V) feature for the demagnetisation of the relay coil, even though a load dump condition exists. In case of watchdog failure the relay drivers will be switched off and the low side driver control bits are cleared.

Note: 1 Due to relays bouncing, high dV/dt and/or dI/dt transients may occur on the low side driver outputs. In case high currents are switched (for example window lift motor), due to parasitic capacitive inductive coupling from load side of relays to the relays coils, the Absolute Maximum Ratings of the Low Side driver outputs may be exceeded. In order to avoid this, it is recommended to place a 10nF capacitor at the Rel1, Rel2 outputs to GND.

2 If a hard short circuit to V_{BAT} is possible at the "Low Side Driver" outputs, an RC network is required with T_{RC} > 1µs, R ≥ 1 Ω (see block diagram, the value is given for an output short circuit of given di/dt = 5A/µs).

2.14 PWM inputs

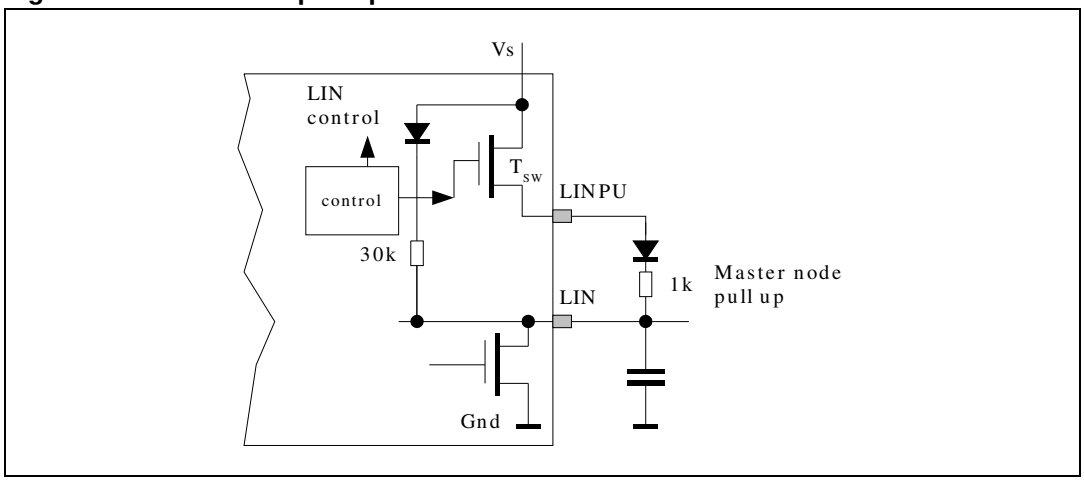
The inputs PWM 1,2 can be used to control the output drivers Out1..4 and OUT_HS with a PWM signal. Each PWM input can be mapped individually to each of the above listed outputs according to the SPI settings.

2.15 Operational amplifiers

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes - 0.2 ... 3V.

The operational amplifiers are designed for GND + 3V... GND – 0.2V input voltage swing and rail-to-rail output voltage range. All Pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.

Figure 7. Lin master pull up



A dedicated built-in switch “Tsw” enables the LIN to act as a master. (see chapter 2.18)

2.16 LIN bus interface

General requirements:

- Speed communication up to 20kbit/s
- LIN 2.0 compliant (SAEJ2602 compatible) transceiver
- Function range from +40V to -18V DC at LIN Pin
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller Interface with CMOS compatible I/O pins.
- Pull up resistor internal.
- ESD: immunity against automotive transients per ISO7637 specification (see application note)
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

2.17 Error handling

The L9952GXP provides the following 3 error handling features which are not described in the LIN Spec. V2.1, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

2.17.1 Dominant TxD time out

If TXI is in dominant state (low) for more than 12ms (typ) the transmitter will be disabled until TXI becomes recessive (high). This feature can be disabled via SPI.

2.17.2 Short to battery time out

If TXI changes to dominant (low) state but RXI signal does not follow within 40µs, the transmitter will be disabled until TXI becomes recessive (high).

2.17.3 Short to ground mode

A wake up caused by a message on the bus will start the voltage regulator and the micro controller to switch the application back to normal operation mode.

2.18 Wake up (from LIN)

In standby mode the L9952GXP can receive a wake up from LIN bus. For the wake up feature the L9952GXP logic differentiates two different conditions.

2.18.1 Normal wake up

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for at least 40µs, will switch the L9952GXP to active mode.

2.18.2 Wake up from short to GND condition

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for at least 40us, will switch the L9952GXP to active mode.

2.18.3 RxD pin in V1 standby

In V1 standby condition the RxD is a tristate pin.

2.19 LINPU

The LINPU (LIN pull up) signal is set by L9952GXP logic in order to drive the LIN transceiver in master mode. The master mode is realized by an internal high side switch and an external diode in series with an external 1k resistor. In master mode the high side switch is closed causing an external pull up path in parallel to the internal one (diode & 30k resistor).

HS (high side) characteristics:

- HS does not have an over current protection.
- The HS remains active in standby mode.
- Switch off only in case of over temperature (TSD2 = thermal shutdown #2).
- Typical R_{DSon}, 10 Ω.

The Linpu is activated by default (LIN master mode) and can be switched off with a SPI command (see register 2) to reduce current in case of LIN shorted to ground.

2.20 Serial Peripheral Interface (SPI)

A 24 bit SPI command (2 adresses + 22 data bits) is used for bi-directional communication with the micro controller.

During active mode, the SPI:

1) triggers the watchdog

2) controls the modes and status of all L9952GXP modules (incl. input and output drivers)

3) provides driver output diagnostic

4) provide L9952 diagnostic (incl. over temperature warning, L9952GXP operation status)

Note: During stand-by modes, the SPI is generally deactivated.

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL=0 and CPHA=0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the global error flag (fault condition) of the device which is a logical -"OR" of all over current, Vs-over / under voltage, temperature warning/shutdown and V1 Fail bits. The micro controller can poll the status of the device without the need of a full SPI-communication cycle.

2.20.1 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

2.20.2 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

2.20.3 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

2.20.4 Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 1MHz.

2.20.5 Data registers

The device has 3 Control registers and 2 Status registers. The first two bits (D22+D23) at the DI-Input are used to select one of the Control registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Control register only if a frame of exact 24 bits is detected. If the Control register 1 is selected for data transfer, the Status register 1 will be transferred to the DO during the current communication frame. For the selection of Control register 0 or Control register 2, the Status register 0 is transferred to DO.

3 Protection and diagnosis

3.1 Power supply fail

Over and under-voltage detection on Vs.

3.1.1 Over voltage

If the supply voltage Vs reaches the over voltage threshold (V_{SOV})

- The outputs HS1..4, OUT_HS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The over voltage bit is set and can be cleared with the clear bit (CR1,CLR)
- Automatic recovery after Vs over-voltage; selectable via SPI (CR2, bit4)

3.1.2 Under voltage

If the supply voltage Vs drops below the under voltage threshold voltage(V_{SUV})

- The outputs HS1..4, OUTHS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The under voltage bit is set
- Automatic recovery after Vs under-voltage; selectable via SPI (CR2, bit4)

3.2 Temperature warning and thermal shutdown

See state chart: " Protection and diagnosis".

3.3 SPI diagnosis

Digital diagnosis features are provided by SPI:

- V1 reset threshold programmable
- Over temperature including pre warning
- Open load separately for each output stage
- Overload status
- Vs-supply over/under voltage
- V1 and V2 fail bit
- Status of the WU1...4, LIN and INH pin
- Cold start bit
- Number of unsuccessful V1 restarts after thermal shutdown
- Number of sequential watchdog failures
- Status of watchdog trigger bit TRIG: (SR1, Bit 16)
- LIN status (short to ground, short to V_{BAT}, dominant TxD)

See the following state chart: "Protection and diagnosis".