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### Features

- Three half bridges for 0.75 A loads ( $R_{DSon} = 1600 \text{ m}\Omega$ )
- Two configurable high-side driver for up to 1.5A load ( $R_{DSon} = 500 \text{ m}\Omega$ ) or 0.35 A load ( $R_{on} = 1800 \text{ m}\Omega$ )
- One high-side driver for 6 A load ( $R_{DSon} = 100 \text{ m}\Omega$ )
- Programmable soft start function to drive loads with higher inrush currents (i.e. current > 6 A, current > 1.5 A)
- Very low current consumption in standby mode ( $I_S < 6 \mu\text{A}$  typ;  $T_j \leq 85 \text{ }^\circ\text{C}$ )
- All outputs short circuit protected
- Current monitor output for high-side OUT1, OUT4, OUT5 and OUT6
- All outputs over temperature protected
- Open-load diagnostic for all outputs
- Overload diagnostic for all outputs
- PWM control of all outputs
- Charge pump output for reverse polarity protection



### Applications

- Door actuator driver with bridges for mirror axis control and high-side driver for mirror defroster and two 10 W light bulbs and/or LEDs.

### Description

The L9954LXP is a microcontroller driven multifunctional door actuator driver for automotive applications. Up to two DC motors and three grounded resistive loads can be driven with three half bridges and three high-side drivers. The integrated standard Serial Peripheral Interface (SPI) controls all operation modes (forward, reverse, brake and high impedance). All diagnostic information is available via SPI.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L9954LXP	L9954LXPTR

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# 1 Block diagram and pin description

Figure 1. Block diagram

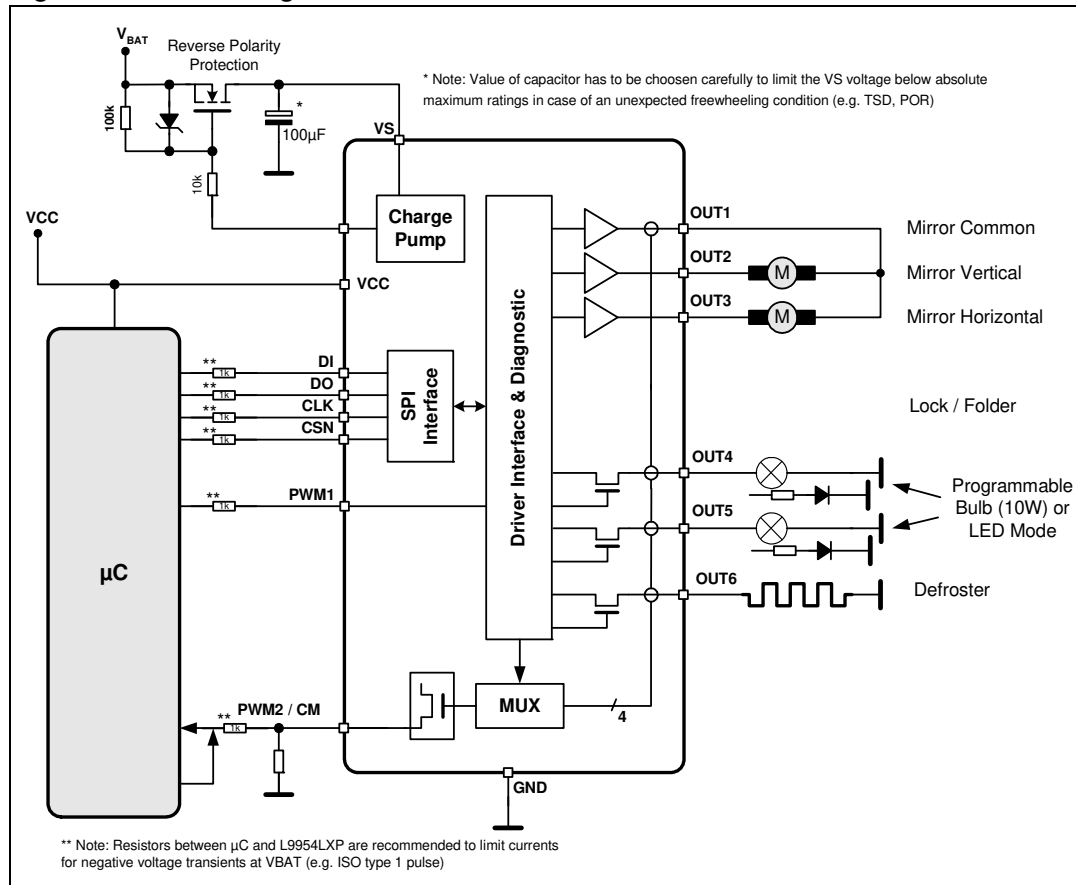


Figure 2. Configuration diagram (top view)

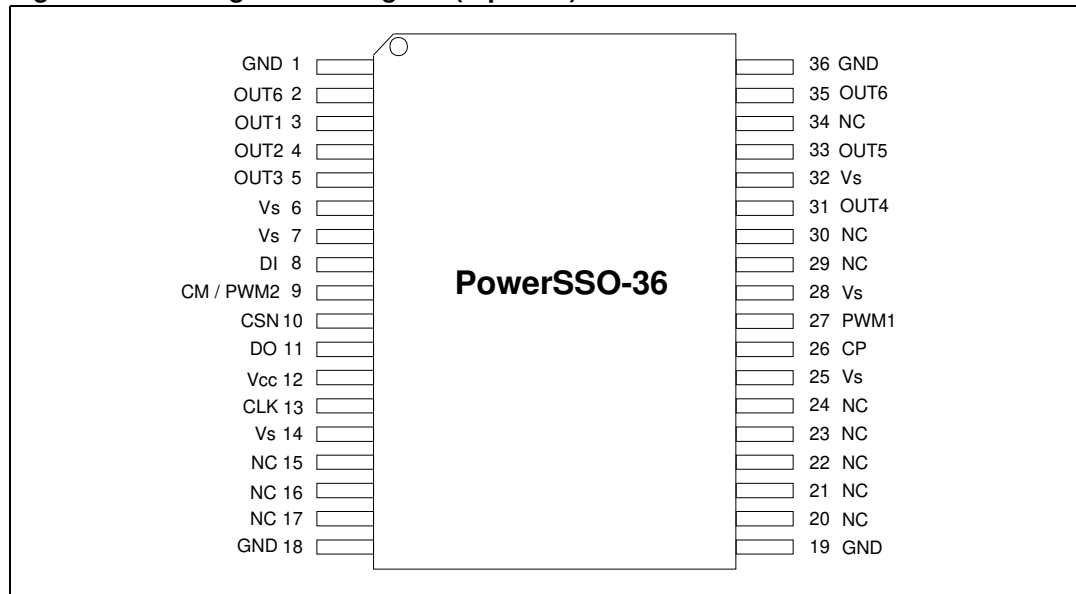


Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground: reference potential. Important: for the capability of driving the full current at the outputs all pins of GND must be externally connected.
2, 35	OUT6	High-side driver output 6 The output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to $V_S$ (bulk-drain-diode). The output is over-current and open-load protected. Important: for the capability of driving the full current at the outputs both pins of OUT6 must be externally connected.
3 4 5	OUT1 OUT2 OUT3	Half-bridge output 1,2,3 The output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to $V_S$ , switches driver from GND to output). This output is over-current and open-load protected.
6, 7, 14, 25, 28, 32	$V_S$	Power supply voltage (external reverse protection required) For this input a ceramic capacitor as close as possible to GND is recommended. Important: for the capability of driving the full current at the outputs all pins of $V_S$ must be externally connected.
8	DI	Serial data input The input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 24bit control word and the least significant bit (LSB, bit 0) is transferred first.
9	CM/PWM2	Current monitor output/PWM2 input Depending on the selected multiplexer bits of input data register this output sources an image of the instant current through the corresponding high-side driver with a ratio of 1/10.000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the output OUT5.
10	CSN	Chip select not input This input is low active and requires CMOS logic levels. The serial data transfer between L9954LXP and micro controller is enabled by pulling the input CSN to low-level.
11	DO	Serial data output The diagnosis data is available via the SPI and this 3-state output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high)



**Table 2. Pin definitions and functions (continued)**

Pin	Symbol	Function
12	V <sub>CC</sub>	Logic supply voltage For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input This input controls the internal shift register of the SPI and requires CMOS logic levels.
26	CP	Charge pump output This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection.
27	PWM1	PWM1 input This input signal can be used to control the drivers OUT1-OUT4 and OUT6 by an external PWM signal.
31 33	OUT4, OUT5	High-side driver output 4 and 5 Each output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. Each high-side driver is a power DMOS transistor with an internal parasitic reverse diode from each output to V <sub>S</sub> (bulk-drain-diode). Each output is over-current and open-load protected.
15, 16, 17, 20, 21, 22, 23, 24, 29, 30, 34	NC	Not connected pins.

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_S$	DC supply voltage	-0.3 to 28	V
	Single pulse $t_{max} < 400$ ms	40	V
$V_{CC}$	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
$V_{DI}, V_{DO}, V_{CLK},$ $V_{CSN}, V_{pwm1}$	Digital input / output voltage	-0.3 to $V_{CC} + 0.3$	V
$V_{CM}$	Current monitor output	-0.3 to $V_{CC} + 0.3$	V
$V_{CP}$	Charge pump output	-25 to $V_S + 11$	V
$I_{OUT1,2,3,4,5}$	Output current	$\pm 5$	A
$I_{OUT6}$	Output current	$\pm 10$	A

### 2.2 ESD protection

**Table 4. ESD protection**

Parameter	Value	Unit
All pins	$\pm 2$ <sup>(1)</sup>	kV
Output pins: OUT1 - OUT6	$\pm 8$ <sup>(2)</sup>	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.

2. HBM with all unzapped pins grounded.

### 2.3 Thermal data

**Table 5. Operating junction temperature**

Symbol	Parameter	Value	Unit
$T_j$	Operating junction temperature	-40 to 150	°C

**Table 6. Temperature warning and thermal shutdown**

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ On}$	Temperature warning threshold junction temperature	$T_j$	130		150	°C
$T_{jSD\ On}$	Thermal shutdown threshold junction temperature	$T_j$ increasing			170	°C
$T_{jSD\ Off}$	Thermal shutdown threshold junction temperature	$T_j$ decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

## 2.4 Electrical characteristics

Values specified in this section are for  $V_S = 8$  to  $16$  V,  $V_{CC} = 4.5$  to  $5.3$  V,  $T_j = -40$  to  $150$  °C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

**Table 7. Supply**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S$	Operating supply voltage range		7		28	V
$I_S$	$V_S$ DC supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V active mode OUT1 - OUT6 floating		7	20	mA
	$V_S$ quiescent supply current	$V_S = 16$ V, $V_{CC} = 0$ V standby mode OUT1 - OUT6 floating $T_{test} = -40$ °C, $25$ °C		4	12	µA
		$T_{test} = 85$ °C <sup>(1)</sup>		6	25	µA
$I_{CC}$	$V_{CC}$ DC supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V CSN = $V_{CC}$ , active mode		1	3	mA
	$V_{CC}$ quiescent supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V CSN = $V_{CC}$ standby mode OUT1 - OUT6 floating		25	50	µA
$I_S + I_{CC}$	Sum quiescent supply current	$V_S = 16$ V, $V_{CC} = 5.3$ V CSN = $V_{CC}$ standby mode OUT1 - OUT6 floating $T_{test} = 130$ °C		50	200	µA

1. Guaranteed by design.

**Table 8. Overvoltage and under voltage detection**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ On}$	$V_S$ UV-threshold voltage	$V_S$ increasing	5.7		7.2	V
$V_{SUV\ Off}$	$V_S$ UV-threshold voltage	$V_S$ decreasing	5.5		6.9	V
$V_{SUV\ hyst}$	$V_S$ UV-hysteresis	$V_{SUV\ On} - V_{SUV\ Off}$		0.5		V
$V_{SOV\ Off}$	$V_S$ OV-threshold voltage	$V_S$ increasing	18		24.5	V
$V_{SOV\ On}$	$V_S$ OV-threshold voltage	$V_S$ decreasing	17.5		23.5	V
$V_{SOV\ hyst}$	$V_S$ OV-hysteresis	$V_{SOV\ Off} - V_{SOV\ On}$		1		V
$V_{POR\ Off}$	Power-on reset threshold	$V_{CC}$ increasing			4.4	V
$V_{POR\ On}$	Power-on reset threshold	$V_{CC}$ decreasing	3.1			V
$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ Off} - V_{POR\ On}$		0.3		V

**Table 9. Current monitor output**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CM}$	Functional voltage range	$V_{CC} = 5\text{ V}$	0		4	V
$I_{CM,r}$	Current monitor output ratio: $I_{CM} / I_{OUT6}$	$0\text{ V} \leq V_{CM} \leq 4\text{ V},$ $V_{CC} = 5\text{ V}$		$\frac{1}{10000}$		-
	Current monitor output ratio: $I_{CM} / I_{OUT1}$			$\frac{1}{3800}$		
	Current monitor output ratio: $I_{CM} / I_{OUT4,5}$ low $R_{DSon}$ mode			$\frac{1}{10200}$		
	Current monitor output ratio: $I_{CM} / I_{OUT4,5}$ high $R_{DSon}$ mode			$\frac{1}{2400}$		

**Table 9. Current monitor output (continued)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{CM\ acc}$	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 8}$	$0\ V \leq V_{CM} \leq 3.8\ V$ , $V_{CC} = 5\ V$ , $I_{Out,min\ 8} = 0.5\ A$ , $I_{Out\ max\ 8} = 5.9\ A$				
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 1}$	$0\ V \leq V_{CM} \leq 3.8\ V$ , $V_{CC} = 5\ V$ , $I_{Out,min\ 1} = 60\ mA$ , $I_{Out\ max\ 1} = 0.6\ A$				
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 4,5}$ high $R_{DSon}$ mode	$0\ V \leq V_{CM} \leq 3.8\ V$ , $V_{CC} = 5\ V$ , $I_{Out,min\ 4,5} = 30\ mA$ , $I_{Out\ max\ 4,5} = 300\ mA$		4% + 1%FS	8% + 2%FS	-
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 4,5}$ low $R_{DSon}$ mode	$0\ V \leq V_{CM} \leq 3.8\ V$ , $V_{CC} = 5\ V$ , $I_{Out,min\ 4,5} = 150\ mA$ , $I_{Out\ max\ 4,5} = 1\ A$				

**Table 10. Charge pump output**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CP}$	Charge pump output voltage	$V_S = 8\ V$ , $I_{CP} = -60\ \mu A$	$V_S+6$		$V_S+13$	V
		$V_S = 10\ V$ , $I_{CP} = -80\ \mu A$	$V_S+8$		$V_S+13$	V
		$V_S \geq 12\ V$ , $I_{CP} = -100\ \mu A$	$V_S+10$		$V_S+13$	V
$I_{CP}$	Charge pump output current	$V_{CP} = V_S + 10\ V$ , $V_S = 13.5\ V$	95	150	300	$\mu A$

**Table 11. OUT1 - OUT6**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DSon\ OUT1}$ , $R_{DSon\ OUT2}$ $R_{DSon\ OUT3}$	On resistance to supply or GND	$V_S = 13.5\ V$ , $T_j = 25\ ^\circ C$ , $I_{OUT1,2,3} = \pm 0.4\ A$		1600	2200	$m\Omega$
		$V_S = 13.5\ V$ , $T_j = 125\ ^\circ C$ , $I_{OUT1,2,3} = \pm 0.4\ A$		2500	3400	$m\Omega$
$R_{DSon\ OUT4}$ , $R_{DSon\ OUT5}$	On resistance to supply in low $R_{DSon}$ mode	$V_S = 13.5\ V$ , $T_j = 25\ ^\circ C$ , $I_{OUT4,5} = -0.8\ A$		500	700	$m\Omega$
		$V_S = 13.5\ V$ , $T_j = 125\ ^\circ C$ , $I_{OUT4,5} = -0.8\ A$		700	950	$m\Omega$
	On resistance in high $R_{DSon}$ mode	$T_j = 25\ ^\circ C$ , $I_{OUT4,5} = -0.2\ A$		2000	2700	$m\Omega$
		$T_j = 125\ ^\circ C$ , $I_{OUT4,5} = -0.2\ A$		3200	4300	$m\Omega$

Table 11. OUT1 - OUT6 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DSon\ OUT6}$	On resistance to supply	$V_S = 13.5\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ , $I_{OUT6} = -3\text{ A}$		100	150	$\text{m}\Omega$
		$V_S = 13.5\text{ V}$ , $T_j = 125\text{ }^\circ\text{C}$ , $I_{OUT6} = -3\text{ A}$		150	200	$\text{m}\Omega$
$I_{OUT1}$ $I_{OUT2}$ $I_{OUT3}$	Output current limitation to GND	Source, $V_S = 13.5\text{ V}$	-1.25		-0.75	A
$I_{OUT1}$ $I_{OUT2}$ $I_{OUT3}$	Output current limitation to supply	Sink, $V_S = 13.5\text{ V}$	0.75		1.25	A
$I_{OUT4}$ $I_{OUT5}$	Output current limitation to GND in low $R_{DSon}$ mode	Source, $V_S = 13.5\text{ V}$	-3.0		-1.5	A
	Output current limitation to GND in high $R_{DSon}$ mode		-0.65		-0.35	A
$I_{OUT6}$	Output current limitation to GND	Source, $V_S = 13.5\text{ V}$	-10.5		-6	A
$t_{d\ On\ H}$	Output delay time, high-side driver on	$V_S = 13.5\text{ V}$ , $R_{load} = (1)$ corresponding low-side driver is not active	10	40	80	$\mu\text{s}$
$t_{d\ Off\ H}$	Output delay time, high-side driver off	$V_S = 13.5\text{ V}$ , $R_{load} = (2)$	15	150	300	$\mu\text{s}$
$t_{d\ On\ L}$	Output delay time, low-side driver on	$V_S = 13.5\text{ V}$ , $R_{load} = (2)$ corresponding high-side driver is not active	15	30	70	$\mu\text{s}$
$t_{d\ Off\ L}$	Output delay time, low-side driver off	$V_S = 13.5\text{ V}$ , $R_{load} = (2)$	20	150	300	$\mu\text{s}$
$t_{d\ HL}$	Cross current protection time, source to sink	$t_{CC\ ONLS\_OFFHS} - t_{d\ Off\ H}^{(2)}$		200	400	$\mu\text{s}$
$t_{d\ LH}$	Cross current protection time, sink to source	$t_{CC\ ONHS\_OFFLS} - t_{d\ Off\ L}^{(2)}$		200	400	$\mu\text{s}$
$I_{QLH}$	Switched-off output current high-side drivers of OUT1-6	$V_{OUT1-6} = 0\text{ V}$ , standby mode	-3	0	-3	$\mu\text{A}$
		$V_{OUT1-2-3-6} = 0\text{ V}$ , active mode	-40	-15	0	$\mu\text{A}$
		$V_{OUT4-5} = 0\text{ V}$ , active mode	-10	-8	0	$\mu\text{A}$
$I_{QLL}$	Switched-off output current low-side drivers of OUT1-3	$V_{OUT1-3} = V_S$ , standby mode	0	80	120	$\mu\text{A}$
		$V_{OUT1-3} = V_S$ , active mode	-40	-15	0	$\mu\text{A}$
$I_{OLD123}$	Open-load detection current of OUT1, OUT2 and OUT3	Source and sink	10	20	30	$\text{mA}$

**Table 11. OUT1 - OUT6 (continued)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I <sub>OLD45</sub>	Open-load detection current of OUT4 and OUT5	Source	15	40	60	mA
	Open-load detection current of OUT4 and OUT5 in high R <sub>DSon</sub> mode		5	10	15	mA
I <sub>OLD6</sub>	Open-load detection current of OUT6	Source	30	150	300	mA
t <sub>d OL</sub>	Minimum duration of open-load condition to set the status bit		500		3000	μs
t <sub>ISC</sub>	Minimum duration of over-current condition to switch off the driver		10		100	μs
f <sub>rec0</sub>	Recovery frequency for OC recovery duty cycle bit=0		1		4	kHz
f <sub>rec1</sub>	Recovery frequency for OC recovery duty cycle bit=1		2		6	kHz
dV <sub>OUT123</sub> /dt dV <sub>OUT45</sub> /dt	Slew rate of OUT <sub>123</sub> and OUT <sub>45</sub>	V <sub>S</sub> = 13.5 V, R <sub>load</sub> = <sup>(2)</sup>	0.1	0.4	0.9	V/μs
dV <sub>OUT6</sub> /dt	Slew rate of OUT <sub>6</sub>	V <sub>S</sub> = 13.5 V, R <sub>load</sub> = <sup>(2)</sup>	0.08	0.2	0.4	V/μs

1. OUT1,2,3 32OHM  
OUT4,5 16OHM  
OUT4,5 high R<sub>DSon</sub> mode 63OHM  
OUT6 4OHM

2. t<sub>CC ON</sub> is the switch On delay time t<sub>d ON</sub> if complement in half bridge has to switch off.

## 2.5 SPI - electrical characteristics

Values specified in this section are V<sub>S</sub> = 8 to 16 V, V<sub>CC</sub> = 4.5 to 5.3 V, T<sub>j</sub> = - 40 to 150 °C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

**Table 12. Delay time from standby to active mode**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t <sub>set</sub>	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	μs

**Table 13. Inputs: CSN, CLK, PWM1/2 and DI**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{inL}$	Input low-level	$V_{CC} = 5\text{ V}$	1.5	2.0		V
$V_{inH}$	Input high-level	$V_{CC} = 5\text{ V}$		3.0	3.5	V
$V_{inHyst}$	Input hysteresis	$V_{CC} = 5\text{ V}$	0.5			V
$I_{CSN\ in}$	Pull up current at input CSN	$V_{CSN} = 3.5\text{ V}, V_{CC} = 5\text{ V}$	-40	-20	-5	$\mu\text{A}$
$I_{CLK\ in}$	Pull down current at input CLK	$V_{CLK} = 1.5\text{ V}$	10	25	50	$\mu\text{A}$
$I_{DI\ in}$	Pull down current at input DI	$V_{DI} = 1.5\text{ V}$	10	25	50	$\mu\text{A}$
$I_{PWM1\ in}$	Pull down current at input PWM1	$V_{PWM} = 1.5\text{ V}$	10	25	50	$\mu\text{A}$
$C_{in}^{(1)}$	Input capacitance at input CSN, CLK, DI and PWM1/2	$0\text{ V} < V_{CC} < 5.3\text{ V}$		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

**Table 14. DI timing <sup>(1)</sup>**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CLK}$	Clock period	$V_{CC} = 5\text{ V}$	1000	-		ns
$t_{CLKH}$	Clock high time	$V_{CC} = 5\text{ V}$	400	-		ns
$t_{CLKL}$	Clock low time	$V_{CC} = 5\text{ V}$	400	-		ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	$V_{CC} = 5\text{ V}$	400	-		ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	$V_{CC} = 5\text{ V}$	400	-		ns
$t_{set\ DI}$	DI setup time	$V_{CC} = 5\text{ V}$	200	-		ns
$t_{hold\ DI}$	DI hold time	$V_{CC} = 5\text{ V}$	200	-		ns
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	$V_{CC} = 5\text{ V}$		-	100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	$V_{CC} = 5\text{ V}$		-	100	ns

1. DI timing parameters tested in production by a passed / failed test:  
 $T_j = -40\text{ }^\circ\text{C} / +25\text{ }^\circ\text{C}$ : SPI communication @ 2 MHz.  
 $T_j = +125\text{ }^\circ\text{C}$ : SPI communication @ 1.25 MHz.

**Table 15. DO**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{DOL}$	Output low-level	$V_{CC} = 5\text{ V}, I_D = -2\text{ mA}$		0.2	0.4	V
$V_{DOH}$	Output high-level	$V_{CC} = 5\text{ V}, I_D = 2\text{ mA}$	$V_{CC} - 0.4$	$V_{CC} - 0.2$		V



**Table 15. DO (continued)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{DOLK}$	3-state leakage current	$V_{CSN} = V_{CC}$ , $0V < V_{DO} < V_{CC}$	-10		10	$\mu A$
$C_{DO}^{(1)}$	3-state input capacitance	$V_{CSN} = V_{CC}$ , $0V < V_{CC} < 5.3V$		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

**Table 16. DO timing**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r DO}$	DO rise time	$C_L = 100 pF$ , $I_{load} = -1 mA$	-	80	140	ns
$t_{f DO}$	DO fall time	$C_L = 100 pF$ , $I_{load} = 1 mA$	-	50	100	ns
$t_{en DO tri L}$	DO enable time from 3-state to low-level	$C_L = 100 pF$ , $I_{load} = 1 mA$ pull up load to $V_{CC}$	-	100	250	ns
$t_{dis DO L tri}$	DO disable time from low-level to 3-state	$C_L = 100 pF$ , $I_{load} = 4 mA$ pull up load to $V_{CC}$	-	380	450	ns
$t_{en DO tri H}$	DO enable time from 3-state to high-level	$C_L = 100 pF$ , $I_{load} = -1 mA$ pull down load to GND	-	100	250	ns
$t_{dis DO H tri}$	DO disable time from high-level to 3-state	$C_L = 100 pF$ , $I_{load} = -4 mA$ pull down load to GND	-	380	450	ns
$t_{d DO}$	DO delay time	$V_{DO} < 0.3 V_{CC}$ , $V_{DO} > 0.7 V_{CC}$ , $C_L = 100 pF$	-	50	250	ns

**Table 17. CSN timing**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI, stb}$	CSN HI time, switching from standby mode	Transfer of SPI command to Input Register	20	-	-	$\mu s$
$t_{CSN\_HI, min}$	CSN HI time, active mode	Transfer of SPI command to input register	4	-	-	$\mu s$

Figure 3. SPI - transfer timing diagram

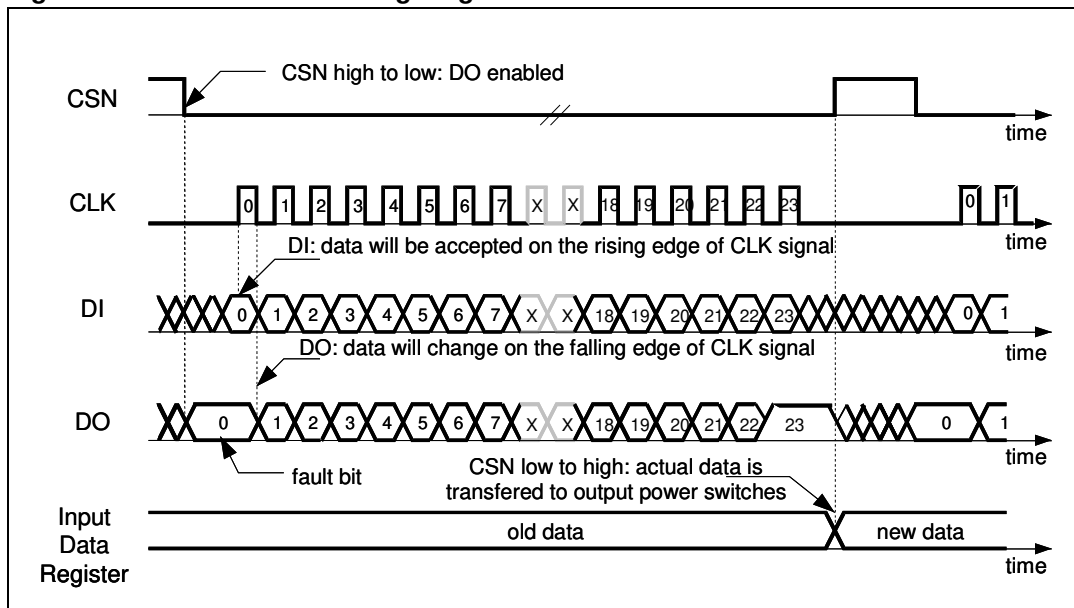
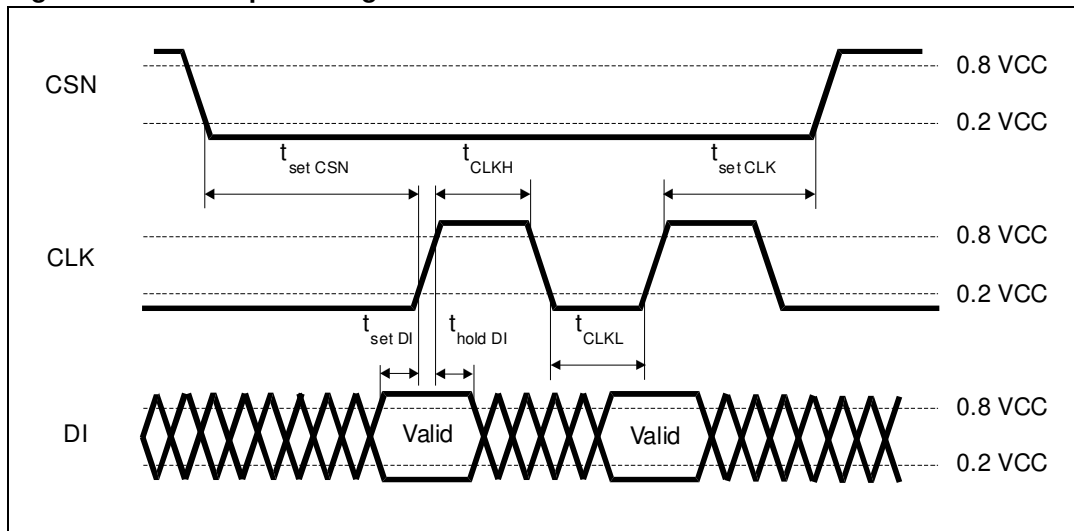
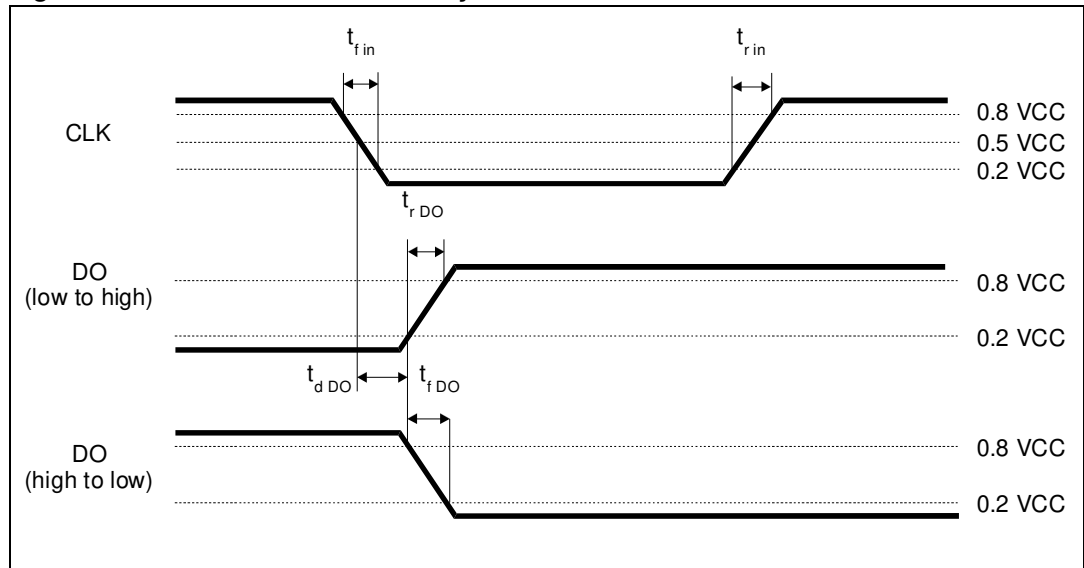


Figure 4. SPI - input timing



**Figure 5. SPI - DO valid data delay time and valid time**



**Figure 6. SPI - DO enable and disable time**

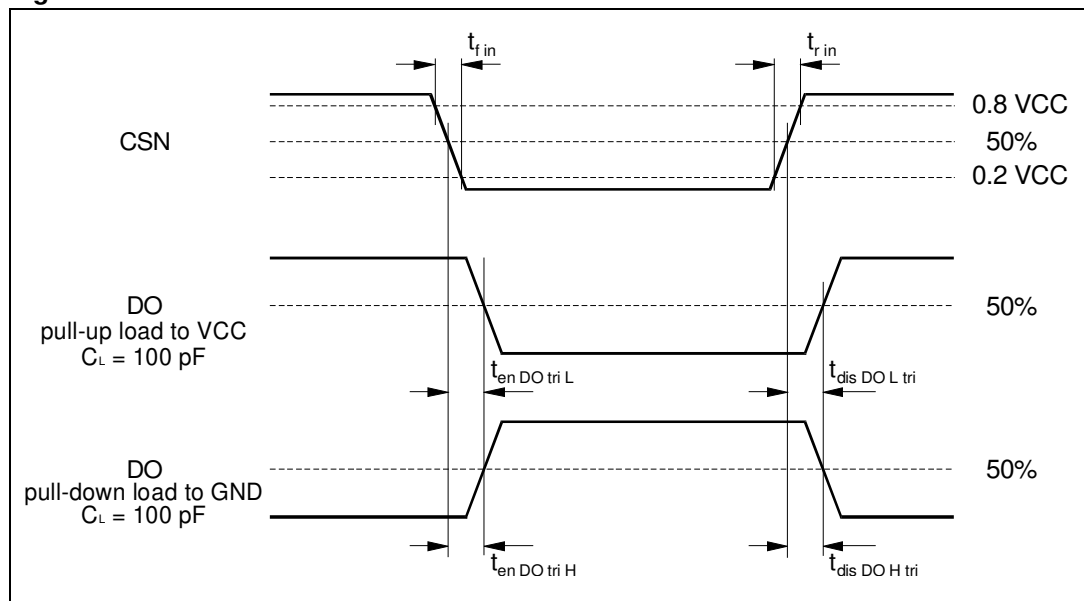


Figure 7. SPI - driver turn-on / off timing, minimum CSN HI time

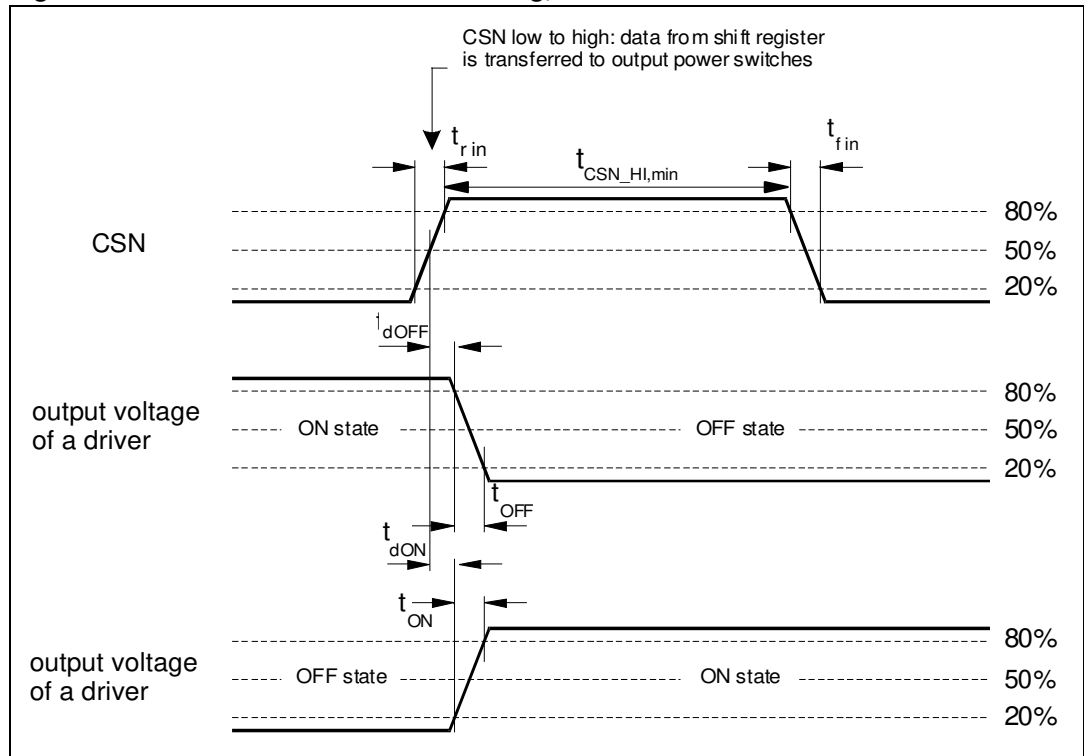
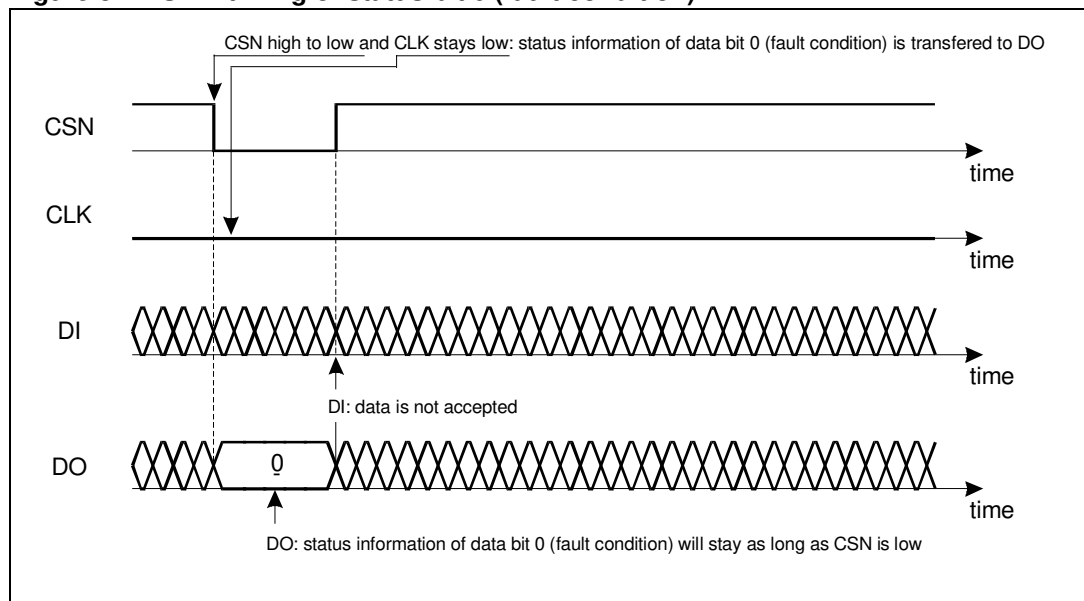


Figure 8. SPI - timing of status bit 0 (fault condition)



## 3 Application information

### 3.1 Dual power supply: $V_S$ and $V_{CC}$

The power supply voltage  $V_S$  supplies the half bridges and the high-side drivers. An internal charge-pump is used to drive the high-side switches. The logic supply voltage  $V_{CC}$  (stabilized 5 V) is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information not are lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on ( $V_{CC}$  increases from under voltage to  $V_{POR\ Off} = 4.2$  V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage  $V_{CC}$  decreases under the minimum threshold ( $V_{POR\ ON} = 3.4$  V), the outputs are switched to 3-state (high impedance) and the status registers are cleared.

### 3.2 Standby mode

The standby mode of the L9954LXP is activated by clearing the bit 23 of the input data register 0. All latched data is cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at  $V_S$  ( $V_{CC}$ ) is less than 6  $\mu$ A (50 $\mu$ A) for CSN = high (DO in 3-state). By switching the  $V_{CC}$  voltage a very low quiescent current can be achieved. If bit 23 is set, the device is switched to active mode.

### 3.3 Inductive loads

Each half bridge is built by an internally connected high-side and a low-side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT3 without external free-wheeling diodes. The high-side drivers OUT4 to OUT6 are intended to drive resistive loads. Hence only a limited energy ( $E < 1$  mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads ( $L > 100$   $\mu$ H) an external free-wheeling diode connected to GND and the corresponding output is needed.

### 3.4 Diagnostic functions

All diagnostic functions (over/open-load, power supply over-/under voltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 32  $\mu$ s (open-load: 1 ms, respectively) before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. Open-load and temperature warning function are intended for information purpose and not changes the state of the output drivers. On contrary, the overload condition disables the corresponding driver (over-current) and overtemperature switches off all drivers (thermal shutdown). Without setting the over-current recovery bits in the input data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

### 3.5 Overvoltage and under voltage detection

If the power supply voltage  $V_S$  rises above the overvoltage threshold  $V_{SOV\ Off}$  (typical 21 V), the outputs OUT1 to OUT6 are switched to high impedance state to protect the load. When the voltage  $V_S$  drops below the under voltage threshold  $V_{SUVOff}$  (UV-switch-off voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage  $V_S$  recovers (register 0: bit 20=0) to normal operating voltage the outputs stages return to the programmed state after at least 32  $\mu$ s.

If the under voltage/overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers. It is strongly recommended to set bit 20 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

### 3.6 Charge pump

The charge pump runs under all conditions in normal mode. In standby the charge pump is out of action.

### 3.7 Temperature warning and thermal shutdown

If junction temperature rises above  $T_{j\ TW}$  a temperature warning flag is set after at least 32  $\mu$ s and is detectable via the SPI. If junction temperature increases above the second threshold  $T_{j\ SD}$ , the thermal shutdown bit is set and power DMOS transistors of all output stages are switched off to protect the device after at least 32  $\mu$ s. Temperature warning flag and thermal shutdown bit are latched and must be cleared by the microcontroller. The related bit is only cleared if the temperature decreases below the trigger temperature. If the thermal shutdown bit has been cleared the output stages are reactivated.

### 3.8 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least 1 ms ( $t_{dOL}$ ) the corresponding open-load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical/electrical state of the loads.

### 3.9 Overload detection

In case of an over-current condition a flag is set in the status register in the same way as open-load detection. If the over-current signal is valid for at least  $t_{ISC} = 32 \mu$ s, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero the microcontroller has to clear the status bits to reactivate the corresponding driver.

### 3.10 Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/10000) of the instantaneous current of the selected high-side driver. Signal at output CM is blanked after switching on of driver until correct settlement of circuitry (at least for 32  $\mu$ s).

The bits 18 and 19 of the input data register 0 control which of the outputs OUT1, OUT4, OUT5 and OUT6 is multiplexed to the current monitor output. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to regulate the power of the defroster more precise by measuring the load current. The current monitor output is bidirectional (c.f. PWM inputs).

### 3.11 PWM inputs

Each driver has a corresponding PWM enable bit which can be programmed by the SPI interface. If the PWM enable bit in Input data register 1 is set, the output is controlled by the logically AND-combination of the PWM signal and the output control bit in input data register 0. The outputs OUT1-OUT4 and OUT6 are controlled by the PWM1 input and the output OUT5 is controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals.

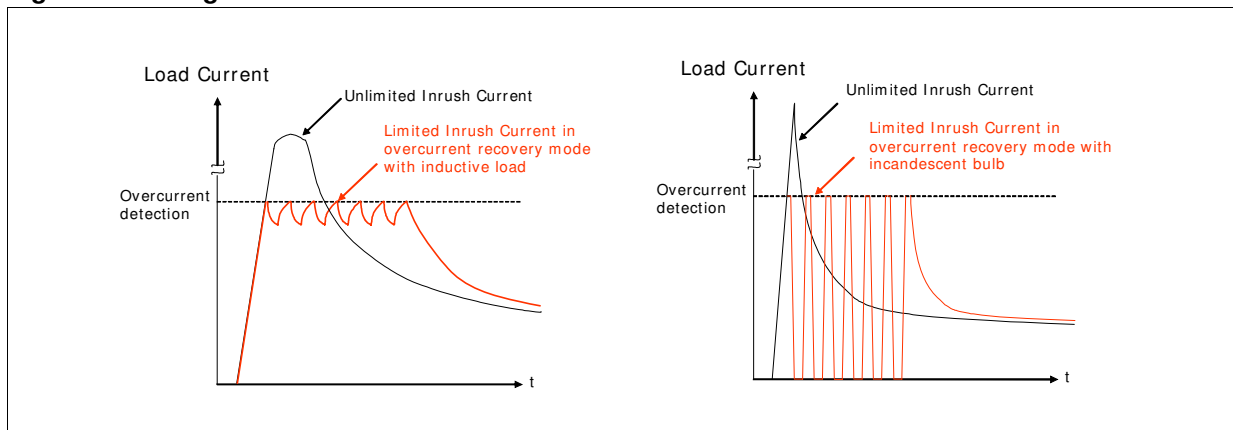
### 3.12 Cross-current protection

The three half-bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge is automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver starts to conduct.

### 3.13 Programmable soft start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable soft start function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device switches automatically on the outputs again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to be about 15 %...25 %. The PWM modulated current provides sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.5 kHz or 3 kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch on light bulbs by setting the over-current recovery bit for the first 50ms. After clearing the recovery bit the output is automatically disabled if the overload condition still exists.

Figure 9. Programmable soft start function for inductive loads and incandescent bulbs





## 4 Functional description of the SPI

### 4.1 Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a build-in SPI. Only three CMOS compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin reflects the status bit 0 (fault condition) of the device which is a logical-or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI communication cycle.

*Note: In contrast to the SPI standard the least significant bit (LSB) is transferred first (see Figure 3).*

### 4.2 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN is called a communication frame.

### 4.3 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to data input register. The writing to the selected data input register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

*Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.*

### 4.4 Serial Data Out (DO)

The data output driver is activated by a logical low-level at the CSN input and goes from high impedance to a low or high-level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

## 4.5 Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal.

## 4.6 Input Data Register

The device has two input registers. The first bit (bit 0) at the DI input is used to select one of the two input registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register is written to the selected input data register only if a frame of exact 24 data bits are detected. Depending on bit 0 the contents of the selected status register is transferred to DO during the current communication frame. Bit 1-17 controls the behavior of the corresponding driver.

If bit 23 is zero, the device goes into the standby mode. The bits 18 and 19 are used to control the current monitor multiplexer. Bit 22 is used to reset all status bits in both status registers. The bits in the status registers is cleared after the current communication frame (rising edge of CSN).

## 4.7 Status register

This devices uses two status registers to store and to monitor the state of the device. No error bit (bit 0) is used as a fault bit and is a logical-NOR combination of bits 1-22 in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI communication cycle. If one of the over-current bits is set, the corresponding driver is disabled. If the over-current recovery bit of the output is not set the microcontroller has to clear the over-current bit to enable the driver. If the thermal shutdown bit is set, all drivers goes into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers.