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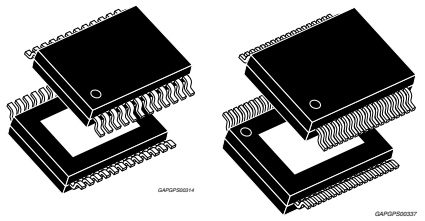
L9959

Single and dual PMOS high-side H-bridge

Datasheet - production data



Features

- Full path R_{DSON} less than 540 mΩ
- Continuous load current > 3 A
- Operating battery supply voltage 5 V to 28 V
- Operating V_{DD} supply voltage 4.5 V to 5.5 V
- All ECU internal pins can withstand up to 18 V
- Output switching frequency up to 11 kHz
- Monitoring of V_{DD} supply voltage
- SPI programmable output current limitation from 5 A to 8.6 A (in 3 steps)
- Over temperature and short circuit protection
- Full diagnosis capability
- Fast switch-off open-drain input/output
- Current-monitoring with current feedback output signal CF
- SPI-interface for configuration and diagnosis
- Error history in second diagnosis register
- Two independent enable pins: "/ABE" and "DIS"
- Control of power stages by SPI or two input signals, PWM and DIR (configurable via SPI)
- Logic levels 5 V compatible
- Conformity to improved EMC requirements due to smart H-bridge switching

Description

L9959S/L9959U and L9959T are single and dual integrated H-bridges for resistive and inductive loads featuring output current direction and supervising functions.

The PowerSSO24 houses one full H-Bridge, while the PowerSSO36 houses both two H-Bridges that can work in parallel, through independent input driving commands, and one full H-bridge, by improving PCB footprint design versus different target applications.

Target application ranges from throttle control actuators to exhaust gas recirculation control valves in automotive domain to a more general use to drive DC and Stepper motors.

Table 1. Device summary

Order code	Package	Packing
L9959S-TR-D	PowerSSO24	Tape & Reel
L9959T-TR-D	PowerSSO36	Tape & Reel
L9959U-TR-D	PowerSSO36	Tape & Reel

This is information on a product in full production. www.st.com

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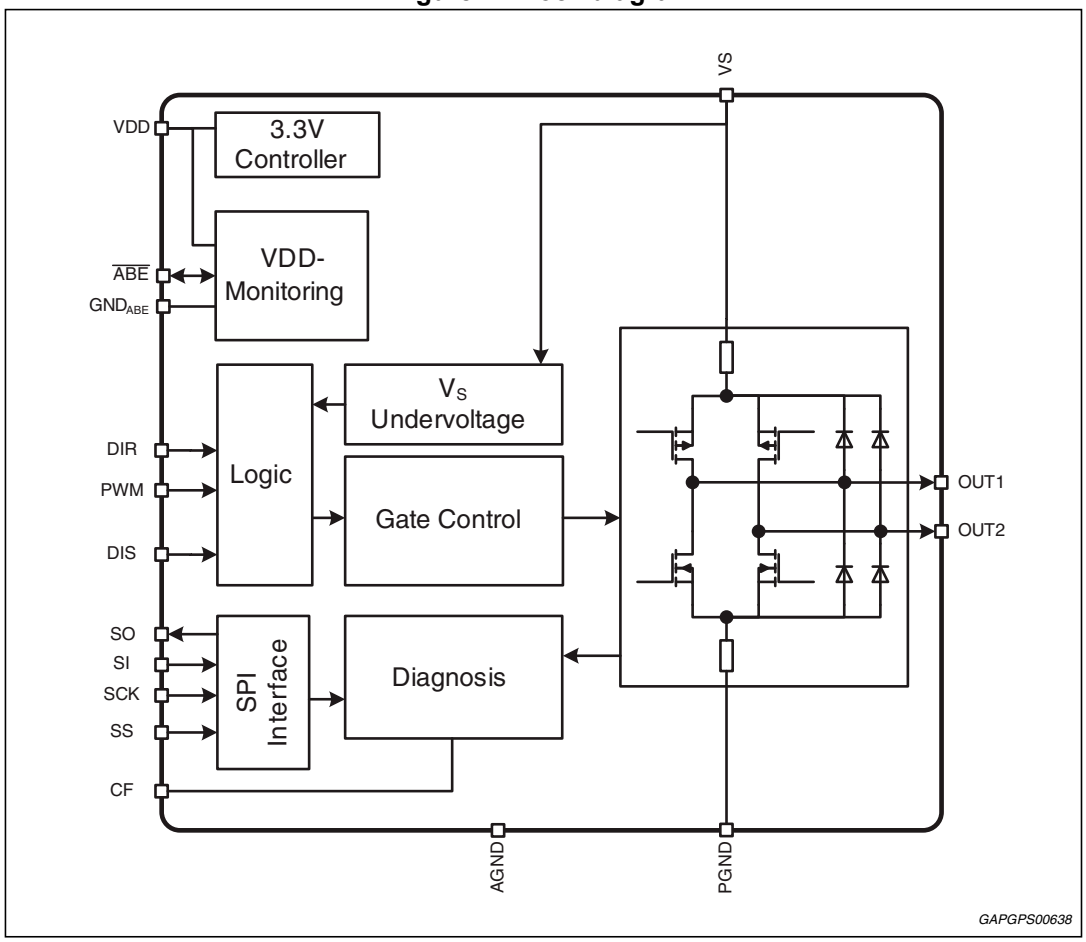
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. PSSO24 pin connection (top view)

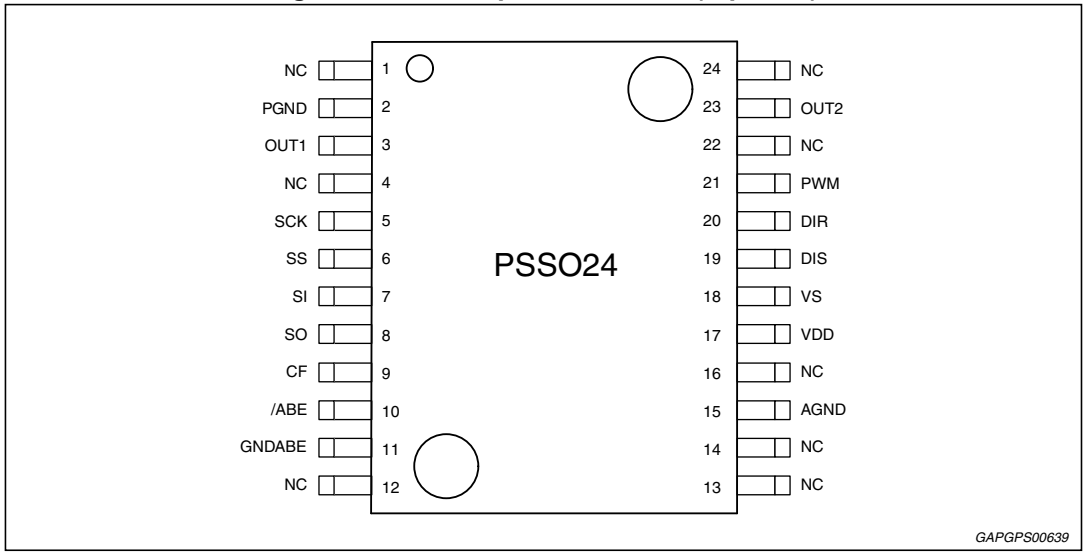


Figure 3. PSSO36 pin connection (top view)

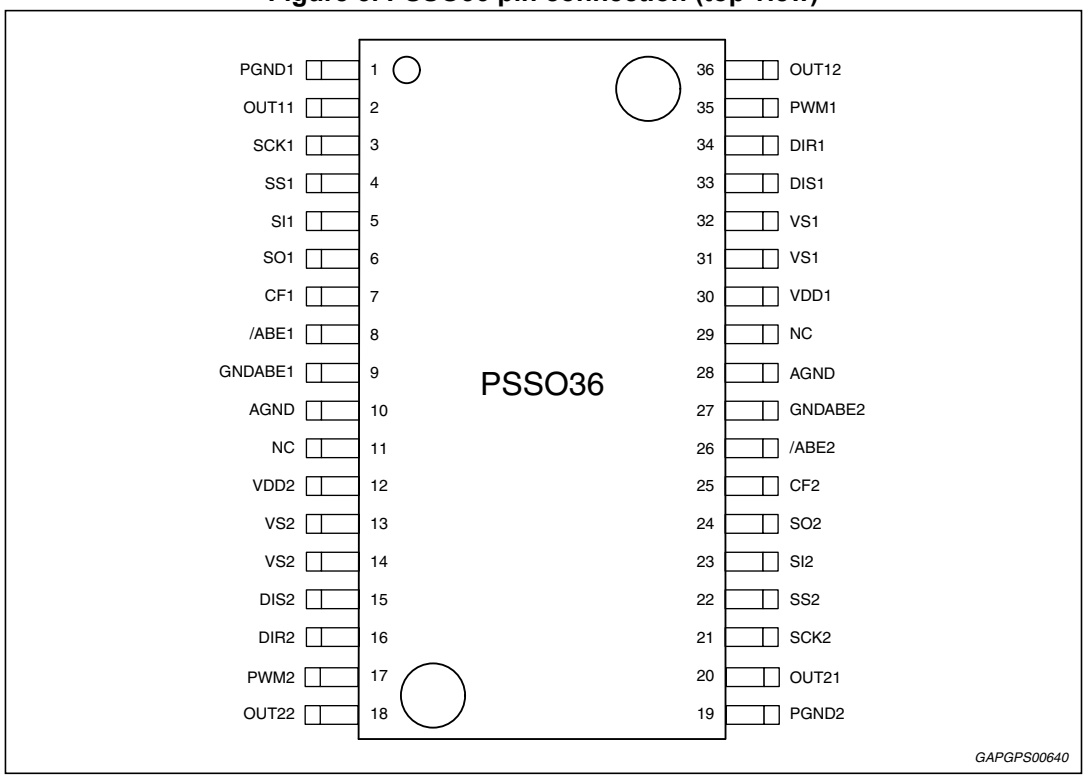
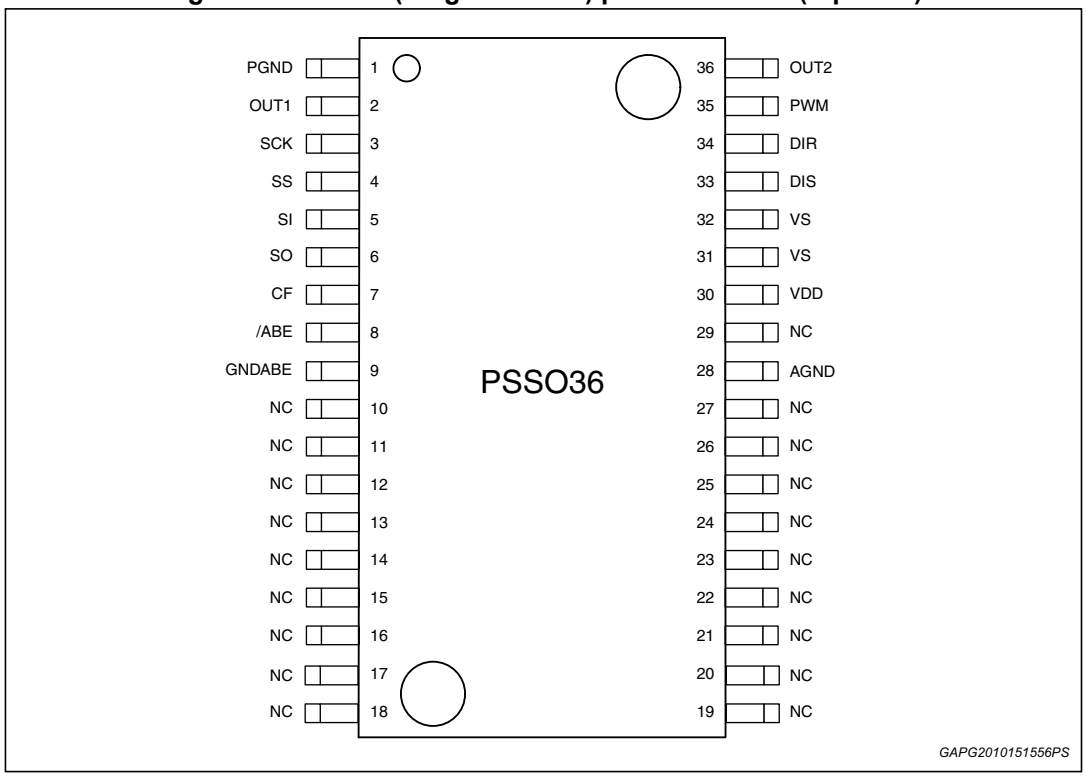


Figure 4. PSSO36 (Single version) pin connection (top view)



2.1 Pin definitions and functions

Table 2. L9959S PSSO24 pin-out

Pin	Symbol	Function
1, 4, 12, 13, 14, 16, 22, 24	NC	To be connected to GND on PCB.
2	PGND	Power Ground
3	OUT1	Bridge output 1 and 2: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor.
5	SCK	Serial clock input: This input controls the internal shift register of the SPI.
6	SS	Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level.
7	SI	Slave in (Serial data input): The input receives serial data from the microcontroller.
8	SO	Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output.

Table 2. L9959S PSSO24 pin-out (continued)

Pin	Symbol	Function
9	CF	Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current.
10	/ABE	Bidirectional Ability/Enable Pin: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off.
11	GNDABE	Sense Ground for VDD monitoring
15	AGND	Device Ground. (Connected to Exposed PAD)
17	VDD	VDD Supply: 5 V Supply
18	VS	Power supply voltage for power stage outputs (external reverse protection required)
19	DIS	Disable input: DIS switches OUT1 and OUT2 to tristate.
20	DIR	Direction input: The DIR pin controls the switch direction of OUT1 and OUT2.
21	PWM	PWM input: The PWM input switches OUT1 and OUT2.
23	OUT2	Bridge output 1 and 2: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor.
EP	AGND	Exposed Pad: Connected to AGND.

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out

Pin	Symbol	Function
1	PGND1(1)	Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected.
2	OUT11	Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22.
3	SCK1	Serial clock input: This input controls the internal shift register of the SPI. SCK1 belongs to chip 1 and SCK2 to chip 2.
4	SS1	Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level. SS1 belongs to chip 1 and SS2 to chip 2.
5	SI1	Slave in (Serial data input): The input receives serial data from the microcontroller. SI1 belongs to chip 1 and SI2 to chip 2.
6	SO1	Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output. SO1 belongs to chip 1 and SO2 to chip 2.

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out (continued)

Pin	Symbol	Function
7	CF1	Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current. CF1 belongs to OUT11 and OUT12, CF2 to OUT21 and OUT22.
8	/ABE1	Bidirectional Ability/Enable Pin 1: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. /ABE1 belongs to chip 1.
9	GNDABE1	Sense Ground for VDD monitoring
10, 28	AGND	Device Ground. (Connected to Exposed PAD)
11, 29	NC	To be connected to GND on PCB.
12	VDD2(2)	VDD Supply: 5V Supply.
13, 14,	VS2(3)	Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected.
15	DIS2	Disable input 2: DIS2 switches OUT21 and OUT22 to tristate.
16	DIR2	Direction input 2: DIR2 pin controls the switch direction of OUT21 and OUT22.
17	PWM2	PWM input 2: PWM1 input switches OUT21 and OUT22.
18	OUT22	Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22.
19	PGND2(1)	Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected.
20	OUT21	Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22.
21	SCK2	Serial clock input: This input controls the internal shift register of the SPI. SCK1 belongs to chip 1 and SCK2 to chip 2.
22	SS2	Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level. SS1 belongs to chip 1 and SS2 to chip 2.
23	SI2	Slave in (Serial data input): The input receives serial data from the microcontroller. SI1 belongs to chip 1 and SI2 to chip 2.
24	SO2	Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output. SO1 belongs to chip 1 and SO2 to chip 2.

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out (continued)

Pin	Symbol	Function
25	CF2	Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current. CF1 belongs to OUT11 and OUT12, CF2 to OUT21 and OUT22.
26	/ABE2	Bidirectional Ability/Enable Pin 2: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. /ABE2 belongs to chip 2.
27	GNDABE2	Sense Ground for VDD monitoring
30	VDD1(2)	VDD Supply: 5V Supply.
31, 32	VS1(3)	Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected.
33	DIS1	Disable input 1: DIS1 switches OUT11 and OUT12 to tristate
34	DIR1	Direction input 1: DIR1 pin controls the switch direction of OUT11 and OUT12.
35	PWM1	PWM input 1: PWM1 input switches OUT11 and OUT12.
36	OUT12	Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22.
EP	AGND(4)	Exposed PAD: connected to AGND

1. Pins 1 is referred to die 1, whereas 19 is referred to die 2.
2. Pins 12 is referred to die 2, whereas 30 is referred to die 1.
3. Pins 13 and 14 are referred to die 2, whereas pins 31 and 32 are referred to die1.
4. Pins 10 is referred to die 2, whereas 28 is referred to die 1.

Table 4. L9959U (Single version in PSSO36) pin out

Pin	Symbol	Function
1	PGND	Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected.
2	OUT1	The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor.
3	SCK	Serial clock input: This input controls the internal shift register of the SPI.
7	CF	Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current
8	/ABE	Bidirectional Ability/Enable Pin: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off.
9	GNDABE	Sense Ground for VDD monitoring
10,11, 12,13, 14,15, 16,17, 18,19, 20,21, 22,23, 24,25, 26,27, 29	NC	To be connected to GND on PCB.
28	AGND	Device Ground. (Connected to Exposed PAD)
30	VDD	VDD Supply: 5 V Supply.
31, 32	VS1	Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected.
33	DIS	Disable input : DIS switches OUT1 and OUT2 to tristate
34	DIR	Direction input: DIR pin controls the switch direction of OUT1 and OUT2.
35	PWM	PWM input: PWM input switches OUT1 and OUT2.
36	OUT2	The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor.

3 Electrical specifications

3.1 Absolute maximum ratings

Warning: **Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.**

Table 5. Absolute maximum ratings

Symbol	Parameter / Test condition	Value [DC Voltage]	Unit
V_{VS}	DC supply voltage The device is able to sustain load dump as specified in the ISO16750 documentation	-1.0 to +40	V
V_{VDD}	Stabilized supply voltage, logic supply	-0.3 to 18	V
C_F (1)	Current feedback output	-0.3 to 18	V
V_{SI}, V_{SCK}, V_{SS}, V_{SO}, V_{DIR}, V_{PWM}, V_{DIS}	Logic input / output voltage range	-0.3 to 18	V
V_{OUTn}	Output voltage (n = 1,2 or 11,12,21,22); $V_{OUTn} < V_S + 1$ V	-1.0 to 40	V
	Dynamic pulse / t < 500ms; $V_{OUTn} < V_S + 2$ V	-2.0 to 40	V
T_j	Operating junction temperature	-40 to 150	°C
	Dynamic junction temperature (1000hrs)	150 to 175	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. It is withstood at V_S = 18 V

3.2 ESD protection

Table 6. ESD protection

Parameter	Value	Unit
All pins versus ground group (AGND, PGND1, PGND2, GND_ABE1, GND_ABE2)	±2(1)	kV
VS pin, Power Output Pins: OUT1, OUT2 or OUT11, OUT12, OUT21, OUT22 versus ground group (AGND, PGND1, PGND2, GND_ABE1, GND_ABE2)	±4(2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
2. HBM with all unzipped pins grounded.

3.3 Thermal data

Table 7. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-to-case (max) for L9959S, L9959T	2.0	°C/W

3.4 Electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 18 V, 4.5 V ≤ V_{DD} ≤ 5.5 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 8. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating voltage range	-	4.5	-	28	V
I_{VS}	V_S current consumption in active mode	V_{DD} = 5 V; V_S = 5 V and V_S = 18 V; Bridge disabled	-	-	5	mA
		V_{DD} = 5 V; V_S = 5 V and V_S = 18 V; f_{OUT} = 2 kHz; I_{OUT} = 0 A	-	-	6	mA
		V_{DD} = 5 V; V_S = 5 V and V_S = 18 V; f_{OUT} = 10 kHz; I_{OUT} = 0 A	-	-	14	mA
		V_{DD} = 5 V; V_S = 28 V; f_{OUT} = 10 kHz; I_{OUT} = 0 A	-	-	14	mA
$I_{VS(stby)}$	V_S current consumption in passive mode	V_{DD} = 0 V	0	-	2.5	mA
V_{VS_slew} (1)	Slew rate on V_S	-	-	-	100	V/µs
V_{VS_slew} (2)	Slew rate on V_S	-	-	-	20	V/µs
V_{DD}	Operating voltage range	-	4.5	-	5.5	V
I_{VDD}	V_{DD} supply current	V_S = 18 V; V_{DD} = 5 V	-	-	10	mA

1. No change of parameters for VDD-monitoring and in SPI logic
2. No change of parameters

Table 9. Power-on reset

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DDRES}	Reset active threshold	-	2.8	-	3.4	V
V_{DDPOR}	Power-on reset threshold	-	3.3	-	4	V
$V_{DDPORHYS}$	Power-on reset hysteresis	-	-	600	-	mV
t_{POR}	Power-on reset extension time	-	-	-	1	ms

Table 10. V_{DD} monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	V_{DD} monitoring voltage range	-	V_{DDPOR}	-	18	V
V_{DD_THL}	Under voltage threshold	V_S = 0 V	4.2	-	4.5	V
V_{DD_THH}	Over voltage threshold	V_S = 0 V	5.25	-	5.5	V
t_{FIL_OFF}	Switch-off filtering time	Guaranteed by scan.	60	-	135	µs
t_{FIL_ON}	Switch-on filtering time		60	-	135	µs
V_{TEST_THL}	Under voltage test threshold	-	5.25	-	5.5	V
V_{TEST_THH}	Over voltage test threshold	-	4.2	-	4.4	V
V_{DD_MR}	Full V_{DD} supply range	-	-0.3	-	18	V
V_{DD_SLEW}	V_{DD} slew	-		-	500	mV/µs
ΔV_{DD_THX}	Threshold (V_{DD_THH}, V_{DD_THL}) shift during vs. inverse current	-	-0.1	-	0.1	V
V_{ABE_INL}	/ABE input low-level	-	-0.3	-	1.65	V
V_{ABE_INH}	/ABE input high-level	-	3.15	-	18	V
V_{ABE_INHYS}	/ABE input hysteresis	-	0.2	-	1.0	V
I_{ABE_IN}	/ABE input pull-down current	0 V < V_{ABE} < 1.5 V	0	-	60	µA
		V_{ABE} = 2.1 V, 5 V, 18 V; V_S = 18 V; V_{DD} = 5 V, 18 V	20	40	60	µA
V_{ABE_OUTL}	/ABE output low voltage	2.5 V < V_{DD} < V_{DD_THL}; I_{ABE_OUTL} < 2.5 mA	0	-	1.0	V
V_{ABE_OUTL}	/ABE output low voltage	V_{DD_THH} < V_{DD} < 18V; I_{ABE_OUTL} < 7.5 mA	0	-	1.2	V
V_{ABE_OUTL}	/ABE output passive low voltage	-	0	-	1.2	V
ΔI_{ABE}	I_{ABE} Change during vs. inverse current	-	-100	-	100	µA

Table 11. Undervoltage shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{UV_OFF}	VS UV threshold	VS decreasing	3.1	3.8	4.5	V
V_{UV_ON}	VS UV threshold	VS increasing	3.3	4.0	4.7	V
V_{UV_HYS}	VS UV hysteresis	V_{UV_ON} - V_{UV_OFF}	0.1	-	1	V
t_{FUV}	VS UV detection time	-	-	-	1.5	µs

3.5 Outputs OUT1 and OUT2

Table 12. On-resistance (4.5 V < V_S < 28 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ONVS\ OUT1,2}$	On-resistance to supply	V_{DD} = 5 V; V_S = 10 V, $I_{OUT1,2}$ = 3 A	-	-	315	mΩ
$r_{ONGND\ OUT1,2}$	On-resistance to PGND	V_{DD} = 5 V; V_S = 10 V, $I_{OUT1,2}$ = 3 A	-	-	225	mΩ
I_{LEAK}	Switched-off output current of OUT1,2	V_{DD} = 5 V; V_S = 13 V; V_{OUT} = 0 V	-200	-	-	µA
		V_{DD} = 5 V; V_S = 13 V; V_{OUT} = V_S	-	-	200	µA

Table 13. Power output switching times (8 V < V_S < 18 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ ON}$	Output delay time driver on	-	-	-	6	µs
$t_{d\ OFF}$	Output delay time driver off	-	-	-	20	µs
$t_{d\ dis}$ (1)	Disable delay time	Guaranteed through scan.	-	-	12.5	µs
$t_{d\ pwon}$	Power-on delay time		-	-	1	ms
$t_{d\ en}$	Enable delay time		-	-	50	µs
dI_{OUT}/dt	Current slew rate	-	-	1.6		A/µs
dV_{OUTHS}/dt (2)	Output rise/fall slew-rate high-side slow selected with bit SR = 0 fast selected with bit SR = 1	V_{DD} = 5 V; V_S = 14 V $R_{LOAD1,2}$ = 2.6 Ω (8 V_S), 6 Ω (18 V_S)	0.975 2.8	-	2.7 8	V/µs
dV_{rOUTLS}/dt (2)	Output rise slew-rate low-side valid only after the toggling of DIR input		0.975	-	2.7	V/µs
dV_{fOUTLS}/dt (2)	Output fall slew-rate low-side		2.5	4	8	V/µs
f_{pwmmax}	PWM input frequency	-	-	-	11	kHz

1. Driven by /ABE or DIS input.
2. The slew-rates ($dV_{OUT}/dt1$) are defined by dV (voltage difference 20% - 80%) divided by the rise-/fall times (t_r/t_f see *Figure 6: Output rise and fall times*).

Figure 5. Output delay times (e.g. low-side output)

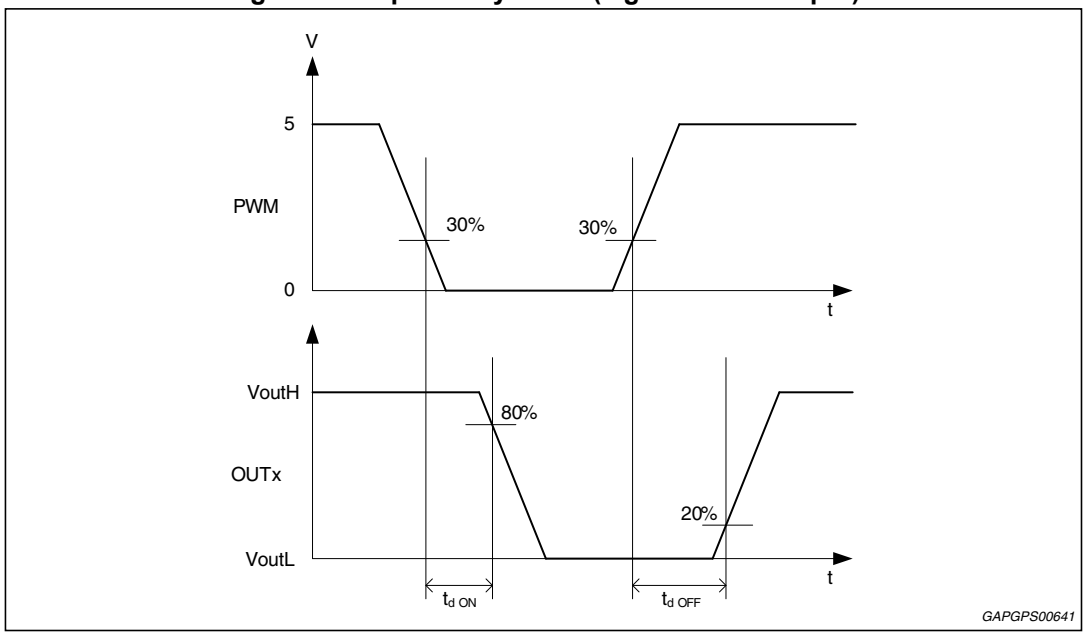


Figure 6. Output rise and fall times

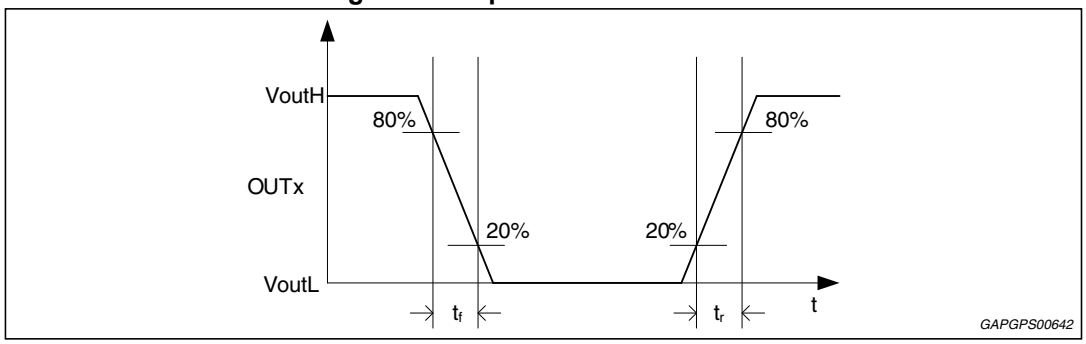


Figure 7. Output disable and enable time (/ABE Input)

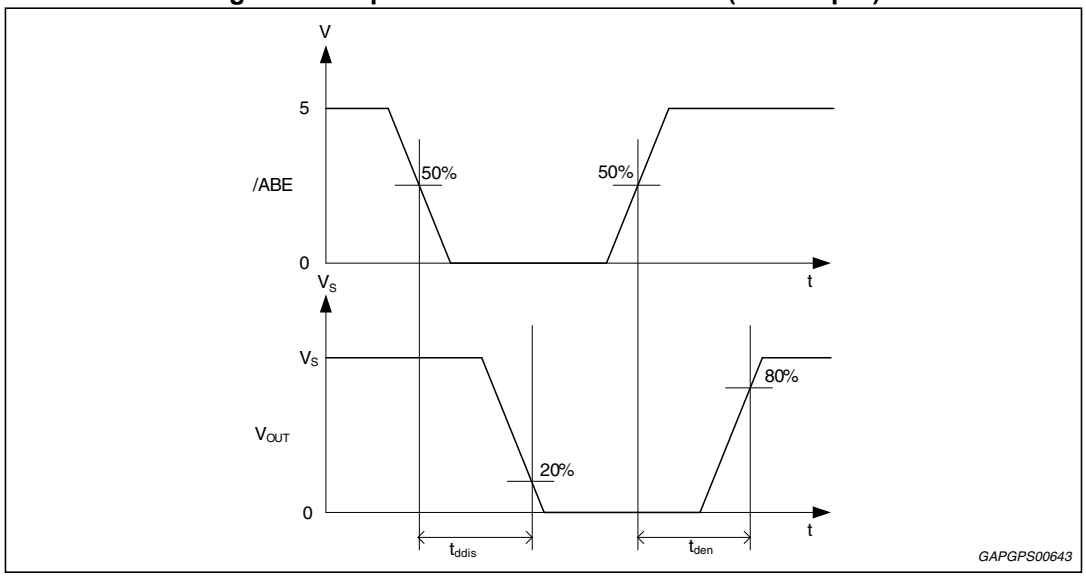


Figure 8. Output disable and enable time (DIS Input)

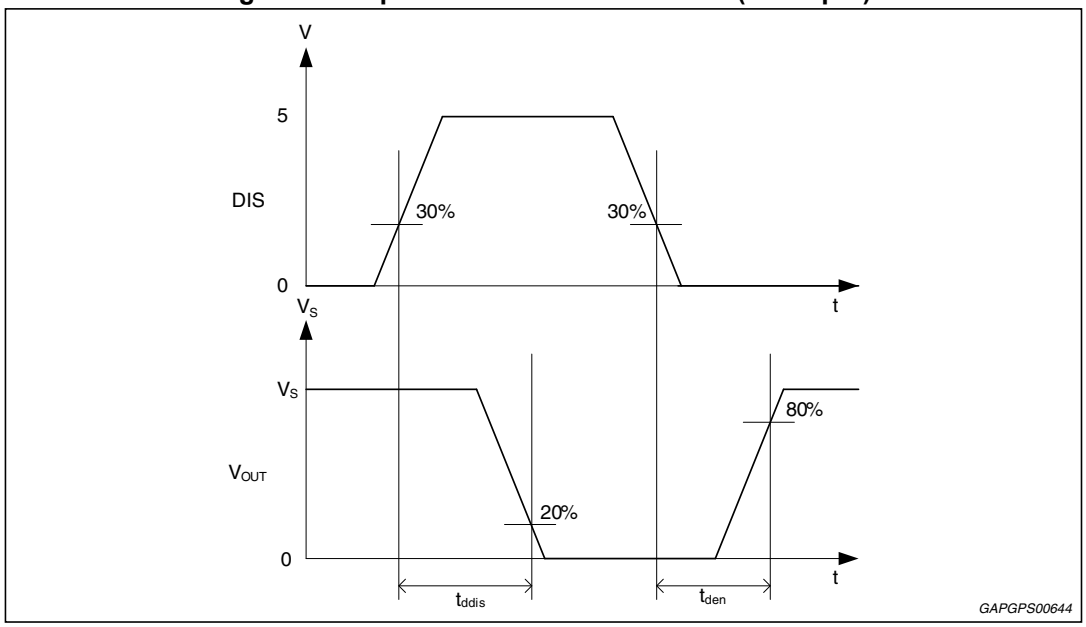


Table 14. Current feedback (CF)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CF} (1)	CF voltage range	V_S > 6.5 V, OUTx = 0 A, $T_{J\ =}$ -40 °C; Current level 2,3,4	0.01	0.05	0.20	V
		V_S > 6.5 V, OUTx = 250mA, T_J = 130 °C; Current level 2,3,4	0.04	0.275	0.5	V
		V_S > 6.5 V, OUTx = 0.4 * I_{clx}, T_J = 130 °C; Current level 2,3,4	1.71	1.80	1.89	V
		V_S > 6.5 V, OUTx = I_{clx} T_J = -40°C to 150°C; Current level 2,3,4	3.82	4.5	5.18	V
R_{CF}(2)	CF resistor range	-	-	5.1	-	kΩ
I_{OFFSET}	CF offset current	-	-	10	-	µA

1. Measured at a 5.1k resistor between CF and GND (R_{CF}).
Levels see *Table 34* Current Level (CONFIG_REG).

2. Defined by design, not tested.

Note: This signal has an individual error ±5 % in each of the three currents levels, at trimming temperature of 130 °C. Additional an individual error ±10 % in each of the three current levels over temperature and aging. So the maximum error is of ±15 % in each of the three current levels. The offset and the gain errors may be different in each current level. The adjustment is done at 130 °C and compensates the error corresponding to 0.4 * Iclx

Table 15. Current limiting

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{CL2}\|^{(1)}$	Current limit$_2$	R_{CF} = 5.1 kΩ	4.25	5	5.75	A
$\|I_{CL3}\|^{(1)}$	Current limit$_3$		5.6	6.6	7.6	A
$\|I_{CL4}\|^{(1)}$	Current limit$_4$		7.3	8.6	9.9	A
$\|I_{HYS2-4}\|^{(1)}$	Current limit hysteresis$_1$	-	-5% ICL_{2-4}	-	-10% ICL_{2-4}	A
t_b	Blanking time	Guaranteed through scan.	8	11	15	µs
t_{trans}	Time between two transient		90	-	130	µs

1. Programmable current levels see *Table 34* Current Level (CONFIG_REG). Measured using a 5.1 kΩ resistor between CF and GND (R_{CF}).

Table 16. Over-current detection (8 V < V_S < 18 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OC2\_LS}\|^{(1)}$	Low side over current threshold$_2$	V_{DD} = 5 V	4.9	-	8.2	A
$\|I_{OC3\_LS}\|^{(1)}$	Low side over current threshold$_3$	V_{DD} = 5 V	6.7	-	11.1	A
$\|I_{OC4\_LS}\|^{(1)}$	Low side over current threshold$_4$	V_{DD} = 5 V	8.4	-	14	A
$\|I_{OC2\_HS}\|^{(1)}$	High side over current threshold$_2$	V_{DD} = 5 V	5.5	-	9.2	A
$\|I_{OC3\_HS}\|^{(1)}$	High side over current threshold$_3$	V_{DD} = 5 V	6.9	-	11.5	A
$\|I_{OC4\_HS}\|^{(1)}$	High side over current threshold$_4$	V_{DD} = 5 V	8.6	-	14.4	A
$I_{TRACK-2}^{(2)}$	$\|I_{OC2}\| - \|I_{CL2}\|$	V_{DD} = 5 V	0.4	-	5.5	A
$I_{TRACK-3}^{(2)}$	$\|I_{OC3}\| - \|I_{CL3}\|$	V_{DD} = 5 V	0.4	-	5.5	A
$I_{TRACK-4}^{(2)}$	$\|I_{OC4}\| - \|I_{CL4}\|$	V_{DD} = 5 V	0.4	-	5.5	A
t_{DF}	Delay time for fault detection	guaranteed by design	1	2	4.5	µs
t_{DF_off}	Switch-off delay time	-			6	µs
t_{DF_del}	Delayed switch-off time	-	20		200	µs
t_{SC}	Short-circuit detection	guaranteed through scan	292	350	413	µs

1. Programmable current levels see *Table 34* Current Level (CONFIG_REG).
2. Tracking values are referred for both LS and HS.

Table 17. Open-load detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{OL}	Open-load detection threshold	-	5	-	50	kΩ
t_{DIAGOL}	Open-load diagnosis enable delay	Guaranteed through scan.	100	-	150	ms
$t_{DIAGOL1}$	Open-load diagnosis filter time$_1$		2.4	-	3.6	ms
$t_{DIAGOL2}$	Open-load diagnosis filter time$_2$		200	-	300	µs
V_{out1_OFF}	Out1 voltage regulator	-	1.67	-	1.97	V

Note: If the value of the connected load is below 5 kΩ no Open Load is detected; whereas if the value of the connected load is more than 50 kΩ, Open Load is detected.
If the load is in the range between (5 to 50) kΩ, the Open Load diagnosis could be not reliable.

Table 18. Retest delay

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{delay\ retest}$	Retest delay for failures: SCB, SCG, SCL	Guaranteed through scan.	290	350	410	µs

3.6 Temperature dependent current reduction

Table 19. Temperature dependent current reduction

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{L\_TSD}\|$	Current limit at T_{SD}	-	1.4	2.5	3.6	A
T_{ILR}	Start of temperature dependent current reduction	-	150	165	-	°C
T_{SD}	Thermal shut-down	-	175	-	-	°C
T_{SD}-T_{ILR}	Range of temperature dependent current reduction	-	20	25	30	°C
T_{fTSD}	Thermo-shut-down detection filter time	Guaranteed through scan.	6	-	18	µs

Note: see also *Figure 17: Temperature dependent current reduction*.

3.7 Free-wheeling diodes

Table 20. Free-wheel diodes

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
U_D	Free-wheeling diode forward voltage	I_{OUT} = 3 A	-	-	2	V
T_{it}(1)	Free-wheeling diode reverse recovery time	-	-	-	100	ns

1. Not subject to production test; specified by design.

3.8 SPI / logic electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 18 V, 4.5 V ≤ V_{CC} ≤ 5.5 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 21. Inputs: SI, SS, SCK, DIR, DIS and PWM; Output: SO

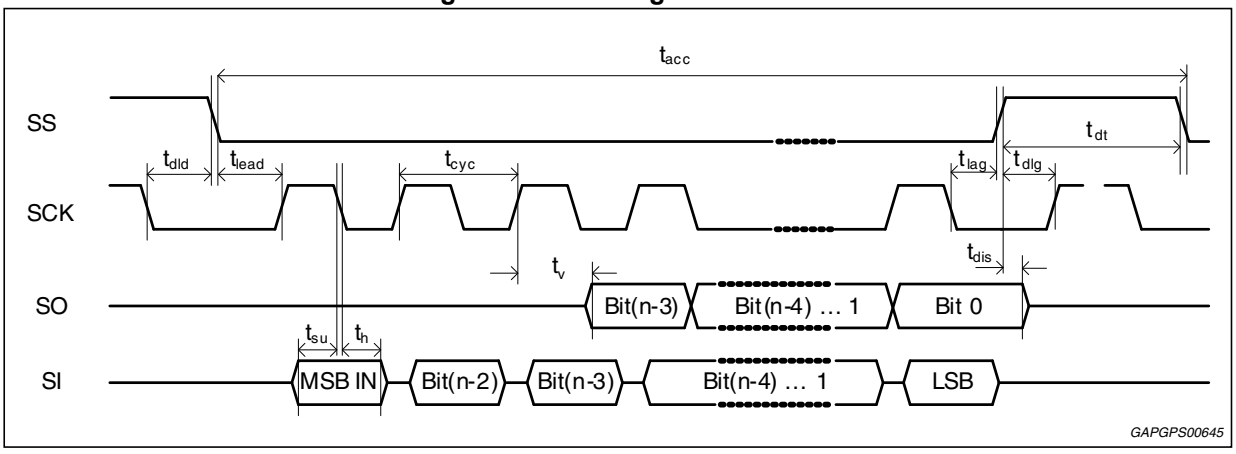
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Inputs: SI, SS, SCK DIR, PWM						
V_{IL}	Input voltage low-level	V_{DD} = 5 V	-0.3	-	0.75	V
V_{IH}	Input voltage high-level	V_{DD} = 5 V	1.75	-	VDD+0.3	V
V_{IHYS}	Input hysteresis	V_{DD} = 5 V	0.2	-	1.0	V
R_{PUin}	Input pull-up resistor	V_{DD} = 5 V	50	-	250	kΩ
I_{INx}	PWM, DIR input current	V_{INx} > 3.0V	-5	-	5	µA
C_{SIin} (1)	SI input capacitance	-	-	-	10	pF
C_{SCKin} (1)	SCK input capacitance	-	-	-	10	pF
C_{SSin} (1)	SS Input Capacitance	-	-	-	15	pF
$C_{DIR,PWMin}$ (1)	DIR, PWM input capacitance	-	-	-	20	pF
Input: DIS						
R_{DISPU}	Pull-up resistor	0 V < V_{DIS} < 2.1 V	10	-	45	kΩ
I_{DISx}	DIS input current	V_{DIS} > 3 V	-5	-	5	µA
$C_{DIS\ in}$ (1)	DIS input capacitance	-	-	-	20	pF
t_{DIS}	DIS pulse width	-	0.5	1	1.5	µs
Input pin disturbance (SI, SS, SCK DIR, PWM,DIS)						
ΔVx_HL	Change of V_{IH} and V_{IL} during inverse current on V_S	Not subjected to test in production.	-0.1	-	0.1	V
ΔISx	Change of input current of SPI input pins during inverse current on V_S		-100	-	100	µA
Output: SO						
V_{SOL}	Output voltage low level	I_{OL} = 2 mA,	0	-	0.4	V
V_{SOH}	Output voltage high level	I_{OH} = -2 mA	VDD-0.5	-	VDD	V
SR_{SO} (1)	Slew rate	C_{LOAD} = 200 pF	0.3	-	0.6	V/ns
I_{SOLK}	Tristate leakage current	V_{SS} = V_{DD}	-10	-	10	µA
$C_{SO\ out}$ (1)	SO output capacitance	-	-	-	10	pF
Output pin disturbance (SO)						
ΔI_{SOLK}	Change of I_{SOLK} during inverse Current on VS	-	-100	-	100	µA

1. Not measured in production test. Parameter guaranteed by design.

Table 22. Dynamic characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{cyc}	Cycle time	-	490	-	-	ns
t_{lead}	Enable lead time	-	300	-	-	ns
t_{lag}	Enable lag time	-	150	-	-	ns
t_v	Data valid	SCK = 2 V; SO = 0.2 V; C_L = 40 pF	40	-	-	ns
		SCK = 2 V; SO = 0.2 V; C_L = 200 pF	150	-	-	ns
		SCK = 2 V; SO = 0.2 V; C_L = 350 pF	230	-	-	ns
t_{su}	Data setup time	-	40	-	-	ns
t_h	Data hold time	-	40	-	-	ns
t_{dis}	Disable time	-	0	-	100	ns
t_{dt}	Transfer delay	-	300	-	-	ns
t_{dld}	Disable lead time	-	250	-	-	ns
t_{dlg}	Disable lag time	-	250	-	-	ns
t_{acc}	Access time	-	8.35	-	-	µs

Figure 9. SPI timing information



4 Application information

4.1 Power stage switching behavior

The L9959 output stages can either be controlled by the pins PWM and DIR or by their corresponding SPI registers (SPWM and SDIR: see *Table 33* in Configuration Register (CONFIG_REG)). The SPI bit MUX in the configuration register (CONFIG_REG) is used to define the driving control strategy of the H-bridge. If the power stages are disabled by /ABE or DIS, this bit is reset and the pins PWM and DIR control the outputs.

The active free-wheeling, in which the body diode is actively shorted by its associated Power-MOS, can be disabled by the bit **FW** in the configuration register (CONFIG_REG). By default, active free-wheeling is enabled.

The device minimizes electro-magnetic emission by switching the high-side and low-side drivers in a special sequence. Two cases are distinguished: The PWM-mode, during which the current direction does not change and the direction switches using the DIR, which changes the current direction (see *Figure 10*, *Figure 12* and *Figure 13*).

4.1.1 PWM mode (same current direction)

The PWM input pin switches the high-/low-side output of the half-bridge, which is selected by the DIR pin.

DIR = '0': OUT1 is switched, DIR = '1': OUT2 is switched.

PWM = '0': Switched low-side is on, PWM = '1': Switched high-side is on.

Figure 10. PWM mode current flow

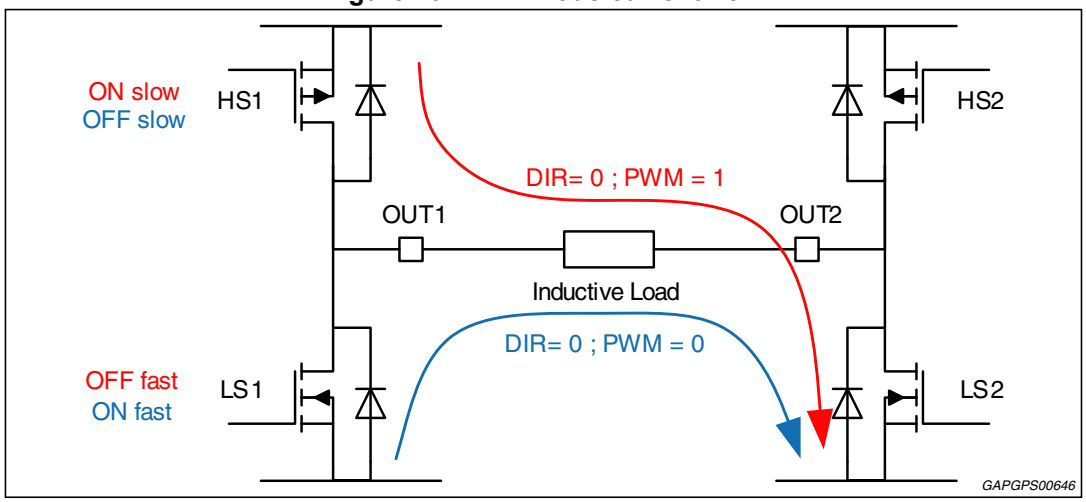
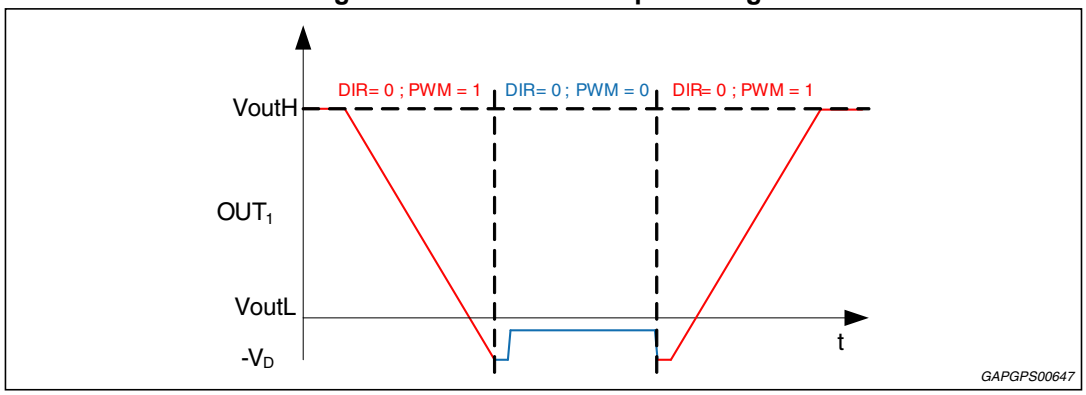


Figure 11. PWM mode output voltage



During PWM mode the high-side (e.g. *Figure 10* HS1) output is switched off with a slow slew rate until it is off and the low-side body-diode has taken over the entire current (passive freewheeling). Then the associated low-side transistor (e.g. *Figure 10* LS1) is turned on with a fast slope to reduce the voltage across the device and to minimize the power.

The output is pulled to high voltage, by first turning off the low-side driver with a fast slew rate and, after it is off, the high-side driver is switched on by a slow one (e.g. *Figure 10* LS1, HS1).

This assures, that the voltage and current change over the body diode is done smoothly, reducing the electromagnetic emission.

4.1.2 DIR-change mode

The first part of the sequence is identical to the PWM-mode (s.a.). After this has been finished and the associated low-side driver is on (e.g. *Figure 12* LS1), in phase 1 the other low-side driver is turned on (e.g *Figure 12* LS2) to enter passive freewheeling phase. Then in phase 2 the low-side output of OUT2 is switched-off slowly and the current through the load is taken over by the body-diode of the high-side (e.g. *Figure 13* HS2).

Depending on the inductance of the load, the current vanishes more or less quickly. After the low-side driver is turned off, the high-side is switched on with a slow slew-rate.

This assures, that direction switch occurs while the current over the load has vanished, which reduces the electromagnetic emission.

Figure 12. DIR-change (current is changing its direction)

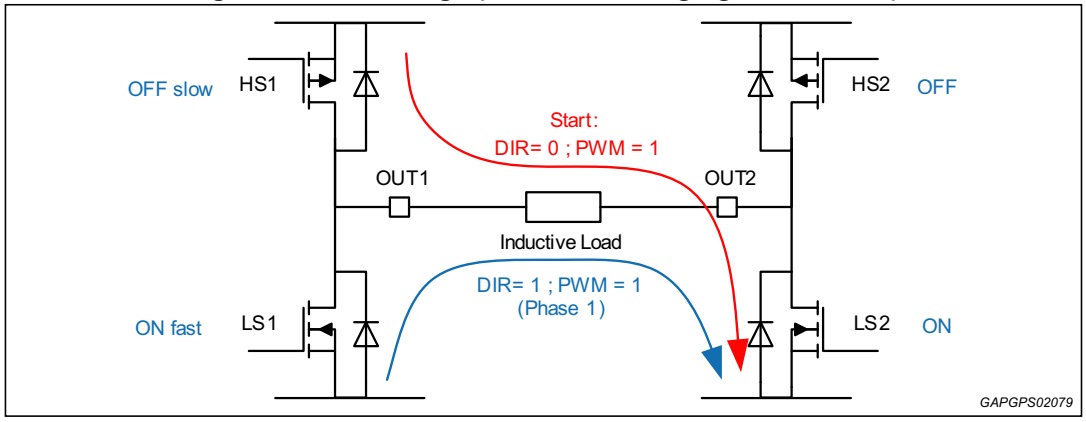


Figure 13. DIR-change current flow phase 2

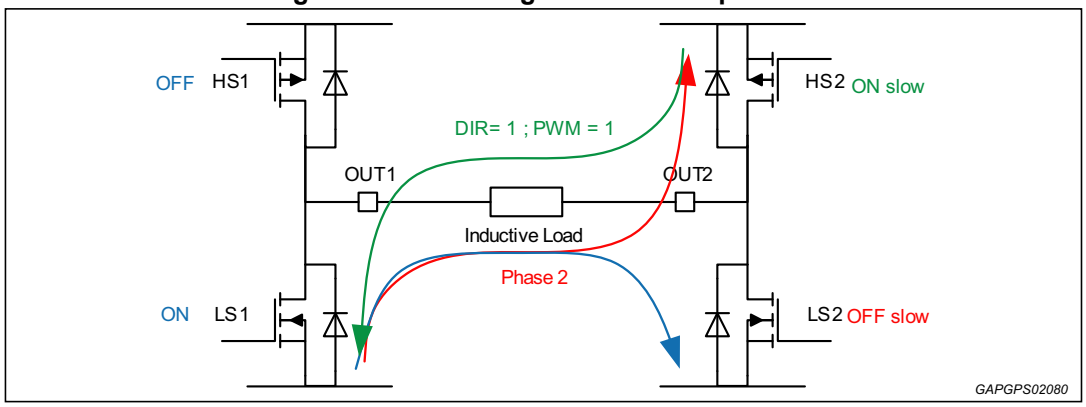
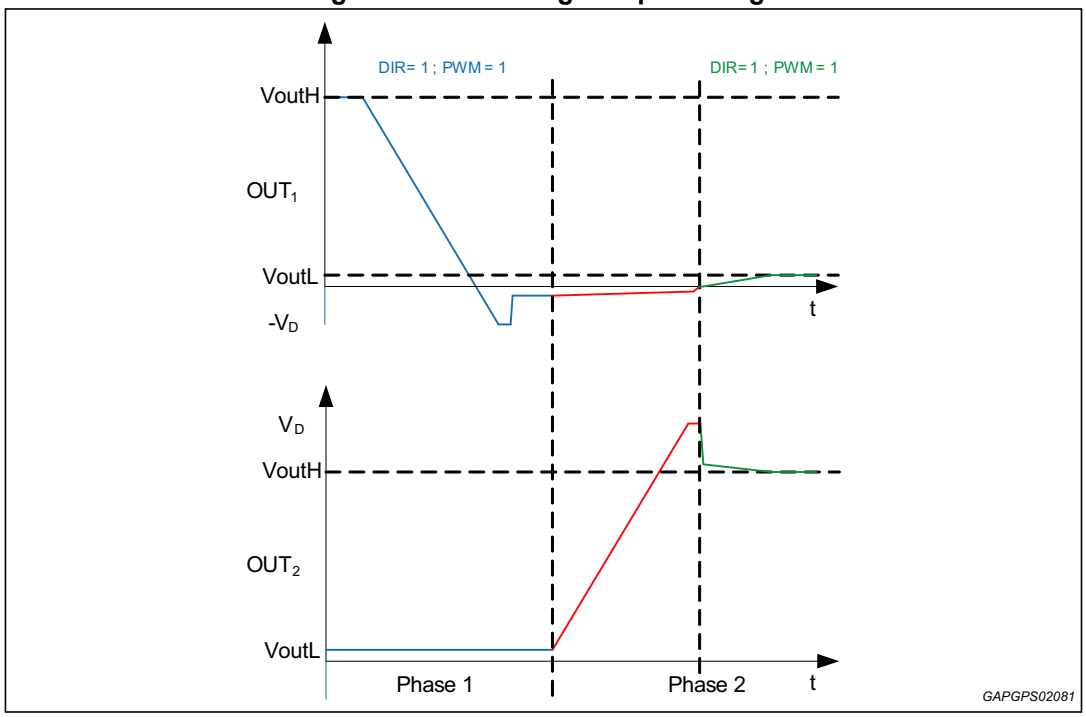


Figure 14. DIR-change output voltage



4.2 Protection and monitoring

A set of failure as Short-circuit to Ground (SCG), Short-circuit to battery (SCB) and Short-circuit to load (SCL) errors (SBC, SCG, SCL) are confirmed after their occurrence by accessing the error condition after time $\mathbf{t_{delay\_retest}}$ a second time. Only after the error is confirmed, it is entered into the diagnosis register 1 (DIA_REG1), and the device is disabled and no further diagnosis is run.

The device can be enabled again by the following actions: Power-on reset, disabling and enabling the device using the pins /ABE or DIS (e.g. disabling - enabling sequence). The diagnosis registers can be cleared by sending a reset command by SPI (**STATCON_REG**) to either diagnosis register 1 (**DIA_REG1**) or 2 (**DIA_REG2**). The bit1 (Reset) of the CONFIG_REG if forced to zero resets both the device registers configuration and diagnosis registers to default but is not able to restart the device. In order to restart IC it is necessary