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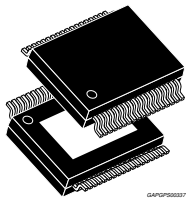
L9960
L9960T

Automotive ETC H-bridge

Datasheet - production data



PowerSSO-36

Features

- AEC-Q100 qualified
- Flexible driving strategy via configurable pins PWM/DIR (IN1/IN2)
- RDSon < 400 mΩ (full path at T_j =150° C)
- Operating battery supply voltage from 4.5 V up to 28 V
- Operating VDD5 supply voltage from 4.5 V to 5.5 V
- Input switching frequency up to 20 kHz
- Built in charge pump supporting 100% duty cycle
- Logic levels compatible to 3.3 V and 5 V
- Monitoring of VDD5 supply voltage with bidirectional switch-off pin
- Current limitation SPI-adjustable in four steps.
- Output stage current limitation with dependence on temperature
- 2 Programmable voltage and current slew rate control
- Short circuit and programmable thermal warning and shutdown thresholds
- Open Load diagnosis in ON condition
- All I/O pins can withstand up to 19 V
- SPI interface for configuration and diagnosis
- Two independent enable/disable pins NDIS and DIS and SOPC (Switch-off Path Check) available
- Spread Spectrum function for EMI reduction
- Available in single (L9960) and Twin (L9960T) option, both in PSSO36 package

Description

The device is an integrated H-Bridge for resistive and inductive loads for automotive applications, such as throttle control actuators or exhaust gas recirculation control valves.

The driving strategy is enhanced by configurable PWM / DIR pins and IN1/IN2.

The H-Bridge contains integrated free-wheel diodes. In case of freewheeling condition, the low-side only is switched on in parallel of its diode to reduce power dissipation.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, to control all operating modes and read out diagnostic information.

Table 1. Device summary

Order code	Package	Packing
L9960	PowerSSO-36	Tube
L9960TR		Tape and Reel
L9960T		Tube
L9960T-TR		Tape and Reel

Contents

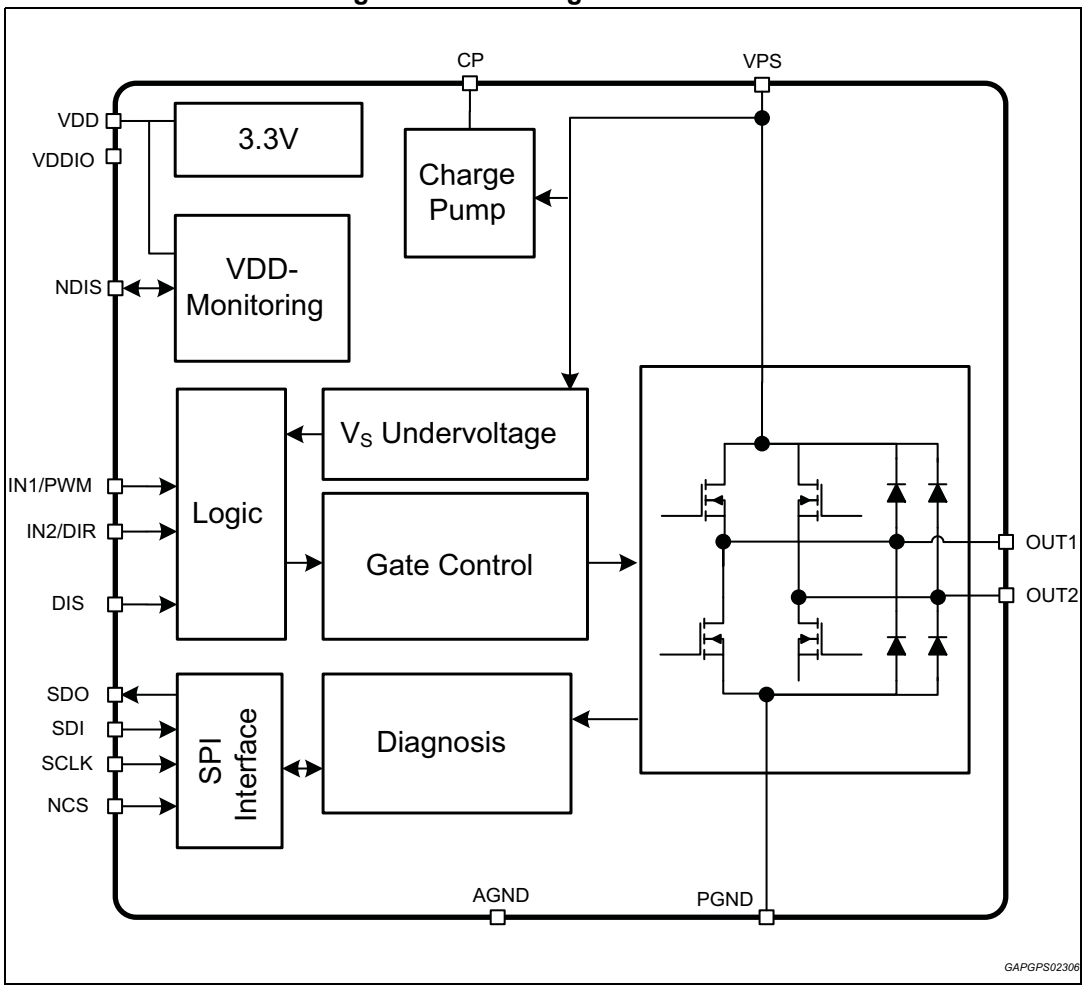
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram for L9960



1.2 Pin description

1.2.1 PowerSSO36 package

Figure 2. Pin connection of L9960 version (top view)

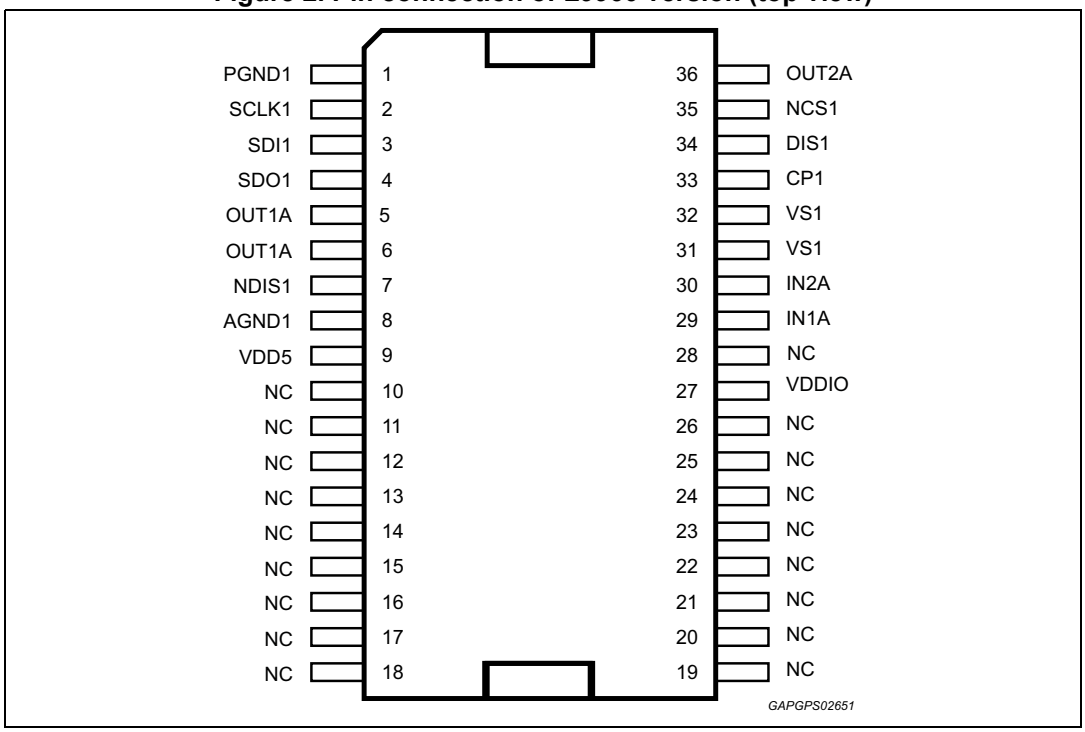


Figure 3. Pin connection of L9960T version (top view)

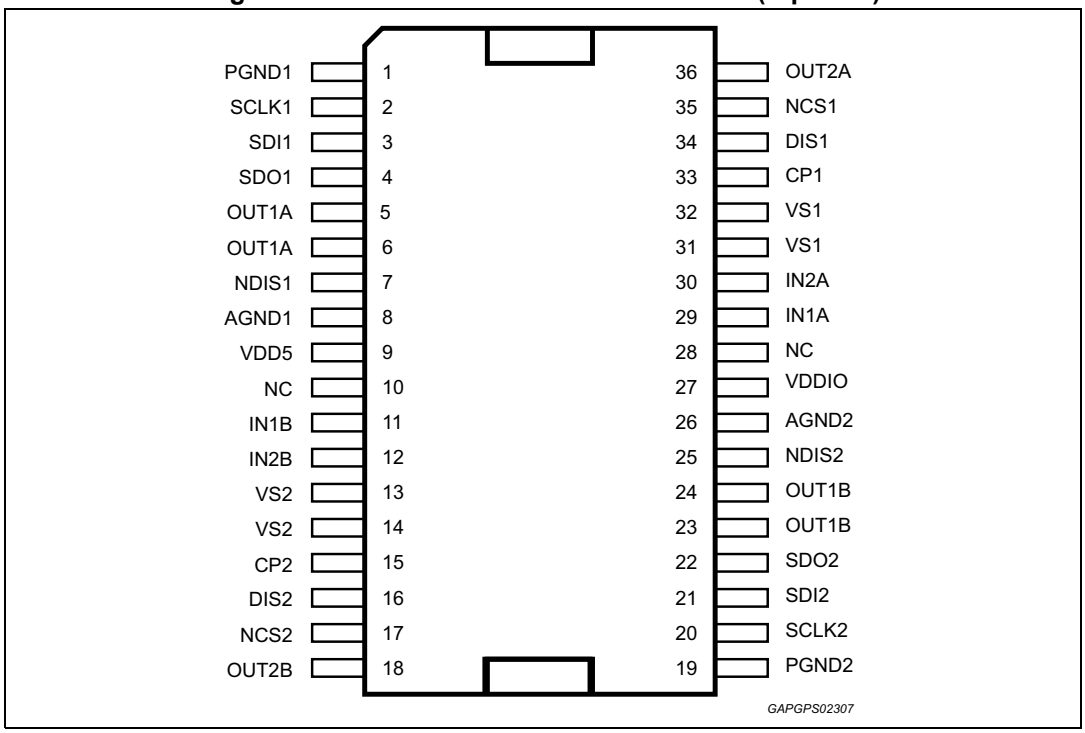


Table 2. Pin definition (PSSO36twin die) and function

Pin #	Pin name	Function	I/O Type
1	PGND1	Power Ground	GND
2	SCLK1	SPI Serial Clock Input (internal pull-down)	I
3	SDI1	SPI Data In Input (internal pull-down)	I
4	SDO1	SPI Serial Data Out. Tri-state output buffer, Transfers data to the µC	O
5	OUT1A	Output of DMOS half bridge 1 [device A]	O
6			
7	NDIS1	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.	I/O
8	AGND1	Analog Ground pin	GND
9	VDD5	Regulated 5V supply	I
10	NC	Not connected pin	
11(1)	IN1B	Input Half Bridge 1 (internal pull-down) [device B]. Acting as PWM at power-up, can be configured to IN1 via SPI frame	I
12(1)	IN2B	Input Half Bridge 2 (internal pull-down) [device B]. Acting as DIR at power-up, can be configured as IN2 via SPI frame.	I
13(1)	VS2	Power supply voltage for Power Stages (external reverse protection required)	I
14(1)			
15(1)	CP2	Tank capacitor for Charge Pump output	O
16(1)	DIS2	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)	I
17(1)	NCS2	SPI Chip Select Input (internal pull-up)	I
18(1)	OUT2B	Output of DMOS half bridge 2 [device B]	O
19(1)	PGND2	Power Ground	GND
20(1)	SCLK2	SPI Serial Clock Input (internal pull-down)	I
21(1)	SDI2	SPI Data In Input (internal pull-down).	I
22(1)	SDO2	SPI Serial Data Out	O
23(1)	OUT1B	Output of DMOS half bridge 1 [device B]. multi-bonding	O
24(1)			
25(1)	NDIS2	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.	I/O
26(1)	AGND2	Analog Ground pin	GND
27	VDDIO	Regulated 3.3/5V supply for SDO output buffer	I
28	NC	Not connected pin	-
29	IN1A	Input Half Bridge 1 (internal pull-down) [device A]. Acting as PWM at power-up, can be configured to IN1 via SPI	I
30	IN2A	Input Half Bridge 2 (internal pull-down) [device A]. Acting as DIR at power-up, can be configured as IN2 via SPI.	I

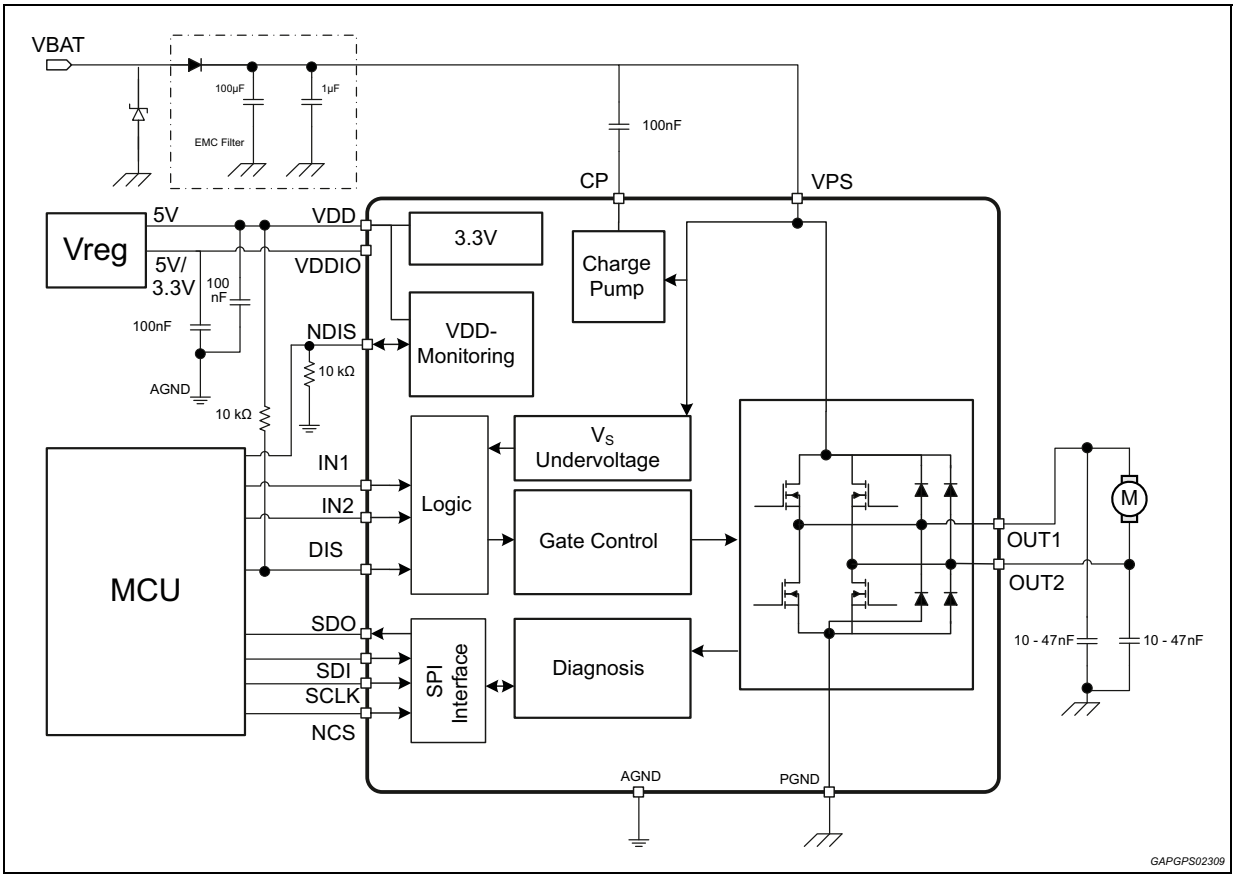
Table 2. Pin definition (PSSO36twin die) and function (continued)

Pin #	Pin name	Function	I/O Type
31	VS1	Power supply voltage for Power Stages (external reverse protection required)	I
32			
33	CP1	Charge Pump output	O
34	DIS1	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)	I
35	NCS1	SPI Chip Select Input (internal pull-up)	I
36	OUT2A	Output of DMOS half bridge 2 [device A]. multi-bonding	O
EP	AGND1	Exposed Pad connected to PCB Ground	

1. For L9960 version in PSSO36, the pins from 11 to 26 are not connected.

2 Application description

Figure 4. Application diagram



2.1 Functionality

The L9960 is dedicated to be part of an H-Bridge module for automotive applications. The module is used for DC motor driving in applications like ETC, EGR or swirl flap. The module is implemented with a microcontroller, an input filter (fulfillment of the EMC/EMI requirements) and an over-voltage protection diode (optional).

2.2 Example of application circuit

Figure 5. Application schematic (example)

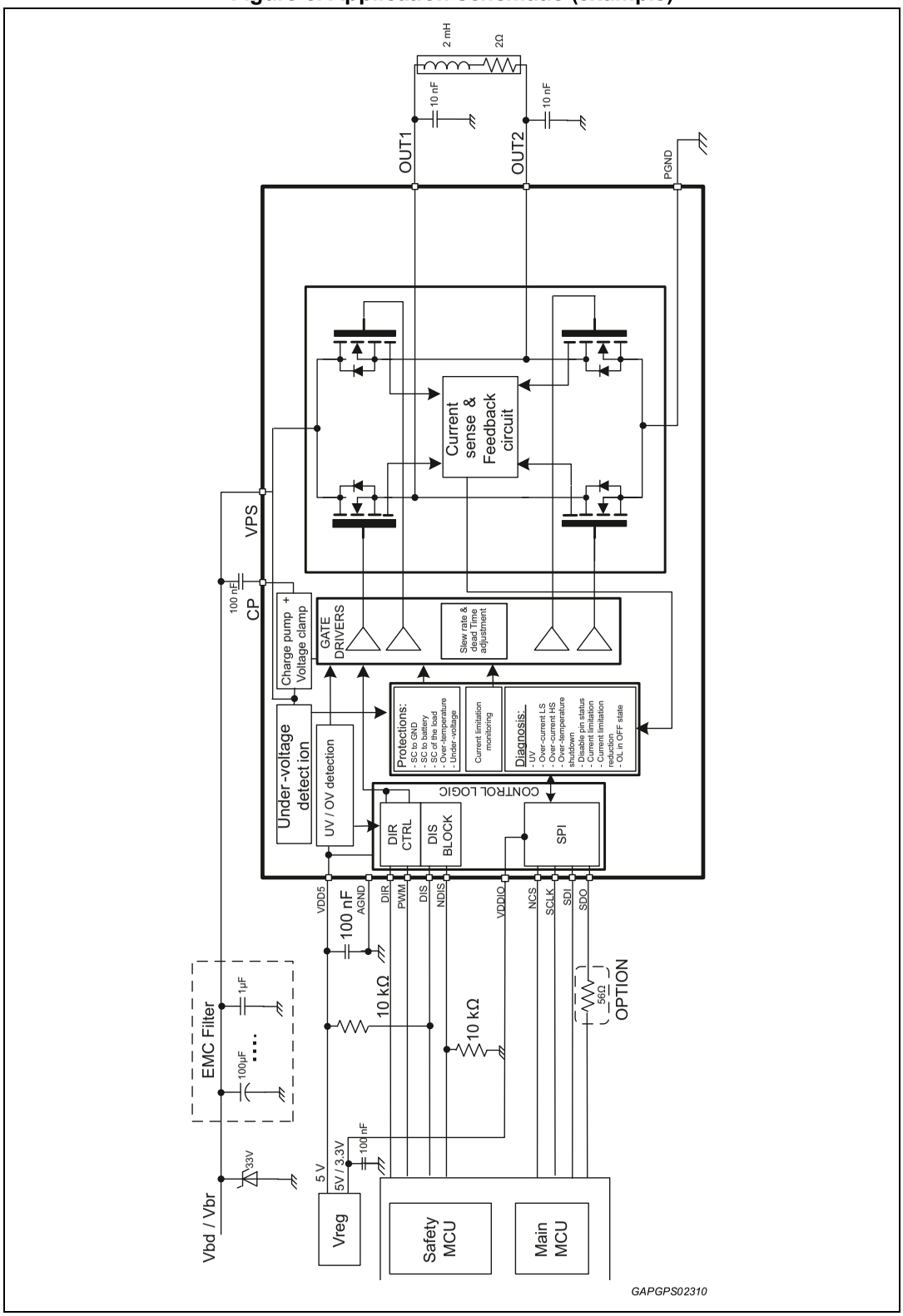
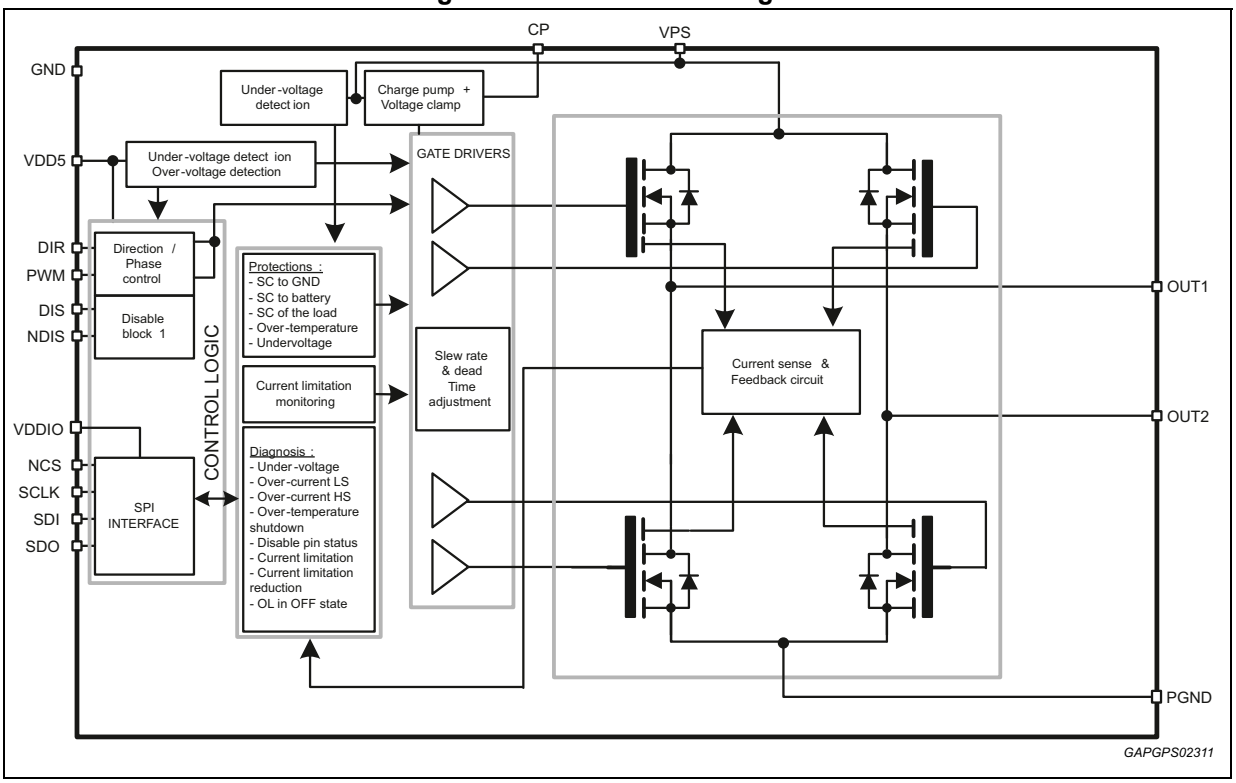


Figure 6. Detailed block diagram



3 General electrical characteristics

3.1 Absolute maximum ratings

Warning: **Warning: stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect the device reliability.**

Table 3. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{ps}	Supply voltage	Continuous	-1	40	V
$V_{out1,2}$	Output voltage	Continuous. OUT is limited by VPS	-1	40	V
VDD5	Logic supply voltage	0 V < Vps < 40 V	-0.3	19	V
VDDIO	SDO supply voltage	0V<Vps<40V	-0.3	19	V
VCP	VCP output voltage	-	-0.3	Vps+5	V
V_{IN}	Logic input voltage (NCS, SDI, SCLK, DIR, PWM, DIS, NDIS)	0 V < Vps < 40 V 0 V < VDD5 < 19 V	-0.3	19	V
V_o	Logic output voltage (SDO, NDIS)		-0.3	19	V
-	Human body model ESD compliance for pins: OUTx,VPS (not tested at ATE)(1)	HBM (100 pF/1.5 kohm)	-4	4	kV
-	Human body model ESD compliance for other pins than OUTx, VPS (not tested at ATE)	HBM (100 pF/1.5 kohm)	-2	2	kV
-	Charge Device Model ESD compliance for all pins (not tested at ATE)	CDM; according to Q100-011 classification C3B	-750 -500	750(2) 500(3)	V V
-	ISO 7637 pulses	Cf. standards	-	-	-
-	Latch-up immunity	According to JEDEC 78 class 2 level A			

1. Versus GND.
2. Corner pins.
3. All pins.

Note: Test circuit according to HBM (EIA/JESD22-A114-B) and CDM (EIA/JESD22-C101-C).

3.2 Thermal ratings

Table 4. Thermal ratings

Symbol	Parameter	Condition	Min	Max	Unit
Tstore	Storage temperature	-	-55	150	°C
$R_{Th\ j\text{-}case}$	Junction-case thermal resistance	With power applied on 2 power MOS	-	2	°C/W

3.3 Range of functionality

All voltages refer to GND.

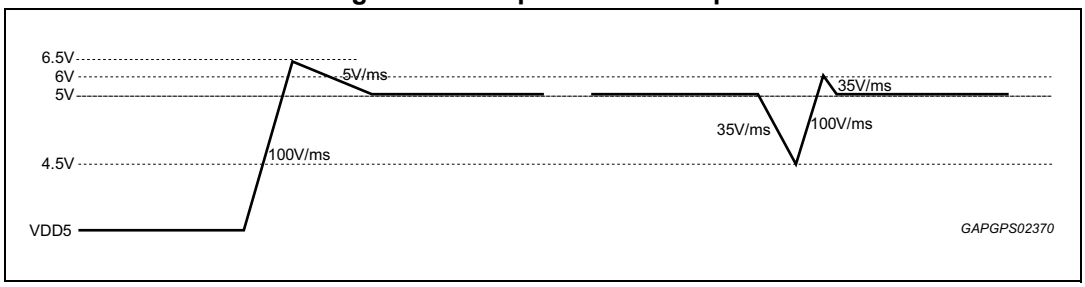
Currents are positive into and negative out of the specified pin.

Table 5. Range of functionality

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{ps}	Supply voltage	Up to 40 V for transient pulses	$V_{ps\_uv\_off}$	14	28	V
dVps/dt	Supply voltage slew rate *(Application info)*	Up to 28 V	-20		20	V/µs
VDD5	Logic supply voltage	-	VDD5_uv	5	VDD5_ov	V
dVdd5/dt	Supply voltage slew rate *(Application info)*	See shapes here below	-35		100	V/ms
V_i	Logic input voltage (SDI, SCLK, NCS, DI, NDIS, DIR, PWM)	See also Max ratings	-0.3		VDD5_ov	V
VDDIO	SDO, NDIS output voltage	-	3	-	5.5	V
f_{spi}	SPI max clock frequency	Guaranteed up to a value of 5 MHz	-	-	5	MHz
f_{pwm}	PWM frequency	Guaranteed up to a value of 20 kHz	-	-	20	kHz
T_j	Junction temperature	(1)	-40	-	170	°C
		Failure condition	170	-	OTsd	°C
R L	Equivalent load range *(Application info)*	-	0.5 0.3	-	10 10	Ohm mH

1. The device is qualified according to mission profile covering 1300 hrs at T_j = 170 °C.

Figure 7. Example of VDD5 slopes



3.4 Electrical characteristics

Tj = -40°C to 150°C unless otherwise specified.

VDD5 = 4.5V to 5.5V unless otherwise specified.

Vps = 4V to 28V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 6. Bridge output drivers

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{dson_tot}	Half bridge total Rdson (High-side + Low-Side)	T_j = -40 °C to 25 °C, I_{out} = 3 A; 4 V < V_{ps} < 7 V	-	-	300	mΩ
		T_j = 25 °C to 170 °C, $T_{case} \leq$ 140 °C I_{out} = 3 A; 4 V < V_{ps} < 7 V	-	-	450	
		T_j = -40 °C to 25 °C, I_{out} = 9 A; V_{ps} > 7V	-	-	300	
		T_j = 25 °C to 150 °C, I_{out} = 7.5 A; V_{ps} > 7 V	-	-	400	
		T_j = 25 °C to 170 °C, $T_{case} \leq$ 140 °C I_{out} = 7.5 A; V_{ps} > 7 V	-	-	450	
V_{bd_h}	Body diode forward voltage drop High-side transistor	Idiode = 9A	-	2	3	V
V_{bd_l}	Body diode forward voltage drop Low-side transistor	Idiode = 9A	-	2	3	V

3.5 Timing characteristics

Table 7. Timing characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{don}	Delay time for switch-on	R_{load} 6 Ω, ISR = 1; VSR = 1 PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	10.5	µs
		R_{load} 6 Ω, ISR = 0; VSR = 0 PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	11.5	µs
		NOSR mode: PWM edge → 10%, TSW_low_current = 0, V_{out} (or 10% I_{out})	-	-	7	µs
T_{doff}	Delay time for switch-off	R_{load} 6 Ω, ISR = 1; VSR = 1 PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	12	µs
		R_{load} 6 Ω, ISR = 0; VSR = 0 PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	13	µs
		NOSR mode PWM edge → 90%, TSW_low_current = 0, V_{out} (or 90% I_{out})	-	-	5.5	µs
T_d	Delay time: symmetry	$\lvert T_{don}-T_{doff}\rvert$ NOSR mode	-	-	5	µs
		$\lvert T_{don}-T_{doff}\rvert$ ISR/VSR mode	2	-	8	µs
T_{rise_L}	Low-side transistor rise time	Non selectable by SPI 10%-90% V_{out} , I_{load} = 3 A	0.04	-	0.5	µs
T_{fall_L}	Low-side transistor fall time		5	-	10	µs

4 Functional description

4.1 Device supply

The L9960 is supplied through 3 pins connected to 3 different external voltage supply sources:

- **VPS,** battery voltage to supply the bridge,
- **VDD5,** 5 V regulated voltage to supply chip digital I/O's,
- **VDDIO,** the supplying SDO output buffer voltage.

4.1.1 Functional State

Following functional states are defined for L9960:

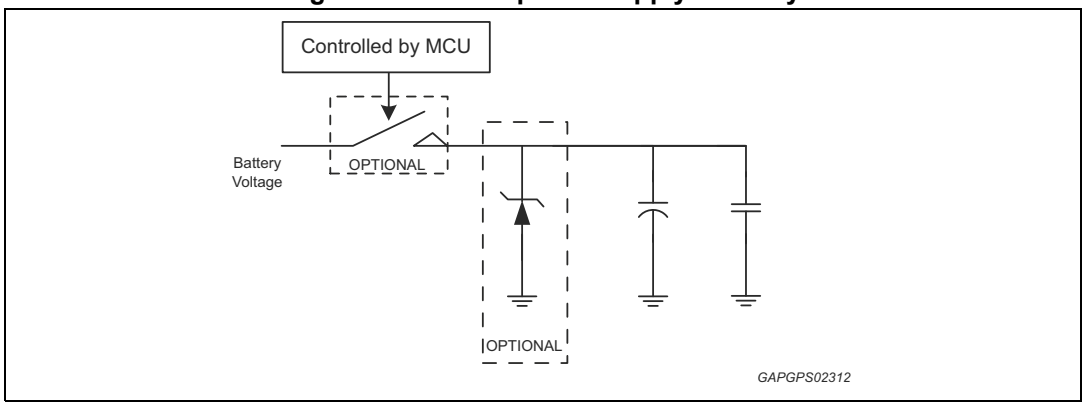
- **Normal Mode**
  - supply voltages are present and no failure. H-bridge is driven by the selected driving control mode (PWM/DIR, IN1/IN2) and it is configurable via SPI (i.e slew rate, current limitation and overcurrent thresholds, OT warning thresholds).
- **Tri-state**
  - H-bridge gate drivers are disabled due to a fault independently from PWM signal (IN1 or IN2). Once the fault condition is disappeared, L9960 restarts working without dedicated fault recovery procedure.
- **Disabled**
  - H-bridge is disabled due to a fault condition and it is necessary to execute the dedicated procedure to initialize the device (please review the below table for the dedicated procedure for each fault). In case the fault is related to an overvoltage or undervoltage on VDD5, the H-bridge is set to tri-state with **NDIS low**.

Note: Please review the dedicated Section 4.8.1: Diagnostic Reset strategy in application note.

4.1.2 Vps power supply

VPS pin is the power supply of the H-bridge. A filter could be implemented, mainly to fulfill the EMC requirements, and an over-voltage protection diode can also be added (optional).

Figure 8. External power supply circuitry



Tri-state mode power consumption

Depending on the error detection affecting L9960, the bridge is switched to tri-state. In this status the output leakage current is less than "**Iout**" (refer to *Table 22*) on the overall range of functionality (Vps and temperature ranges).

Normal and VVL modes power consumption

In normal and VVL modes, the current consumption on Vps is mainly based on the output current delivered to the load and the High-Side Power MOS supply consumption.

Battery voltage monitoring

The Vps voltage is monitored internally to detect undervoltage conditions on power supply line.

When Vps decreases below the under-voltage threshold "***Vps_uv***" longer than a filter "***Tvps_uv***", the bridge is disabled (*SPI communication is still working*).
The filtering time "***Tvps_uv***" is implemented to avoid unwanted detection due to parasitic glitches when Vps increases as well as decreases.

As soon as the voltage rises again above the Vps under-voltage threshold (***hysteresis implemented***), the bridge is switched back to normal mode driven by DIR and PWM levels (or IN1/IN2). All the settings are kept as before the under-voltage event. No PWM toggle is necessary to restart the H-bridge if the condition is disappeared.

The Vps voltage monitoring information is readable via SPI by ***VPS_UV*** bit which is not latched.

Table 8. VPS_UV

Bit status	Description	Condition
0	Vps > Vps_uv longer than Tvps_uv	Default value
1	Vps < Vps_uv longer than Tvps_uv	-

The info is available in position R0 of the answer frame 8a.

The information is also readable by ***VPS_UV_REG*** bit which is latched.

Table 9. VPS_UV_REG

Bit status	Description	Condition
0	latched Vps > Vps_uv longer than Tvps_uv	Default value
1	latched Vps < Vps_uv longer than Tvps_uv	-

The info is available in position R5 of the answer frame 8a.

Battery voltage monitoring electrical characteristics

T_j = -40 °C to 150 °C, VDD5 = 4.5 V to 5.5 V, Vps = 4 V to 28 V unless otherwise specified.

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

Table 10. VPS electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Vs_clamp_neg	Negative clamp on VPS battery line	-3 A from VPS, 3 ms	-2.5	-	-0.5	V
Vps_uv_off	Vps under-voltage threshold	Vps decreasing	3.7	-	4.2	V
Vps_uv_on	Vps under-voltage threshold	Vps increasing	4.2	-	4.7	V
Vps_uv_hys	Vps under-voltage hysteresis	-	0.1	-	1	V
Tvps_uv	Vps under-voltage filtering time (guaranteed by scan)	Digital filter	1	-	3	µs

Undervoltage protection

A counter is implemented to measure if two consecutive Vps under-voltage events occur within a fixed time frame, defined by the parameter (**UV_WIN**), which is programmable via SPI in two different values: 20 or 40 µs; if it happens, a specific bit named **"UV_CNT_REACHED"** is set to 1 and the bridge is disabled.

The **"UV_PROT_EN**" bit is used to enable the counter **UV_WIN** and an echo answer is available. In below listed tables, the configuration and functions for each of these parameters are shown:

Table 11. UV_PROT_EN

Bit status	Description	Condition
0	Counter and disabling protection are not enabled	Reset value
1	Counter and disabling protection are enabled	-

Note: (-) available in position D3 of the SPI command frame 4.

Table 12. UV_PROT_EN_echo

Bit status	Description	Condition
0	Echo counter and disabling protection not enabled	Reset value
1	Echo counter and disabling protection enabled	-

Note: (-) available in position R3 of the SPI answer frame 7b.

Table 13. UV_WIN

Bit status	Description	Condition
0	UV_WIN window is set to 20 µs	Reset value
1	UV_WIN window is set to 40 µs	-

Note: (-) available in position D0 of the SPI command frame 4.

Table 14. UV_WIN_echo

Bit status	Description	Condition
0	Echo: UV_WIN window is set to 20 µs	Reset value
1	Echo: UV_WIN window is set to 40 µs	-

Note: (-) available in position R0 of the SPI answer frame 7b.

Table 15. UV_CNT_REACHED

Bit status	Description	Condition
0	No VS under voltage events closer than UV_WIN	Default Value
1	Two VS under voltage events closer than UV_WIN	-

Note: (-) available in position R5 of the SPI answer frame 8c.

If this UV protection option is not enabled, an indefinite number of consecutive battery under-voltage events can occur with the only action taken by the device to disable the bridge, when the battery level is below **“vps_uv threshold”**.

Figure 9 and *Figure 10* show the cases of **VPS UV** events are greater or less than 2 in the time frame defined by **UV_WIN**.

Case 1 (no enabled protection)

The first VPS transition under the **VPs_uv_off** threshold is disregarded, due to the event duration less than **Tvps_uv**.

After the second UV transition on Vps, the bridge is put in tri-state. As the protection has not been enabled via **UV_PROT** bit, the H-bridge keeps on switching between On-state and tri-state.

Figure 9. Battery voltage monitoring – case1

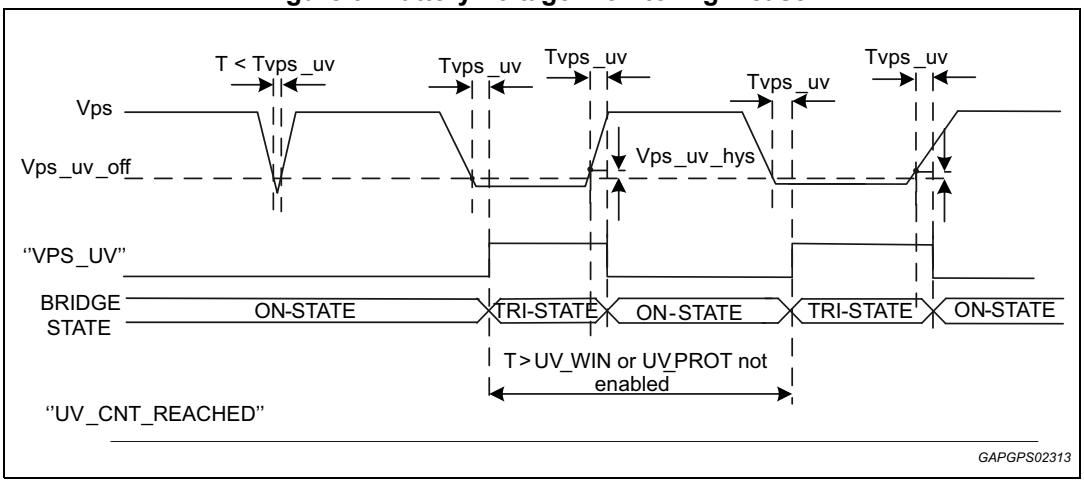
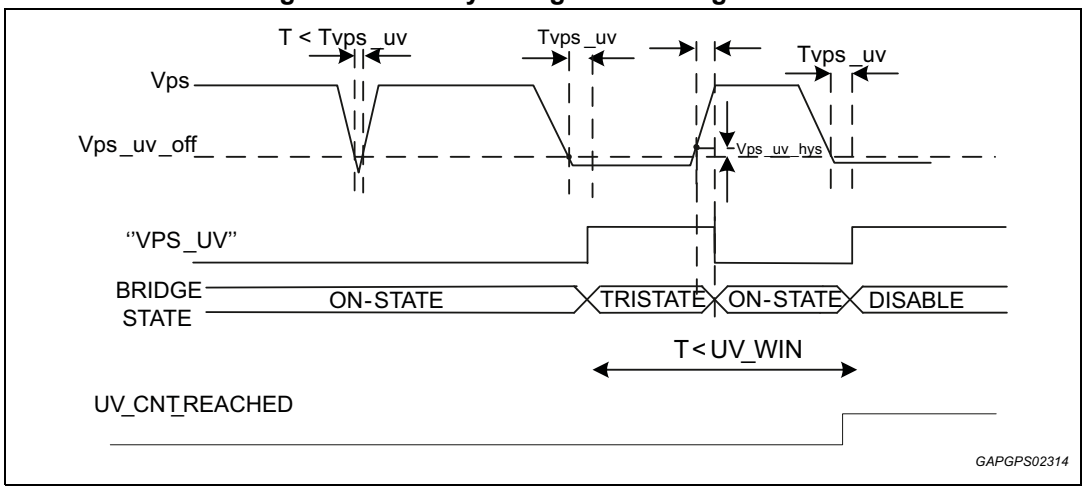


Figure 10. Battery voltage monitoring – case2



Case 2

In this scenario, after the second UV transition on VPS, with the enabled protection via **UV_PROT** set to 1, if two UV events occur by the **UV_WIN** timeframe expiration, the H-bridge is set in Disable condition consequently.

4.1.3 VDD5 regulated voltage supply

The VDD5 Input voltage is provided by an external power supply, supplying the corresponding L9960 digital I/O's.

When VDD5 is not supplied, there is only a small leakage current sank from VPS, see parametric table with condition VDD5 <0.7V.

Voltage supply range

The L9960 has a VDD5 operating voltage supply range from "***VDD5_uv***" up to "***VDD5_ov***" thresholds, however, the absolute maximum rating is defined up to 19 V DC.

VDD5 under-voltage detection

NDIS status depends on the UV event duration affecting VDD5:

- When the VDD5 voltage falls below the under-voltage detection threshold "***VDD5_uv_th***" longer than a filter "***TVDD5_uv1***", the bridge is switched to **disable**.
- When VDD5 voltage falls below the under-voltage detection threshold "***VDD5_uv_th***" longer than "***TVDD5_uv2***", the condition is feedbacked to control logic, pulling LOW the pin NDIS, **NDIS pin is pulled to LOW**.

When VDD5 voltage increases above the "*VDD5_uv_th" threshold* (hysteresis and ***TVDD5_uv1*** filtering implemented), under-voltage condition is removed and L9960 keeps all the settings set.

The NDIS pin is released when under-voltage condition is removed, in condition that NDIS was hold at least for a minimum time ***"Thold_ndis"***.

The UV detection information is readable via 2 diagnostics bits called ***VDD_UV_REG*** (latched) and ***VDD_UV*** (unlatched).

Table 16. VDD_UV_REG

Bit status	Description	Condition
0	Latched Vdd > Vdd_uv longer than Tvdd_uv1	Default Value
1	Latched Vdd < Vdd_uv longer than Tvdd_uv1	-

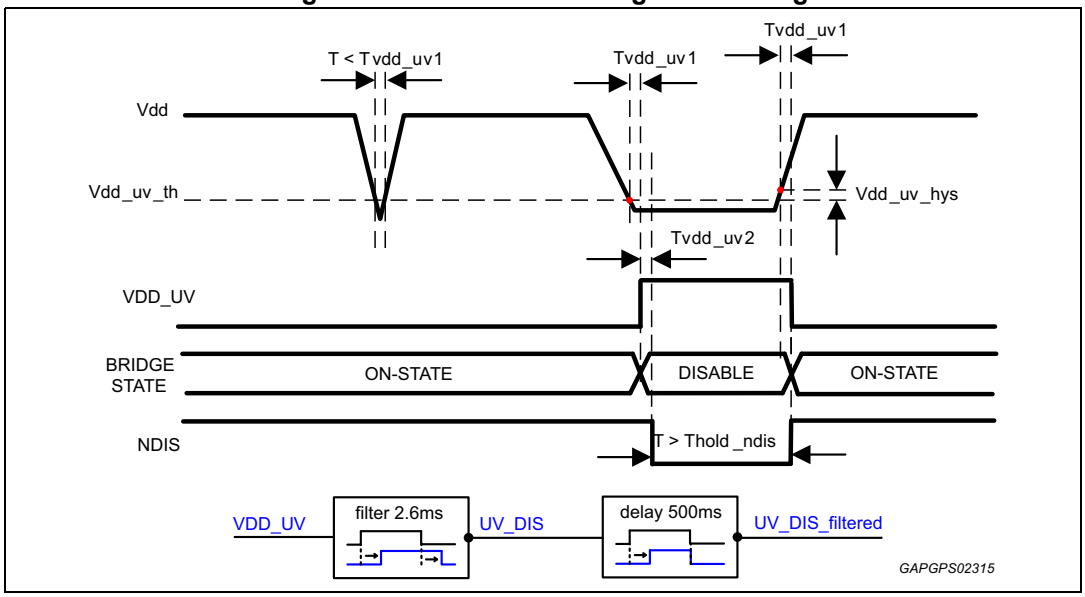
Note: (-) available in position R1 of the SPI answer frame 8a.

Table 17. VDD_UV

Bit status	Description	Condition
0	Vdd > Vdd_uv longer than Tvdd_uv1	Default Value
1	Vdd < Vdd_uv longer than Tvdd_uv1	-

Note: (-) available in position R0 of the SPI answer frame 12b.

Figure 11. VDD5 under voltage monitoring



VDD5 over-voltage protection

Although the VDD5 input pin and all I/O's withstand up to 19 V, an over-voltage circuitry is implemented to ensure that the bridge is kept in disable condition when VDD5 voltage is higher than the VDD5 over-voltage threshold (***VDD5_ov_th)*** for duration longer than "***TVDD5_ov***".

This VDD5 over-voltage condition is also feedbacked directly to NDIS pin, by pulling NDIS to LOW after the filter time "***TVDD5_ov*** ".

The NDIS pin is released when VDD5 voltage decreases below the "***VDD5_ov_th***" threshold and wait hysteresis as well as ***TVDD5_ov*** filtering implemented + **Thold_ndis** filter time are expired.

The information is readable via 2 diagnostics bits called ***VDD5_OV_REG*** (latched) and ***VDD_OV*** (unlatched).

Table 18. VDD_OV_REG

Bit status	Description	Condition
0	Latched Vdd < Vdd_ov_th longer than Tvdd_ov	Default Value
1	Latched Vdd > Vdd_ov_th longer than Tvdd_ov	-

Note: (-) available in position R2 of the SPI answer frame 8a.

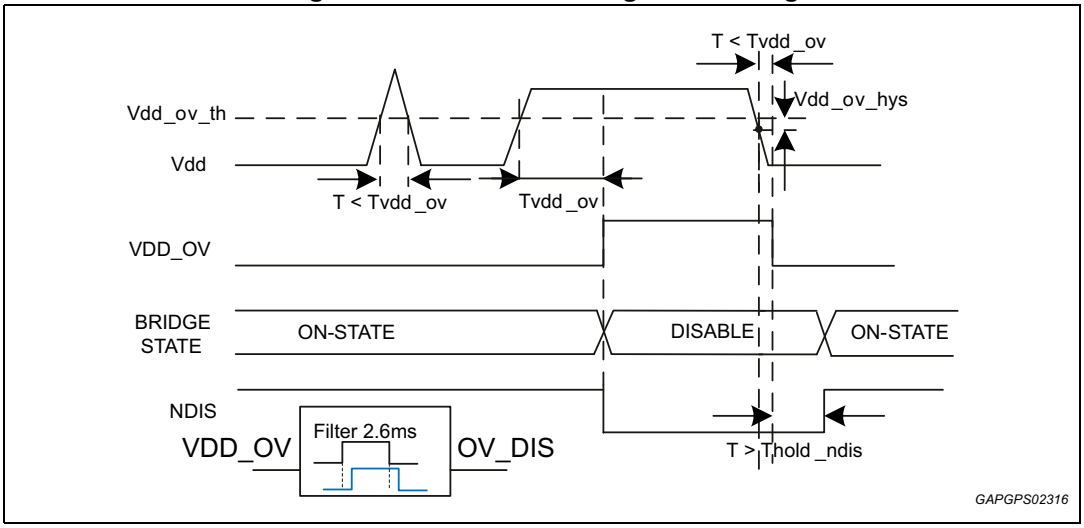
Table 19. VDD_OV

Bit status	Description	Condition
0	Vdd < Vdd_ov_th longer than Tvdd_ov	Default value
1	Vdd > Vdd_ov_th longer than Tvdd_ov	-

Note: (-) available in position R1 of the SPI answer frame 12b.

In case of VDD5 over-voltage condition, the bridge is kept in disable until the over-voltage condition is removed (hysteresis as well as ***TVDD5_ov*** filtering implemented).

Figure 12. VDD5 over voltage monitoring



This information is filtered, and reported in **NGFAIL** (*Global Failure Bit NGFAIL definition on page 64*).

A counter is available to inform about the overvoltage event length *(guaranteed by scan)*.

The counter starts as soon as ***VDD5_OV*** event occurs.

The counter stops for the following conditions:

- when its max value was reached,
- when the ***VDD5_OV*** condition is removed.

The ***VDD5_OV*** length information is readable in a latched 3 bits word called ***VDD5_OV_L***.

These 3 bits define the time range of the current counter value, according to the following table:

Table 20. VDD_OV_L[2:0]

Bit status	min	max	Condition
000	not used	-	-
001	No VDD_OV event	-	default value
010	T_vdd_ov	10 ms	-
011	10 ms	30 ms	-
100	30 ms	100 ms	-
101	100 ms	300 ms	-
110	300 ms	1000 ms	-
111	1000 ms	-	-

Note: (-) available in positions R11/R10/R9 of the SPI answer frame 12a.

- A new ***VDD5_OV*** event overwrites previous **VDD5_OV** length, except if the new event length is shorter than the value defined in ***VDD5_OV_L***.
- A reading of ***VDD5_OV_L*** through SPI clears the current value; if event is still present when SPI reading occurs, the counter restarts counting until **VDD5_OV** condition is removed or counter itself has reached its max value.