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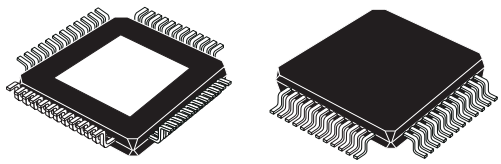
L99ASC03G

Brushless / sensorless 3-phase motor pre-driver for automotive applications

Datasheet - production data



TQFP48-EP

Features

- AEC-Q100 qualified
- 5 V low-drop voltage regulator (200 mA continuous mode)
- Very low current consumption in standby mode (typ. 15 µA)
- ST SPI interface for control and diagnostics
- Window watchdog and fail-safe functionality
- Two separate power supply pins
- Three half-bridge drivers to control external MOSFETs (configurable by SPI)
- Full drive of external MOSFETs down to 6 V input voltage
- Input pin for each gate driver (with cross-current protection)
- Two-stage charge pump supporting 100% duty cycle
- PWM operation up to 80 kHz (not restricted)
- Current-sense amplifier (configurable by SPI)
- Disable input to turn off gate driver outputs
- Analog multiplexer output to monitor external power supply voltages and internal junction temperature
- Advanced BEMF detection IP
- Overcurrent protection (programmable)
- Drain-source monitoring and open-load detection
- TQFP48 7 x 7 x 1 mm with Exposed Pad (4.5 x 4.5 mm) package

Applications

Mechatronic three-phase motor application such as engine cooling fans, fuel pumps, water pumps, oil pumps

Description

The L99ASC03G is a multifunctional system IC designed for three-phase motor control applications.

The device features a voltage regulator to supply an external microcontroller and an operation amplifier for motor current sensing. It is designed to control six external N-channel MOSFETs in bridge configuration to drive three-phase motors in automotive applications. All gate driver outputs are controlled by separate inputs.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, control all operating modes and read out diagnostic information.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and real
TQFP48-EP	L99ASC03G	L99ASC03GTR

Contents

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1 Block diagram and pin descriptions

Figure 1. Block diagram

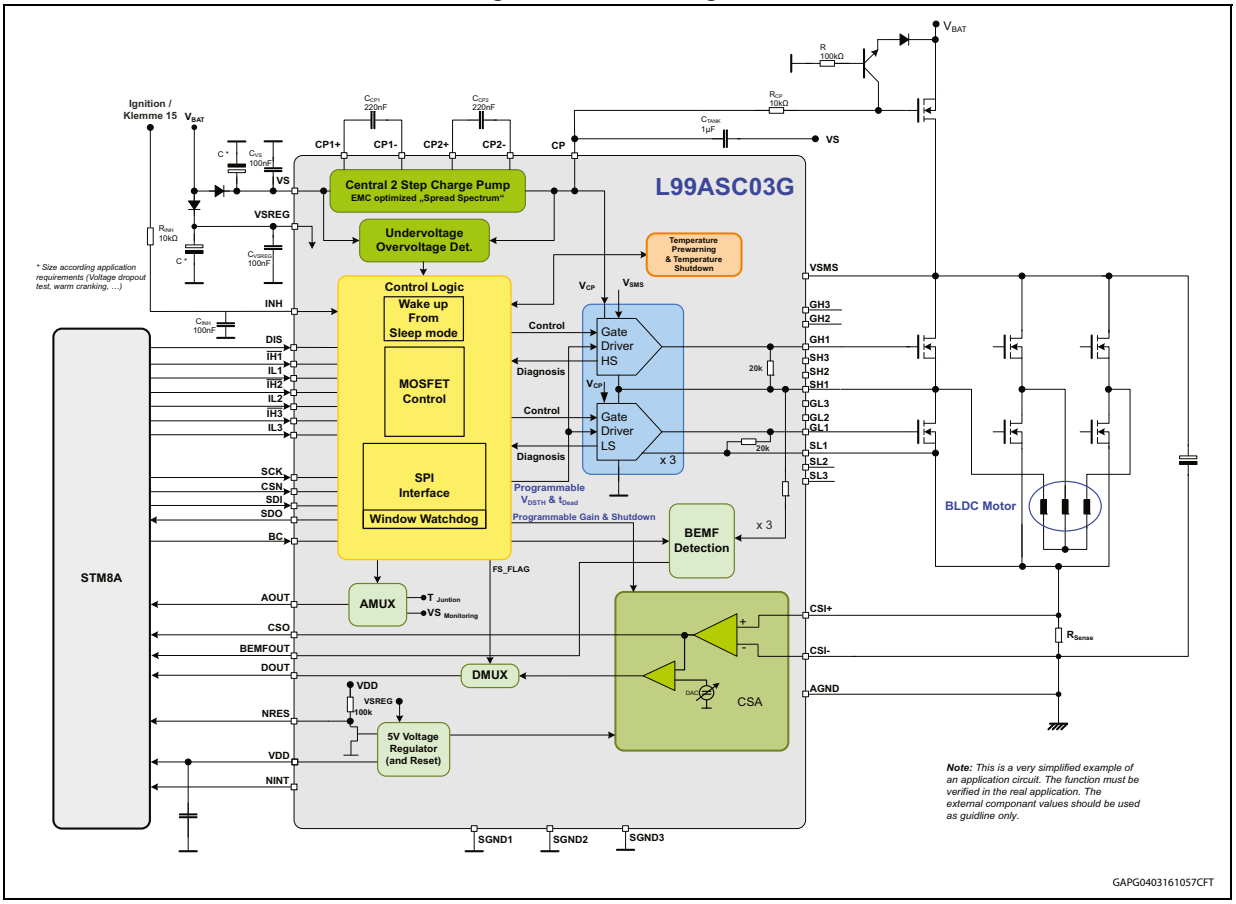


Table 2. Pin definition and function

Pin number	Symbol	Function	I/O type
1	SL3	Source of external low-side MOSFET 3	I/O
2	CSI+	Current-sense amplifier positive input	I
3	CSI-	Current-sense amplifier negative input	I
4	SGND2	Signal Ground 2	GND
5	CSO	Current-sense amplifier output	O
6	IL3	Input of low-side switch 3	I
7	$\overline{IH3}$	Input of high-side switch 3	I
8	IL2	Input of low-side switch 2	I
9	$\overline{IH2}$	Input of high-side switch 2	I
10	IL1	Input of low-side switch 1	I
11	$\overline{IH1}$	Input of high-side switch 1	I

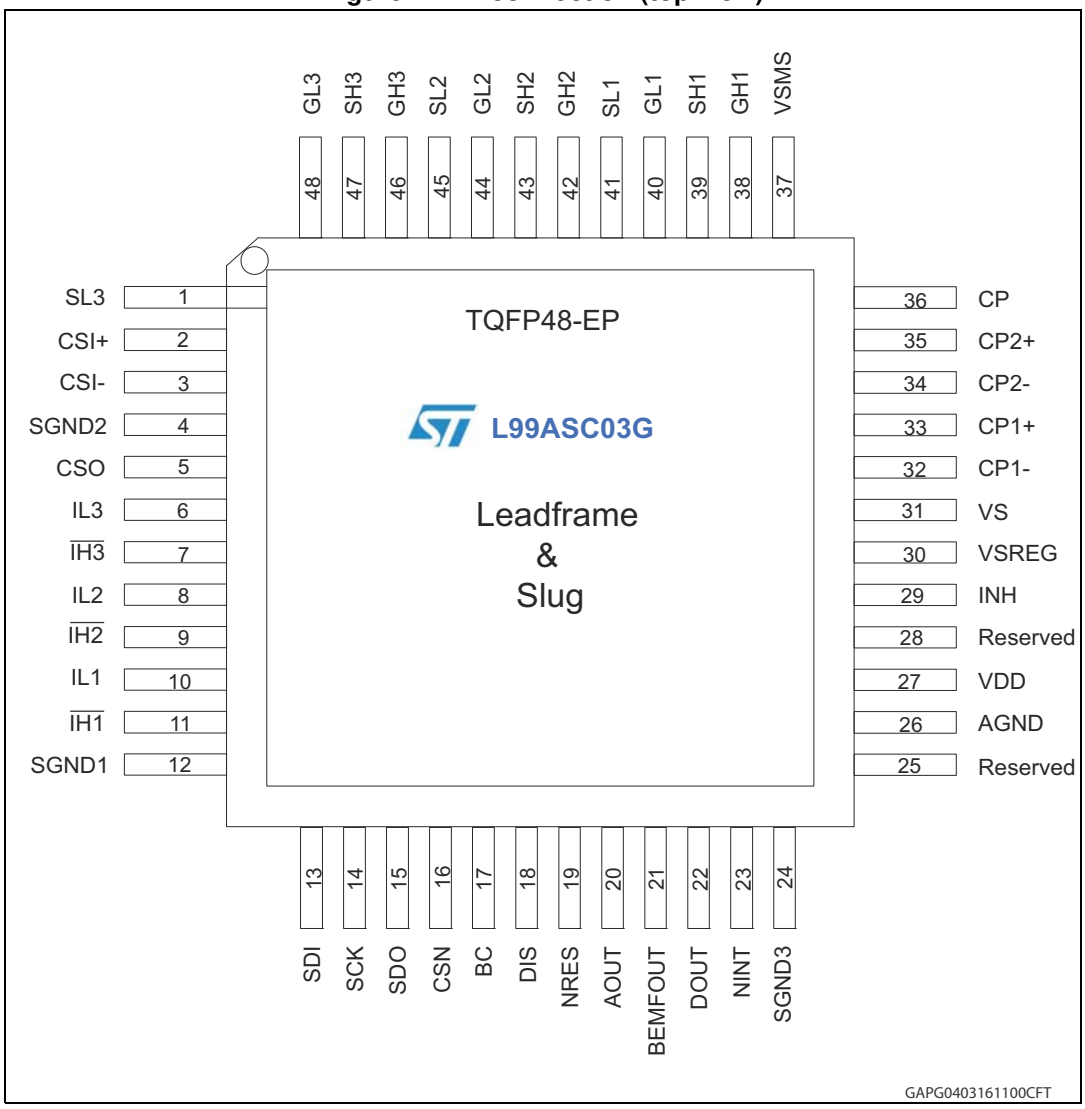
Table 2. Pin definition and function (continued)

Pin number	Symbol	Function	I/O type
12	SGND1	Signal ground 1	GND
13	SDI	SPI Serial data input	I
14	SCK	SPI clock input	I
15	SDO	SPI Serial data output	O
16	CSN	SPI Chip Select Not input	I
17	BC	Block Commutation Sync Pin	I
18	DIS	Disable input	I
19	NRES	NReset output	O
20	AOUT	Analog multiplexer output	O
21	BEMFOUT	Back EMF output	O
22	DOUT	Digital multiplexer output	O
23	NINT	Interrupt output	O
24	SGND3	Signal ground 3	GND
25	Reserved	Pin must be kept not connected	Not to be connected
26	AGND	Analog ground	GND
27	VDD	Voltage regulator output	O
28	Reserved	Pin must be kept not connected	Not to be connected
29	INH	Inhibit input (wake-up)	I
30	VSREG	Voltage regulator power supply	I
31	VS	Charge pump power supply	I
32	CP1-	Charge pump pin for capacitor 1, negative side	O
33	CP1+	Charge pump pin for capacitor 1, positive side	O
34	CP2-	Charge pump pin for capacitor 2, negative side	O
35	CP2+	Charge pump pin for capacitor 2, positive side	O
36	CP	Charge pump output	O
37	VSMS	Motor supply sense pin	I
38	GH1	Gate of external high-side MOSFET 1	O
39	SH1	Source of external high-side MOSFET 1	I/O
40	GL1	Gate of external low-side MOSFET 1	O
41	SL1	Source of external low-side MOSFET 1	I/O
42	GH2	Gate of external high-side MOSFET 2	O
43	SH2	Source of external high-side MOSFET 2	I/O
44	GL2	Gate of external low-side MOSFET 2	O

Table 2. Pin definition and function (continued)

Pin number	Symbol	Function	I/O type
45	SL2	Source of external low-side MOSFET 2	I/O
46	GH3	Gate of external high-side MOSFET 3	O
47	SH3	Source of external high-side MOSFET 3	I/O
48	GL3	Gate of external low-side MOSFET 3	O

Figure 2. Pin connection (top view)



2 Device description

2.1 Supply pins (V_S, V_{SREG}, V_{SMS})

The device has three different supply input pins. V_S and V_{SREG} have to be protected against negative voltages, while V_{SMS} is robust against negative voltages.

The two-stage charge pump is supplied from V_S. External capacitors are used to achieve high current capability of the charge pump. The gate drivers (for both high-side and low-side MOSFETs) are supplied from the charge pump to ensure full drive of the external MOSFETs.

The internal power-on reset (POR) circuitry and the V_{DD} voltage regulator are supplied from the V_{SREG} pin. Some external protection has to be provided in the application for V_S and V_{SREG} to prevent the capacitor connected to these pins from being discharged by negative transients or low input voltage.

V_{SMS} is used to monitor the power supply of the external MOSFETs and as a reference for the BEMF detection.

2.1.1 V_S, V_{SREG} and V_{SMS} overvoltage warning

In case any of the supply inputs reach the overvoltage warning threshold, the corresponding overvoltage warning flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the warning is no longer present.

2.1.2 V_S, V_{SREG} and V_{SMS} overvoltage

In case any of the supply inputs reach the overvoltage threshold, the corresponding overvoltage flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the overvoltage is no longer present.

In case of V_S and V_{SMS} overvoltage, the gate drivers are disabled, along with other functions (for further details see *Table 5*). V_{SREG} overvoltage is used only for information.

2.1.3 V_S, V_{SREG} and V_{SMS} undervoltage

In case any of the supply inputs reach the undervoltage threshold, the corresponding undervoltage flag is set. This flag can be cleared by an SPI “Read & Clear” command provided that the cause of the undervoltage is no longer present.

The V_s, V_{SMS} and V_{SREG} undervoltage flags are used only for information.

2.2 V_{DD} (5V) voltage regulator

The device integrates a fully protected low-drop voltage regulator, which is designed for very fast transient response.

The voltage regulator provides a 5 V output and a continuous load current up to 200 mA to supply external devices (e.g.an external microcontroller). In addition, this regulator powers the internal 5 V loads such as the I/O pins and the current-sense amplifier (CSA). The voltage regulator is protected against overload and overtemperature. The output voltage is

stable for output capacitor greater than/equal to 660 nF (ESR < 50 mΩ) close to the device. An additional external capacitor up to 47 µF is permitted.

In case of a short circuit to GND on V_{DD} when V_{DD} is turned on (V_{DD} < V_{DDFAIL} for at least 4 ms), the device automatically enters the V_{BAT} Standby Mode and the V_{DDFAIL} flag is set. Reactivation of the device is possible through a wake-up event. The V_{DDFAIL} flag can be cleared by an SPI “Read & Clear” command, once the short circuit is removed and the device leaves the V_{BAT} Standby Mode.

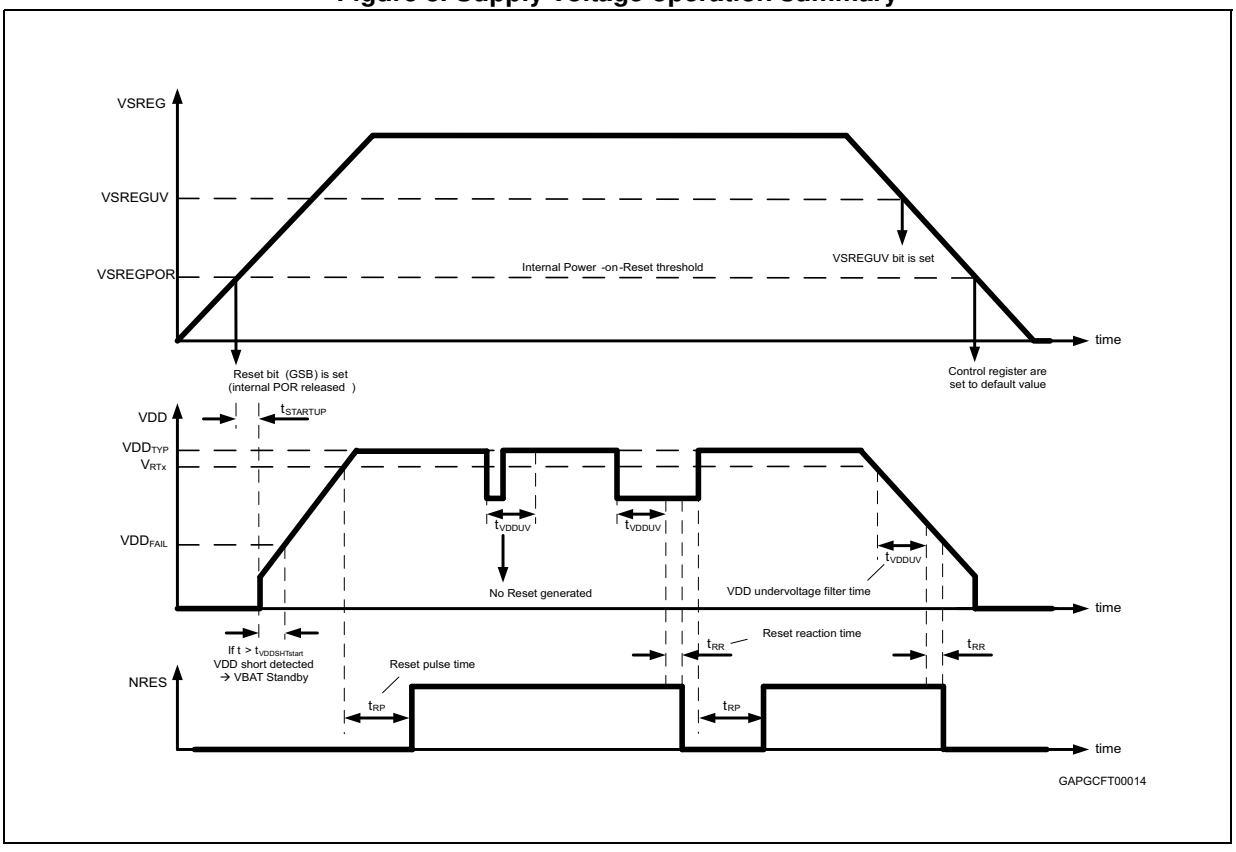
2.3 NRES reset output

In case the V_{DD} regulator is turned on and its output voltage rises above the V_{DD} reset threshold, the reset pin NRES is pulled up to V_{DD} by an internal pull-up resistor after a delay equal to t_{RP} (typ. 2 ms).

A reset pulse is generated if:

- V_{DD} drops below the V_{DD} reset threshold (VRT1 or VRT2, configurable by SPI through the VDD_VTH bit). In this case, the V_{DDUV} flag is also set and can be cleared by an SPI "Read & Clear" command, once the V_{DD} rises back above the programmed VDD_UV threshold.
- a watchdog failure occurs.

Figure 3. Supply voltage operation summary



2.4 Watchdog

A window watchdog is integrated in the device. The watchdog supervises the operation of the external microcontroller in Active Mode and, if the ICMP bit is set to '0' and $I_{VDD} > I_{CMP}$, also in V_{DD} Standby Mode.

When the device powers up and the NRES pin is released, the watchdog is started with a long open window (typ. 65 ms). The microcontroller has to write the WDTRIG bit to '1' within this time in order to terminate the long open window and start the window watchdog. After that, the watchdog has to be serviced properly by alternating the logic value written to the WDTRIG bit within the watchdog open window. A correct watchdog trigger immediately starts the next cycle.

After eight consecutive watchdog failures, the V_{DD} regulator is turned off for a time equal to t_{VDDoff} (typ. 200 ms). In case seven additional and consecutive watchdog failures occur, the V_{DD} regulator is completely turned off and the device enters V_{BAT} Standby Mode.

A watchdog failure causes a reset pulse at the NRES pin and the deactivation of the gate drivers (fail-safe condition, for further details see *Table 5*).

When the device is in Flash Mode, the watchdog is disabled. Besides even in V_{DD} Standby Mode with I_{CMP} = 1 the WDG is always disabled. If the WDDIS bit is set to '1' in Flash Mode and then a transition to Active Mode occurs, the watchdog remains disabled in Active Mode until the next POR.

After a WDG failure event, after a VDD_UV event or after a wake event from V_{BAT} Standby Mode the watchdog starts again in LOW mode. Once properly toggled the WDGTRIG bit, writing the same WDGTRIG bit value anywhere within the WDG window does not generate any WDG failure event.

Figure 4. Watchdog in normal operation mode (part 1)

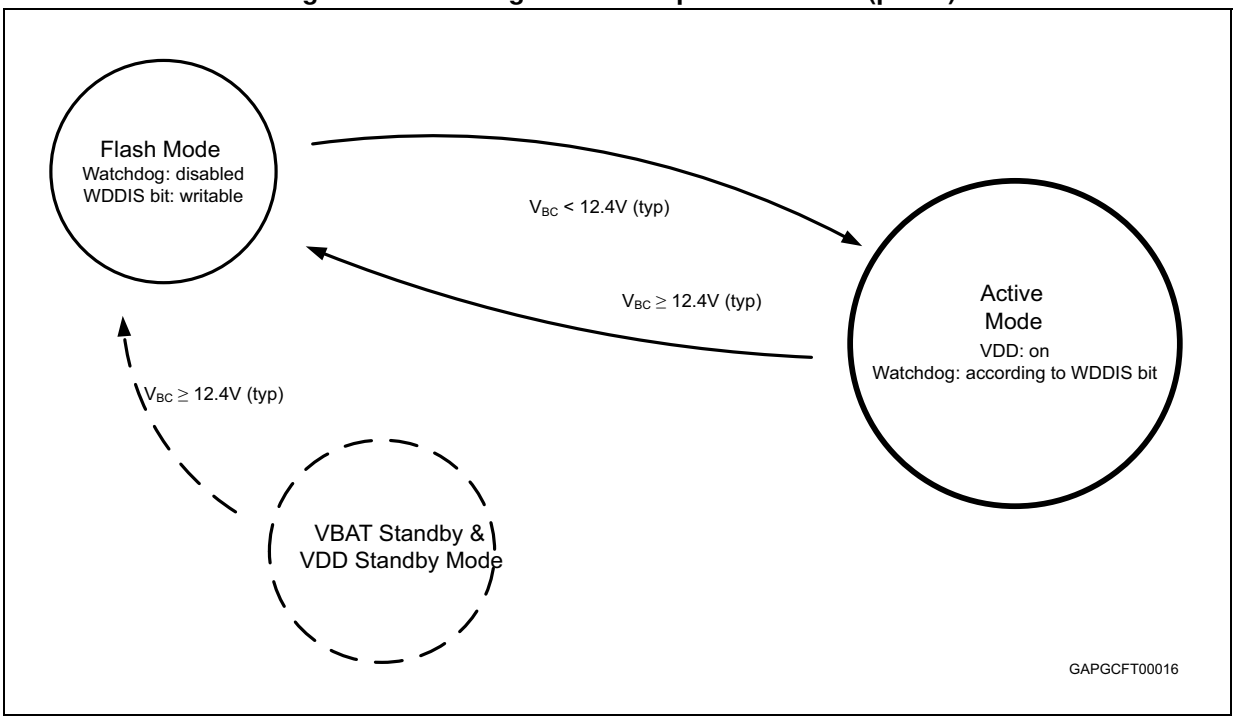


Figure 5. Watchdog in normal operation mode (part 2)

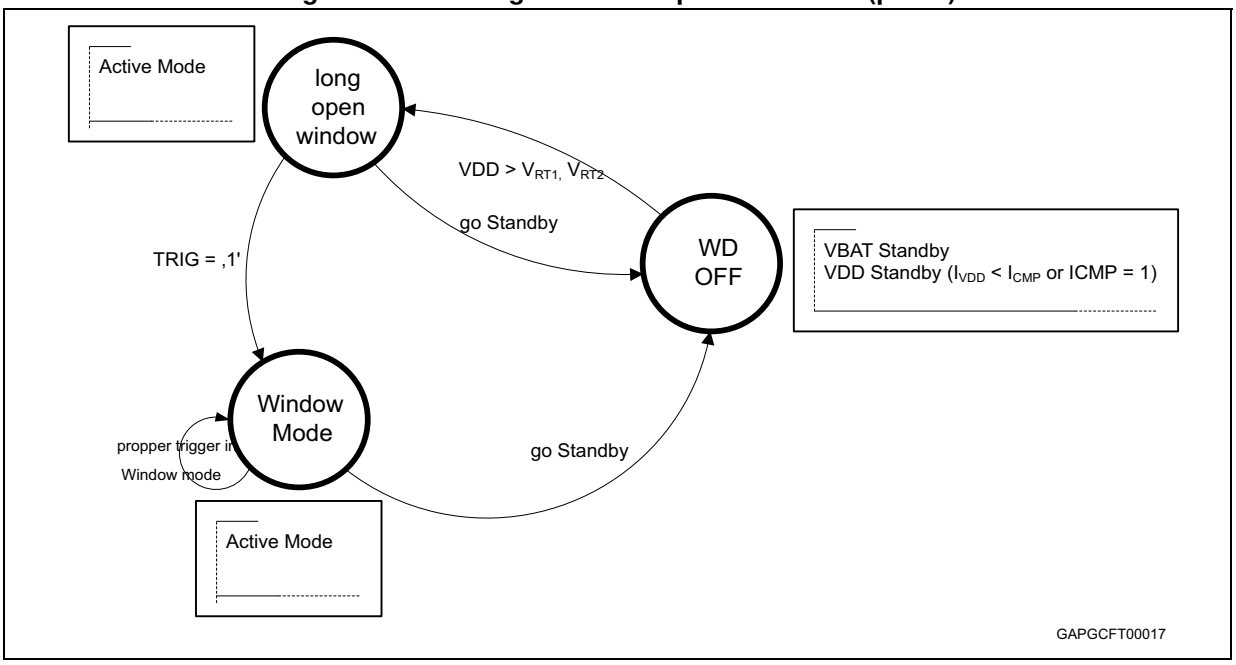


Figure 6. Watchdog in Flash Mode

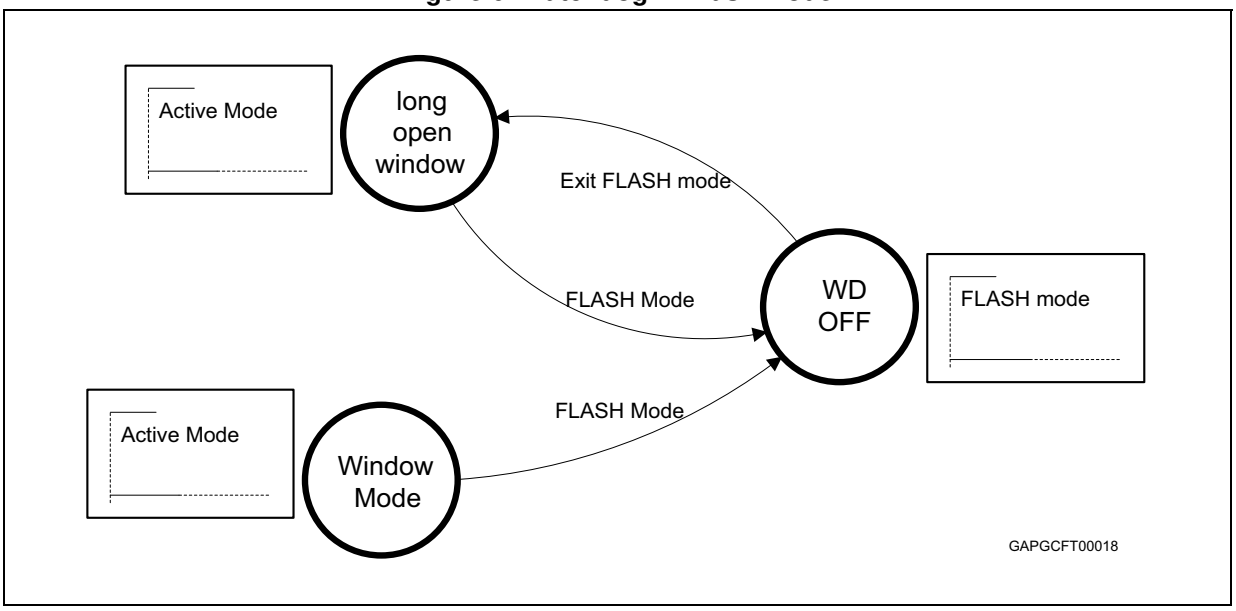
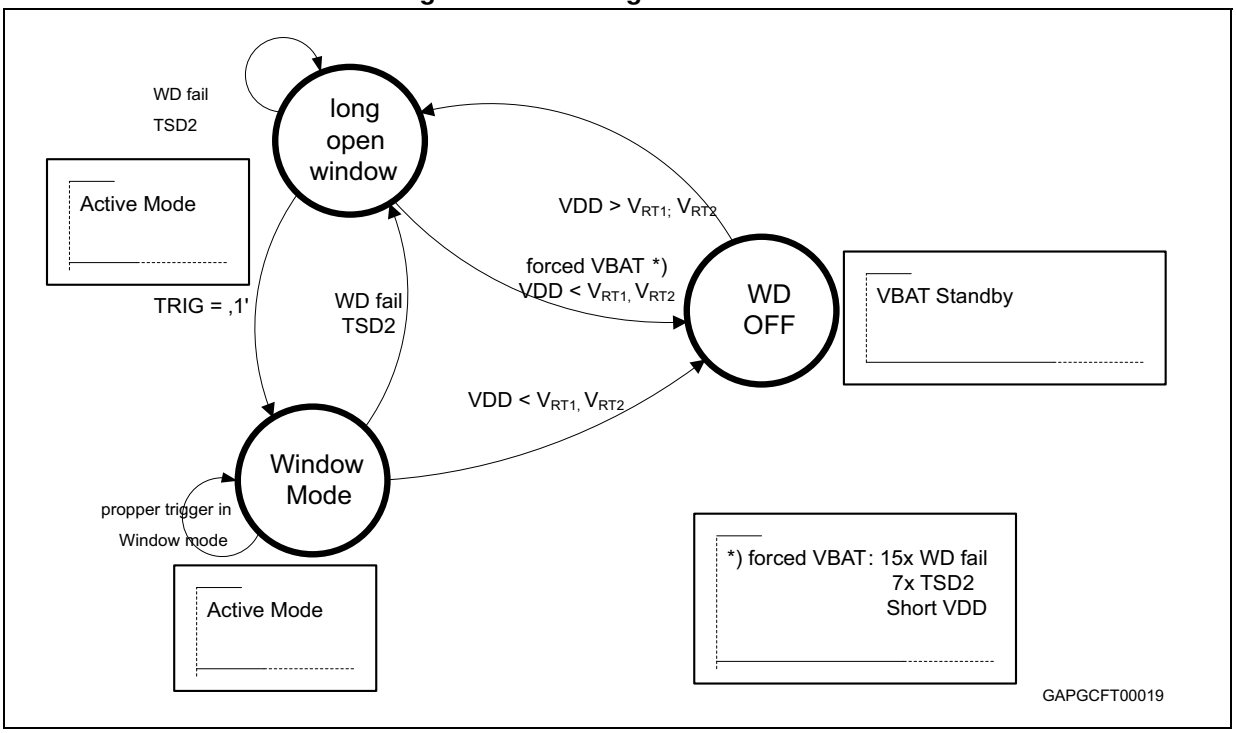


Figure 7. Watchdog in failure mode



2.5 Device operating modes

The device can be operated in four different modes:

- **Active Mode**
- **Flash Mode**
- **VDD Standby Mode**
- **VBAT Standby Mode**

2.5.1 Active Mode

The device operates with all its functions being available (VDD regulator, watchdog, gate drivers, etc).

2.5.2 Flash Mode

To program the system microcontroller, the L99ASC03G can be operated in Flash Mode where the internal watchdog is disabled and the other functions (see *Table 3*) remain available. Flash mode is entered by applying on the BC pin a voltage higher than $V_{BC,rising}$; to guarantee the proper behavior of the device, the rising V_{BC} slope must not exceed 10 V/µs.

In case $V_{BC} = V_{BC,rising}$ during device power-up (V_{SREG} connecting to VBAT), it has to be assured that the SDI pin is at GND level (V_{SDI} < 1.3 V, no external pull-up).

2.5.3 VDD Standby Mode

When the device is in VDD Standby Mode, the gate drivers, the charge pump and the CSA are disabled (SPI activation or INH pin will act as a wake-up). To supply the microcontroller in a low-power mode, the VDD voltage regulator remains active. After any wake-up event, the device switches to Active Mode and a negative pulse (typ. 56 µs) is generated on NINT pin.

The transition from Active Mode to VDD Standby Mode is selected through the STBYSEL and the GOSTBY bits.

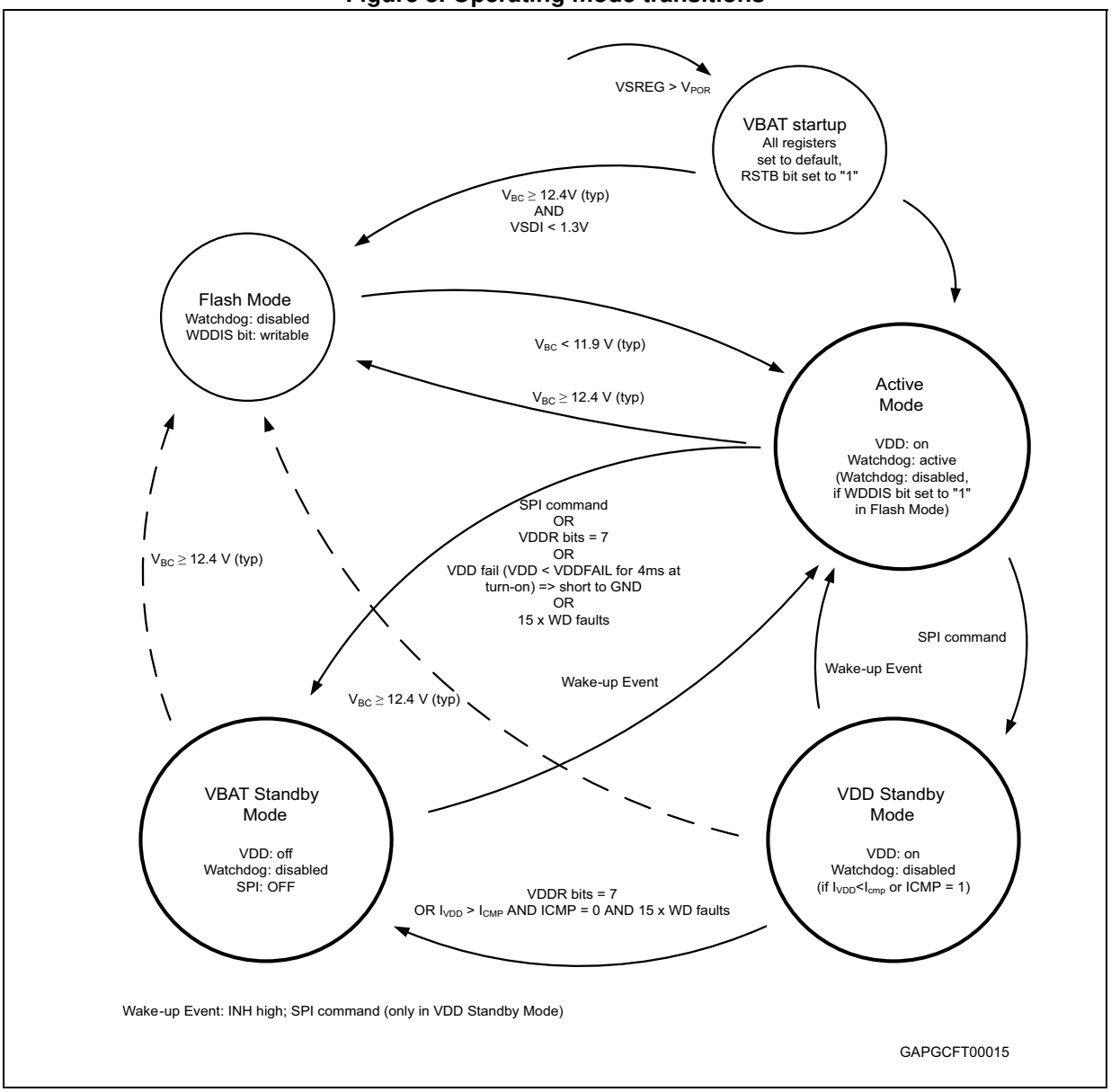
2.5.4 VBAT Standby Mode

When in VBAT Standby Mode, the VDD voltage regulator is turned off to achieve the lowest current consumption and the device monitors the occurrence of a wake-up event. After any wake-up event, the device transitions to Active Mode. The internal SPI register content is preserved.

The transition from Active Mode to VBAT Standby Mode is selected through the STBYSEL and the GOSTBY bits. This transition can also occur in case of persistent fault conditions.

2.5.5 Device mode state diagram

Figure 8. Operating mode transitions



2.5.6 Functional overview

Table 3. Functional overview

Function	Operating mode				
	Active mode		FLASH mode	VDD standby	VBAT standby
	Normal	Fail-safe			
VDD voltage regulator	ON(1)		ON	ON	OFF
Reset generator	ON		ON	ON	OFF
Interrupt generator	OFF		OFF	ON	ON
Window watchdog	ON		OFF	OFF(2)	OFF
Gate driver	ON	OFF	ON	OFF	OFF
Charge pump	ON	OFF	ON	OFF	OFF
CSA	ON	OFF	ON	OFF	OFF
BEMF module	ON	OFF	ON	OFF	OFF
Oscillator	ON		ON	OFF(3)	OFF(3)
Diagnostics	ON		ON	OFF(4)	OFF

1. OFF in case T_j > TSD2
2. ON when I_{VDD} > I_{CMP} and SPI bit I_{CMP} = 0
3. ON during wake-up event, temperature and I_{CMP} filtering
4. Temperature, I_{CMP} monitoring and V_{DD} undervoltage detection are active

2.6 DIS pin

The DIS pin allows turning off the gate drivers when applying an external signal to it. A logic low signal enables the gate drivers, whereas a logic high signal disables the gate drivers. The state of the DIS pin is reported in the DISABLE flag. To activate the gate drivers, the DIS pin has to be pulled low and the DISABLE flag has to be cleared by an SPI "Read & Clear" command. An internal pull-up resistor is integrated for this pin.

2.7 INH pin

The INH pin can be used as a wake-up source connected to ignition through an external resistor. An internal comparator detects a high level and generates a wake-up event. The INHST bit reflects the current logic state of this pin.

2.8 Thermal warning and thermal shutdown

To allow for different application requirements, two temperature modes with their respective diagnostics can be selected via SPI.

2.8.1 Normal mode: TEMPM = ‘0’ (TW1, TSD1, TSD2)

If the junction temperature reaches the TW1 threshold, the TW1 flag is set and latched as a thermal warning for the external microcontroller. In case the junction temperature increases and reaches the TSD1 threshold, the gate drivers and the charge pump are disabled and the TSD1/TW2 flag is set and latched. If the junction temperature rises further and reaches the TSD2 threshold, the VDD regulator is also turned off to reduce power dissipation and the TSD2 flag is set and latched. A counter (VDDR bits) is increased upon the VDD turn-off. After a time equal to t_{TSD}, the VDD regulator is turned on again. If the VDDR bits reach the '111' state, the device is forced into VBAT Standby Mode. This mode is left upon any wake-up event.

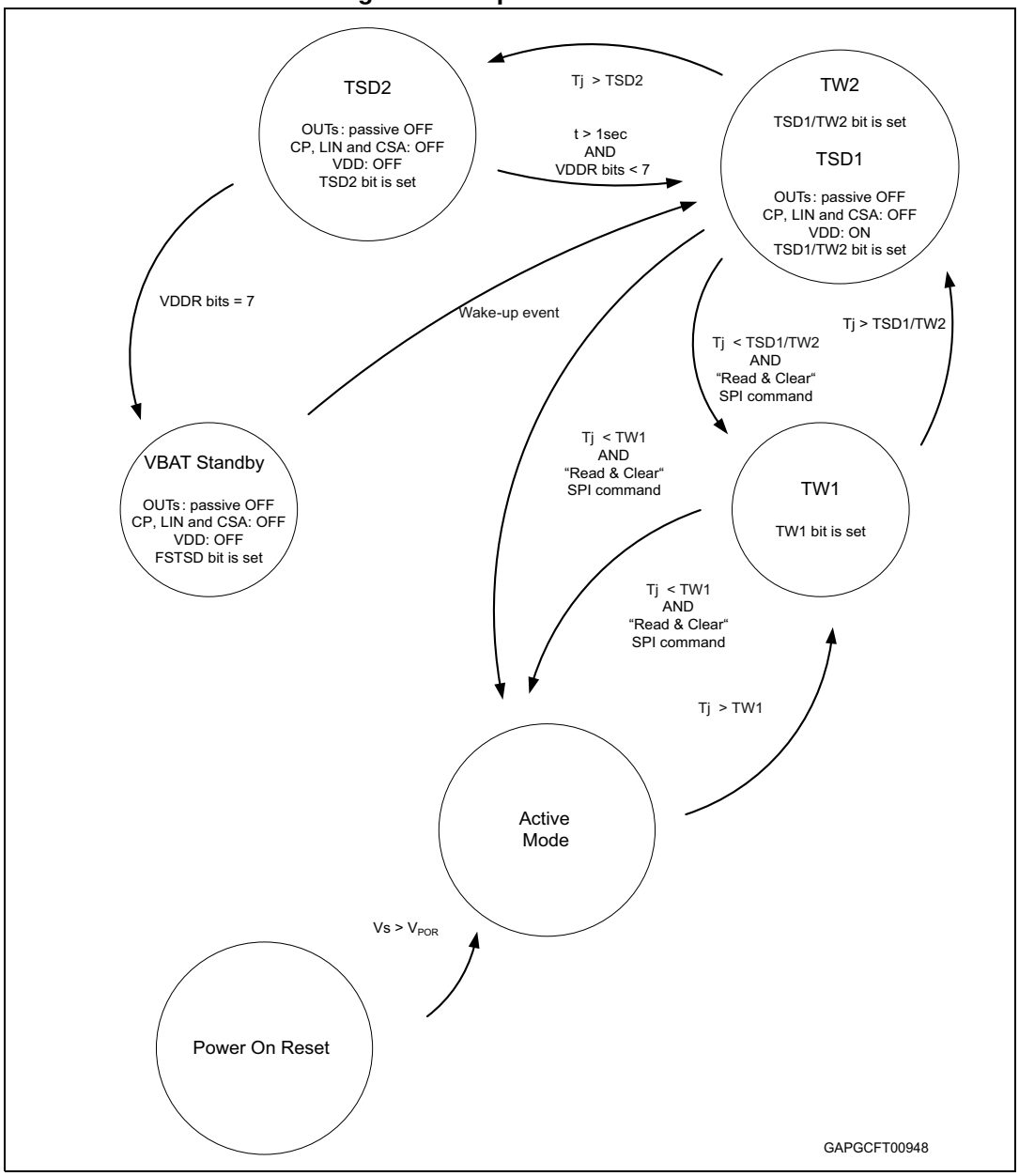
The TW1, TSD1/TW2 and TSD2 flags can all be cleared by an SPI Read & Clear command, provided that the junction temperature is below the respective temperature threshold.

2.8.2 Warning mode: TEMP = ‘1’ (TW1, TW2, TSD2)

If the junction temperature reaches the TW1 threshold, the TW1 flag is set and latched as a first thermal warning for the external microcontroller. In case the junction temperature increases and reaches the TW2 threshold, the TSD1/TW2 flag is set and latched as a second thermal warning. If the junction temperature rises further and reaches the TSD2 threshold, the gate drivers and the charge pump are disabled, the VDD regulator is turned off to reduce power dissipation and the TSD2 flag is set and latched. A counter (VDDR bits) is increased upon the VDD turn-off. After a time equal to t_{TSD}, the VDD regulator is turned on again. If the VDDR bits reach the '111' state, the device is forced into VBAT Standby Mode. This mode is left upon any wake-up event.

The TW1, TSD1/TW2 and TSD2 flags can all be cleared by an SPI Read & Clear command, provided that the junction temperature is below the respective temperature threshold.

Figure 9. Temperature modes



2.9 Wake-up events

A wake-up event in standby mode generates a transition to Active Mode. Three possible wake-up sources are defined, as illustrated in *Table 4*.

Table 4. Wake-up events

Wake-up source	Description
SPI Access	CSN pin low and first rising edge on SCK pin, active only in VDD Standby Mode
INH	High level on the INH pin, active in both standby modes

All wake-up events from VDD Standby Mode generate a low-pulse on NINT pin for 56 µs (typical).

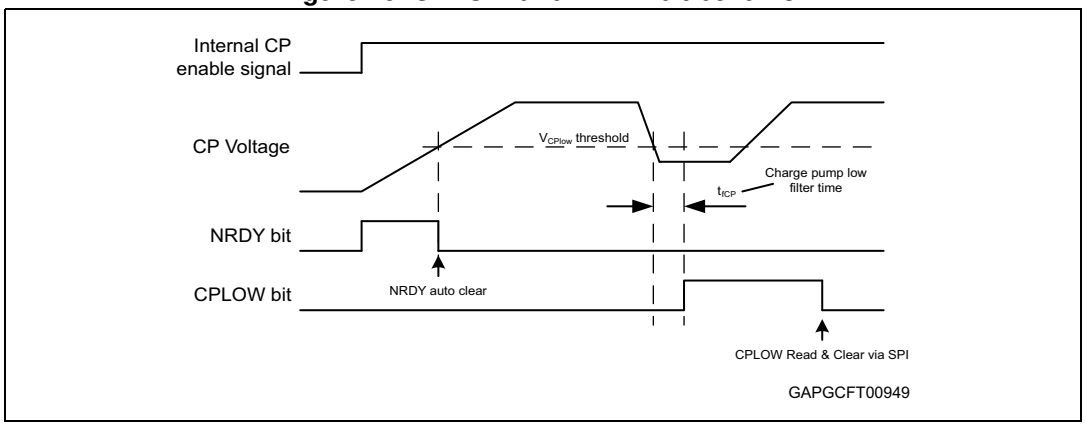
2.10 Charge pump

The two-stage charge pump is supplied from the V_S pin. External charging capacitors are used to achieve a high current capability of the charge pump. In VBAT Standby Mode, VDD Standby Mode or after thermal shutdown the charge pump is disabled. It is also possible to disable the charge pump by setting the CPDIS bit to "1".

In case the charge pump output voltage remains below the V_{CPLOW} threshold for longer than t_{fCP}, all gate drivers are switched off (resistive path to source) and the CPLOW flag is set and latched. The NRDY flag shows that the charge pump is not ready after a startup condition.

In order to minimize electromagnetic emissions, the charge pump frequency can be modulated in a programmable range through the WOBM and WOBF bits.

Figure 10. CPLOW and NRDY bit behavior



2.11 Gate drivers

Each of the three half-bridge drivers is controlled independently by dedicated inputs for the high-side driver (IHx, active low, with internal pull-up resistor) and for the low-side driver (ILx, active high, with internal pull-down resistor). All the gate drivers feature a minimum cross-current protection time (dead-time) t_{CCP} (programmable through the CCT bits) and

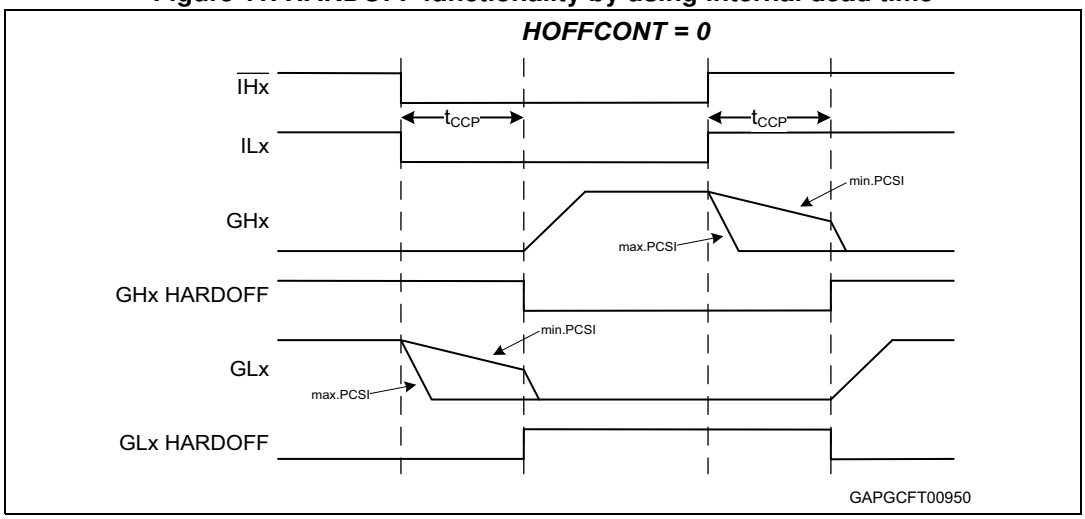
shoot-through protection. The minimum t_{CCP} is applied between outputs GHx and GLx only if a lower (or null) dead-time is present between inputs ILx and $\overline{IHx}$ (see *Figure 18*). In case the $\overline{IHx}$ and the ILx input of a half bridge are active at the same time, both gate driver outputs (high side and low side) are turned off. In addition, if $\overline{IHx}$ and ILx are both driven active for longer than t_{CCP}, the affected half bridge is disabled and the ST(x) error flag is set. To re-enable the half bridge, this fault condition has to be removed and the corresponding ST(x) flag has to be reset through an SPI "Read & Clear" command.

The gate driver circuit limits the gate-source voltage of the external MOSFETs. All gate driver circuits are independent of each other and use their source connection to the external MOSFET as a reference.

In order to drive different MOSFETs and adjust the gate currents according to external conditions (e.g. temperature), the source and sink current (i.e. the charging and discharging current) of the gate driver can be programmed via SPI.

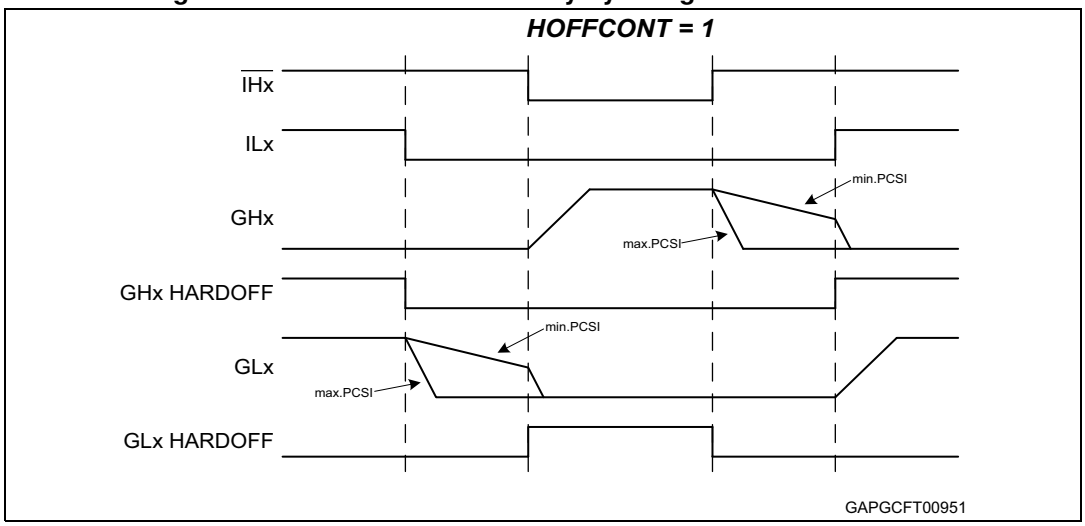
The HARDOFF feature is an additional measure against cross-current conduction in a half bridge. When the HOFFCONT bit is set to 0, any of the outputs GHx and GLx is switched off using maximum sink current (max PCSI) after a t_{CCP} from related turn-off command. When the HOFFCONT bit is set to 1, any of the outputs GHx and GLx is switched off using maximum sink current (max PCSI) as soon as the complementary output signal (respectively GLx or GHLx) goes to high.

Figure 11. HARDOFF functionality by using internal dead time



1. Propagation delay is omitted for convenience.

Figure 12. HARDOFF functionality by using external dead time



1. Propagation delay is omitted for convenience.

2.12 Drain-source monitoring

2.12.1 Drain-source monitoring in ON state (short-circuit detection)

The drain-source voltage of each activated external MOSFET is monitored by internal comparators to detect short circuits to ground or battery. In case the voltage drop over the external MOSFET exceeds the threshold voltage VSCd, the corresponding DSHS(x) or DSLS(x) flag is set. In addition, if the DSFT_DIS bit is set to "0", the affected MOSFET is turned off and the related gate driver is disabled.

The drain-source monitoring has a filter time and is only active when the corresponding gate driver is in source condition.

The threshold voltage VSCd can be programmed in four steps between 0.5 V and 2 V via SPI.

2.12.2 Drain-source monitoring in OFF state (open-load / short-circuit detection)

In Active Mode, each gate driver sources a current of typ. 500 µA at the SHx pins in OFF condition. By programming the ISTEST(x) bits to "1", a sink current of typ. 800 µA is applied to the corresponding pin.

By using these internal test currents, an open load, a leakage to GND or to battery can be detected on each motor phase in OFF state, i.e. without turning on the external MOSFETs.

If the ISTEST_EN bit is set to "1", the drain-source voltage monitoring is enabled also in OFF condition and the Status Register 7 reflects the result of the voltage comparison (i.e. drain-source voltage below or above the programmed threshold) in real time (i.e. the status bits are not latched) and without setting the FE bit in the Global Status Byte. See *Section 2.18: Diagnostics* for more details about diagnostics.

In order to allow the SHx pins to go below GND, the current sink has a diode in series and the sink current will disappear below 0.8V. Therefore, when using the test currents, the drain-source voltage threshold should be programmed to a value greater than 0.8V.

2.13 Current-sense amplifier

The current-sense amplifier (CSA) is designed for low-side current measurement in automotive motor control applications. The CSA differential input stage measures the voltage generated by the motor current over an external shunt resistor. The input common-mode range allows the CSA input pins to go below GND, as typically required in PWM motor control applications due to switching transients. The CSA gain can be programmed over a wide range by setting the GCSA bits.

In case of zero differential input voltage, the output voltage is at half scale:

VCSO = 0.5 * VDD

2.14 Overcurrent detection

To protect the application from overcurrent, an overcurrent threshold can be programmed via SPI by setting the OCTH bits. The CSA output is compared to the programmed threshold. In case of overcurrent, the CSAOC flag is set and, depending on the DMUX bit, the DOUT output goes high. In addition, if the OCSHUTD bit is set, the gate drivers are disabled.

The overcurrent detection feature can be used to estimate the rotor position of the motor at standstill without any rotation by applying voltage to the motor windings and detecting overcurrent with respect to an appropriate threshold.

2.15 BEMF module

The programmable BEMF (back electromotive force) module integrated in the device provides a flexible means to support those applications where the BLDC motor is driven in sensorless mode and that are based on BEMF detection.

2.15.1 BEMF comparator

Depending on the PWM driving method used in the application, three different comparators can be selected through the BEMFMOD bits to detect the BEMF zero-crossing point. BEMF detection can be done during the PWM ON state or the PWM OFF state. In the former case, the $V_{SMS}/2$ comparator (i.e. internally referenced to half of the V_{SMS} supply) can be used. In the latter case, the GND comparator (i.e. internally referenced to GND) or the V_{SMS} comparator (i.e. internally referenced to the V_{SMS} supply) can be used, depending on whether the PWM signal is applied to the external high-side or low-side MOSFET (this reflects the setting of the BEMFSW bit).

As some applications may require advancing the timing of a phase commutation (“pre-commutation”), it is possible to add an offset to the internal reference voltage of the $V_{SMS}/2$ comparator. The absolute offset value can be programmed through the BEMFOS bits. To achieve pre-commutation, the offset sign (i.e. positive or negative) has to vary, depending on whether the BEMF is rising or falling. The offset sign can be selected via SPI by programming the BEMFSIGN bit.

2.15.2 BEMF comparator sampling

In order to avoid unwanted commutations of the BEMF comparator due to PWM switching and spurious noise on the motor phases, an intelligent sampling mechanism is implemented to detect the BEMF zero-crossing point. Depending on the BEMFSW bit (PWM switching mode), BEMFMOD bit (comparator selection) and BEMFPOL bit, it is possible to select the triggering instant used to sample and latch the output of the selected BEMF comparator, which is in turn made available at the BEMFOUT pin. The following cases are possible:

- PWM on high-side MOSFET
  - BEMF detection in PWM ON state, BEMF sampling on PWM switch turn-off
  - BEMF detection in PWM OFF state, BEMF sampling on PWM switch turn-on or complementary PWM switch turn-off
- PWM on low-side MOSFET
  - BEMF detection in PWM ON state, BEMF sampling on PWM switch turn-off
  - BEMF detection in PWM OFF state, BEMF sampling on PWM switch turn-on or complementary PWM switch turn-off

It is worth noting that this method allows having a stabilized BEMF signal at the motor phase before the phase voltage can change, thanks to the turn-on and turn-off delay associated to the gate driver and the external MOSFET.

If no PWM is applied to the motor (100% duty cycle), the output of the BEMF comparator can be sampled by using an internal clock edge. In this case, the BEMFBY bit has to be set.

2.15.3 BEMF commutation driving mode

The BEMFCNT bits are used to set the motor phase to be monitored by the BEMF comparator. According to BEMFCM bit value, BEMFCNT bits can be either programmed through SPI by the system microcontroller or automatically updated by L99ASC03G.

In particular:

- If BEMFCM = '0', the external microcontroller is intended to update BEMFCNT bits through SPI command every time the BEMF comparator has to monitor another motor phase.
- If BEMFCM = '1', the BMFCNT bits are automatically increased (if BEMFDIR = '0') or decreased (if BEMFDIR = '1') whenever the L99ASC03G receives a triggering pulse on BC pin. In order to properly operates, triggering pulse amplitude on BC pin must be coherent with $V_{in\,H}$ (see *Table 24*) electrical parameter.

2.16 Digital multiplexer (DOUT)

An integrated digital multiplexer provides a digital signal on the DOUT pin. Depending on the setting of the DMUX bit and of the OCFT_DIS bit, it is possible to select between a fail-safe flag signal, a CSA overcurrent flag signal or the overcurrent comparator output.

2.17 Analog multiplexer (AOUT)

By setting the AMUX bits via SPI, an integrated analog multiplexer provides an output voltage proportional to the input supply voltages (V_S, V_{SREG} or V_{SMS}), to the internal chip temperature T_j or to the CSA reference voltage.

2.18 Diagnostics

All diagnostic functions are internally filtered and each fault/warning condition has to be valid for a defined time before the corresponding status bit is set in the status register. The filters are used to improve the noise immunity of the device. Several error types and warnings can be distinguished. All errors and warnings are reported in the corresponding status bits and are mirrored in the associated bits of the Global Status Byte (GSB).

- The device reacts to several error types by changing its state. The different error types can be grouped as follows:
- fail-safe errors (mirrored in the FS bit of the GSB)
- device errors (mirrored in the DE bit of the GSB)
- functional errors (mirrored in the FE bit of the GSB)
- physical-layer errors (mirrored in the PLE bit of the GSB)
- SPI errors (mirrored in the SPIE bit of the GSB)

In order for the device to recover from an error condition, the error itself must be removed and the associated status bit in the device has to be cleared via SPI by a “Read & Clear” command.

Warning functions are intended only for information and will not change the state of the device. Warnings are mirrored in the GW bit of the GSB. To clear a warning, the source of the warning must be removed and the associated flag has to be cleared via SPI by a “Read & Clear” command.

Table 5. Diagnostics overview

Source	Cause	Event type	Diagnosis	Device action	Clear error / warning flag
MCU	Watchdog not triggered or triggered out of the open window	FS (FS = 1 in the GSB)	FSWD = 1; Watchdog fail counter WDF>0	– NRES asserted low – Gate drivers actively discharged; charge pump, CSA and BEMF module OFF – Control registers (except Control Register 1 and DSFT_DIS) reset to default value	– After NRES is released, write WDTRIG = 1 during watchdog long open window to reset WDF counter bits – Read & Clear FSWD