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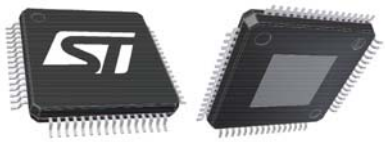
L99DZ120

Automotive door actuator driver with embedded LIN

Datasheet - production data



Features

- AEC-Q100 qualified
- 1 half bridge for 7.5 A load (R_{ON} = 100 mΩ)
- 1 half bridge for 7.5 A load (R_{ON} = 150 mΩ)
- 2 half bridges for 3 A load (R_{ON} = 300 mΩ)
- 1 configurable high-side driver for up to 1.5 A (R_{ON} = 500 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- 1 configurable high-side driver for 0.8 A (R_{ON} = 800 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- 3 configurable high-side drivers for 0.15 A/0.35 A (R_{ON} =2 Ω)
- 1 configurable high-side driver for 0.25 A/0.5 A (R_{ON} = 2 Ω)
- 4 configurable high-side drivers for 0.15 A/0.25 A (R_{ON} = 5 Ω)
- Internal 10bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (OUT15 & OUT_HS / both P-channel) to supply e.g. external contacts
- Programmable soft-start function to drive loads with higher inrush currents as current limitation value (for OUT1-6, OUT7, OUT8 and OUT_HS) with thermal expiration feature
- All the embedded outputs come with protection and supervision features:
  - Current Monitor (high-side only)
  - Open-load
  - Overcurrent
  - Thermal warning
  - Thermal shutdown
- Fully protected driver for external MOSFETs in H-bridge configuration
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- LIN 2.2a compliant (SAEJ2602 compatible) transceiver
- Separated (Isolated) fail-safe block with 2 LS (R_{ON} = 1 Ω) to pull down the gates of the external HS MOSFETs
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- Embedded and programmable VS duty cycle adjustment for LED driver outputs

Applications

Door zone applications.

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1 Description

The L99DZ120 is a door zone systems IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN physical communication layers.

The two low-drop voltage regulators of the devices supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability. In addition 8 high-side drivers to supply LEDs, 2 high-side drivers to supply bulbs increase the system integration level.

Up to 3 DC motors and 4 external MOS transistors in H-bridge configuration can be driven. All outputs are SC protected and implement an open-load diagnosis.

The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

2 Block diagram and pin descriptions

Figure 1. Block diagram

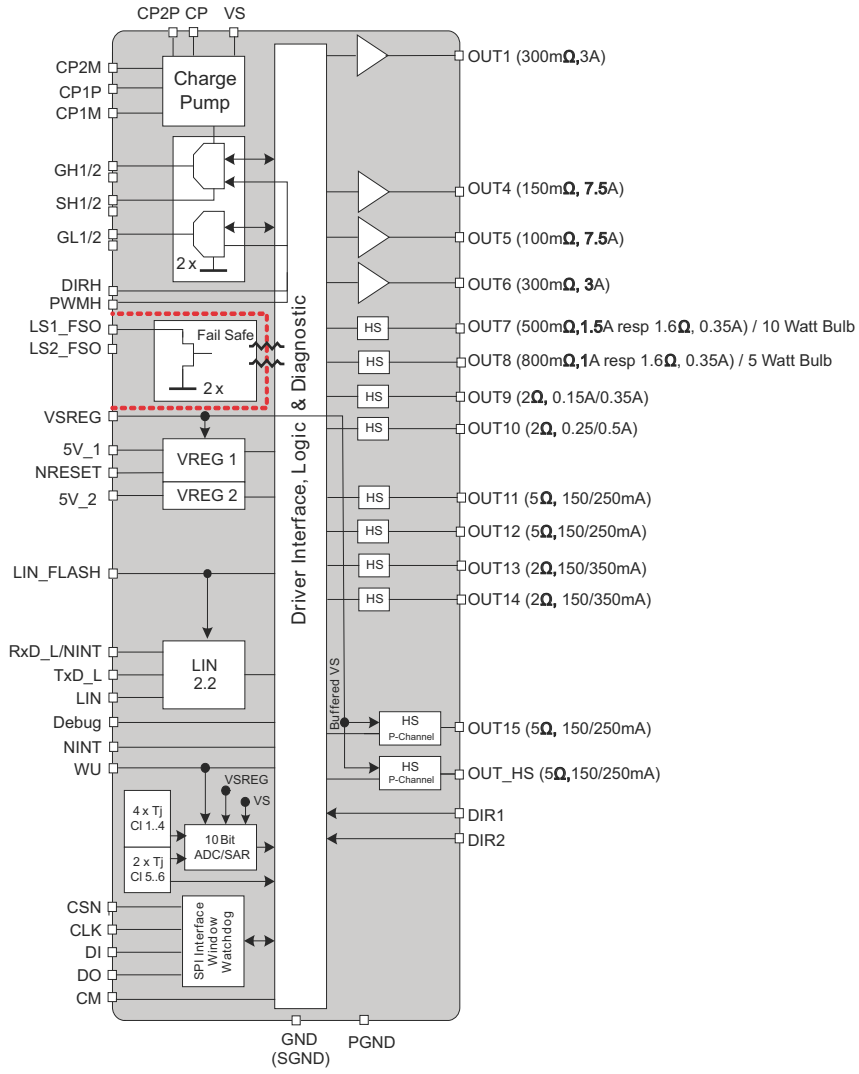


Table 1. Pin definitions and functions

Pin	Symbol	Function
1	WU	Wake-up Input: Input pin for static or cyclic monitoring of external contacts
2	CP2M	Charge pump pin for capacitor 2, negative side
3	CP2P	Charge pump pin for capacitor 2, positive side
4	CP	Charge pump output
5	CP1P	Charge pump pin for capacitor 1, positive side
6	CP1M	Charge pump pin for capacitor 1, negative side

Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
7	NC	Not connected
8	NC	Not connected
9	OUT14	High-side-driver output to drive LEDs
10	OUT13	High-side-driver output to drive LEDs
11	OUT12	High-side-driver output to drive LEDs
12	OUT9	High-side-driver output to drive LEDs
13	OUT10	High-side-driver-output
14	OUT11	High-side-driver output to drive LEDs
15	LS1_FSO	Fail Safe low-side switch (Active low)
16	LS2_FSO	Fail Safe low-side switch (Active low)
17	VS	Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving, the full current at the outputs all pins of VS must be connected externally!
18	VS; 2nd pin	Current capability (pin description see above)
19	OUT7	High-side-driver output to drive LEDs or a 10 Watt bulb (programmable R_{dson})
20	OUT6	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
21	OUT1	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output)
22	NC	Not connected
23	OUT5	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, low-side driver from GND to output)
24	OUT5; 2nd pin	Current capability (pin description see above)
25	V_{SREG}	Power supply voltage to supply the internal voltage regulators, OUT15 and the OUT_HS (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.
26	OUT_HS	High-side-driver output to drive LEDs or to supply contacts

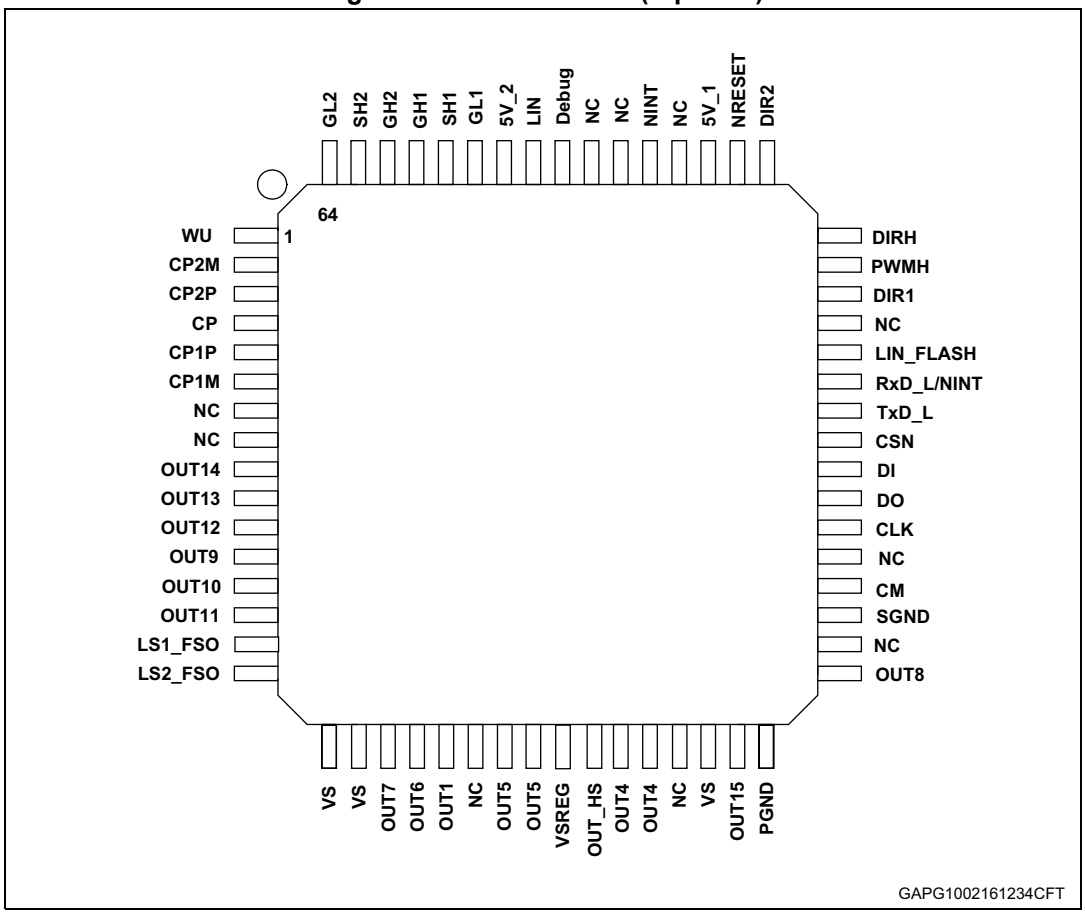
Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
27	OUT4	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, low-side driver from GND to output)
28	OUT4; 2nd pin	Current capability (pin description see above)
29	NC	Not connected
30	VS; 3rd pin	Current capability (for the pin description see above)
31	OUT15	High-side-driver output to drive LEDs
32	PGND	Power GND
33	OUT8	High-side-driver output to drive LEDs or a 5 Watt bulb (programmable R_{dson})
34	NC	Not connected
35	SGND	Signal Ground
36	CM	Current monitor output: depending on the selected multiplexer bits *CM_SEL_x* (*CR 7*) of the; Control Register this output sources an image of the instant current; through the corresponding high-side driver with a fixed ratio
37	NC	Not connected
38	CLK	SPI: serial clock input
39	DO	SPI: serial data output (push pull output stage)
40	DI	SPI: serial data input
41	CSN	SPI: chip select not input
42	TxD_L	LIN Transmit data input
43	RxD_L/NINT	RxDL -> LIN receive data output; NINT -> indicates local/remote wake-up events (push pull output stage)
44	LIN_FLASH	LIN Flash Mode enable (former TxD_C pin, to guarantee family compatibility)
45	NC	Not connected
46	DIR1	Direct Drive Input 1
47	PWMH	PWMH input: this input signal can be used to control the H-bridge Gate Drivers.
48	DIRH	Direction Input: this input controls the H-bridge Drivers for the external MOSFETs
49	DIR2	Direct Drive Input 2
50	NRESET	NReset output to micro controller; (reset state = LOW) (low-side switch with drain connected to the output pin and internal pull up resistance to 5V_1)
51	5V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller
52	NC	Not connected

Table 1. Pin definitions and functions (continued)

Pin	Symbol	Function
53	NINT	Interrupt output (low active; push-pull output stage) to indicate V_{SREG} early warning (Active mode); indicates wake-up events from V1_standby mode
54	NC	Not connected
55	NC	Not connected
56	Debug	Debug input to deactivate the window watchdog (high active)
57	LIN	LIN bus line
58	5V_2	Voltage regulator 2 output: 5 V supply for external loads (potentiometer, sensors). V_2 is protected against reverse supply
59	GL1	Gate driver for PowerMOS low-side switch in half-bridge 1
60	SH1	Source of high-side switch in half-bridge 1
61	GH1	Gate driver for PowerMOS high-side switch in half-bridge 1
62	GH2	Gate driver for PowerMOS high-side switch in half-bridge 2
63	SH2	Source of high-side switch in half-bridge 2
64	GL2	Gate driver for PowerMOS low-side switch in half-bridge 2

Figure 2. Pin connection (top view)



3 Electrical specifications

3.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V_S, V_{SREG}	DC supply voltage / “jump start”	-0.3 to +28	V
	Load dump	-0.3 to +40	V
5V_1	Stabilized supply voltage, logic supply	-0.3 to 6.5 V1 < V_{SREG}	V
5V_2(1)	Stabilized supply voltage	-0.3 to +28(2)	V
V_{DI}, V_{CLK} V_{CSN} V_{DO}, $V_{RXDL/NINT}$, V_{NRESET}, V_{CM}, V_{DIR}, V_{DIR2}, V_{PWMH}, V_{DIRH}, V_{INT}	Logic input / output voltage range	-0.3 to V1+0.3	V
V_{LIN_FLASH}, V_{TXDL}	Multi Level Inputs	-0.3 to 40	V
V_{Debug}	Debug input pin voltage range	-0.3 to 40	V
V_{LS1_FSO}, V_{LS2_FSO}	Output voltage range of Fail-Safe low-side Switches	-0.3 to 35	V
V_{WU}	DC Wake up input voltage / “jump start”	-0.3 to +28	V
	Load dump	-0.3 to +40	V
V_{LIN}	LIN bus I/O voltage range	-20 to +40	V
I_{Input}(3)	Current injection into V_S related input pins	20	mA
I_{OUT_INJ}(3)	Current injection into V_S related outputs	20	mA
V_{OUTn}, V_{out_HS}	Output voltage (n = 1 to 15)	-0.3 to V_S+0.3	V
V_{GH1}, V_{GH2} (V_{Gxy})	High Voltage Signal Pins	V_{Sxy}-0.3 to V_{Sxy}+13; V_{CP}+0.3	V
V_{GL1}, V_{GL2}, (V_{Gxy})	High Voltage Signal Pins	V_{Sxy}-0.3 to V_{Sxy}+13; V_{CP}-0.3V to +12V; Vcp+0.3V	V
V_{SH1}, V_{SH2} (V_{Sxy})	High Voltage Signal Pins	-1 to 40	V
	High Voltage Signal Pins; single pulse with t_{max} = 200ns	-5 to 40	V
V_{CP1P}	High Voltage Signal Pins	V_S-0.3 to V_S+14	V
V_{CP2P}	High Voltage Signal Pins	V_S-0.6 to V_S+14	V

Table 2. Absolute maximum ratings (continued)

Symbol	Parameter / test condition	Value [DC voltage]	Unit
V_{CP1M}, V_{CP2M}	High Voltage Signal Pins	-0.3 to V_S+0.3	V
V_{CP}	High Voltage Signal Pin $V_S \leq 26$ V	V_S-0.3 to V_S+14	V
	High Voltage Signal Pin $V_S > 26$ V	V_S-0.3 to +40	V
I_{OUT9}, I_{OUT10}, I_{OUT11}, I_{OUT12}, I_{OUT13}, I_{OUT14}, I_{OUT15}, I_{OUT_HS}	Output current(2)	±1.25	A
I_{OUT8}		±2.5	A
I_{OUT7}		±5	A
$I_{OUT1,6}$		±5	A
$I_{OUT4,5}$		±10	A
I_{VScum}	Maximum cumulated current at V_S drawn by OUT1(2)	±7.5	A
	Maximum cumulated current at V_S drawn by OUT8 & OUT10(2)	±2.5	A
	Maximum cumulated current at V_S drawn by OUT4(2)	±10	A
	Maximum cumulated current at V_S drawn by OUT5(2)	±10	A
	Maximum cumulated current at V_S drawn by OUT6 & OUT7(2)	±7.5	A
	Maximum cumulated current at V_S drawn by OUT9, OUT11, OUT12, OUT13, OUT14, OUT15 and CP	±2.5	A
I_{VSREG}	Maximum current at V_{SREG} pin (2) (5V_1. 5V_2 and OUT_HS)	±2.5	A
$I_{PGNDcum}$	Maximum cumulated current at PGND drawn by OUT1 & OUT6(2)	±7.5	A
	Maximum cumulated current at PGND drawn by OUT5(2)	±12.5	A
	Maximum cumulated current at PGND drawn by OUT4(2)	±12.5	A
I_{SGND}	Maximum current at SGND(2)	±1.25	A
GND pins	PGND versus SGND	-0.3 to 0.3	V

1. 5V_2 is robust against SC to 28 V only in case V_{SREG} is supplied.
2. Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.
3. Guaranteed by design.

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

Note: Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

3.2 ESD protection

Table 3. ESD protection

Parameter	Value	Unit
All pins(1)	+/-2	kV
All power output pins (2): OUT1 – OUT15, OUT_HS	+/-4	kV
LIN	+/-8(2) +/-10(3) +/-6(4)	kV
All pins(5)	+/-500	V
Corner pins(5)	+/-750(6)	V
All pins(7)	+/- 200	V

1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
2. HBM with all none zapped pins grounded.
3. Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
4. Direct ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.3, 2012-05-04).
5. Charged device model.
6. For WU, these limits are referred to one-zap stress; in case of three-zap stress, the limits are +750V/-400V.
7. Machine model; C = 220 pF, R = 0 Ω.

3.3 Thermal data

Table 4. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 175	°C

All parameters are guaranteed in the junction temperature range -40 to 150°C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175°C).

Note: Parameters limits at higher junction temperatures than 150°C may change respect to what is specified as per the standard temperature range.

Note: Device functionality at high junction temperature is guaranteed by characterization.

Table 5. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_W	Thermal overtemperature warning threshold	T_j(1)	140	150	160	°C
T_{SD1}	Thermal shutdown junction temperature 1	T_j(1) Cluster 1-4 Cluster 5-6	 165 165	 175 175	 185 190	°C
T_{SD2}	Thermal shutdown junction temperature 2	T_j(1)	175	185	195	°C
$T_{SD12hys}$		Hysteresis		5		°C
T_{jtft}	Thermal warning / shutdown filter time			32		µs

1. Non-overlapping.

3.3.1 LQFP64 thermal data

Devices belonging to L99DZxxx family embed a multitude of junctions (i.e. Outputs based on a PowerMOSFET stage) housed in a relatively small piece of silicon. The most complex device contains, among all the described features, 6 half-bridges (12 N-Channel PowerMOS), 10 high-sides and two voltage regulators; all the other derivatives, even if smaller than the family super set device, still contain a significant number of junctions.

For this reason, using the Thermal Impedance of a single junction (i.e. voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics.

Thermal information is provided as temperature reading by different clusters placed close to the most dissipative junctions.

Some representative and realistic worst-case thermal profiles are described in the below paragraph.

Following measurement methods can be easily implemented, by final user, for a specific activation profile.

L99DZ120 thermal profiles

Profile 1

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation)
- OUT14: 300 Ω resistor (DC activation)

Cyclic activation

- OUT4 – OUT5: 3,3 Ω resistor placed across those outputs
  - 10 activations of Lock/Un-lock (250 ms ON Lock; 500 ms wait; 250 ms ON Un-lock unlock; 500 ms wait)
- OUT5 – OUT6: 10 Ω resistor placed across those outputs
  - (250 ms ON Safe Lock; 500 ms wait; 250 ms ON Safe unlock; 500 ms wait)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

Temperature reading is logged just at the end of the whole sequence.

Figure 3. Activation profile 1

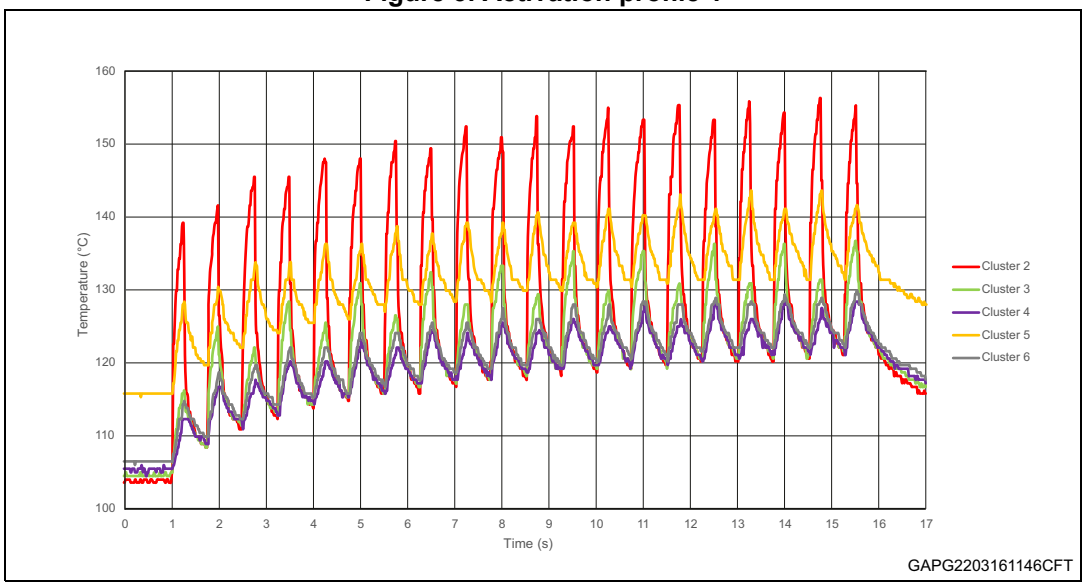
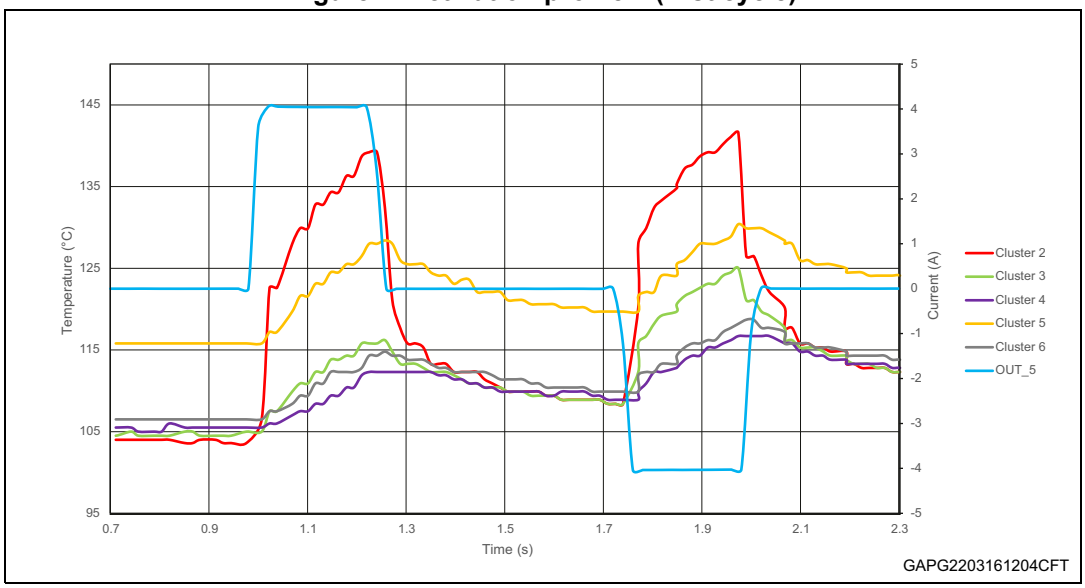


Figure 4. Activation profile 1 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

Profile 2

Battery Voltage: 16V, Ambient temperature start: 85°C

DC activation

- V1 charged with 70 mA (DC activation)
- V2 charged with 30 mA (DC activation)
- OUT7: 1 x10W bulb (DC activation)
- OUT8: 1 x 5W bulb (DC activation)
- OUT11: 300 Ω resistor (DC activation)
- OUT12: 300 Ω resistor (DC activation)
- OUT13: 300 Ω resistor (DC activation
- OUT14: 300 Ω resistor (DC activation)

Cyclic activation

- OUT1 – OUT6: 6,8 Ω resistor placed across those outputs
  - 2 activations (3s ON; 1s OFF; 2x)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic Activation” sequence is applied.

Figure 5. Activation profile 2

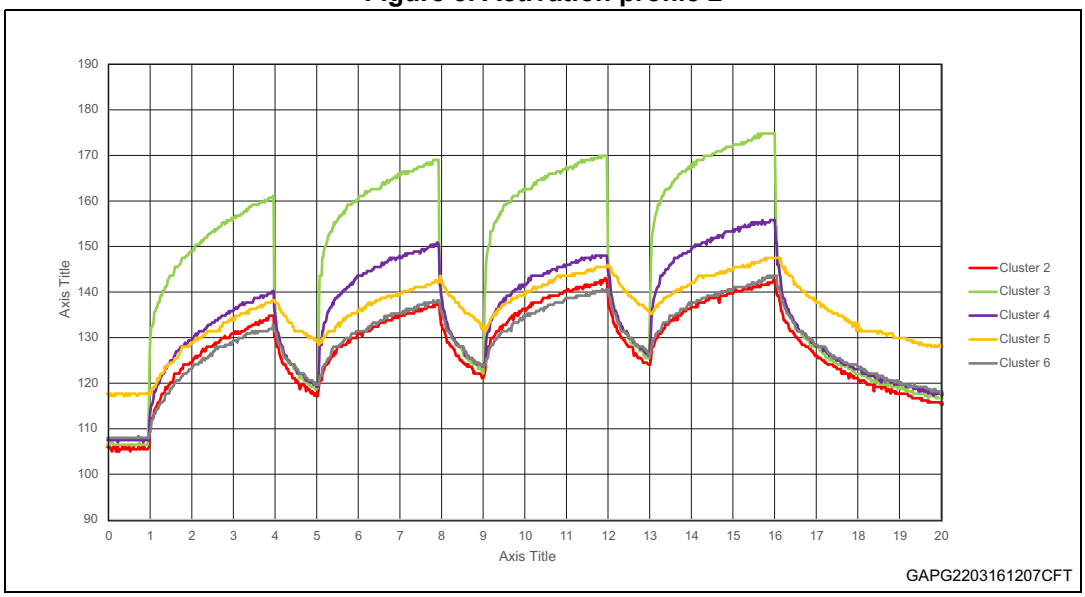
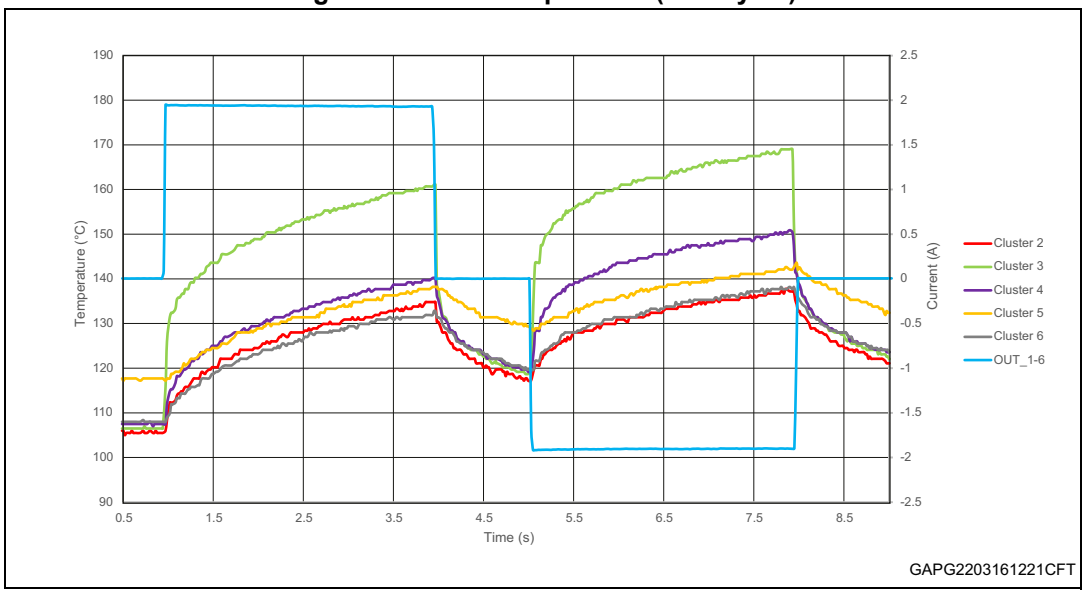
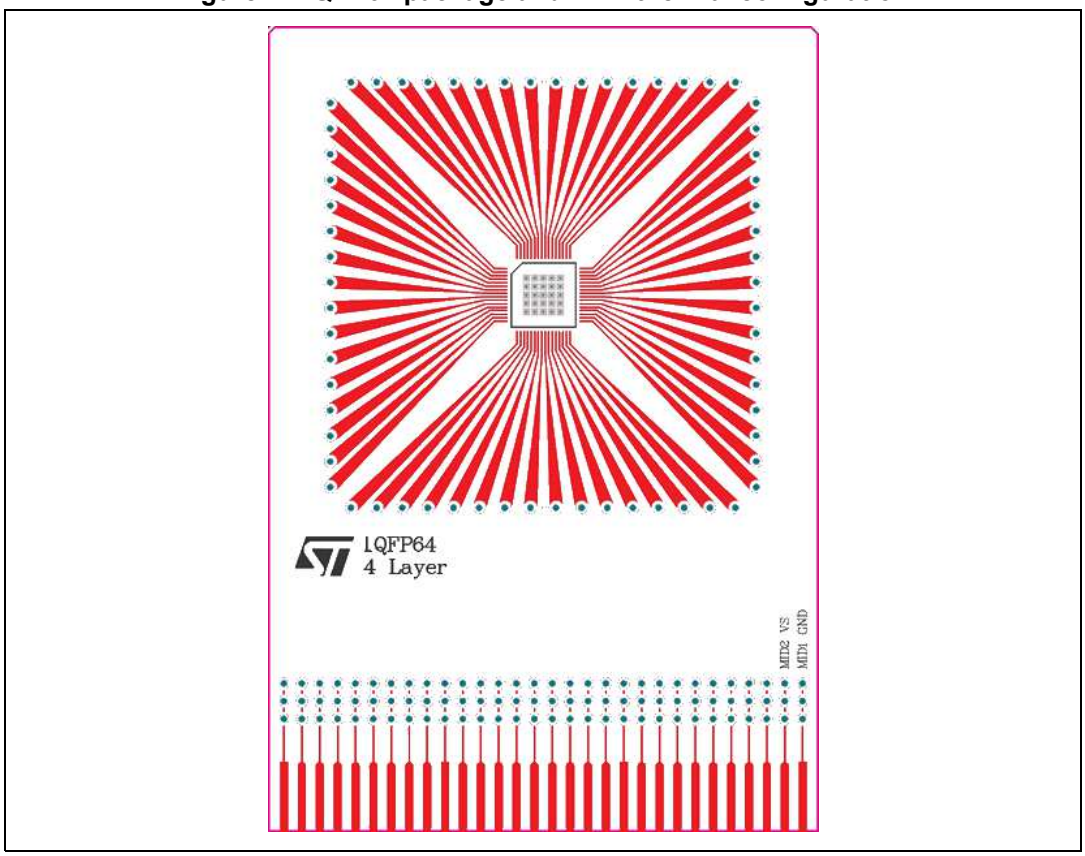


Figure 6. Activation profile 2 (first cycle)



Note: All curves are plotted interpolating measured samples with 15 ms of period.

Figure 7. LQFP64 package and PCB thermal configuration



Note: Layout condition for Thermal Characterization (board finishing thickness 1.5 mm +/- 10%, board four layers, board dimension 77 mm x 114 mm, board material FR4, Cu thickness 0,070 mm for outer layers, 0.0035 mm for inner layers, thermal vias separation 1.2 mm).

3.4 Electrical characteristics

3.4.1 Supply and supply monitoring

All SPI communication, logic and oscillator parameters are working down to V_{SREG} = 3.5 V and parameters are as specified in the following chapters (guaranteed by design).

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for $V_{SREG} < V_{POR}$)
- Reset threshold correctly detected

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 28 V; 6 V ≤ V_{SREG} ≤ 28 V; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 6. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SUV}	V_S undervoltage threshold	V_S increasing / decreasing	4.7		5.4	V
V_{hyst_UV}	V_S undervoltage hysteresis		0.04	0.1	0.2	V
V_{SOV}	V_S overvoltage threshold	V_S increasing	20		22.5	V
		V_S decreasing	18.5		22.5	
V_{hyst_OV}	V_S overvoltage hysteresis		0.5	1	1.5	V
V_{SREG_UV}	V_{SREG} undervoltage threshold	V_{SREG} increasing / decreasing	4.2		4.9	V
V_{hyst_UV}	V_{SREG} undervoltage hysteresis		0.04	0.1	0.2	V
V_{SREG_OV}	V_{SREG} overvoltage threshold	V_{SREG} increasing	20		22.5	V
		V_{SREG} decreasing	18.5		22.5	
V_{hyst_OV}	V_{SREG} overvoltage hysteresis		0.5	1	1.5	V
t_{ovuv_filt}	V_S/V_{SREG} over/undervoltage filter time			64		µs
$I_{V(act)}$	Current consumption in Active mode	V_S = V_{SREG} = 12 V; TxD LIN = high; V1 = ON; V2 = ON; HS/LS Driver OFF; CP = ON		11	14	mA
$I_{V(BAT)}$	Current consumption in V_{bat}_standby mode (1)	V_S = 12 V; Both voltage regulators deactivated; HS/LS Driver OFF	8	16	30	µA
$I_{V(BAT)CS}$	Current consumption in V_{bat}_standby mode with cyclic sense enabled (1)	V_S = 12 V; Both voltage regulators deactivated; T = 50 ms, t_{ON} = 100 µs	30	80	130	µA
$I_{V(BAT)CW}$	Current consumption in V_{bat}_standby mode with cyclic wake enabled (1)	V_S = 12 V; Both voltage regulators deactivated during standby phase	30	80	130	µA