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L99DZ80EP

Automotive door actuator driver

TQFP-64

GAPGCFT00080
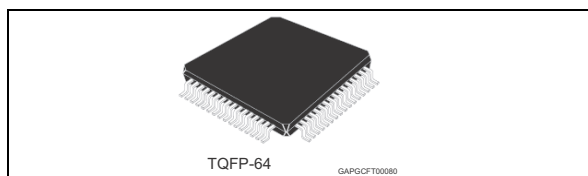
Features

- AEC-Q100 qualified
- One full bridge for 6 A load (R_{ON} = 150 mΩ)
- Two half bridges for 3 A load (R_{ON} = 300 mΩ)
- Two half bridges for 0.5 A load (R_{ON} = 1600 mΩ)
- One high-side driver for 5 A load (R_{ON} = 100 mΩ)
- One configurable high-side driver for up to 1.5 A (R_{ON} = 500 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- One configurable high-side driver for 0.7 A (R_{ON} = 800 mΩ) or 0.35 A (R_{ON} = 1600 mΩ) load
- Two high-side drivers for 0.5 A load (R_{ON} = 1600 mΩ)
- Programmable softstart function to drive loads with higher inrush currents as current limitation value
- Very low V_S current consumption in standby mode (I_S < 6 µA typ; T_j ≤ 85 °C)
- Current monitor output for all high-side drivers
- Central two-stage charge pump
- Motor bridge driver with full R_{dson} down to 6 V
- Device contains temperature warning and protection
- Open-load detection for all outputs
- Overcurrent protection for all outputs
- Separated half bridges for door lock motor
- Programmable PWM control of all outputs

- STM standard serial peripheral interface (ST-SPI 3.1)
- Control block for electrochromic element
- Electrochromic element can be negatively discharged
- Prepared for additional fail-safe path for H-bridge

Applications

- Door actuator driver with 6 bridges for double door lock control, mirror fold and mirror axis control, high-side driver for mirror defroster, bulbs and LEDs.
- Control block with external MOS transistor for charging / discharging of electrochromic glass. Motor bridge driver.
- H-bridge control for external power transistors

Description

The L99DZ80EP is a microcontroller driven multifunctional door actuator driver for automotive applications. Up to five DC motors and five grounded resistive loads can be driven with six half bridges and five high-side drivers. Four external MOS transistors in bridge configuration can be driven. An electrochromic mirror glass can be controlled using the integrated SPI-driven module in conjunction with an external MOS transistor. The mirror glass can also be discharged through a negative supply. The integrated SPI controls all operating modes (forward, reverse, brake and high impedance). All diagnostic information is available via SPI read.

Table 1. Device summary

Package	Order codes	
	Tray	**Tape and reel**
TQFP-64	L99DZ80EP	L99DZ80EPTR

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List of figures

1 Block diagram and pin description

Figure 1. Block diagram

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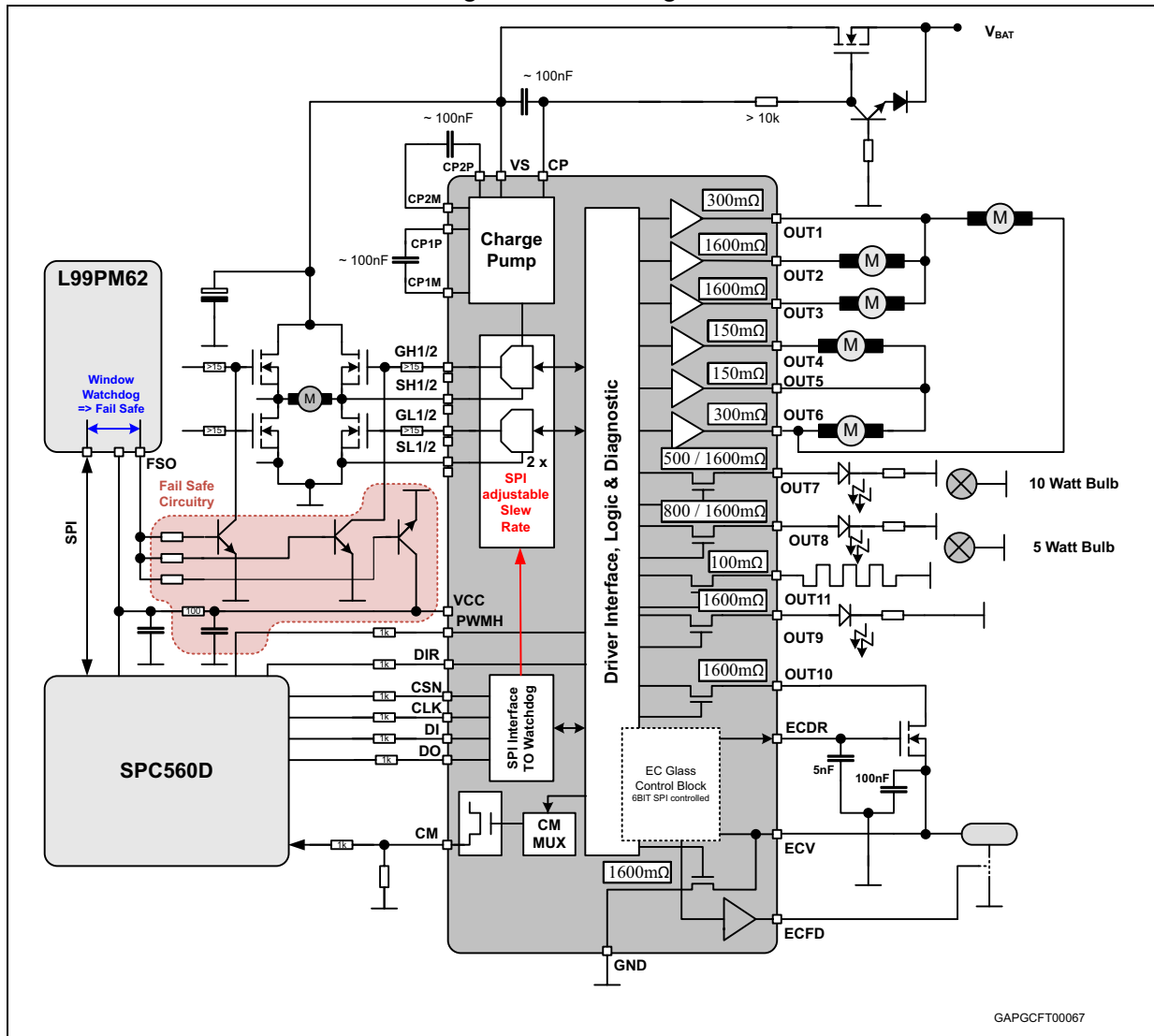
Table 2. Pin definitions and functions

Pin	Symbol	Function
57, 58	GND$_1$	Ground: reference potential. GND1 and GND2 are internally connected. GND1 supplies OUT1-3, GND2 supplies OUT4-6
17, 18, 26, 31, 32	GND$_2$	Important: For the capability of driving the full current at the outputs, all pins of GND must be externally connected!
17	SGND	Signal Ground: this pin is shared with GND2 pin
2, 3, 45, 46, 51, 52	VS$_1$	Power supply voltage for power stage outputs (external reverse protection required): for this input a ceramic capacitor as close as possible to GND is recommended. VS1 supplies OUT1-3, OUT7-11 and the internal VS supply, VS2 supplies OUT4-6
11, 12, 23, 36, 37	VS$_2$	Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected!
48, 49, 50	OUT11	High-side-driver output 11: the output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The High-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is overcurrent and open load protected. Important: For the capability of driving the full current at the outputs all pins of OUT11 must be externally connected!
59, 60	OUT1	Half-bridge outputs 1,2,3,4,5,6: the output is built by a high side and a low side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high side driver from output to VS, low side driver from GND to output). This output is over current and open load protected.
56	OUT2	
55	OUT3	
19, 20, 21, 22	OUT4	
27, 28, 29, 30	OUT5	
24, 25	OUT6	
40	DO	Serial data output: the diagnosis data is available via the SPI and this 3-state-output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high).
34	CM	Current monitor output: depending on the selected multiplexer bits of the Control Register this output sources an image of the instant current through the corresponding high side driver with a fixed ratio.
35	CSN	Chip-Select-Not input: this input is low active and requires CMOS logic levels. The serial data transfer between the device and the micro controller is enabled by pulling the input CSN to low level.
41	DI	Serial data input: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB, bit 23) is transferred first.
38	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.
33	DIR	Direction Input: this input controls the H-Bridge Drivers

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
39	VCC	Supply Voltage: 5 V supply. A ceramic capacitor as close as possible to GND is recommended.
44	OUT9	High-side-driver output 9: the output is built by a high side switch and is intended for resistive loads; hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over current and open load protected.
42	PWMH	PWMH input: this input signal can be used to control the H-Bridge Gate drivers
43	ECDR	ECDR: using the device in EC control mode this pin is used to control the Gate of an external MOSFET.
62, 63	OUT7	High side driver output 8: see OUT9
61	OUT8	Important: This output can be configured to supply a bulb with low on-resistance or a LED with higher on-resistance in a different application.
47	OUT10/EC	High-side-driver-output 10: see OUT9 Important: Beside the OUT10-HS on/off bit this output can be switched on setting the ECON bit for electrochrome control mode with higher priority.
54	ECFD	ECFD: using the device in EC control mode this pin is used as "virtual GND" for the EC-glass. For EC-glasses, that require a negative discharge voltage, this supplies the fast discharge voltage. If no EC-glass is used, this pin must be connected to ground.
53	ECV	ECV: using the device in EC control mode this pin is used as voltage monitor input. For fast discharge an additional low-side-switch is implemented.
13	GH2	GH2: gate driver for power MOS high side switch in half-bridge 2
14	SH2	SH2: source of high-side switch in half-bridge 2
15	GL2	GL2: gate driver for power MOS low side switch in half-bridge 2
16	SL2	SL2: source of low side switch in half-bridge 2
64	GH1	GH1: gate driver for power MOS high side switch in half-bridge 1
1	SH1	SH1: source of high-side switch in half-bridge 1
4	GL1	GL1: gate driver for power MOS low side switch in half-bridge 1
5	SL1	SL1: source of low side switch in half-bridge 1
7	CP1P	CP1P: charge pump pin for capacitor 1, positive side
8	CP1M	CP1M: charge pump pin for capacitor 1, negative side
9	CP2P	CP2P: charge pump pin for capacitor 2, positive side
10	CP2M	CP2M: charge pump pin for capacitor 2, negative side
6	CP	CP: charge pump output

Figure 2. Pin connection (top view)

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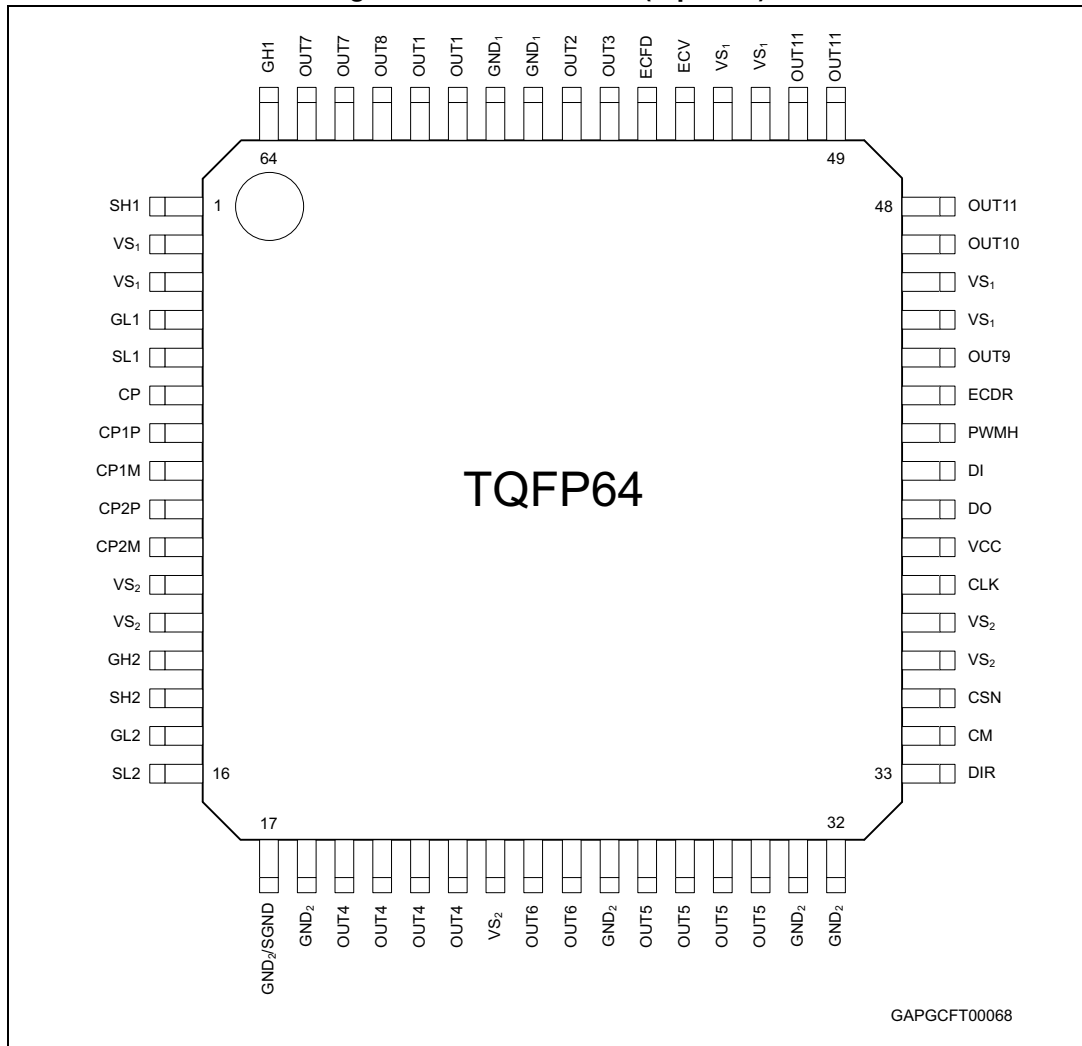
2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter/test condition		Value [DC Voltage]	Unit
V_{S1}, V_{S2}	DC supply voltage		-0.3 to +28	V
	Single pulse / t_{max} < 400 ms "transient load dump"		-0.3 to +40	V
V_{CC}	Stabilized supply voltage, logic supply		-0.3 to V_S + 0.3	V
V_{DI}, V_{CLK}, V_{CSN}, V_{DO}, V_{CM}, V_{DIR}, V_{PWMH}, V_{DIR}	Logic input / output voltage range		-0.3 to V_{CC} + 0.3	V
$V_{OUTn, ECDR, ECV, ECFD}$	Output voltage (n = 1 to 11)		-0.3 to V_S + 0.3	V
V_{SL1}, V_{SH1}, V_{SL2}, V_{SH2} (V_{Sxy})	High voltage signal pins		-6 to 40	V
V_{GL1}, V_{GH1}, V_{GL2}, V_{GH2} (V_{Gxy})	High voltage signal pins		V_{Sxy} - 1 to V_{Sxy} + 10; V_{CP} + 0.3	V
V_{CP1P}	High voltage signal pins		V_S - 0.3 to V_S + 10	V
V_{CP2P}	High voltage signal pins		V_S - 0.6 to V_S + 10	V
V_{CP1M}, V_{CP2M}	High voltage signal pins		-0.3 to V_S + 0.3	V
V_{CP}	High voltage signal pin	$V_{S1,2} \leq 26$ V	V_S - 0.3 to V_S + 14	V
		$V_{S1,2}$ > 26 V	V_S - 0.3 to +40	V
$I_{OUT2,3,9,10, ECV, ECFD}$	Output current[1]		±1.25	A
$I_{OUT1,6,7}$	Output current[1] (low on-resistance mode)		±5	A
I_{OUT7}	Output current[1] (high on-resistance mode)		±5	A
I_{OUT8}	Output current[1]		±2.5	A
$I_{OUT4,5}$	Output current[1]		±10	A
I_{OUT11}	Output current[1]		±7.5	A
I_{VS1cum}	Maximum cumulated input current at VS_1 pins[1]		±12.5	A
I_{VS2cum}	Maximum cumulated input current at VS_2 pins[1]		±12.5	A
$I_{GND1cum}$	Maximum cumulated output current at GND_1 pins[1]		±5	A
$I_{GND2cum}$	Maximum cumulated output current at GND_2 pins[1]		±12.5	A

1. Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	$\pm 2^{(1)}$	kV
Power output pins: OUT1 – OUT11, ECV, ECFD	$\pm 4^{(1)}$	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold (junction temperature)		130		150	°C
$T_{jTS\ ON}$	Thermal shutdown threshold (junction temperature)		150		170	°C
T_{jtft}	Thermal warning / shutdown filter time			32		μs

Table 7. Package thermal impedance

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction to ambient (max)	See *Figure 5*	K/W

2.4   Package and PCB thermal data
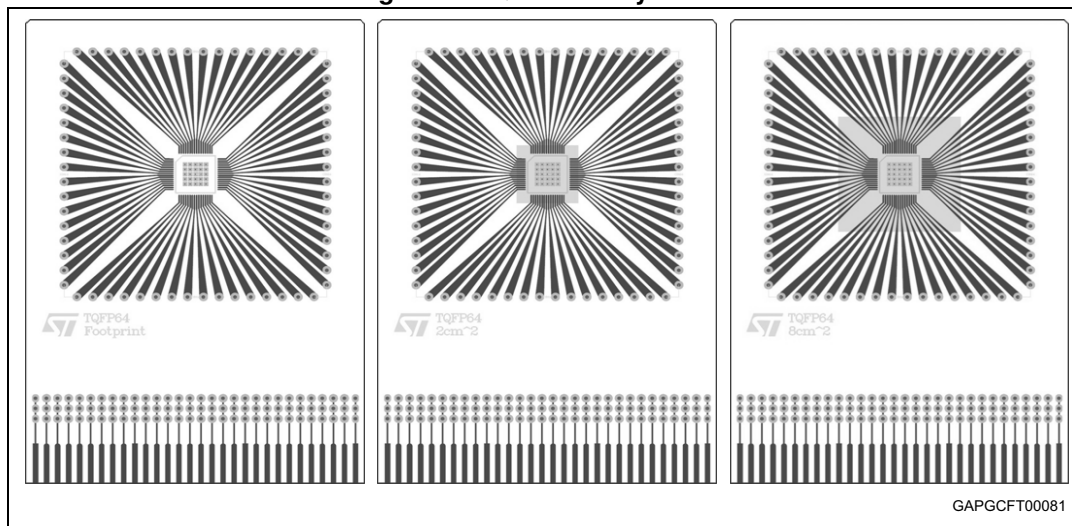
2.4.1   TQFP-64 thermal data

Figure 3. TQFP-64 2 layer PCB

Figure 4. TQFP-64 4 layer PCB

Note: *Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%, board double layer and four layers, board dimension 77 mm x114 mm, board material FR4, Cu thickness 0.070mm (outer layers), Cu thickness 0.035mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 6 mm x 6 mm). 4-layer PCB: Cu on mid1 layer, Cu on mid2 layer and Cu on bottom layer: 62 cm^2. Z_{th} measured on the major power dissipator contributor*

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2.4   Package and PCB thermal data

2.4.1   TQFP-64 thermal data

Figure 3. TQFP-64 2 layer PCB

Figure 4. TQFP-64 4 layer PCB

Note: *Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10%, board double layer and four layers, board dimension 77 mm x114 mm, board material FR4, Cu thickness 0.070mm (outer layers), Cu thickness 0.035mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 6 mm x 6 mm). 4-layer PCB: Cu on mid1 layer, Cu on mid2 layer and Cu on bottom layer: 62 cm^2. Z_{th} measured on the major power dissipator contributor*

Figure 5. TQFP-64 thermal impedance junction to ambient vs PCB copper area
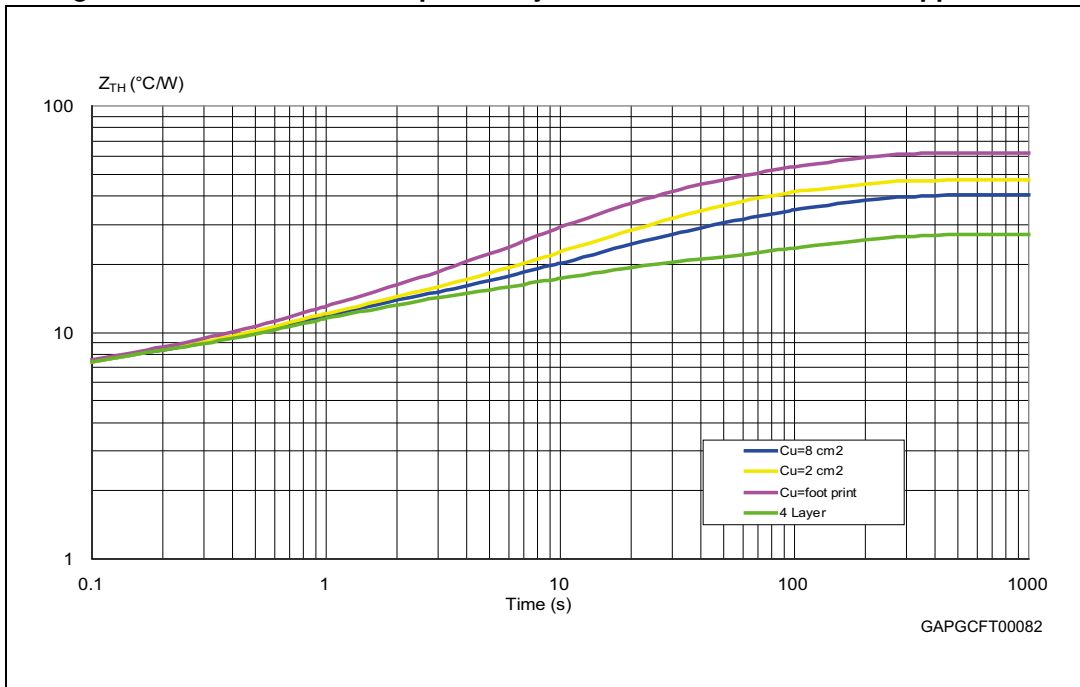
2.5 Electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6\ V \leq V_S \leq 18\ V$, $4.75\ V \leq V_{CC} \leq 5.5\ V$; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 8. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating voltage range		5		28	V
$I_{VS(act)}$	Current consumption in active mode	V_S = 13.5 V[1]		5	10	mA
$I_{VS(stby)}$	Current consumption in standby mode	V_S = 16 V; V_{CC} = 5.3 V; standby mode OUT1 - OUT11; ECV; ECDR floating T_{TEST} = -40 °C to 25 °C		4	12	µA
		T_{TEST} = 85 °C[1]		6	25	µA
V_{CC}	Operating voltage range		4.5		5.5	V
$I_{VCC(active)}$	V_{CC} supply current	V_S = 16 V; V_{CC} = 5.3 V; CSN = V_{CC}; active mode OUT1 - OUT11; ECV; ECDR floating		5	10	mA
$I_{VCC(stby)}$	V_{CC} standby current	V_S = 16 V; V_{CC} = 5.0 V; CSN = V_{CC}; active mode OUT1 - OUT11; ECV; ECFD ECDR floating T_{TEST} = -40 °C to 25 °C		3	6	µA
		T_{TEST} = 85 °C[1]		4	8	µA
		V_S = 16 V; V_{CC} = 5.3 V; CSN = V_{CC}; active mode OUT1 - OUT11; ECV; ECFD ECDR floating T_{TEST} = -40 °C to 125 °C			25	µA

1. This parameter is guaranteed by design

Table 9. Overvoltage and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	VS UV threshold voltage[1]	V_S increasing	5.6		7.2	V
$V_{SUV\ OFF}$	VS UV threshold voltage[1]	V_S decreasing	5		5.9	V
$V_{SUV\ hyst}$	VS UV hysteresis[1]	$V_{SUV\ ON}$-$V_{SUV\ OFF}$		0.5		V
$t_{vsuvfilt}$	VS UV filter time			48		µs
$V_{SOV\ OFF}$	VS OV threshold voltage[1]	V_S increasing	18.5		24.5	V
$V_{SOV\ ON}$	VS OV threshold voltage[1]	V_S decreasing	18.0		23.5	V
$V_{SOV\ hyst}$	VS OV hysteresis[1]	$V_{SOV\ OFF}$-$V_{SOV\ ON}$		1		V

Table 9. Overvoltage and undervoltage detection (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{vsovfilt}$	VS OV filter time			48		µs
$V_{VCCRESHU}$	Upper V_{CC} reset threshold[2]	V_{CC} increasing	5.8		7.5	V
$V_{VCCRESHD}$	Upper V_{CC} reset threshold	V_{CC} decreasing	5.5		7.1	V
$V_{VCCRES\ hysth}$	Upper reset hysteresis	$V_{VCCRESHU}$ - $V_{VCCRESHD}$		0.1		V
V_{POROFF}	Power-on-reset threshold	V_{CC} increasing	3.4		4.4	V
V_{PORON}	Power-on-reset threshold	V_{CC} decreasing	3.1		4.1	V
$V_{POR\ hystL}$	Power-on-reset hysteresis	$V_{POROFFL}$ - V_{PORONL}		0.3		V

1. VS = 5V to 28V

2. If V_{CC} exceeds this value all registers are reset and the device enters standby mode.

Table 10. Current monitor output (CM)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range		0		V_{CC} - 1 V	V
$I_{CM\ r}$	Current monitor output ratio: $I_{CM}/I_{OUT1,4,5,6,11\ and\ 7}$ (low on-resistance)	$0\ V \leq V_{CM} \leq V_{CC}$ - 1 V		1/10000		
	I_{CM}/I_{OUT8} (low on-resistance)			1/6500		
	$I_{CM}/I_{OUT2,3,7,8,9,10\ and\ 7,8}$ (high on-resistance)			1/2000		
$I_{CM\ acc}$	Current monitor accuracy $accI_{CMOUT1,4,5,6,11\ and\ 7}$(low on-res.)	$0\ V \leq V_{CM} \leq V_{CC}$ - 1 V; I_{OUTmin} = 500 mA; $I_{OUT4,5max}$ = 5.9 A; $I_{OUT11max}$ = 4.9 A; $I_{OUT1,6max}$ = 2.9 A; $I_{OUT7max}$ = 1.4 A		4 % + 1 % FS [1]	8 % + 2 % FS [1]	
	$accI_{CMOUT2,3,8,9,10\ and\ 7}$(high on-res.)	$0\ V \leq V_{CM} \leq V_{CC}$ - 1 V; $I_{OUT.min}$ = 100 mA; $I_{OUT2,3,9,10max}$ = 0.4A; $I_{OUT7max}$ = 0.3 A; $I_{OUT8(low\ rdson)max}$ = 0.6 A; $I_{OUT8(high\ rdson)max}$ = 0.3 A				
t_{cmb}	Current monitor blanking time			32		µs

1. FS (full scale) = $I_{OUTmax} * I_{CMr}$

Table 11. Charge pump

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 6 V; I_{CP} = -10 mA	V_S + 6	V_S + 7	V_S + 7.85	V
		$V_S \geq 10$ V; I_{CP} = -15 mA	V_S + 11	V_S + 12	V_S + 13.5	V

Table 11. Charge pump (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CP}	Charge pump output current[1]	$V_{CP} = V_S + 10$ V; $V_S = 13.5$ V; $C_1 = C_2 = C_{CP} = 100$ nF	25		47	mA
I_{CPlim}	Charge pump output current limitation[2]	$V_{CP} = V_S$; $V_S = 13.5$ V; $C_1 = C_2 = C_{CP} = 100$ nF	29		70	mA
V_{CP_low}	Charge pump low threshold voltage		$V_S + 4.6$	$V_S + 5$	$V_S + 5.4$	V
T_{CP}	Charge pump low filter time			64		µs

1. I_{CP} is the minimum current the device can provide to an external circuit without V_{CP} going below $V_S + 10$ V

2. I_{CPlim} is the maximum current, which flows out of the device in case of a short to V_S

2.6 Outputs OUT1 - OUT11, ECV, ECFD

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V $\leq V_S \leq 18$ V, 4.75 V $\leq V_{CC} \leq 5.5$ V; all outputs open;
$T_j = -40$ °C to 150 °C, unless otherwise specified.

Table 12. On-resistance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT1,6}$	On-resistance to supply or GND	$V_S = 13.5$ V; $T_{amb} = +25$ °C; $I_{OUT1,6} = \pm1.5$ A		300	400	mΩ
		$V_S = 13.5$ V; $T_{amb} = +125$ °C; $I_{OUT1,6} = \pm1.5$ A		450	600	mΩ
$r_{ON\ OUT2,3}$	On-resistance to supply or GND	$V_S = 13.5$ V; $T_{amb} = +25$ °C; $I_{OUT2,3} = \pm0.4$ A		1600	2200	mΩ
		$V_S = 13.5$ V; $T_{amb} = +125$ °C; $I_{OUT2,3} = \pm0.4$ A		2500	3400	mΩ
$r_{ON\ OUT4,5}$	On-resistance to supply or GND	$V_S = 13.5$ V; $T_{amb} = +25$ °C; $I_{OUT4,5} = \pm3.0$ A		150	200	mΩ
		$V_S = 13.5$ V; $T_{amb} = +125$ °C; $I_{OUT4,5} = \pm3.0$ A		225	300	mΩ
$r_{ON\ OUT7}$	On-resistance to supply in low resistance mode	$V_S = 13.5$ V; $T_{amb} = +25$ °C; $I_{OUT7} = -0.8$ A		500	700	mΩ
		$V_S = 13.5$ V; $T_{amb} = +125$ °C; $I_{OUT7} = -0.8$ A		700	950	mΩ
	On-resistance to supply in high resistance mode	$V_S = 13.5$ V; $T_{amb} = +25$ °C; $I_{OUT7} = -0.2$ A		1600	2400	mΩ
		$V_S = 13.5$ V; $T_{amb} = +125$ °C; $I_{OUT7} = -0.2$ A		2500	3400	mΩ

Table 12. On-resistance (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ OUT8}$	On-resistance to supply in low resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT8} = -0.4 A		800	1200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT8} = -0.4 A		1200	1700	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT8} = -0.2 A		1600	2400	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT8} = -0.2 A		2500	3400	mΩ
$r_{ON\ OUT9,10}$	On-resistance to supply	V_S = 13.5 V; T_{amb} = +25 °C; $I_{OUT9,10}$ = -0.4 A		1600	2200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; $I_{OUT9,10}$ = -0.4 A		2500	3400	mΩ
$r_{ON\ OUT11}$	On-resistance to supply	V_S = 13.5 V; T_{amb} = +25 °C; I_{OUT11} = -3.0 A		100	140	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; I_{OUT11} = -3.0 A		140	190	mΩ
$r_{ON\ ECV,ECFD}$	On-resistance to GND	V_S = 13.5 V; T_{amb} = +25 °C; $I_{OUTECV,ECFD}$ = +0.4 A		1600	2200	mΩ
		V_S = 13.5 V; T_{amb} = +125 °C; $I_{OUTECV,ECFD}$ = +0.4 A		2500	3400	mΩ
I_{QLH}	Switched-off output current high side drivers of OUT1-6,9-11	V_{OUT} = 0 V; standby mode	-5	-2		µA
		V_{OUT} = 0 V; active mode	-10.2	-7		µA
$I_{QLH7,8}$	Switched-off output current high side drivers of OUT7,8	V_{OUT} = 0 V; standby mode	-5	-2		µA
		V_{OUT} = 0 V; active mode	-15	-10		µA
I_{QLL}	Switched-off output current low side drivers of OUT1-6	V_{OUT} = V_S; standby mode		80	165	µA
		V_{OUT} = V_S - 0.5 V; active mode	-10	-7		µA
	Switched-off output current low side drivers of ECV	V_{OUT} = V_S; standby mode	-15		15	µA
		V_{OUT} = V_S - 0.5 V; active mode	-10	-7		µA
	Switched-off output current low side drivers of ECFD	V_{OUT} = 4 V; standby mode		80	165	µA
		V_{OUT} = 4 V; active mode	-10		10	µA

Table 13. Power outputs switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\,ON\,H}$	Output delay time high side driver on (all OUT except $OUT_{7,8}$)	$V_S = 13.5\ V$; $V_{CC} = 5\ V$; corresponding low side driver is not active[1][2][3]	10	40	80	µs
	Output delay time high side driver on ($OUT_{7,8}$ in high R_{DSON} mode)		15	35	60	µs
	Output delay time high side driver on ($OUT_{7,8}$ in low R_{DSON} mode)		10	35	80	µs
$t_{d\,OFF\,H}$	Output delay time high side driver off ($OUT_{1,4,5,6,11}$)	$V_S = 13.5\ V$; $V_{CC} = 5\ V$[1][2][3]	50	150	300	µs
	Output delay time high side driver off ($OUT_{2,3,\,7,8,9,10}$)		40	70	100	µs
$t_{d\,ON\,L}$	Output delay time low side driver on	$V_S = 13.5\ V$; $V_{CC} = 5\ V$; corresponding low side driver is not active[1][2][3]	15	30	70	µs
$t_{d\,OFF\,L}$	Output delay time low side driver (OUT_{1-6}) off	$V_S = 13.5\ V$; $V_{CC} = 5\ V$ [1][2][3]	40	150	300	µs
	Output delay time low side driver (ECV, ECFD) off	$V_S = 13.5\ V$; $V_{CC} = 5\ V$[1][2][3]	15	45	88	µs
$t_{d\,HL}$	Cross current protection time (OUT_{1-6})	$t_{cc\,ONLS\_OFFHS} - t_{d\,OFF\,H}$[4]	40	200	400	µs
$t_{d\,LH}$		$t_{cc\,ONHS\_OFFLS} - t_{d\,OFF\,L}$[4]				
dV_{OUT}/dt	Slew rate of OUTx, ECV, ECFD	$V_S = 13.5\ V$; $V_{CC} = 5\ V$[1][2][3]	0.08	0.2	0.6	V/µs
$f_{PWMx(low)}$	Low PWM switching frequency	$V_S = 13.5\ V$; $V_{CC} = 5\ V$		122		Hz
$f_{PWMx(high)}$	High PWM switching frequency	$V_S = 13.5\ V$; $V_{CC} = 5\ V$		244		Hz

1. $R_{load} = 16\ \Omega$ at $OUT_{1,6}$ and $OUT_{7,8}$ in low on-resistance mode

2. $R_{load} = 4\ \Omega$ at $OUT_{4,5,11}$

3. $R_{load} = 64\ \Omega$ at $OUT_{2,3,4,9,10}$ ECV, ECFD and $OUT_{7,8}$ in high on-resistance mode

4. t_{CC} is the switch-on delay time if complement in half bridge has to switch off

Table 14. Current monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$|I_{OC1}|$, $|I_{OC6}|$	Overcurrent threshold to supply or GND	$V_S = 13.5\ V$; $V_{CC} = 5\ V$; sink and source	3		5.3	A
$|I_{OC2}|$, $|I_{OC3}|$, $|I_{OCECFD}|$			0.5		1.0	A
$|I_{OC4}|$, $|I_{OC5}|$			6		9.2	A

Table 14. Current monitoring (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$|I_{OC7}|$	Overcurrent threshold to supply in low on-resistance mode	V_S = 13.5 V; V_{CC} = 5 V; source	1.5		2.5	A
	Overcurrent threshold to supply in high on-resistance mode		0.35		0.65	A
$|I_{OC8}|$	Overcurrent threshold to supply in low on-resistance mode		0.7		1.3	A
	Overcurrent threshold to supply in high on-resistance mode		0.35		0.65	A
$|I_{OC9}|$, $|I_{OC10}|$	Overcurrent threshold to supply		0.5		1.0	A
$|I_{OC11}|$			5		7.5	A
$|I_{OCECV}|$	Output current limitation to GND	V_S = 13.5 V; V_{CC} = 5 V; sink	0.5		1.0	A
t_{FOC}	Filter time of overcurrent signal	Duration of overcurrent condition to set the status bit	10	55	100	μs
f_{rec0}	Recovery frequency for OC; recovery frequency bit = 0		1		4	kHz
f_{rec1}	Recovery frequency for OC; recovery frequency bit = 1		2		6	kHz
$|I_{OLD1}|$, $|I_{OLD6}|$		V_S = 13.5 V; V_{CC} = 5 V; sink and source	8	30	80	mA
$|I_{OLD2}|$, $|I_{OLD3}|$, $|I_{OLDECFD}|$	Undercurrent threshold to supply or GND		10	20	30	mA
$|I_{OLD4}|$, $|I_{OLD5}|$			60	150	300	mA
$|I_{OLD7}|$	Undercurrent threshold to supply in low on-resistance mode		15	40	60	mA
	Undercurrent threshold to supply in high on-resistance mode		5	10	15	mA
$|I_{OLD8}|$	Undercurrent threshold to supply in low on-resistance mode	V_S = 13.5 V; V_{CC} = 5 V; source	10	30	45	mA
	Undercurrent threshold to supply in high on-resistance mode		5	10	15	mA
$|I_{OLD9}|$, $|I_{OLD10}|$	Undercurrent threshold to supply		10	20	30	mA
$|I_{OLD11}|$			30	150	300	mA

Table 14. Current monitoring (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$|I_{OLDECV}|$	Undercurrent threshold to GND	$V_S = 13.5$ V; $V_{CC} = 5$ V; sink	10	20	30	mA
t_{FOL}	Filter time of open-load signal	Duration of open-load condition to set the status bit	0.5	2.0	3.0	ms

2.7 H-bridge driver

Table 15. Gate drivers for the external Power-MOS (H-bridge)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high-side Power-MOS						
$I_{GHx(Ch)}$	Average charge current (charge stage)	$T_j = 25$ °C		0.3		A
R_{GHx}	On-resistance (discharge-stage)	$V_{SHx} = 0$ V; $I_{GHx} = 50$ mA; $T_j = 25$ °C	4	6	8	Ω
		$V_{SHx} = 0$ V; $I_{GHx} = 50$ mA; $T_j = 125$ °C		8	10	Ω
V_{GHxH}	Gate-on voltage	Outputs floating	$V_{SHx} + 8$	$V_{SHx} + 10$	$V_{SHx} + 11.5$	V
R_{GSHx}	Passive gate-clamp resistance	$V_{GHx} = 0.5$ V		15		kΩ
Drivers for external low-side Power-MOS						
$I_{GLx(Ch)}$	Average charge-current (charge stage)	$T_j = 25$ °C		0.3		A
R_{GLx}	On-resistance (discharge-stage)	$V_{SLx} = 0$ V; $I_{GHx} = 50$ mA; $T_j = 25$ °C	4	6	8	Ω
		$V_{SLx} = 0$ V; $I_{GHx} = 50$ mA; $T_j = 125$ °C		8	10	Ω
V_{GHLx}	Gate-on voltage	Outputs floating	$V_{SLx} + 8$	$V_{SLx} + 10$	$V_{SLx} + 11.5$	V
R_{GSLx}	Passive gate-clamp resistance			15		kΩ

Table 16. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode)[1]	$V_S = 13.5$ V; $V_{SHx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		1.5		µs
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)[1]	$V_S = 13.5$ V; $V_{SLx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		1.5		µs

Table 16. Gate drivers for the external Power-MOS switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{GHxrmax}$	Maximum charge current (current mode)	$V_S = 13.5$ V; $V_{SHx} = 0$; $V_{GHx} = 1$ V; SLEW < 4:0 ≥ 1 F_H	24.5	31	38.5	mA
$I_{GHxfmax}$	Maximum discharge current (current mode)	$V_S = 13.5$ V; $V_{SHx} = 0$; $V_{GHx} = 2$ V; SLEW < 4:0 ≥ 1 F_H	18.5	25	33	mA
dI_{IGHxr}	Charge current accuracy	$V_S = 13.5$ V; $V_{SHx} = 0$; $V_{GHx} = 1$V		See *Figure 6*		
dI_{IGHxf}	Discharge current accuracy	$V_S = 13.5$ V; $V_{SHx} = 0$; $V_{GHx} = 2$ V		See *Figure 7*		
$V_{DSHxrSW}$	Switching Voltage (V_S - V_{SH}) between current mode and switch mode (rising)	$V_S = 13.5$ V		1.5		V
V_{TDSHxf} [2]	Trigger Voltage to sample the V_{GSH} for switching between switch mode and current mode (falling)	$V_S = 13.5$ V; $V_{GHx} = 4$ V		1.5		V
$V_{TGSHxacc}$ [2]	Sampled trigger voltage accuracy	$V_S = 13.5$ V; $V_{SHx} = 0$		1		V
$t0_{GHxr}$	Rise time (switch mode)	$V_S = 13.5$ V; $V_{SHx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		45		ns
$t0_{GHxf}$	Fall time (switch mode)	$V_S = 13.5$ V; $V_{SHx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		85		ns
$t0_{GLxr}$	Rise time	$V_S = 13.5$ V; $V_{SLx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		45		ns
$t0_{GLxf}$	Fall time	$V_S = 13.5$ V; $V_{SLx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF		85		ns
t_{CCP}	Programmable cross-current protection time		0.1		5	µs
f_{PWMH}	PWMH switching frequency[1]	$V_S = 13.5$ V; $V_{SLx} = 0$; $R_G = 0$ Ω; $C_G = 2.7$ nF; PWMH - duty cycle = 50 %			50	kHz

1. Without cross-current protection time t_{CCP}

2. Parameter not tested, typical value validated by characterization.
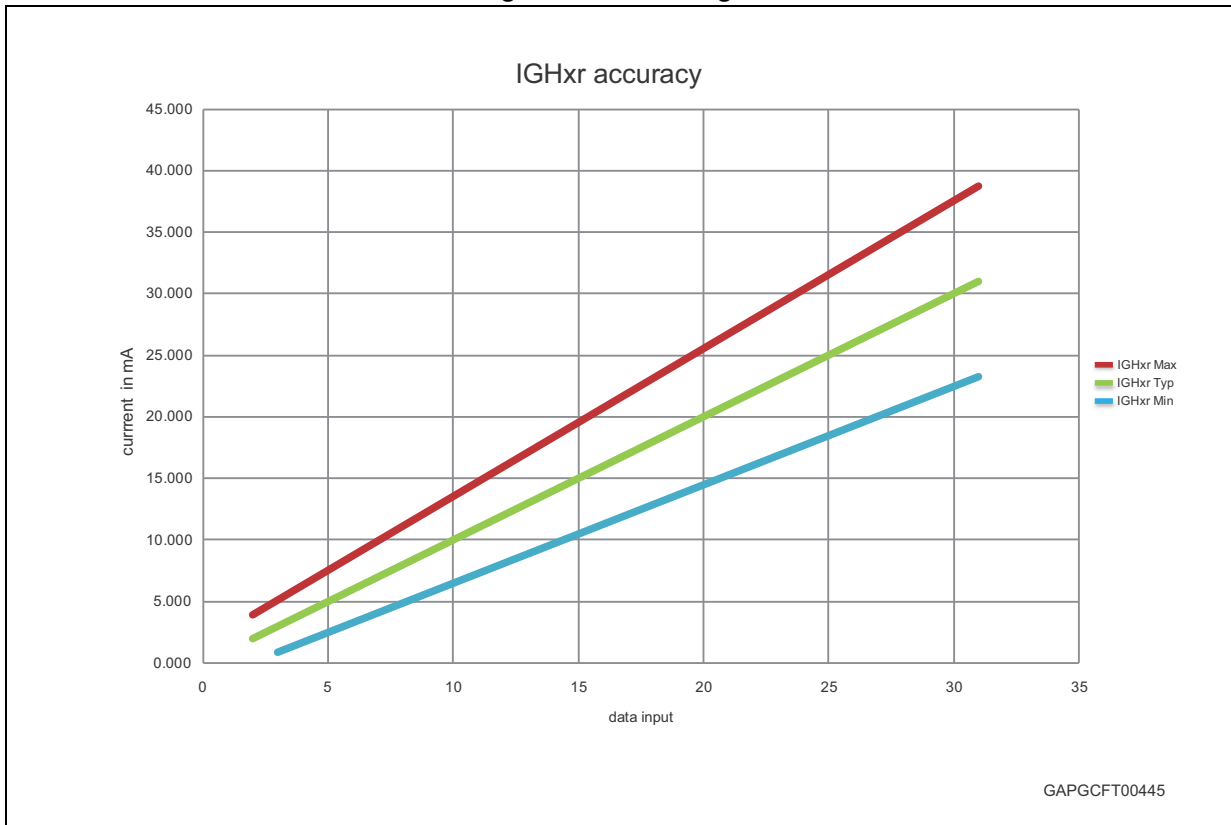
Figure 6. IGHxr ranges

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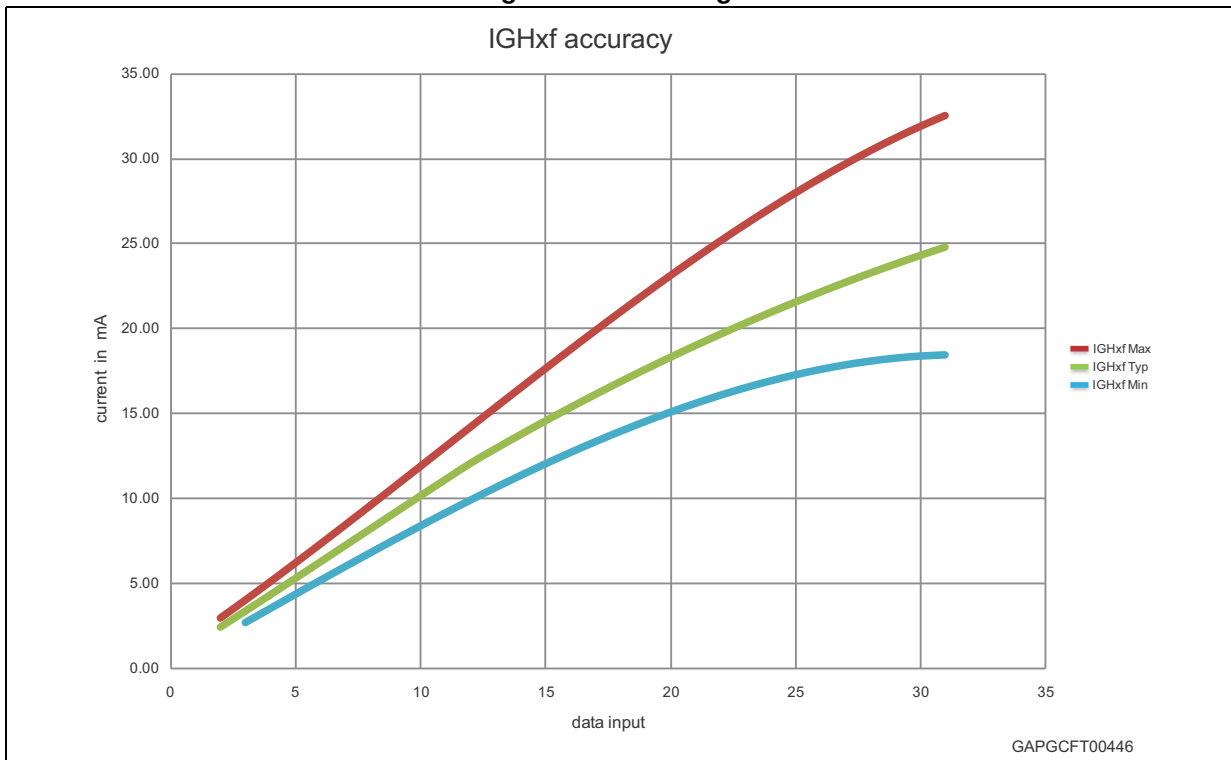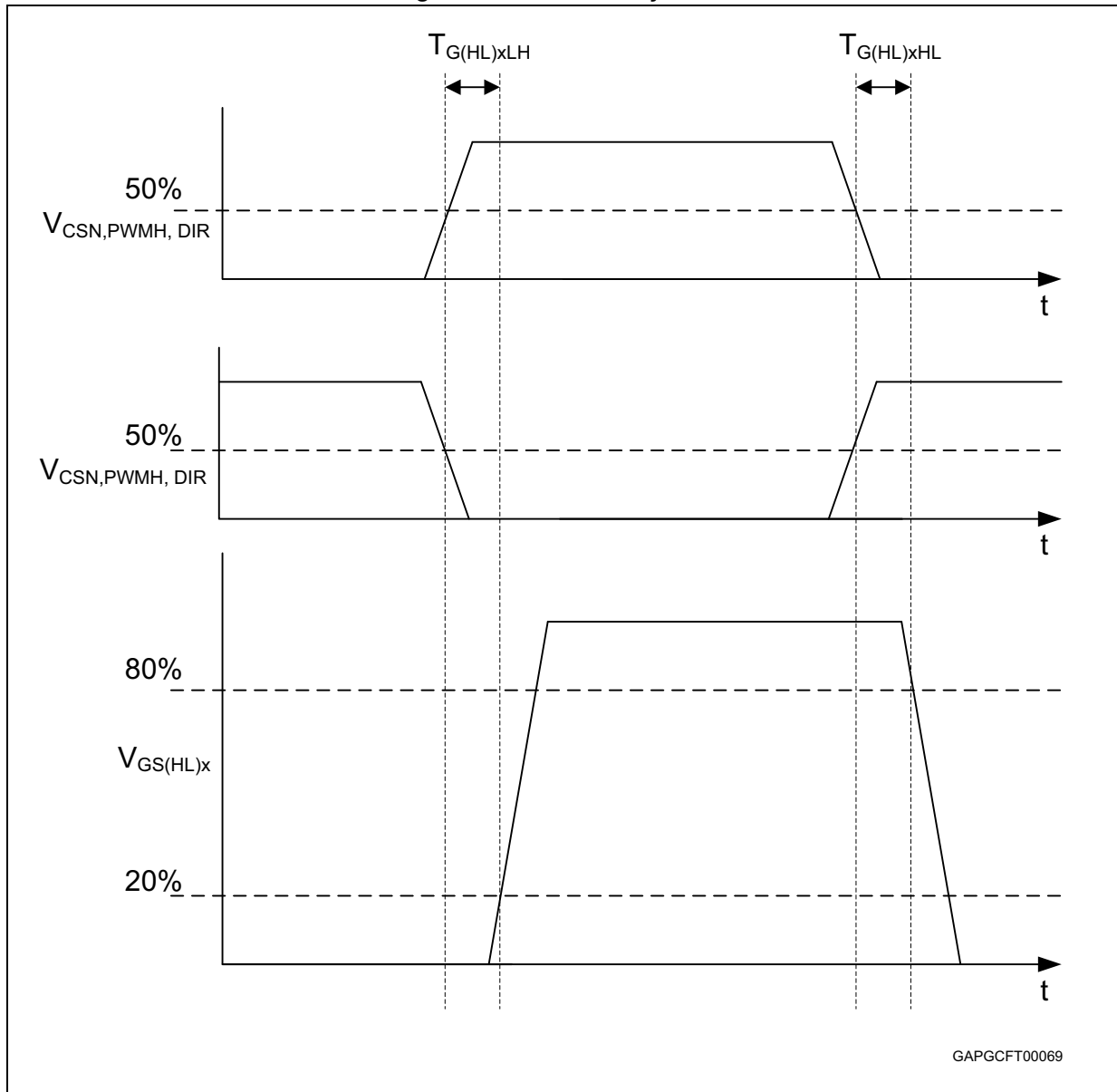**Figure 7. IGHxf ranges**

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Figure 8. H-driver delay times

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Table 17. Drain source monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SCd1}	Drain-source threshold voltage	V_S = 13.5 V	0.3	0.5	0.7	V
V_{SCd2}	Drain-source threshold voltage	V_S = 13.5 V	0.8	1	1.2	V
V_{SCd3}	Drain-source threshold voltage	V_S = 13.5 V	1.2	1.5	1.8	V
V_{SCd4}	Drain-source threshold voltage	V_S = 13.5 V	1.6	2	2.4	V
t_{SCd}	Drain-source monitor filter time		3	5.5	8	µs
t_{scs}	Drain-source comparator settling time	V_S = 13.5 V; V_{SH} = jump from GND to V_S	—		5	µs

Table 18. Open-load monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ODSL}	Low-side drain-source monitor low off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.14 * V_S	0.18 * V_S	0.21 * V_S	V
V_{ODSH}	Low-side drain-source monitor high off-threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.75 * V_S	0.85 * V_S	0.95 * V_S	V
V_{OLSHx}	Output voltage of selected SHx in open-load test mode	V_{SLx} = 0 V; V_S = 13.5 V		0.5 * V_S		V
R_{pdOL}	Pull-down resistance of the non-selected SHx pin in open-load mode	V_{SLx} = 0 V; V_S = 13.5 V; V_{SHX} = 4.5 V		20		kΩ
T_{OL}	Open-load filter time			2		ms

2.8 Electrochrome mirror driver

Table 19. Electrochrome mirror driver

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$V_{CTRLmax}$	Maximum EC-control voltage	Bit0 = 1 control reg. 2[1]		1.4		1.6	V
		Bit0 = 0 control reg. 2[1]		1.12		1.28	V
DNL_{ECV}[2]	Differential non linearity			-1		1	LSB[3]
$IdV_{ECV}I$	Voltage deviation between target and ECV	dV_{ECV} = V_{target}[4] - V_{ECV}; $II_{ECDR}I$ < 1 µA		-5 % - 1LSB[3]		+5 % + 1LSB[3]	mV
dV_{ECVnr}	Difference voltage between target and ECV sets flag if V_{ECV} is	below it	dV_{ECV} = V_{target}[4] - V_{ECV}; toggle bitx = 1 status reg. x		120		mV
dV_{ECVhi}		above it			-120		mV
t_{FECVNR}	ECV_{NR} filter time				32		µs
t_{FECVHI}	ECV_{HI} filter time				32		µs
$V_{ECDRminHIGH}$	Output voltage range	I_{ECDR} = -10 µA		4.5		5.5	V
$V_{ECDRmaxLOW}$		I_{ECDR} = 10 µA		0		0.7	V
I_{ECDR}	Current into ECDR	V_{target}[4] > V_{ECV} + 500 mV; V_{ECDR} = 3.5 V		-100		-10	µA
		V_{target}[4] < V_{ECV} - 500 mV; V_{ECDR} = 1.0 V; V_{target} = 0 V; V_{ECV} = 0.5 V		10		100	µA
$R_{ecdrdis}$	Pull-down resistance at ECDR in fast discharge mode and while EC-mode is off	V_{ECDR} = 0.7 V; ECON = '1'; EC<5:0> = 0 or ECON = '0'				10	kΩ
DNL_{ECFD}[2]	Differential Non Linearity			-1		1	LSB[3]
$IdVECFDI$	Voltage deviation between target and ECFD	dV_{ECFD} = V_{target}[4] - V_{ECFD}; I_{ECFD} < TBD mA		-5 %- 1LSB[3]		+5 %+ 1LSB[3]	mV