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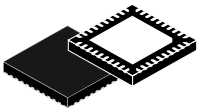
L99LD20

High power LED driver for automotive applications

Datasheet - production data



QFN-40L 6x6

Features

- AEC-Q100 qualified
- General
  - ST SPI communication v4.1
  - 5.5 to 24 V Operating battery voltage range
  - Load dump protected
  - QFN40L 6x6 (wettable flanks) with exposed pad
  - Timeout watchdog and limp home function
  - Low standby current
- Buck section
  - Integrated switching mosfets
  - Lossless current sensing without need of external components
  - Very accurate LED current setting programming inductor's peak current and peak-to-peak current ripple
  - Adjustable peak current by SPI
  - Adjustable current ripple by SPI
  - Integrated PWM generation unit with 10-bit resolution and phase shift
  - Peak current control
  - Constant VLED x TOFF architecture
- Protection and diagnostic
  - Battery under voltage
  - Temperature warning (2 thresholds)
  - Overtemperature shutdown
  - LED voltage digital feedback through SPI
  - Buck outputs short circuit and open load protection

Applications

- Low Beam
- High beam
- Daytime running light
- Turn indicator
- Position light
- Side marker
- Fog light

Description

The L99LD20 is a flexible LED driver, which is specifically designed for the control of two independent high brightness LED strings for automotive front lighting applications. It consists of a high efficiency monolithic dual buck converter.

The buck converters integrate n-channel MOSFET which is driven by a bootstrap circuit.

When more than two LED channels are required on one module, then more devices L99LD20 can be combined; also with L99LD21 device – incorporating Boost Controller - from which L99LD20 derivate.

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1 Introduction

The L99LD20 is a monolithic driver IC, which controls the current of two independent high power LED strings, whose forward current and voltage can reach up to 1.5 A (average) and up to 50 V respectively.

This device has been designed with dedicated functions, in order to fulfill the stringent requirements of automotive front lighting applications.

The device offers a high level of flexibility, without any change of the external components, thanks to its programmability through the ST SPI interface. This feature support generic platform approaches, which require a software configurability of several parameters. This robust interface, offers a detailed diagnostic of the device itself, as well as of the controlled LED strings.

As the device potentially controls safety critical functions such as low beams and turn indicators, built-in features are integrated in order to support a high level of functional safety. The L99LD20 features a timeout watchdog, a monitoring of the watchdog counter, a limp home function and a direct input. The ST SPI protocol takes into account FMEA case.

The device consists of two independent integrated buck converters, whose input voltage is compatible with V_{BUCKIN}. The integrated buck converters are based on constant off-time architecture (for a given LED output voltage) and control the peak current and the peak-to-peak current ripple of their respective inductors. Operating in continuous conduction mode, the average of each LED string's current, which is connected to the output of each buck converter, is tightly controlled. This architecture, which consists of two independent buck stages, allows the control of a wide range of LED strings, whose forward voltage is independent from the battery voltage.

With the aim of ensuring a wide operating inductor current range, the Buck mosfets can be set in low or high R_{DS_ON} modes, so that two different inductor peak current (I_{Lx_PEAK}) ranges [0.179 A ÷ 0.849 A] or [0.362 A ÷ 1.695 A] can be selected.

The average LED current is controlled by setting the inductor's peak current and peak-to-peak current ripple. Sensing of the peak current is integrated, not requiring any external shunt resistance, which saves cost and reduces the power dissipation.

Buck n-channel mosfet R_{DS_ON} value depends on the operative conditions as junction temperature, Input voltage and LED string current. For example, at V_{Buckin} = 45 V, I_{led} = 700 mA, T_j = 25 °C the maximum R_{DS_ON} is 400 mΩ (low R_{DS_ON} mode).

1.1 Typical application

Figure 1. Functional block diagram

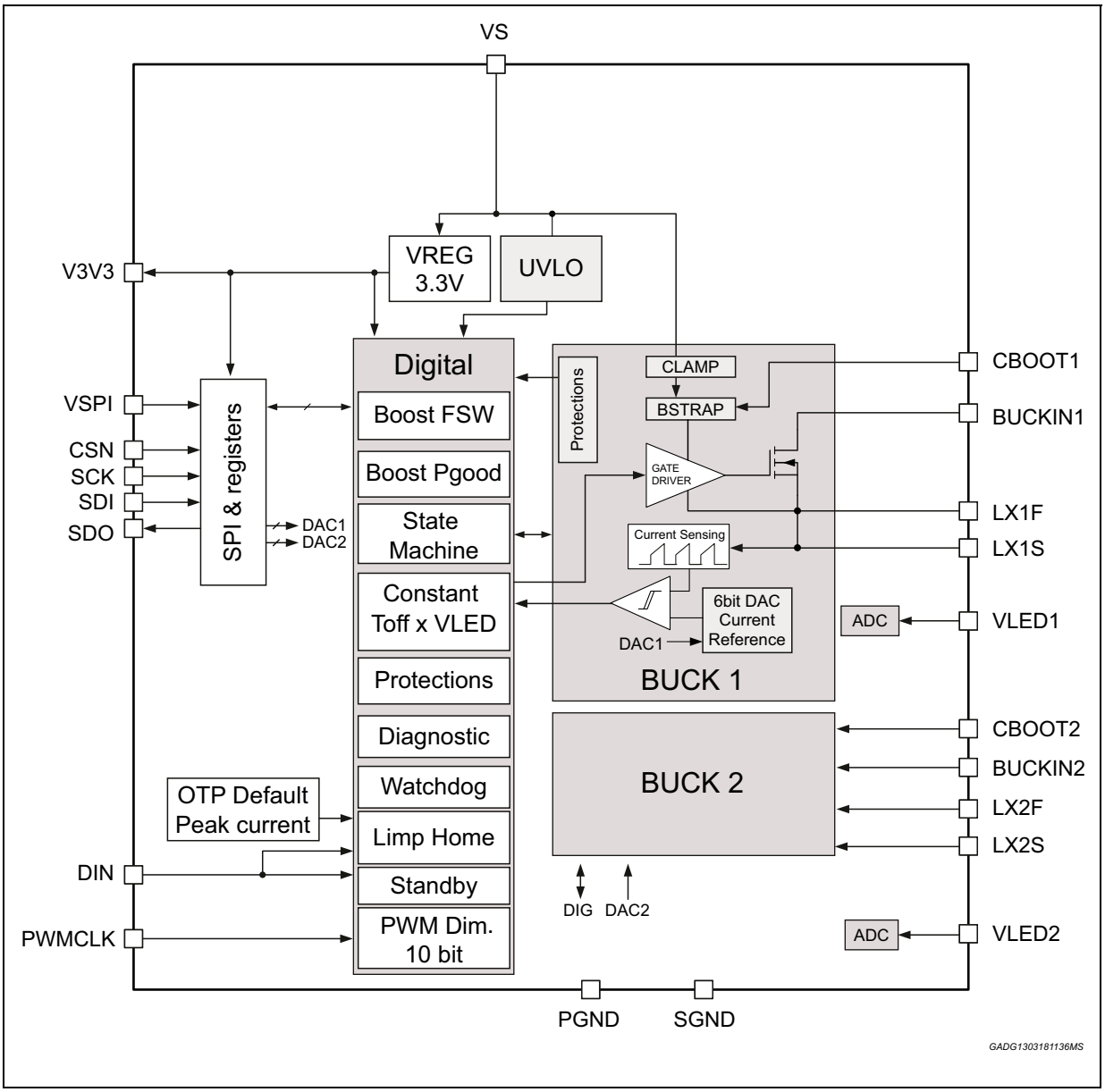


Figure 2. Typical application schematic

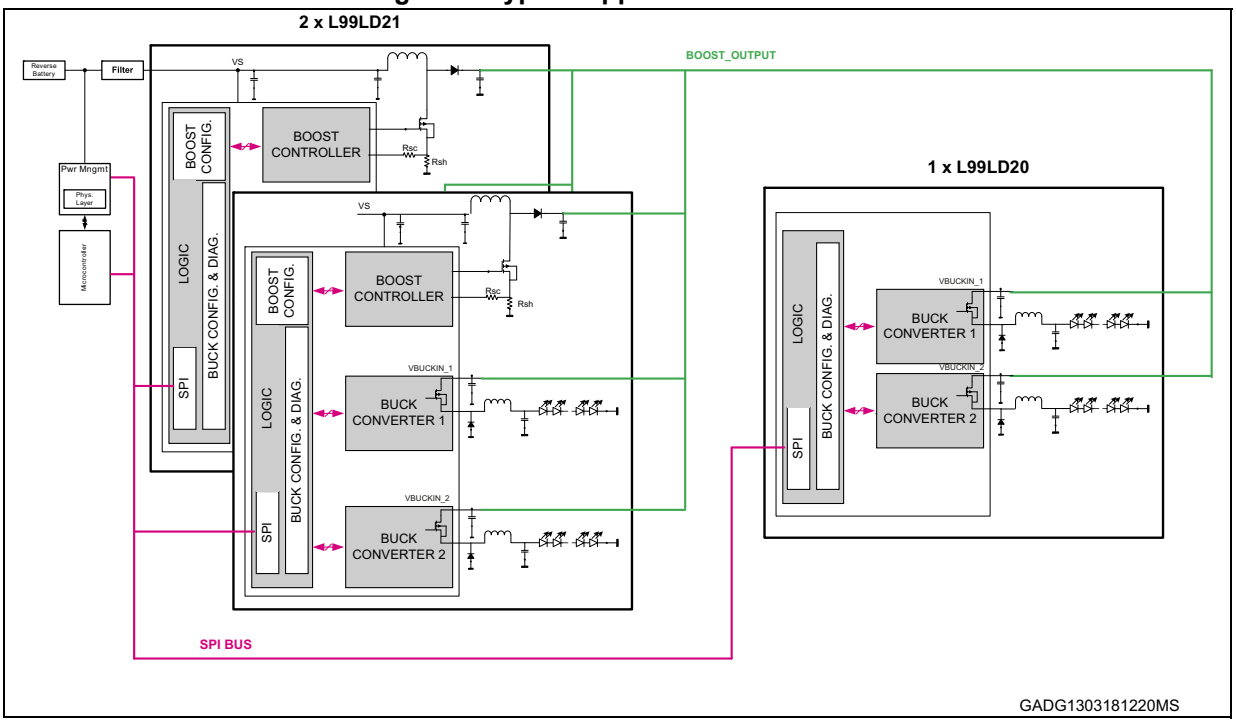


Figure 3. Application diagram

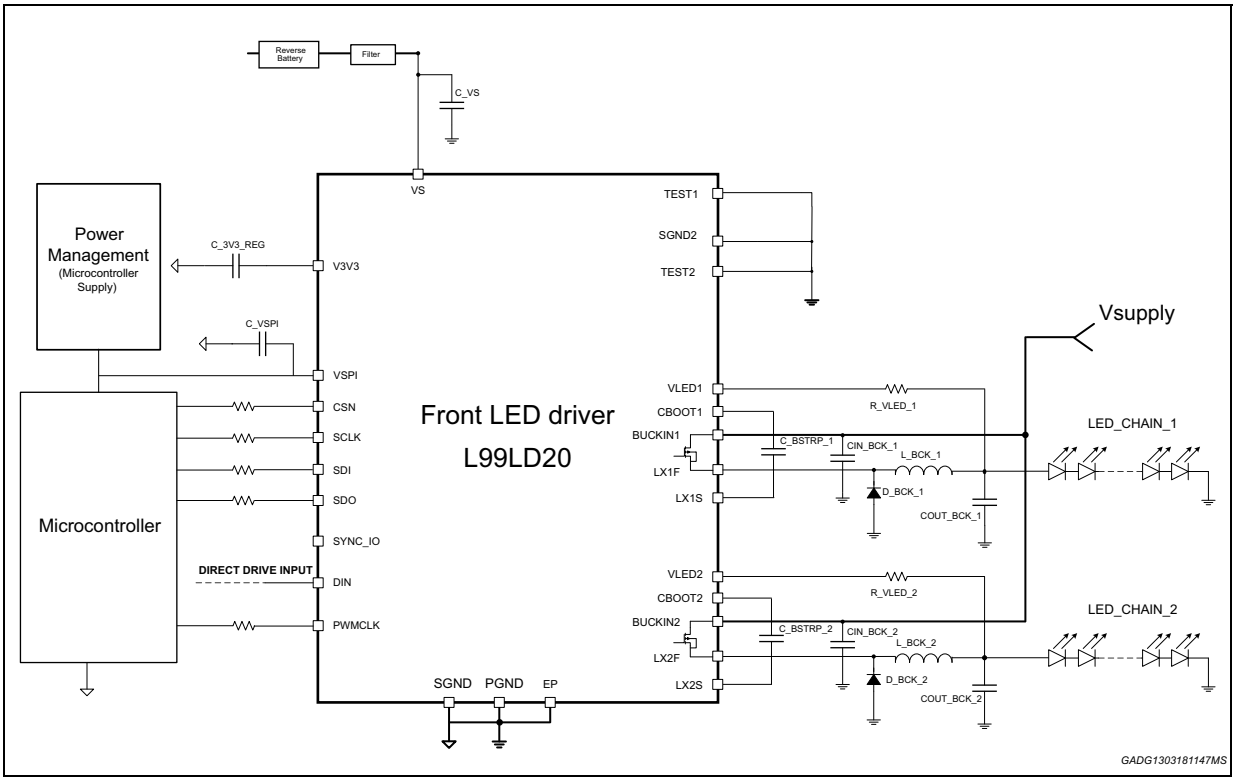


Figure 4. Connection diagram

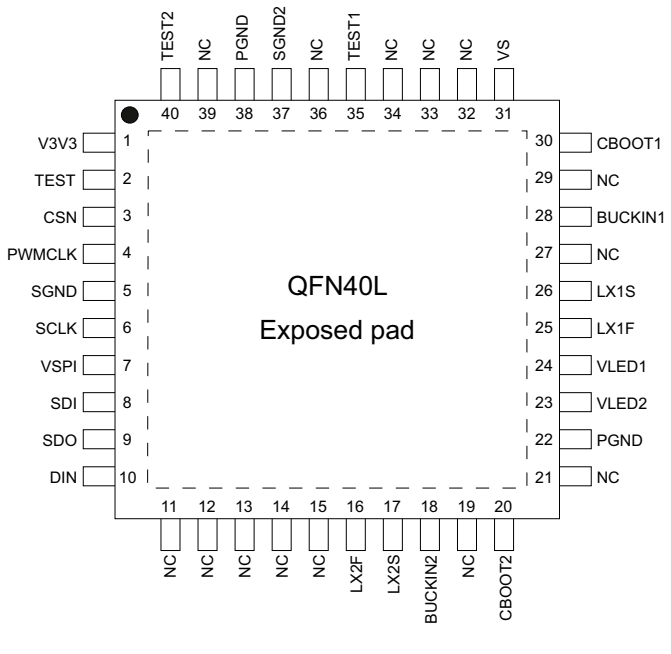


Table 1. Pin functionality

Pin #	Name	Function
1	V3V3	Output of the 3.3 V regulated internal supply. Connect a low ESR capacitor (4.7 µF) close to this pin.
2	TEST	Internal function. Left open.
3	CSN	Chip Select Not (active low) for SPI communication. It is the selection pin of the device. It is a CMOS compatible input.
4	PWMCLK	Clock input for the internal PWM dimming generator.
5	SGND	Signal Ground connection.
6	SCK	Serial Clock for SPI communication. It is a CMOS compatible input.
7	VSPI	Connection to external 3.3 V or 5 V supplies voltage. The external supply powers SPI interface and the I/O signal pins to the microcontroller. It is suggested to connect 100nF capacitor close to this pin.
8	SDI	Serial Data Input for SPI communication. Data is transferred serially into the device on SCK rising edge.
9	SDO	Serial Data Output for SPI communication. Data is transferred serially out of the device on SCK falling edge.
10	DIN	Direct input pin.
16	LX2F	Connection to the switching source node of the buck2. This pin must be connected to external free-wheeling diode.
17	LX2S	Kelvin connection to the switching source node of the buck2. This pin has to be connected to external bootstrap capacitance.

Table 1. Pin functionality (continued)

Pin #	Name	Function
18	BUCKIN2	Connection to the input of the buck channel 2
20	CBOOT2	Connection to the bootstrap capacitor (100nF) of the buck channel 2.
22, 38	PGND	Power Ground connection.
23	VLED2	Connection to the anode of the LED string for read back of the forward voltage of the channel 2.
24	VLED1	Connection to the anode of the LED string for read back of the forward voltage of the channel 1.
25	LX1F	Connection to the switching source node of the buck1. This pin must be connected to external free-wheeling diode.
26	LX1S	Kelvin connection to the switching source node of the buck1. This pin has to be connected to external bootstrap capacitance.
28	BUCKIN1	Connection to the input of the buck channel 1.
30	CBOOT1	Connection to the bootstrap capacitor (100 nF) of the buck channel 1.
31	VS	Input supply pin of the IC. Connect VS to the battery voltage.
35	TEST1	Internal function. To be tied to GND.
37	SGND2	Signal ground connection.
40	TEST2	Internal function. To be tied to GND.
11, 12, 13, 14, 15, 19, 21, 27, 29, 32, 33, 34, 36, 39	NC	Not connected

2 Buck converters

2.1 General description

The L99LD20 features two independent buck converters with integrated switching mosfets with forward peak current as high as specified maximum I_{Lx_PEAK} (where x indicates Buckx peak current) 1.695 A. They are optimized to deliver a constant current to LED strings.

The R_{DS_ON} of the n-channel mosfets can be set programming the appropriate bit in the control register (see bits <3:2> on *Table 13: CR#1: Control Register 1*): high R_{DS_ON} mode (only one half power stage enabled) or low R_{DS_ON} mode (both half power stages enabled).

This feature allows having two different inductor peak current ranges, 0.179 A ÷ 0.849 A or 0.362 A ÷ 1.695 A, respectively for high R_{DS_ON} and low R_{DS_ON} mode, so achieving the highest of current sense accuracy in the whole current range.

The buck converters are based on constant off-time architecture, which regulates the peak current in each inductor. The monitoring of the inductor peak current is done through integrated senseFETs. This results in a lossless high side current sensing, which does not require any external shunt resistor, and improves the system efficiency.

This architecture provides an inherent cycle-by cycle current limitation and a fast transient response, without any compensation of the control loop.

The average LED current in each LED string is configurable by the SPI, through configuration of the inductor peak current and peak-to-peak current.

The dimming of the LED strings can be realized through the direct input pin (DIN) or through the internal 10-bit PWM dimming generator.

2.2 Bootstrap circuit

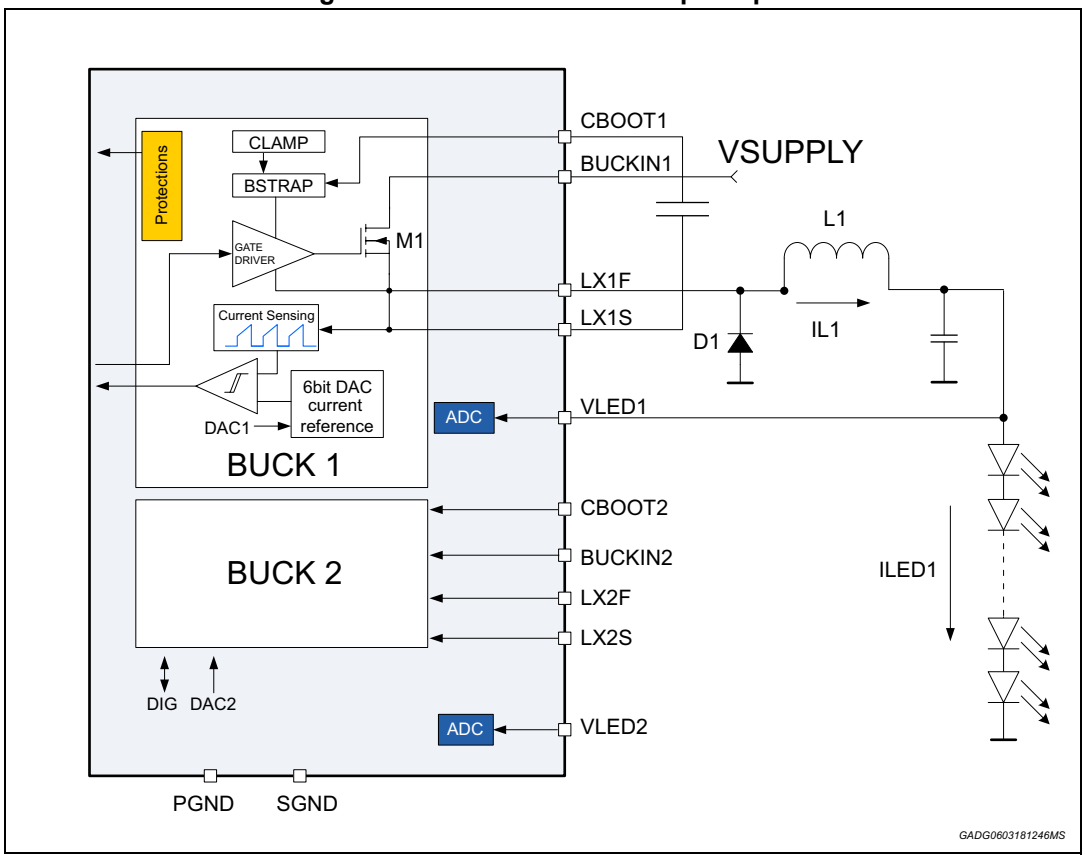
The L99LD20 has built-in high side n-channel switching mosfets, which are driven by gate drivers. Each gate driver uses a bootstrap circuit, consisting of an integrated diode and an external capacitor between the LX1S and CBOOT1 pins, respectively between the LX2S and CBOOT2 pins.

The buck converters impose a minimum off-time (T_{OFF_MIN}) to ensure that the bootstrap capacitor recharges every cycle to a voltage which avoids the switching mosfet to operate in linear mode. T_{OFF_MIN} restricts the maximum duty cycle of the buck converters for a given switching frequency. This effect is more pronounced at high switching frequencies and limits the maximum ratio between the buck input voltage (V_{BOOST}) and the LED strings' forward voltage. One way to overcome this limitation is reducing switching frequency, by selecting high constant VLED xTOFF and/or increase the inductance value.

2.3 Peak and average current setting

In buck converters, the inductor is directly connected to the load during the complete switching cycle (see *Figure 5: Peak current control principle*). The average inductor current is equal to the average LED string current. Operating in continuous conduction mode (i.e. the inductor current never decays to zero during the off-phase), if the inductor current is tightly controlled, the LED current will be regulated as well.

Figure 5. Peak current control principle



At the beginning of a switching period the MOSFET M1 is turned on, and the inductor current I_{L1} increases. The mosfet is activated for a minimum on-time T_{ON_MIN} in order to avoid that the on-phase is ended up by spurious noise, which is caused by the switch-on.

During mosfet activation, the inductor current, I_{L1}, increases until reaching a maximum value, I_{L1_PEAK}, which is set through a dedicated control register (see bits <23:18> and bits <17:12> on *Table 14: CR#2: Control Register 2*). When I_{L1} reaches its peak value, the switching mosfet is turned off. The mosfet remains off for a time T_{OFF}, which is derived from the configured constant VLED1xTOFF1 (see bits <11:8> and bits <7:4> on *Table 14: CR#2: Control Register 2*), where V_{LED1} is the forward voltage of the LED string, which is connected at the output of the buck converter 1.

During T_{OFF}, the inductor current decreases by:

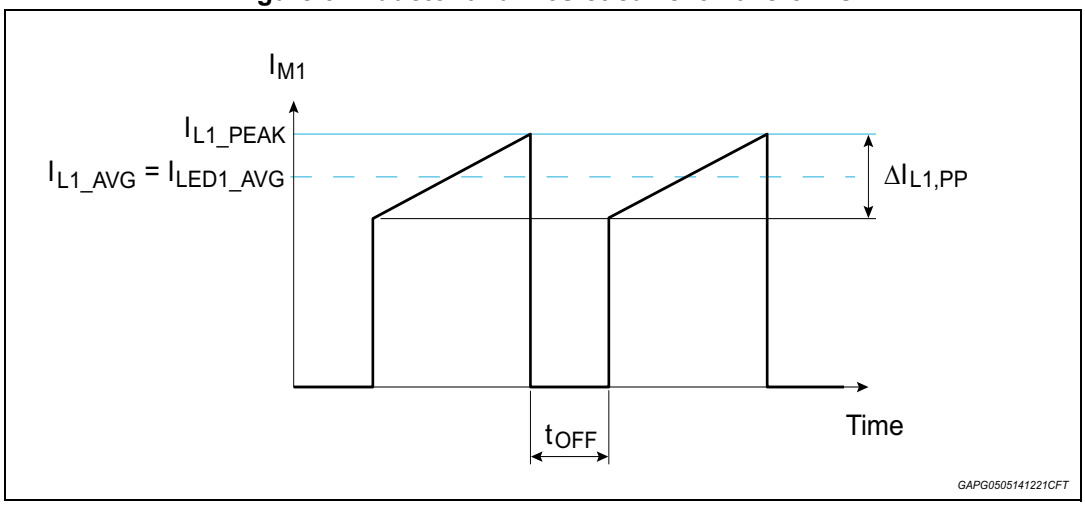
$$\Delta I_{L1\_PP} = \frac{(V_{LED1} - V_{F\_D1})}{L_1} \cdot T_{OFF1} \sim \frac{V_{LED1} \cdot T_{OFF1}}{L_1}$$

where ΔI_{L1_PP} is the inductor peak to peak current and V_{F_D1} is the forward voltage of the diode D1. As D1 is a Schottky diode with a low forward voltage, V_{F_D1} can be in general neglected, compared to V_{LED1}.

Note: Once the VLEDxTOFF constant for a given buck converter is selected by SPI, the peak-to-peak inductor current ripple is constant. In particular, it depends neither on the boost voltage nor on the LED forward voltage.

The ripple current through the LED strings is reduced by means of an external capacitor in parallel with the LEDs.

Figure 6. Inductor and mosfet current waveforms



Referring to the *Figure 5* and *Figure 6* the average LED current - valid for both Buck 1 and Buck 2 - is therefore:

$$I_{LED1\_AVG} = I_{L1\_AVG} = I_{L1\_PEAK^*} - \frac{(\Delta I_{L1\_PP})}{2} = I_{L1\_PEAK^*} - \frac{(V_{LED} \cdot T_{OFF1})}{2L}$$

where $I_{L1\_PEAK^*}$ results from I_{L1_PEAK} (see *Table 35*) corrected with loop delay (t_{loop_delay})

In order to achieve the best accuracy versus input voltage variation during current sensing process, a defined buck input voltage window must be selected, by means of a dedicated control register (see bits <5:4> and bits <3:2> on *Table 15: CR#3: Control Register 3*).

2.4 Buck converter's blank time

The buck converters have a minimum on-time T_{BLANK_BUCK}. Although the inductor's target peak current I_{Lx_PEAK} is reached before this time has elapsed, the switch is kept on. This delay is used as a leading-edge blank time, in order to avoid a premature end of the switching cycle, which might be caused by the noise, which results from the commutation of the buck's mosfet.

2.5 Buck converter's start-up

While the device and the system are protected against short circuit conditions of the buck's output to GND, the device inhibits the detection of the short circuit during the startup phase $T_{STARTUP}$.

A startup phase is applied in the following conditions:

- If one of the buck converters is activated for the first time after a power on reset (POR), including buck activation after device wake-up;
- If one of the buck converters has been deactivated for more than t_{DELAY};
- If one of the buck converters has been latched off prior to a Read and Clear command;
- If one of the buck converters is re-activated after a VS under voltage event.

After these events, it is possible that the output capacitors of the buck converters are completely discharged. The charging of the buck output capacitors might lead switching cycles with short on-time (shorter than T_{ON_MIN}), which could potentially lead to a wrong detection of a shorted buck output. The introduction of this start-up phase avoids this wrong diagnostic.

2.6 Switching frequency

For a given buck converter, the switching frequency depends on the buck input voltage and the forward voltage of the LED string, which is connected to its output.

In continuous conduction mode, T_{OFF} is given by:

$$T_{OFF} = (1 - D) \cdot T = \frac{1 - D}{F_{SW}}$$

Where D is the buck converter's duty cycle, T and F_{SW} are respectively the switching period and frequency.

Neglecting the drop voltage across the mosfet, the inductor's DC resistance and the diode's forward voltage, compared to V_{BUCKIN} and V_{LED}, we have:

$$D = \frac{V_{LED}}{V_{BUCKIN}}$$

$$F_{SW} = \frac{1 - \frac{V_{LED}}{V_{BUCKIN}}}{T_{OFF}} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{V_{LED} \cdot T_{OFF}}$$

For a given application (given inductance and V_{LED}), it is possible to set I_{LEDx_AVG} by selecting different combinations of I_{Lx_PEAK} and $V_{LED}xT_{OFF}$ in order to avoid critical frequency ranges such as the AM radio band.

To avoid buck operation at not allowed T_{ON} and/or T_{OFF} times, frequency range has to be kept inside F_{SWmin} and F_{SWmax}, where:

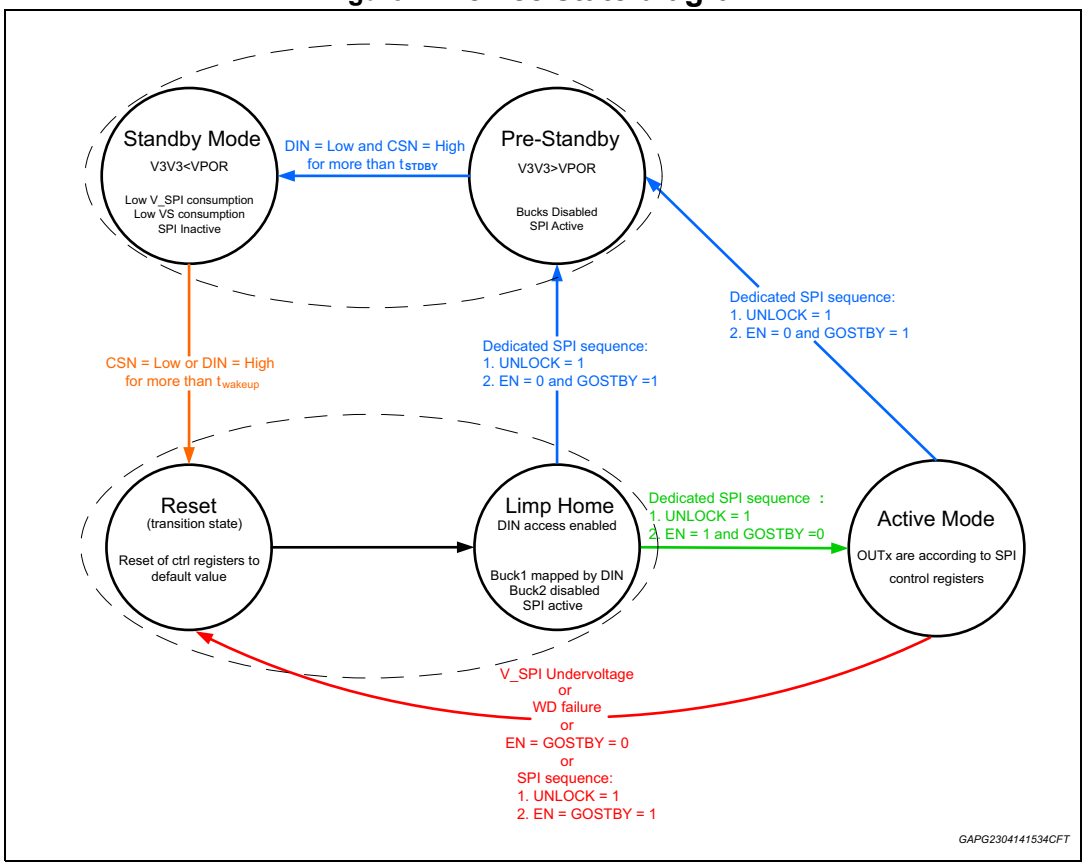
$F_{SWmin} = 1/(T_{ON\_MAX\_BUCK} + T_{OFF\_MAX\_BUCK})$

$F_{SWmax} = 1/(T_{ON\_MIN\_BUCK} + T_{OFF\_MIN\_BUCK})$

3 Functional description

3.1 Operating modes

Figure 7. Device state diagram



3.1.1 Standby mode

The pre-requisite for this mode is:

- Device in Pre-Standby mode.

The device enters Standby mode under the following conditions:

- By default, once the device is powered (VS present);
- CSN High and DIN Low for more than t_{STDBY}

The Standby mode characteristics are:

- V3V3 < VPOR
- V_{SPI} and V_S low consumption
- SPI inactive

The device leaves this mode if:

- DIN High or CSN Low for a time t > t_{WAKEUP}

Note: V_s must be stable above minimum value specified (5.5 V) before rising edge on DIN or falling edge on CSN.

3.1.2 Pre-standby mode

The device enters Pre-standby mode under the following conditions:

- upon the two following consecutive SPI frames setting:
  - UNLOCK = 1
  - (EN, GOSTBY) = (0, 1)

The Pre-standby mode characteristics are:

- V3V3 > VPOR
- Bucks disabled
- SPI active

The device leaves automatically Pre-standby mode entering standby:

- if CSN High and DIN Low for a time t > t_{STDBY}

3.1.3 Reset mode

The device enters Reset mode under the following conditions:

- By default, once the device leaves Standby mode;
- If device state is Active mode, when one of the following events occur:
  - V_{SPI} under voltage;
  - Watchdog failure
  - One SPI frame setting (EN,GOSTBY) = (0,0)
  - Two consecutive SPI frames setting
    UNLOCK = 1
    (EN,GOSTBY) = (1,1)

The Reset mode characteristics are:

- V3V3 > VPOR
- All the control and status registers set to their default values
- SPI inactive

The device leaves automatically Reset mode and enters Limp home after 400 ns (typical).

3.1.4 Limp home

The device enters Limp Home automatically 400 ns after Reset mode.

Limp home characteristics are:

- Direct Input access enabled
- Buck1 according DIN
- Buck2 OFF
- SPI active:
  - All SPI write operations must be allowed without any effects on the device behavior.

When the device leaves this mode, it can enter Standby or Active mode.

If the microcontroller sends to the device the following SPI frames sequence:

- The first SPI frame sets UNLOCK bit = 1
  (see bit <1> on *Table 13: CR#1: Control Register 1*)
- The second consecutive SPI frame sets GOSTBY bit = 1 and EN bit = 0
  (see bit <3> and bit <2> on *Table 14: CR#2: Control Register 2*)

The device enters Standby mode.

If the microcontroller sends to the device the sequence of the following SPI frames:

- The first SPI frame sets UNLOCK bit = 1;
  (see bit <1> on *Table 13: CR#1: Control Register 1*)
- The second consecutive SPI frame sets GOSTBY bit = 0 and EN bit = 1.
  (see bit <3> and bit <2> on *Table 14: CR#2: Control Register 2*)

The device enters Active mode.

In Limp Home, after setting bit 27 on GSB (FE1, functional error bit), an auto restart procedure is implemented: every $t_{AUTORESTART}$, functional error bit eventually set is automatically cleared.

3.1.5 Active mode

The device enters the Active mode if the microcontroller sends the following SPI frames sequence:

- In a first SPI frame set the UNLOCK bit to 1
  (see bit <1> on *Table 13: CR#1: Control Register 1*)
- In a second frame, set EN bit to 1 and GOSTBY bit to “0”
  (see bit <2> and bit <3> on *Table 14: CR#2: Control Register 2*)

Table 2. Operating modes

Operating mode	Entering conditions	Leaving condition	Characteristics
Standby mode	– By default, once powered on (VS present); – SPI active and micro sending following consecutive frames: UNLOCK = 1 (EN,GOSTBY) = (0,1)	DIN = High for t_{WAKEUP} and/or CSN = Low for t_{WAKEUP}	– V3V3 < VPOR; – V_S and V_{SPI} low consumption; – SPI inactive
Pre-standby mode	– Under the following conditions: Two following consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (0,1)	CSN High and DIN Low for a time t > t_{STDBY}	– V3V3 > VPOR – Bucks disabled – SPI active
Reset mode	– By default, when device leaves Standby mode – Under following condition, when device is in Active mode: V_{SPI} Under voltage WD failure; One SPI frame setting (EN,GOSTBY) = (0,0) Two consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (1,1)	Automatic transition after 400 ns	– All registers reset to default values – V3V3>VPOR – SPI inactive

Table 2. Operating modes (continued)

Operating mode	Entering conditions	Leaving condition	Characteristics
Limp Home	400 ns after Reset mode	– SPI sequence to enter Active mode: UNLOCK = 1 (EN,GOSTBY) = (1,0) – SPI sequence to enter Standby mode: UNLOCK = 1 (EN,GOSTBY) = (0,1)	– DIN access enabled: Buck1 is according to DIN; Buck2 is OFF – SPI active
Active mode	SPI sequence: – UNLOCK = 1 – EN = 1 and GOSTBY = 0	– V_{SPI} undervoltage – WD failure – SPI sequence to enter Standby mode: UNLOCK = 1 (EN,GOSTBY) = (0,1)	– Buck converters are active – SPI is active

3.2 Programmable functions

3.2.1 Activation of the buck output

In Active mode, the activation of the Buck converters is performed according to the configuration of control register CR#3<15:14> for Buck1 and CR#3<13:12> for Buck2, as showed in the following table. See *Table 15: CR#3: Control Register 3*.

Table 3. DIN pin Map for Buck1 and Buck2

CR#3<15> or CR#3<13>	CR#3<14> or CR#3<12>	Buck1 and Buck2 status
0	0	Buckx always OFF (default for Buck2)
0	1	Buckx attached to internal PWM generator
1	0	Buckx always ON
1	1	Buckx controlled by DIN Input (default for Buck1)

3.2.2 PWM dimming

The device allows modifying the brightness of the LEDs string simply managing the average current.

The PWM dimming could be achieved in two different ways:

- Through direct input, DIN
- With integrated PWM generator

Dimming with direct input

The signal applies to buck1, buck2 or both, depending on DIN mapping bit configuration (see bits <15:14> and bits <13:12> on *Table 15: CR#3: Control Register 3*). If the control

registers are configured accordingly, one (or both) buck converter(s) are activated and directly controlled by DIN pin.

The default configuration is set in order to allow direct driving only for buck1, whilst buck2 is turned off. In case of limp home function, the default conditions are applied.

PWM control through DIN has to take into account the DIN filter time (t_{DIN_FT}, 32 µs typical) on rising edge to properly set the desired duty cycle.

Dimming with integrated PWM generator

This function allows modifying the average current on the LEDs by means of a dedicated control register (see bits <23:14> and bits <13:4> on *Table 13: CR#1: Control Register 1*).

This function must be activated setting the right mapping bits configuration inside the control register 3, and in particular, CR#3<15:14> for Buck1 and CR#3<13:12> for Buck2.

To set duty cycle, a 10-bit number must be written in the corresponding register, resulting in a 1024 steps of resolution. The duty cycle is determined through the following equation:

$$DC_{\%} = \frac{N}{1024} \cdot 100$$

Where N is the 10-bit number.

The PWM frequency is depending on the PWM_CLK input signal with the following equation:

$$PWM\_LF = \frac{PWM\_CLK}{1024}$$

Where PWM_LF is the LEDs dimming frequency.

If PWM signal fails, an error bit is reported in the STATUS register where PWMCLK fail is located. An internal fallback oscillator is enabled in order to provide a fixed PWM frequency clock signal ($F_{FALLBACK\_CLK}$), whilst no changes is applied on the duty cycle.

Once the external PWM is available again and after a read & clear operation on Status Register 2, the internal clock is disabled and PWM operation continues with the external clock (see *Figure 12*).

3.3 Protections

3.3.1 Temperature warning

The device integrates a temperature warning with two thresholds TW_1 and TW_2 in each buck's mosfet. If the T_j of the buck mosfet1 or buck mosfet2 rises above TW_1 or TW_2, the status bit TWxy is set (x = 1 or x = 2, it stands for the buck1 or buck2, y = 1 or y = 2, it stands for the TW_1 or TW_2) . TW_{XY} bit is set on the status registers: SR#1<4:3> for Buck1 and SR#2<22:21> for Buck2. Thermal warning is also reported in the Global Status Byte register, and in particular, bit 25 (GW) is set.

If the T_j drops below the temperature warning reset threshold 1 (TW_1-TW_{1_HYS}), respectively TW_2 – TW_{2_HYS}, the corresponding status bit is automatically reset.

As long as the Tj does not exceed the over temperature shutdown, the device does not latches off the buck mosfets, even if a temperature warning is detected.

3.3.2 Overtemperature shutdown

If the junction temperature of one of the buck mosfets rises above the shutdown temperature T_{TSD}, an overtemperature event (OVT) is detected. The channel is switched off and the corresponding bit (OVT1 or OVT2) is set in the status register SR#1<5> for Buck1 and SR#2<23> for Buck2.

Overtemperature events are also reported in the Global Status Byte register and in particular bit 27 FE1 is set.

In normal mode the corresponding buck converter is latched off, until the following conditions are fulfilled:

1. T_{JX} drops below the thermal shutdown reset threshold T_{TSD}-T_{TSD_HYS}.
2. Subsequently the microcontroller sends a read and clear command, in order to reset OVT1 or OVT2 bit located in the Status register SR#1<5> or SR#2<23>.

In fail safe mode (Limp Home), the device applies an auto restart of the fault buck converter with a period equal to $t_{AUTORESTART}$, provided that the T_{JX} falls below TSD reset threshold (T_{TSD}-T_{TSD_HYS}).

3.3.3 VS under voltage lockout

If the VS supply falls below V_{S_UV} (VS under voltage threshold), the boost controller and the buck converters will be deactivated, regardless of the SPI control registers or DIN.

This feature is implemented, in order to avoid an operation of the external mosfet of the boost controller in linear mode, due to a too low gate driver supply.

3.3.4 Buck T_{ON} minimum operation

Buck minimum on time operation is detected when the corresponding failure counter counts N_Ton_min_fail switching cycles (also nonconsecutive), during which I_{Lx_PEAK} is reached between T_{BLANK_BUCK} and $T_{ON\_MIN\_BUCK}$. In normal mode (Active mode), once minimum T_{ON} operation is validated, flag $\overline{T_{ON\_MIN\_OPx}}$ is set and the corresponding Buckx converter is latched off, until the microcontroller sends a frame and clears the corresponding status bit (SR#1<2> and SR#1<1>).

In fail safe mode (Limp Home), once a minimum T_{ON} violation is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to $t_{AUTORESTART}$.

The failure counter is not incremented during the startup phase ($T_{STARTUP}$). The failure counter is reset if Nton_min_fail_reset consecutive pulses are detected with T_{ON} longer than $T_{ON\_MIN\_BUCK}$.

3.3.5 Buck output's short circuit to GND

A shorted buck output to GND is detected when LED string voltage (V_{LED}) is lower than a specified threshold (V_{LED_SHT}) and the corresponding failure counter counts Nton_min_fail switching cycles (also nonconsecutive), during which I_{Lx_PEAK} is reached between T_{BLANK_BUCK} and $T_{ON\_MIN\_BUCK}$. In normal mode (Active mode), once a short circuit is validated, flag SHTx is set and the corresponding Buckx converter is latched off, until the microcontroller sends a frame and clears the corresponding status bit (SR#1<7> and SR#1<6>).

In fail safe mode (Limp Home), once a short circuit is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to $t_{AUTORESTART}$.

The failure counter is not incremented during the startup phase. The failure counter is reset if Nton_min_fail_reset consecutive pulses are detected with T_{ON} longer than $T_{ON\_MIN\_BUCK}$.

3.3.6 Buck T_{ON} maximum operation

Buck maximum on time operation is detected when switching on time is equal to $t_{ON\_MAX\_BUCK}$ for two consecutive cycles.

Once maximum Ton operation is validated, flag TON_MAX_OPx is set and the corresponding Buckx converter is temporarily switched off for a Ttonmax_off.

Then, Buckx is enabled to switch on again while TON_MAX_OPx bit will be latched until a R&C command clears corresponding status bit (SR#2<20> or SR#2<19>).

In fail safe mode (Limp Home), once a maximum T_{ON} violation is validated, the corresponding buck converter is latched off until automatically cleared by an auto-restart procedure, with a period equal to $t_{AUTORESTART}$.

3.3.7 Buck Open Load detection

If one of the LED strings is disconnected, the converter will charge the output capacitor of the buck converter by regulating the peak current of the switch, until V_{LED} is equal to the buck input voltage. From this point, since the output capacitor is charged at the maximum possible value, it cannot absorb any current despite the activation of the switch, and the target I_{Lx_PEAK} cannot be reached.

Upon these conditions, Buckx starts switching at maximum Ton: maximum Ton operation detection (described in *Section 3.3.6*) guarantees Open Load failure protection as well.

4 SPI functional description

4.1 SPI protocol

ST-SPI is a standard used in ST automotive ASSP devices. SPI protocol standardization here described defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI will allow usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition to that, fail safe mechanisms are implemented to protect the communication from external influence and wrong or unwanted usage.

4.2 SPI communication

At the beginning of each communication the master can read the content of the <SPI Mode> register (ROM address 10h) of the slave device. This 8 bit register indicates the SPI frame length (32 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 3 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status Byte>. It provides general status information about the device. It is followed by 3 data bytes (i.e. “in-frame-response”).

For write cycles the <Global Status Byte> is followed by the previous content of the addressed register.

Table 4. Command byte (8 bit)

	Operating code		Address					
Bit	31	30	29	28	27	26	25	24
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

Table 5. Data byte 2

	Data byte 2							
Bit	23	22	21	20	19	18	17	16
Name	D23	D22	D21	D20	D19	D18	D17	D16

Table 6. Data byte 1

	Data byte 1							
Bit	15	14	13	12	11	10	9	8
Name	D15	D14	D13	D12	D11	D10	D9	D8

Table 7. Data byte 0

	Data byte 0							
Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Where:

OCx: Operation Code

Ax : Address

Dx: Data bit

Command Byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear>, <Read Device Information>) and a 6 bit address.

Table 8. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clears its content.

The <Read Device Information> allows access to the ROM area which contains device related information.

Global Status Byte

According to the ST SPI 4.1 standard, the first byte on the SDO pad during each command reports the global status of the chip:

Table 9. Global Status Byte

	Global Status Byte							
Bit	31	30	29	28	27	26	25	24
Name	GSBN	RSTB	SPIE	FE2	FE1	DE	GW	FS

Table 10. Global Status Byte description

Bit	Name	Description
31	GSBN	Global Status Bit Not This bit is a NOR combination of the remaining bits of this register: RSTB nor SPIE nor FE2 nor FE1 nor DE nor GW nor FS
30	RSTB	Reset Bit The RSTB indicates a device reset. In case this bit is set, all internal *Control Registers* are set to default and kept in that state until the bit is automatically cleared by any valid SPI communication.
29	SPIE	SPI Error The SPIE is a logical OR combination of errors related to a wrong SPI communication (SDI stuck, wrong number of clock, parity check error)
28	FE2	Functional Error 2 (logic OR combination of errors which does not cause parts of the device to be disabled) TOFF1_MAX or TOFF2_MAX or TOFF1_MIN or TOFF2_MIN or TON_MAX_OP1 or TON_MAX_OP2
27	FE1	Functional Error 1 (logic OR combination of critical errors which cause parts of the device to be disabled) VS_UV or OL1 or OL2 or OVT1 or OVT2 or SHT1 or SHT2 ot TON_MIN_OP1 or TON_MIN_OP2.
26	DE	Device error PWMCLK_FAIL.
25	GW	Global warning TW11 or TW12 or TW21 or TW22
24	FS	Fail safe If this bit is set, the device is in limp home mode

4.3 Address mapping

Table 11. RAM memory map

Address	Name	Access	Content
01h	Control Register 1	R/W	CR#1: 1st Control Register
02h	Control Register 2	R/W	CR#2: 2nd Control Register
03h	Control Register 3	R/W	CR#3: 3rd Control Register
04h	Control Register 4	R/W	CR#4: 4th Control Register
05h	Status Register 1	R/C	SR#1: 1st Status Register
06h	Status Register 2	R/C	SR#2: 2nd Status Register
07h	Status Register 3	R/C	SR#3: 3rd Status Register

Table 11. RAM memory map (continued)

Address	Name	Access	Content
3Eh	Customer Trimming Register	R/W (W only when EOT bit = 0)	CT: Customer Trimming Register
3Fh	Advanced Operation Code	Clear	A R&C operation to this address causes all status registers to be cleared

Table 12. ROM memory map

Address	Name	Access	Content	Comments
00h	Company Code	R	00h	STMicroelectronics
01h	Device family	R	02h	LED product family
02h	Device number 1	R	55h	‘U’ in ASCII
03h	Device number 2	R	41h	‘A’ in ASCII
04h	Device number 3	R	52h	‘R’ in ASCII
05h	Device number 4	R	07h	‘7’ in hex
0Ah	Silicon version	R	04h	Fifth version
10h	SPI Mode	R	31h	Bit7 = 0, burst read is disabled SPI data length = 32 bits Bit6, DL2 = 0 Bit5, DL1 = 1 Bit4, DL0 = 1 Bit3, SPI8 = 0: 8 bit frame option not available Bit2 =0 Parity check is used Bit1, S1=0 Bit0, S0=1
11h	WD Type 1	R	4Ah	A WD is implemented Bit7, WD1 =0 Bit6, WD0 =1 WD period 50 ms = 10 * 5 ms -> WT[5:0] = 0xA Bit5, WT5 = 0 Bit4, WT4 = 0 Bit3, WT3 = 1 Bit2, WT2 = 0 Bit1, WT1 = 1 Bit0, WT0 = 0
13h	WD bit pos. 1	R	44h	Bit7, WB1 = 0 Bit6, WB2 = 1 WBA[5-0], Bit[5-0] = address of the configuration register, where the WD bit is located = 04d = 000100b