Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

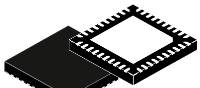
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

L99LD21

High power LED driver for automotive applications

Datasheet - production data



QFN-40L 6x6

Features

- AEC-Q100 qualified
- General
  - ST SPI communication v4.1
  - 5.5 to 24 V Operating battery voltage range
  - Load dump protected
  - QFN40L 6x6 (wettable flanks) with exposed pad
  - Timeout watchdog and limp home function
  - Low standby current
- Boost Section
  - Fixed frequency architecture, programmable by SPI
  - Peak current mode control
  - Dual phase operation supported
  - Input current limitation
  - Soft start
  - Overvoltage protection (OVP)
  - Short feedback failure protection
  - Constant voltage control
- Buck section
  - Integrated switching mosfets
  - Lossless current sensing without need of external components
  - Very accurate LED current setting programming inductor's peak current and peak-to-peak current ripple
  - Adjustable peak current by SPI
  - Adjustable current ripple by SPI
  - Integrated PWM generation unit with 10-bit resolution and phase shift
  - Peak current control
  - Constant VLED x TOFF architecture
- Protection and diagnostic
  - Battery under voltage
  - Temperature warning (2 thresholds)
  - Overtemperature shutdown
  - LED voltage digital feedback through SPI
  - Buck outputs short circuit and open load protection

Applications

- Low Beam
- High beam
- Daytime running light
- Turn indicator
- Position light
- Side marker
- Fog light

Description

The L99LD21 is a flexible LED driver, which is specifically designed for the control of two independent high brightness LED strings for automotive front lighting applications. It consists of a high efficiency monolithic boost controller and a dual buck converter.

The boost controller integrates a high current gate driver for an external n-channel mosfet. It delivers a constant output voltage, up to 60 V, which supplies the inputs of the two integrated or external buck converters.

The boost controller of two devices can be stacked, in order to operate in dual phase for high power applications, with an interleaving pattern for an improved input current ripple.

The buck converters integrate n-channel mosfet which is driven by a bootstrap circuit.

This is information on a product in full production. www.st.com

Contents

List of tables

List of figures

1 Introduction

The L99LD21 is a monolithic driver IC, which controls the current of two independent high power LED strings, whose forward current and voltage can reach up to 1.5 A (average) and up to 50V respectively.

This device has been designed with dedicated functions, in order to fulfill the stringent requirements of automotive front lighting applications.

The device offers a high level of flexibility, without any change of the external components, thanks to its programmability through the ST SPI interface. This feature support generic platform approaches, which require a software configurability of several parameters. This robust interface, offers a detailed diagnostic of the device itself, as well as of the controlled LED strings.

As the device potentially controls safety critical functions such as low beams and turn indicators, built-in features are integrated in order to support a high level of functional safety. The L99LD21 features a timeout watchdog, a monitoring of the watchdog counter, a limp home function and a direct input. The ST SPI protocol takes into account FMEA case.

The device consists of a boost controller, which controls the PWM of an external n-channel mosfet and provides a stabilized voltage (V_{BOOST}). The input of the boost stage must be connected to the battery voltage through a reverse polarity protection.

The boost controllers of two L99LD21 can be combined to form a dual-phase, interleaved boost controller. Special care has been taken for the current balancing between the different phases and for the switching activity of the boost mosfets with 180° phase shift.

The output of the boost controller supplies the input of the two independent integrated buck converters, or any other external buck converters, whose input voltage is compatible with V_{BOOST}. The integrated buck converters are based on constant off-time architecture (for a given LED output voltage) and control the peak current and the peak-to-peak current ripple of their respective inductors.

Operating in continuous conduction mode, the average of each LED string’s current, which is connected to the output of each buck converter, is tightly controlled.

This architecture, which consists of cascaded boost and buck stages (see *Figure 2*), allows the control of a wide range of LED strings, whose forward voltage is independent from the battery voltage.

With the aim of ensuring a wide operating inductor current range, the Buck mosfets can be set in low or high R_{DS_ON} modes, so that two different inductor peak current (I_{Lx_PEAK}) ranges [0.179 A ÷ 0.849 A] or [0.362 A ÷ 1.695 A] can be selected.

The average LED current is controlled by setting the inductor's peak current and peak-to-peak current ripple. Sensing of the peak current is integrated, not requiring any external shunt resistance, which saves cost and reduces the power dissipation.

Buck n-channel mosfet R_{DS_ON} value depends on the operative conditions as junction temperature, Input voltage and LED string current. For example, at V_{Buckin} = 45 V, I_{led} = 700 mA, T_j = 25 °C the maximum R_{DS_ON} is 400 mΩ (low R_{DS_ON} mode).

1.1 Typical application

Figure 1. Functional block diagram

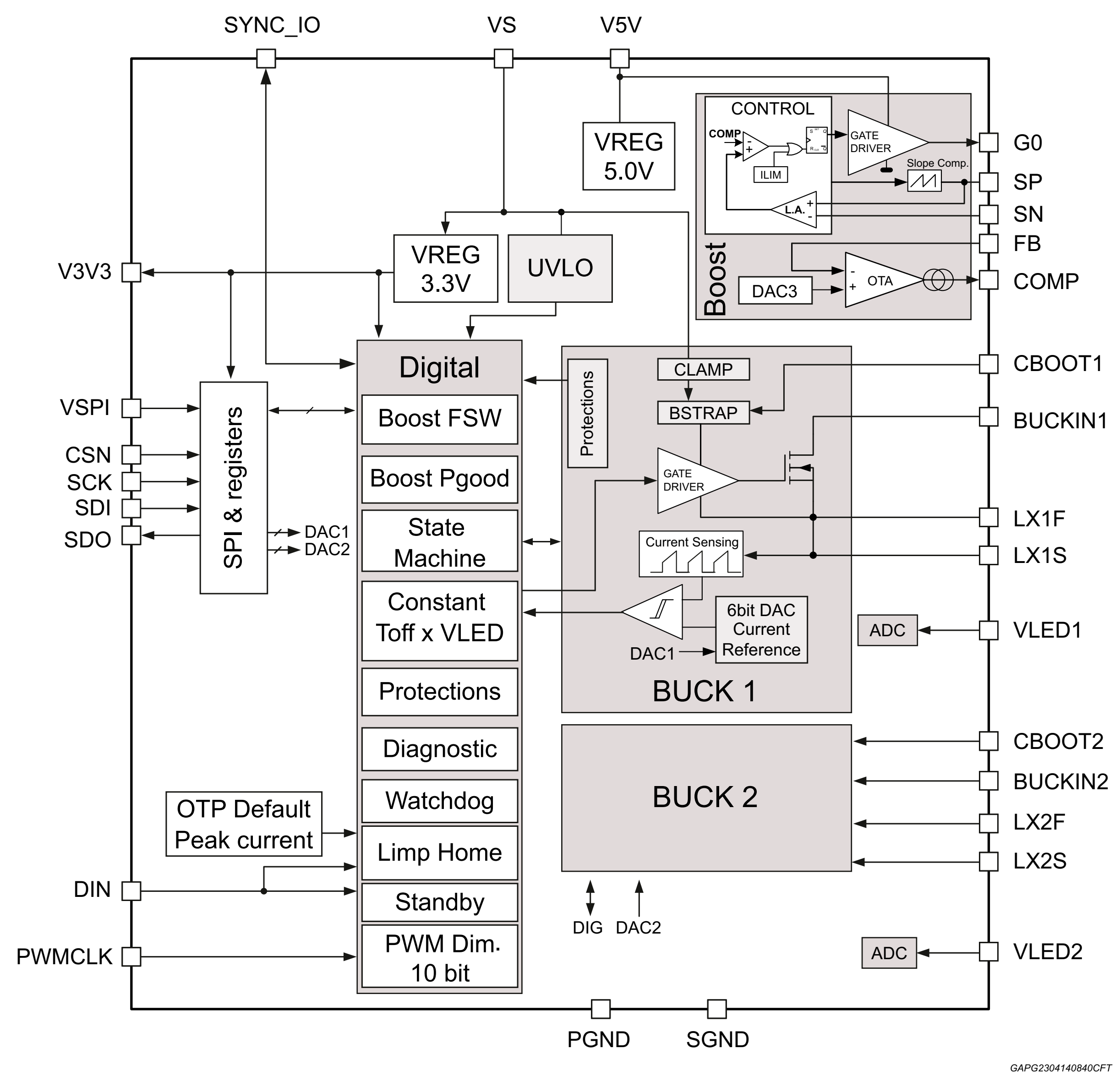


Figure 2. Typical application schematic

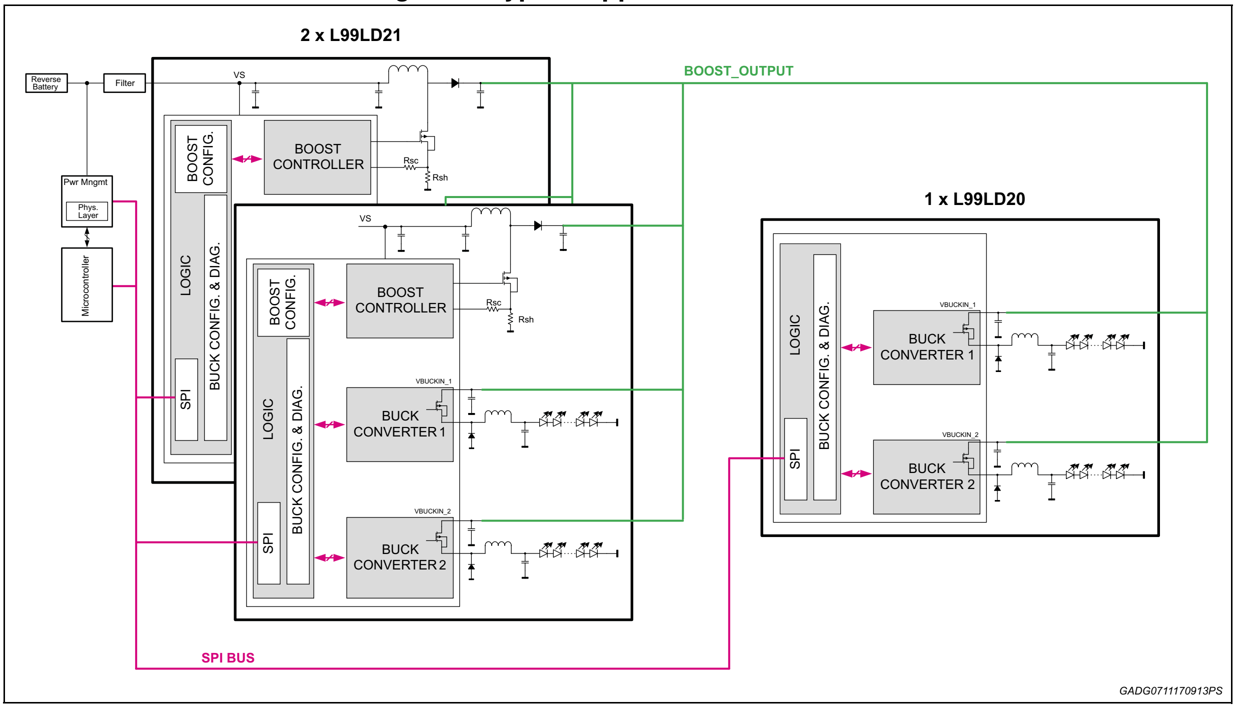


Figure 3. Application diagram

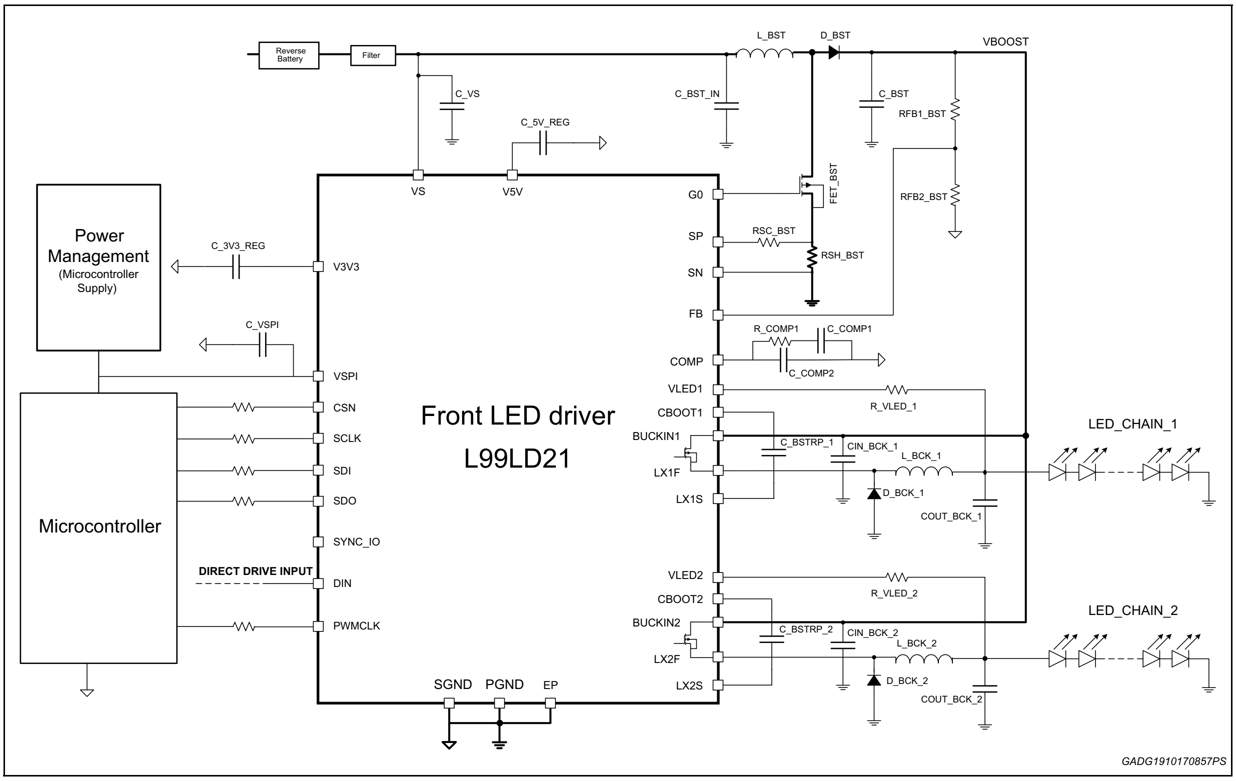


Figure 4. Connection diagram

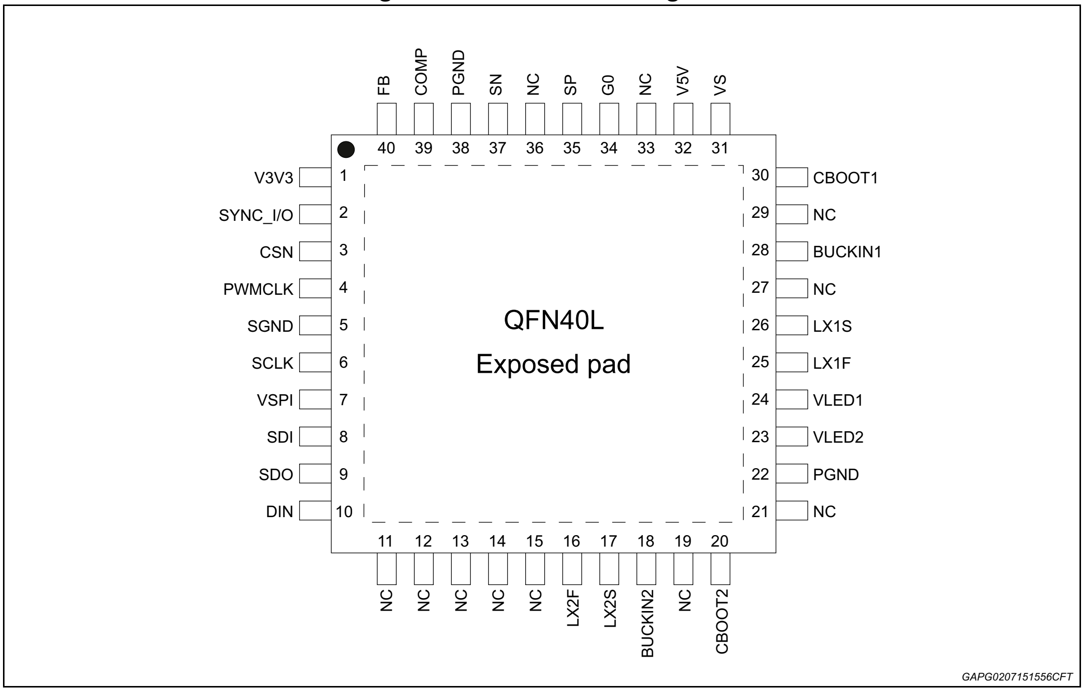


Table 1. Pin functionality

Pin #	Name	Function
1	V3V3	Output of the 3.3 V regulated internal supply. Connect a low ESR capacitor (4.7 µF) close to this pin.
2	SYNC_I/O	Boost synchronization Input or Output. This pin generates the clock signal for synchronizing another L99LD21 Boost in dual phase configuration.
3	CSN	Chip Select Not (active low) for SPI communication. It is the selection pin of the device. It is a CMOS compatible input.
4	PWMCLK	Clock input for the internal PWM dimming generator.
5	SGND	Signal Ground connection.
6	SCK	Serial Clock for SPI communication. It is a CMOS compatible input.
7	VSPI	Connection to external 3.3 V or 5 V supplies voltage. The external supply powers SPI interface and the I/O signal pins to the microcontroller. It is suggested to connect 100nF capacitor close to this pin.
8	SDI	Serial Data Input for SPI communication. Data is transferred serially into the device on SCK rising edge.
9	SDO	Serial Data Output for SPI communication. Data is transferred serially out of the device on SCK falling edge.
10	DIN	Direct input pin.
16	LX2F	Connection to the switching source node of the buck2. This pin must be connected to external free-wheeling diode.

Table 1. Pin functionality (continued)

Pin #	Name	Function
17	LX2S	Kelvin connection to the switching source node of the buck2. This pin has to be connected to external bootstrap capacitance.
18	BUCKIN2	Connection to the input of the buck channel 2
20	CBOOT2	Connection to the bootstrap capacitor (100nF) of the buck channel 2.
22, 38	PGND	Power Ground connection.
23	VLED2	Connection to the anode of the LED string for read back of the forward voltage of the channel 2.
24	VLED1	Connection to the anode of the LED string for read back of the forward voltage of the channel 1.
25	LX1F	Connection to the switching source node of the buck1. This pin must be connected to external free-wheeling diode.
26	LX1S	Kelvin connection to the switching source node of the buck1. This pin has to be connected to external bootstrap capacitance.
28	BUCKIN1	Connection to the input of the buck channel 1.
30	CBOOT1	Connection to the bootstrap capacitor (100 nF) of the buck channel 1.
31	VS	Input supply pin of the IC. Connect VS to the battery voltage.
32	V5V	Output of the 5V regulated internal supply. Connect a low ESR capacitor (4.7 µF) close to this pin.
34	G0	Output of the boost gate driver for the external switching mosfet.
35	SP	Positive connection to the boost shunt resistor, in series to the boost switching mosfet.
37	SN	Negative connection (Ground) to the boost shunt resistor, in series to the boost switching mosfet.
39	COMP	Output of the error amplifier of the boost controller. Connect the compensation network between this pin and SGND.
40	FB	Boost output voltage feedback. Connect the FB pin to the boost output voltage, via a resistor divider.
11, 12, 13, 14, 15, 19, 21, 27, 29, 33, 36	NC	Not connected

2 Boost controller

2.1 General description

The L99LD21 integrates one boost controller, which is based on a fixed frequency, peak current mode architecture. It drives the gate of an external n-channel mosfet in order to step up the VS input voltage to a higher stabilized output voltage.

2.2 Frequency selection

The boost controller operates at a fixed frequency which can range from 100 kHz to 450 kHz. The switching frequency is set by a SPI control register (CR#3<9:7>, see *Section 5.4: Registers description*).

2.3 Output voltage setting

The control loop regulates the voltage at the FB pin to a reference voltage, which value, according table 2, is configurable by the control register CR#3<11:10> (see *Section 5.4: Registers description*). Connect the resistor divider tap, top and bottom respectively to the FB pin, to output of the boost controller and to the bottom to SGND.

The resulting boost output voltage is given by:

$$V_{BOOST} = V_{FB\_REF}[b_1, b_0] \cdot \left[1 + \frac{R_1}{R_2}\right]$$

Table 2. Reference voltage configuration

b1	b0	V_{FB_REF} [V]
0	0	0.596
0	1	0.895
1	0	1.242
1	1	1.496

2.4 Overvoltage protection

The peak current mode requires a minimum on-time, because of the noise generated right after the turn-on of the switching mosfet. At light load (very low output current), this minimum on-time, in combination with the selected switching frequency is no longer able to regulate the output voltage to the requested voltage. The device enters in overvoltage protection (OVP), in order to prevent an excessive rise of the boost output voltage above the target voltage.

This mode is activated when the voltage on FB pin is higher than the selected internal reference voltage of a specified threshold value ($V_{FB\_OV\_ON}$).

The switching activity is resumed as soon as the voltage on FB pin decreases to the selected internal reference voltage (V_{FB_REF}[xx]).

In case of FB voltage increases above $V_{FB\_OV\_ON}$, an output digital flag, called BST_OVP, is set.

As soon as feedback voltage decreases down to target value (V_{FB_REF}[xx]), the bit is reset after $t_{BST\_OVP\_RST}$ delay time. This delay time is implemented in order to eliminate the diagnostic ambiguity (toggling of the OVP flag) during permanent no load / light load operation.

BST_OVP bit is not set in case of boost disabled or boost feedback failure.

2.5 Feedback failure protection

L99LD21 is protected in case of boost controller feedback pin failure. More in detail, a specific bit, called BST_FB_FAIL, is set in case of feedback pin is shorted to ground.

When this bit is set:

- If device is OFF, boost controller does not start;
- If device is ON in single phase configuration, boost controller is immediately switched OFF;
- If device is ON in dual phase configuration and it is in Active mode: both boost controllers are switched off when the failure is recognized on Master side; only Slave controller is switched off when the failure is recognized on Slave side while the Master is managed by the microcontroller;
- If device is ON in dual phase configuration and it is in Limp Home: both boost controllers are switched off when the failure is recognized on Master side; only Slave controller is switched off when the failure is recognized on Slave side, while the Master is forced to work at minimum duty cycle.

The reset of FB failure bit is demanded to the microcontroller (in Active mode) or to an auto-restart function (in Limp Home) that cyclically clears this bit with a period equal to $t_{AUTORESTART}$.

This bit is not set if L99LD21 internal boost controller is not used (in this case, BST_DIS bit is set).

If left floating, feedback pin will be pulled up internally. In this case, BST_OVP bit will be set permanently and boost gate driver will be permanently off. Since the feedback pin voltage is in any case high, N_PWR_GOOD flag is reset in such condition and shall be ignored.

Note: Setting this bit doesn't imply any action on buck converters.

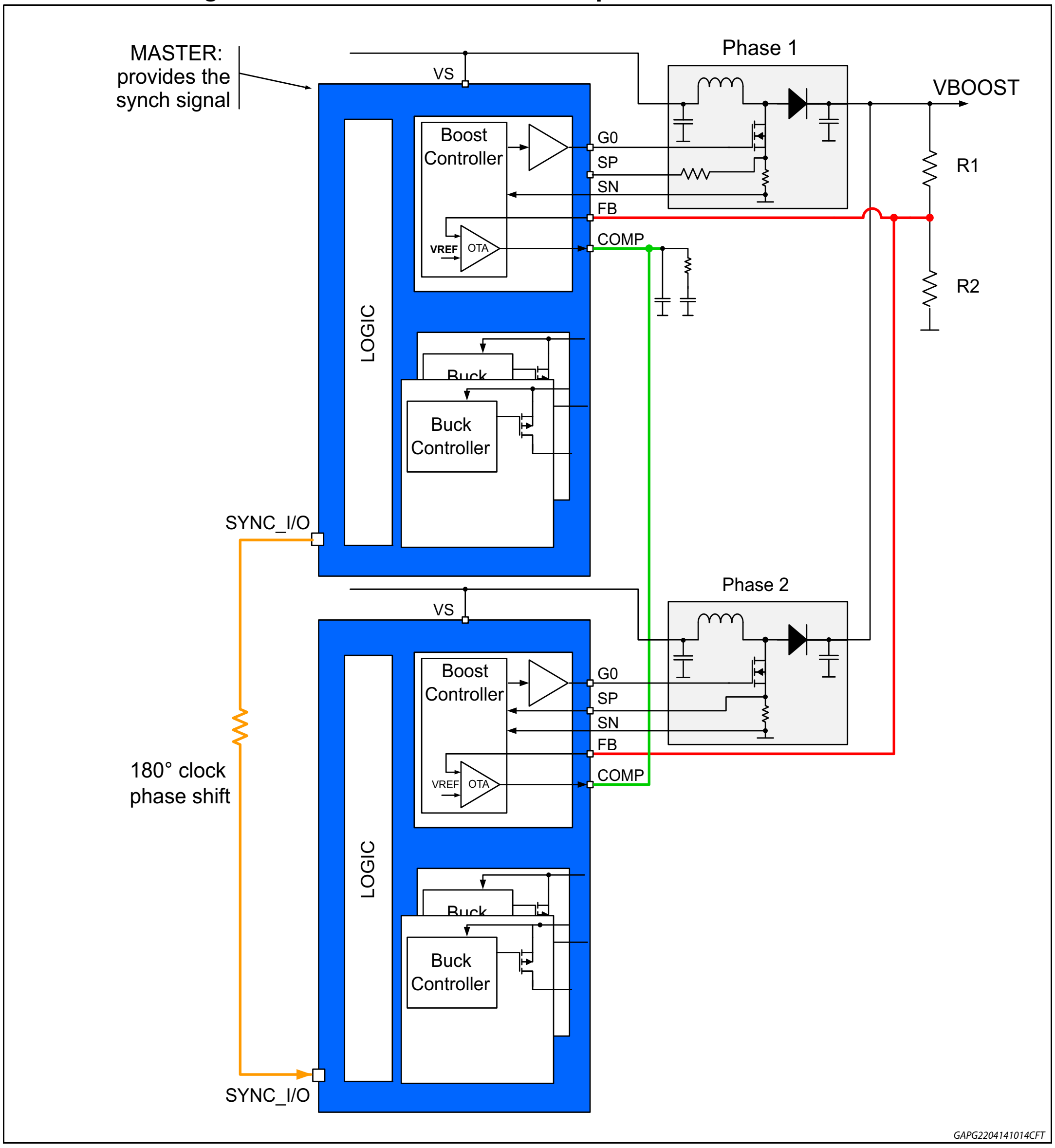
2.6 Operation in dual phase interleaved mode

It is possible to combine the boost controllers of two L99LD21, for high power applications, in dual phase configuration. In this configuration, the switching mosfets of the boost controllers are driven at 180° out of phase. By sharing the current between two phases, the conduction losses (which are proportional the square of the conducted current) are reduced and the efficiency of the boost stage increases, in comparison to a single-phase.

The effective switching frequency is doubled and the ripple cancellation effect results in a reduction of the input and output current ripple. This allows small input and output capacitances.

For an operation in dual-phase configuration, FB, COMP and SYNC_I/O pins must be respectively connected together as shown in *Figure 5*.

Figure 5. Pin connections in dual-phase boost controller



One of the L99LD21 must be configured as the master and the other device must be configured as the slave (see bit <1> on *Table 15: CR#2: Control Register 2*). The SYNC_I/O of the master acts as an output, whilst the slave one respectively as an input. The master boost provides a clock signal to the slave, in order to achieve an interleaved switching activity of the slave boost controller, which is 180° out of phase to that of the master.

For a proper current balancing between the boost phases, the shunt resistors, which are placed in series to the source of the mosfets, and the inductors, must be identical.

2.7 Soft start

The L99LD21 features an internal soft start function, which gradually increases the boost mosfet current limit in 8 steps, in order to avoid a voltage overshoot of the boost output. The threshold of the current limitation reaches its nominal value after a specified soft start time (t_{SS}).

A soft-start phase is initiated at the activation of the boost controller:

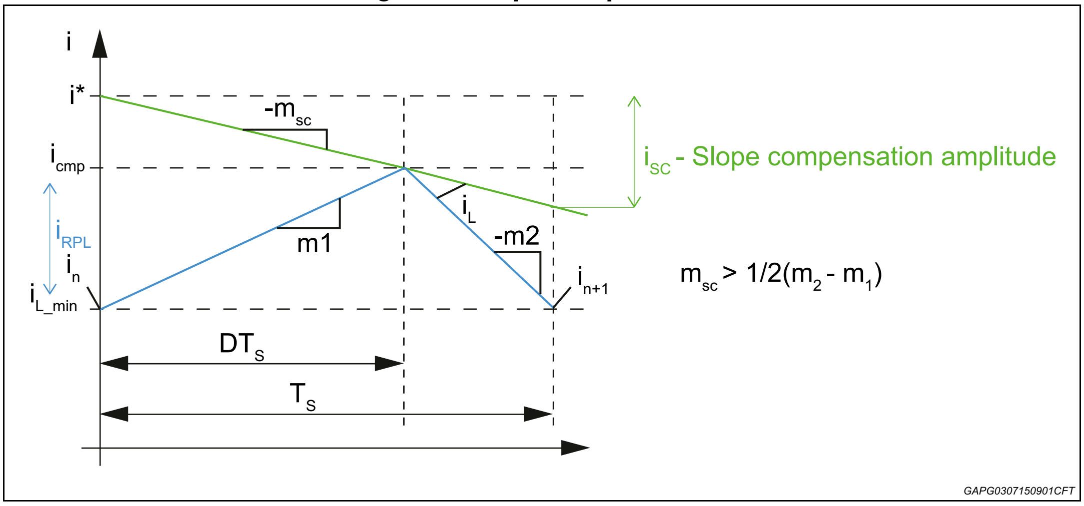
- after leaving standby mode;
- after deactivation of the boost controller due to a VS under voltage;
- after a previous de-activation of the boost by SPI (see bit <1> on *Table 16: CR#3: Control Register 3*);
- after deactivation of the boost controller due to a BST_FB_FAIL.

2.8 Slope compensation

Slope compensation is needed to ensure loop stability with all possible values of duty cycle: $D = T_{ON} / T$ ($0 < D < 1$) especially when duty cycle is greater than 0.5. The slope of the additional ramp is proportional to converter inductor current slope during the turn off phase.

The L99LD21 generates an internal peak current value, I_{SLOPE}, which is added to the sensing signal at the output of the OTA. The percentage of slope compensation is achieved by choosing a proper value of the R_{SC} resistor (see *Figure 2* for R_{SC} resistor proper connection).

Figure 6. Slope compensation



2.9 Operation together with the buck converters

Right after a power on reset (POR) of the device or after a fault event leading to a latch-off of the boost controller (VS under voltage), a soft start phase is initiated and the boost is activated.

The buck converters activation depends on device status (see *Section 4.1: Operating modes*):

- Active mode: in this case, bucks are immediately operative. Their status will depend on DINMAP register configuration (see *Section 4.2.1*);
- Limp Home:
  - we have to distinguish two different cases:

    Boost Enabled with output voltage higher than 92.5% of final target value. In this case, buck converters are immediately operative according to DIN_MAP register configuration;

    Boost Disabled or Enabled with output voltage lower than 92.5 % of final target value. In this case, the buck converters are kept disabled for a specified time delay (t_{DELAY}) independently from DINMAP status. Once this time elapses, bucks are operative according to DINMAP register configuration.

On the other hand, when boost and bucks are active and a VS undervoltage fault event occurs, buck converters are immediately disabled while the boost is kept alive for t_{DELAY} before being switched off.

3 Buck converters

3.1 General description

The L99LD21 features two independent buck converters with integrated switching mosfets with forward peak current as high as specified maximum I_{Lx_PEAK} (where x indicates Buckx peak current) 1.695 A. They are optimized to deliver a constant current to LED strings.

The R_{DS_ON} of the n-channel mosfets can be set programming the appropriate bit in the control register (see bits <3:2> on *Table 14: CR#1: Control Register 1*): high R_{DS_ON} mode (only one half power stage enabled) or low R_{DS_ON} mode (both half power stages enabled).

This feature allows having two different inductor peak current ranges, 0.179 A ÷ 0.849 A or 0.362 A ÷ 1.695 A, respectively for high R_{DS_ON} and low R_{DS_ON} mode, so achieving the highest of current sense accuracy in the whole current range.

The buck converters are based on constant off-time architecture, which regulates the peak current in each inductor. The monitoring of the inductor peak current is done through integrated senseFETs. This results in a lossless high side current sensing, which does not require any external shunt resistor, and improves the system efficiency.

This architecture provides an inherent cycle-by cycle current limitation and a fast transient response, without any compensation of the control loop.

The average LED current in each LED string is configurable by the SPI, through configuration of the inductor peak current and peak-to-peak current.

The dimming of the LED strings can be realized through the direct input pin (DIN) or through the internal 10-bit PWM dimming generator.

3.2 Bootstrap circuit

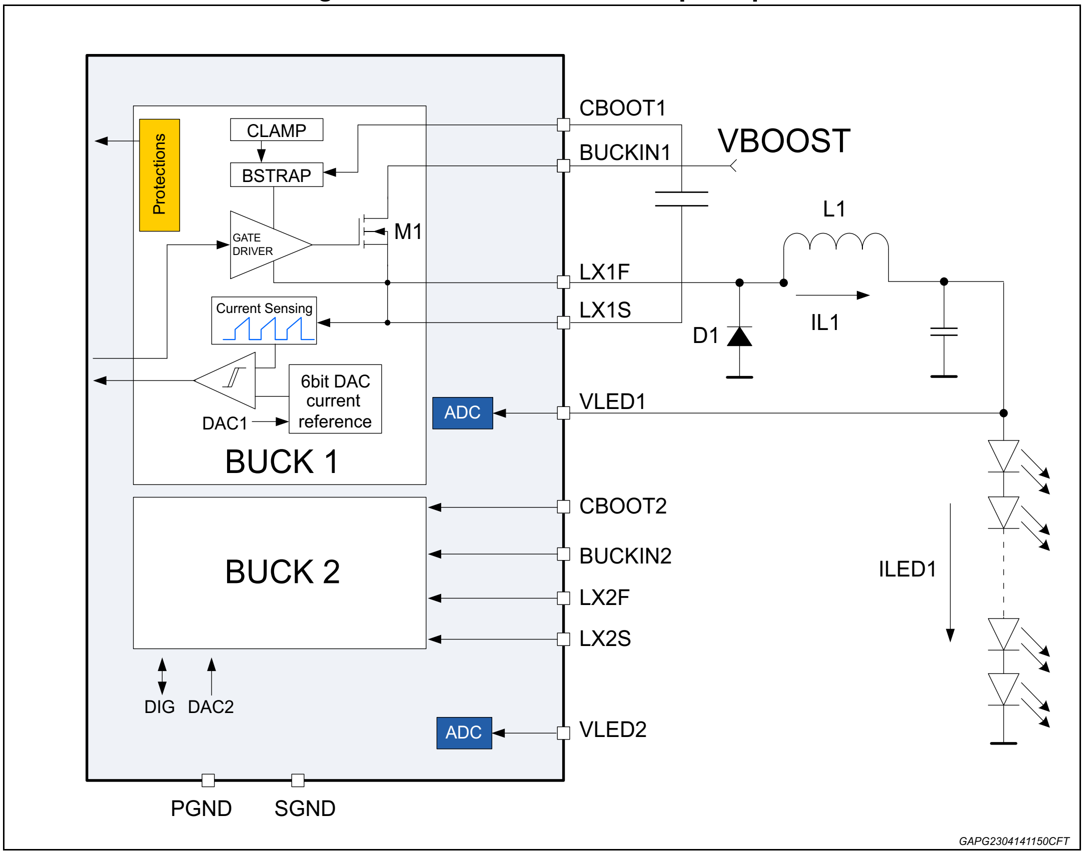
The L99LD21 has built-in high side n-channel switching mosfets, which are driven by gate drivers. Each gate driver uses a bootstrap circuit, consisting of an integrated diode and an external capacitor between the LX1S and CBOOT1 pins, respectively between the LX2S and CBOOT2 pins.

The buck converters impose a minimum off-time (T_{OFF_MIN}) to ensure that the bootstrap capacitor recharges every cycle to a voltage which avoids the switching mosfet to operate in linear mode. T_{OFF_MIN} restricts the maximum duty cycle of the buck converters for a given switching frequency. This effect is more pronounced at high switching frequencies and limits the maximum ratio between the buck input voltage (V_{BOOST}) and the LED strings' forward voltage. One way to overcome this limitation is reducing switching frequency, by selecting high constant VLED xTOFF and/or increase the inductance value.

3.3 Peak and average current setting

In buck converters, the inductor is directly connected to the load during the complete switching cycle (see *Figure 7: Peak current control principle*). The average inductor current is equal to the average LED string current. Operating in continuous conduction mode (i.e. the inductor current never decays to zero during the off-phase), if the inductor current is tightly controlled, the LED current will be regulated as well.

Figure 7. Peak current control principle



At the beginning of a switching period the MOSFET M1 is turned on, and the inductor current I_{L1} increases. The mosfet is activated for a minimum on-time T_{ON_MIN} in order to avoid that the on-phase is ended up by spurious noise, which is caused by the switch-on.

During mosfet activation, the inductor current, I_{L1}, increases until reaching a maximum value, I_{L1_PEAK}, which is set through a dedicated control register (see bits <23:18> and bits <17:12> on *Table 15: CR#2: Control Register 2*). When I_{L1} reaches its peak value, the switching mosfet is turned off. The mosfet remains off for a time T_{OFF}, which is derived from the configured constant VLED1xTOFF1 (see bits <11:8> and bits <7:4> on *Table 15: CR#2: Control Register 2*), where V_{LED1} is the forward voltage of the LED string, which is connected at the output of the buck converter 1.

During T_{OFF}, the inductor current decreases by:

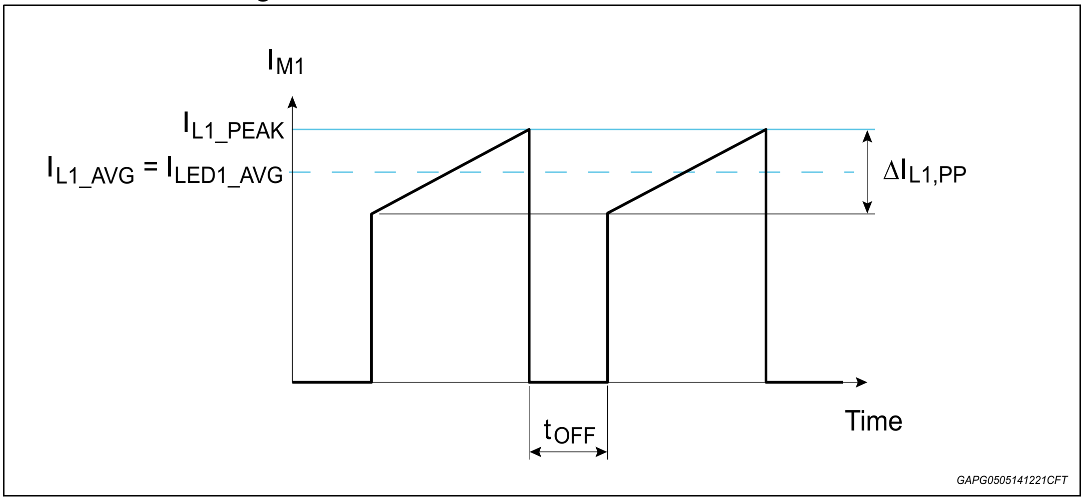
$$\Delta I_{L1\_PP} = \frac{(V_{LED1} - V_{F\_D1})}{L_1} \cdot T_{OFF1} \sim \frac{V_{LED1} \cdot T_{OFF1}}{L_1}$$

where ΔI_{L1_PP} is the inductor peak to peak current and V_{F_D1} is the forward voltage of the diode D1. As D1 is a Schottky diode with a low forward voltage, V_{F_D1} can be in general neglected, compared to V_{LED1}.

Note: Once the VLEDxTOFF constant for a given buck converter is selected by SPI, the peak-to-peak inductor current ripple is constant. In particular, it depends neither on the boost voltage nor on the LED forward voltage.

The ripple current through the LED strings is reduced by means of an external capacitor in parallel with the LEDs.

Figure 8. Inductor and mosfet current waveforms



Referring to the *Figure 7* and *Figure 8* the average LED current - valid for both Buck 1 and Buck 2 - is therefore:

$$I_{LED1\_AVG} = I_{L1\_AVG} = I_{L1\_PEAK^*} - \frac{(\Delta I_{L1\_PP})}{2} = I_{L1\_PEAK^*} - \frac{(V_{LED} \cdot T_{OFF1})}{2L}$$

where $I_{L1\_PEAK^*}$ results from I_{L1_PEAK} (see *Table 40*) corrected with loop delay (t_{loop_delay})

In order to achieve the best accuracy versus input voltage variation during current sensing process, a defined buck input voltage window must be selected, by means of a dedicated control register (see bits <5:4> and bits <3:2> on *Table 16: CR#3: Control Register 3*).

3.4 Buck converter's blank time

The buck converters have a minimum on-time T_{BLANK_BUCK}. Although the inductor's target peak current I_{Lx_PEAK} is reached before this time has elapsed, the switch is kept on. This delay is used as a leading-edge blank time, in order to avoid a premature end of the switching cycle, which might be caused by the noise, which results from the commutation of the buck's mosfet.

3.5 Buck converter's start-up

While the device and the system are protected against short circuit conditions of the buck's output to GND, the device inhibits the detection of the short circuit during the startup phase $T_{STARTUP}$.

A startup phase is applied in the following conditions:

- If one of the buck converters is activated for the first time after a power on reset (POR), including buck activation after device wake-up;
- If one of the buck converters has been deactivated for more than t_{DELAY};
- If one of the buck converters has been latched off prior to a Read and Clear command;
- If one of the buck converters is re-activated after a VS under voltage event.

After these events, it is possible that the output capacitors of the buck converters are completely discharged. The charging of the buck output capacitors might lead switching cycles with short on-time (shorter than T_{ON_MIN}), which could potentially lead to a wrong detection of a shorted buck output. The introduction of this start-up phase avoids this wrong diagnostic.

3.6 Switching frequency

For a given buck converter, the switching frequency depends on the buck input voltage (output of the boost controller) and the forward voltage of the LED string, which is connected to its output.

In continuous conduction mode, T_{OFF} is given by:

$$T_{OFF} = (1 - D) \cdot T = \frac{1 - D}{F_{SW}}$$

Where D is the buck converter's duty cycle, T and F_{SW} are respectively the switching period and frequency.

Neglecting the drop voltage across the mosfet, the inductor's DC resistance and the diode's forward voltage, compared to V_{BUCKIN} and V_{LED}, we have:

$$D = \frac{V_{LED}}{V_{BUCKIN}}$$

$$F_{SW} = \frac{1 - \frac{V_{LED}}{V_{BUCKIN}}}{T_{OFF}} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{V_{LED} \cdot T_{OFF}}$$

For a given application (given inductance and V_{LED}), it is possible to set I_{LEDx_AVG} by selecting different combinations of I_{Lx_PEAK} and $V_{LED}xT_{OFF}$ in order to avoid critical frequency ranges such as the AM radio band.

To avoid buck operation at not allowed T_{ON} and/or T_{OFF} times, frequency range has to be kept inside F_{SWmin} and F_{SWmax}, where:

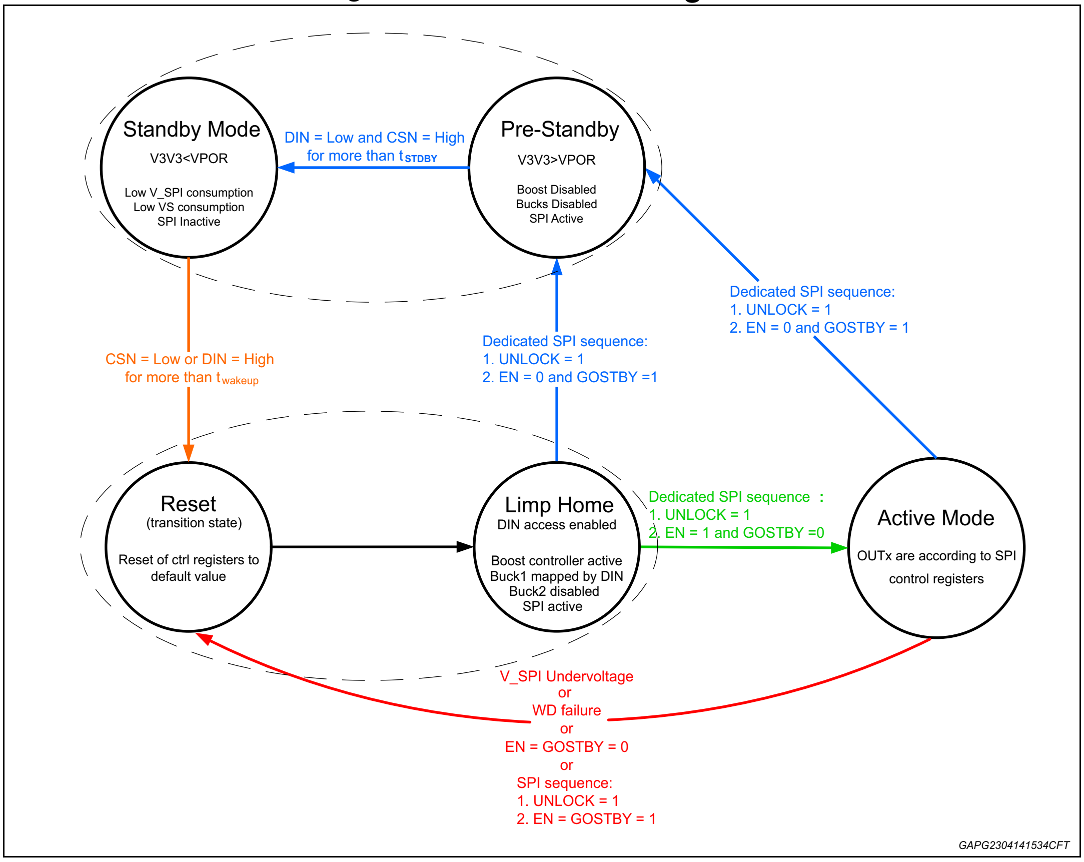
$F_{SWmin} = 1/(T_{ON\_MAX\_BUCK} + T_{OFF\_MAX\_BUCK})$

$F_{SWmax} = 1/(T_{ON\_MIN\_BUCK} + T_{OFF\_MIN\_BUCK})$

4 Functional description

4.1 Operating modes

Figure 9. **Device state diagram**



4.1.1 Standby mode

The pre-requisite for this mode is:

- Device in Pre-Standby mode.

The device enters Standby mode under the following conditions:

- By default, once the device is powered (VS present);
- CSN High and DIN Low for more than t_{STDBY}

The Standby mode characteristics are:

- V3V3 < VPOR
- V_{SPI} and V_S low consumption
- SPI inactive

The device leaves this mode if:

- DIN High or CSN Low for a time t > t_{WAKEUP}

Note: V_S must be stable above minimum value specified (5.5 V) before rising edge on DIN or falling edge on CSN.

4.1.2 Pre-standby mode

The device enters Pre-standby mode under the following conditions:

- upon the two following consecutive SPI frames setting:
  - UNLOCK = 1
  - (EN, GOSTBY) = (0, 1)

The Pre-standby mode characteristics are:

- V3V3 > VPOR
- Boost disabled
- Bucks disabled
- SPI active

The device leaves automatically Pre-standby mode entering standby:

- if CSN High and DIN Low for a time t > t_{STDBY}

4.1.3 Reset mode

The device enters Reset mode under the following conditions:

- By default, once the device leaves Standby mode;
- If device state is Active mode, when one of the following events occur:
  - V_{SPI} under voltage;
  - Watchdog failure
  - One SPI frame setting (EN,GOSTBY) = (0,0)
  - Two consecutive SPI frames setting
    UNLOCK = 1
    (EN,GOSTBY) = (1,1)

The Reset mode characteristics are:

- V3V3 > VPOR
- All the control and status registers set to their default values
- SPI inactive

The device leaves automatically Reset mode and enters Limp home after 400 ns (typical).

4.1.4 Limp home

The device enters Limp Home automatically 400 ns after Reset mode.

Limp home characteristics are:

- Direct Input access enabled
- Boost active
- Buck1 according DIN
- Buck2 OFF
- SPI active:
  - All SPI write operations must be allowed without any effects on the device behavior.

When the device leaves this mode, it can enter Standby or Active mode.

If the microcontroller sends to the device the following SPI frames sequence:

- The first SPI frame sets UNLOCK bit = 1
  (see bit <1> on *Table 14: CR#1: Control Register 1*)
- The second consecutive SPI frame sets GOSTBY bit = 1 and EN bit = 0
  (see bit <3> and bit <2> on *Table 15: CR#2: Control Register 2*)

The device enters Standby mode.

If the microcontroller sends to the device the sequence of the following SPI frames:

- The first SPI frame sets UNLOCK bit = 1;
  (see bit <1> on *Table 14: CR#1: Control Register 1*)
- The second consecutive SPI frame sets GOSTBY bit = 0 and EN bit = 1.
  (see bit <3> and bit <2> on *Table 15: CR#2: Control Register 2*)

The device enters Active mode.

In Limp Home, after setting bit 27 on GSB (FE1, functional error bit), an auto restart procedure is implemented: every $t_{AUTORESTART}$, functional error bit eventually set is automatically cleared.

4.1.5 Active mode

The device enters the Active mode if the microcontroller sends the following SPI frames sequence:

- In a first SPI frame set the UNLOCK bit to 1
  (see bit <1> on *Table 14: CR#1: Control Register 1*)
- In a second frame, set EN bit to 1 and GOSTBY bit to “0”
  (see bit <2> and bit <3> on *Table 15: CR#2: Control Register 2*)

Table 3. Operating modes

Operating mode	Entering conditions	Leaving condition	Characteristics
Standby mode	– By default, once powered on (VS present); – SPI active and micro sending following consecutive frames: UNLOCK = 1 (EN,GOSTBY) = (0,1)	DIN = High for t_{WAKEUP} and/or CSN = Low for t_{WAKEUP}	– V3V3 < VPOR; – V_S and V_{SPI} low consumption; – SPI inactive
Pre-standby mode	– Under the following conditions: Two following consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (0,1)	CSN High and DIN Low for a time $t > t_{STDBY}$	– V3V3 > VPOR – Boost disabled – Bucks disabled – SPI active
Reset mode	– By default, when device leaves Standby mode – Under following condition, when device is in Active mode: V_{SPI} Under voltage WD failure; One SPI frame setting (EN,GOSTBY) = (0,0) Two consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (1,1)	Automatic transition after 400 ns	– All registers reset to default values – V3V3>VPOR – SPI inactive

Table 3. Operating modes (continued)

Operating mode	Entering conditions	Leaving condition	Characteristics
Limp Home	400 ns after Reset mode	– SPI sequence to enter Active mode: UNLOCK = 1 (EN,GOSTBY) = (1,0) – SPI sequence to enter Standby mode: UNLOCK = 1 (EN,GOSTBY) = (0,1)	– Boost controller is active – DIN access enabled: Buck1 is according to DIN; Buck2 is OFF – SPI active
Active mode	SPI sequence: – UNLOCK = 1 – EN = 1 and GOSTBY = 0	– V_{SPI} undervoltage – WD failure – SPI sequence to enter Standby mode: UNLOCK = 1 (EN,GOSTBY) = (0,1)	– Boost controller is active – Buck converters are active – SPI is active

4.2 Programmable functions

4.2.1 Activation of the buck output

In Active mode, the activation of the Buck converters is performed according to the configuration of control register CR#3<15:14> for Buck1 and CR#3<13:12> for Buck2, as showed in the following table. See *Table 16: CR#3: Control Register 3*.

Table 4. DIN pin Map for Buck1 and Buck2

CR#3<15> or CR#3<13>	CR#3<14> or CR#3<12>	Buck1 and Buck2 status
0	0	Buckx always OFF (default for Buck2)
0	1	Buckx attached to internal PWM generator
1	0	Buckx always ON
1	1	Buckx controlled by DIN Input (default for Buck1)

4.2.2 PWM dimming

The device allows modifying the brightness of the LEDs string simply managing the average current.

The PWM dimming could be achieved in two different ways:

- Through direct input, DIN
- With integrated PWM generator

Dimming with direct input

The signal applies to buck1, buck2 or both, depending on DIN mapping bit configuration (see bits <15:14> and bits <13:12> on *Table 16: CR#3: Control Register 3*). If the control