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L99MD02

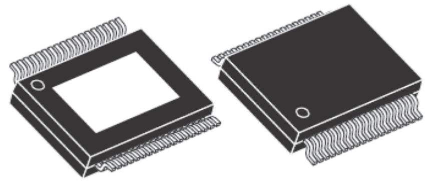
Hexa half-bridge driver with SPI control for automotive applications

Features

- 6 half bridges
- R_{ON} = typ.0.9 Ω (HS), 0.64 Ω (LS) at T_j = 25 °C
- Current limit of each output at minimum 0.8 A
- Internal PWM generation
- PWM mode option for all half bridges for hold current
- Two current monitor outputs
- SPI interface for data communication
- Temperature warning
- All outputs overtemperature protected
- All outputs short circuit protected
- V_{CC} supply voltage 3.0 to 5.3 V
- Very low current consumption in standby mode typ. 5 µA
- V_S operating range compliant: 6 – 18 V

Applications

- DC motor driver Intended to drive HVAC flaps



PowerSSO-36

Description

The L99MD02 IC is a 6 x half bridge driver for automotive applications. The device is intended to drive DC-motors. It is possible to drive 3 DC-motors simultaneously or up to 5 DC-motors sequentially.

The integrated 24 bit standard serial peripheral interface (SPI) controls all outputs and provides diagnostic information: normal operation, open-load in on-state, overcurrent, temperature warning and overtemperature.

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
PowerSSO-36	L99MD02XP	L99MD02XPTR

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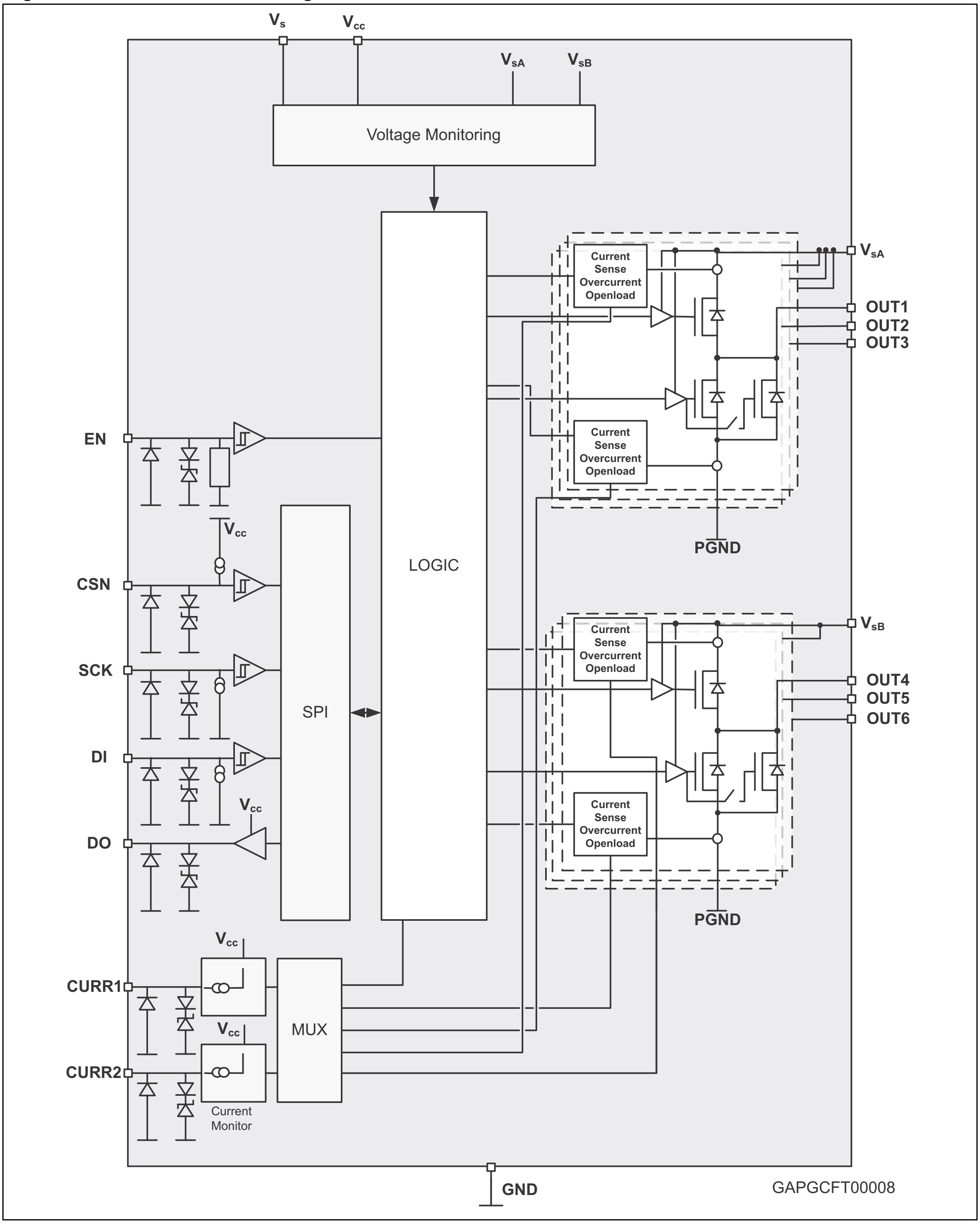
1 Block diagram

Figure 1. Detailed block diagram

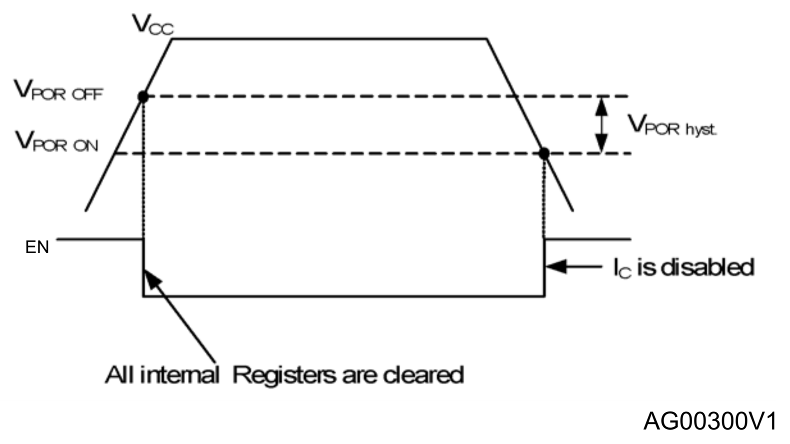


2 Overview

2.1 Power supply: V_{CC}

The supply voltage V_{CC} (3.3 V / 5 V) supplies the whole device. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 2.75 V, typical) the circuit is initialized by an internally generated power-on reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 2.55 V, typical), the outputs are switched off in 3-state (high impedance). The status registers are cleared and the control registers are reset to their default.

Figure 2. Power on reset



2.2 Power supply: V_{SA}, V_{SB}

Each V_{SA} and V_{SB} supplies the half bridges independently.

V_{SA} → Out 1 to Out 3

V_{SB} → Out 4 to Out 6

2.3 Standby mode

The standby mode of the L99MD02 is activated by EN pin to low. The inputs and outputs are switched off. The status registers are cleared and the control registers are reset to their default values.

In the standby mode the current consumption is typically 5 µA.

2.4 PWM mode

PWM frequency typ. 100 Hz.

Duty cycle (SPI 2bit): 15%, 30%, 45% and 60%.

Each half-bridge is independently addressable (SPI 8bit).

2.5 Current monitor

The current monitor output sources a current image at the current monitor output which has a programmable ratio (1/250, 1/500, 1/750, 1/1000) of the instantaneous current of the selected half bridge (high side or low side). Via SPI it can be programmed which of the outputs will be multiplexed to the current monitor output.

The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled).

2.6 Inductive loads

Each half bridge is built by an internally connected high-side and a low-side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs

2.7 Diagnostic functions

All diagnostic functions (over/open-load, temperature warning and thermal shutdown, over/undervoltage) are internally filtered and the condition has to be valid for at least 32 µs (open-load: typ. 2 ms, respectively) before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open-load and temperature warning function are intended for information purpose and will not change the state of the output drivers. On contrary, the overload and thermal shutdown condition will disable the corresponding driver (overload) or all drivers (thermal shutdown), respectively. The microcontroller has to clear the overcurrent status bit to reactivate the corresponding driver.

2.8 Temperature warning and thermal shutdown

If the junction temperature rises above $T_{j\ TW\ ON}$ a temperature warning flag is set and is detectable via the SPI. If the junction temperature increases above the second threshold $T_{j\ SD\ ON}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to protect the device. Temperature warning flag and thermal shutdown bits are latched. In order to reactivate the output stages, the junction temperature must decrease below $T_{j\ SD\ ON} - T_{j\ SD\ HYS}$ and the thermal shutdown bit has to be cleared by the microcontroller.

2.9 V_S, V_{SA}, V_{SB} monitoring

V_S undervoltage: Status bit will be set. Have to be cleared via SPI.
All outputs will be switched off.

V_S overvoltage: Status bit will be set. Has to be cleared via SPI.
All outputs will be switched off (default). Can be deactivated via SPI.

V_{SA} undervoltage: Status bit will be set. Has to be cleared via SPI.
Out 1 to Out 6 will be switched off.

V_{SB} undervoltage: Status bit will be set. Has to be cleared via SPI.
Out 1 to Out 6 will be switched off.

Table 2. V_S, V_{SA}, V_{SB} monitoring

	‘typ	Out x
V_S undervoltage	5.7 V	Status + off
V_S overvoltage	22.0 V	Status + (off or mask)
V_{SA} undervoltage	5.7 V	Status + off
V_{SB} undervoltage	5.7 V	Status + off

2.10 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least 2 ms (t_{dOL}) the corresponding open-load bit is set in the status register.

Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical/ electrical state of the loads.

2.11 Overload detection

In case of an overcurrent condition, a flag is set in the corresponding status register. If the overcurrent signal is valid for at least t_{ISC} = 32 µs, the overcurrent flag is set and the corresponding switch is switched off to reduce the power dissipation and to protect the integrated circuit. The microcontroller has to clear the status bit to reactivate the corresponding driver.

2.12 Cross-current protection

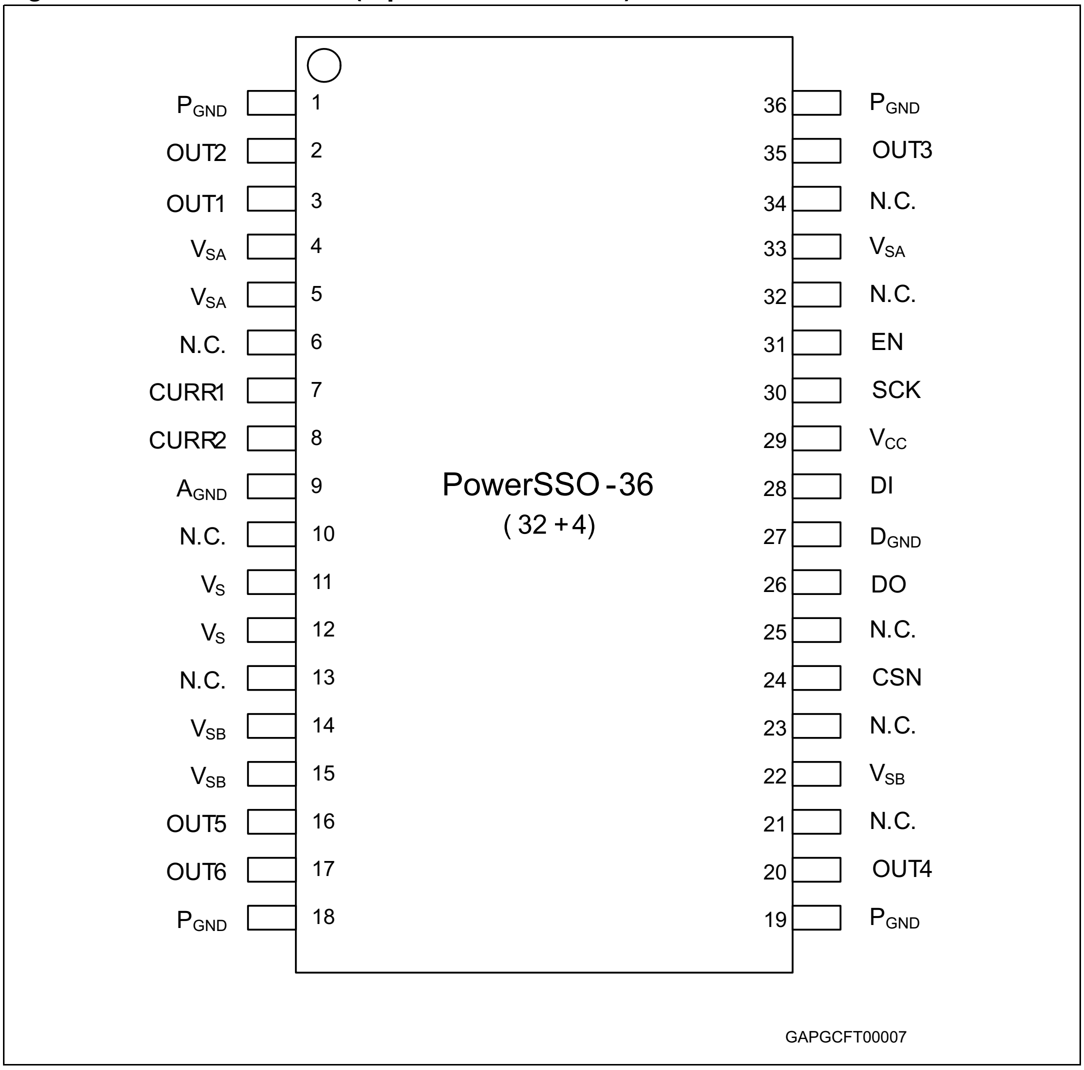
The device is cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver will be changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver will start to conduct. If wrong SPI commands try to turn-on both driver (LS and HS) simultaneously, the high side and the low side will be (or stay) deactivated (3-state).

3 Pin definitions and functions

Table 3. Pin description

Pin	Symbol	Function
1, 18, 19, 36	P_{GND}	Power ground: reference potential
9	A_{GND}	Analog ground: reference potential
27	D_{GND}	Digital ground: reference potential
6, 10, 13, 21, 23, 25, 32, 34	N.C.	Not connected
		Exposed pad: reference potential connected to P_{GND}
2, 3, 16, 17, 20, 35	OUT 1 -6	Half bridge-output: the output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_{Sx}, low-side driver from P_{GND} to output).
29	V_{CC}	Logic voltage supply 3.3V / 5V for this input a ceramic capacitor as close as possible to GND is recommended
4, 5, 33	V_{SA}	Power supply voltage for OUT 1 to 3 (external reverse protection required): for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving the full current at the outputs all pins of V_{SA} must be externally connected!
14, 15, 22	V_{SB}	Power supply voltage for OUT 4 to 6 (external reverse protection required): for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving the full current at the outputs all pins of V_{SB} must be externally connected!
11	V_S	V_S
12	V_S	V_S supply and monitoring
7, 8	CURR1 / 2	Current monitor 1 / 2
31	EN	Enable enable the L99MD02
28	DI	SPI data in the input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB) is transferred first.
26	DO	SPI data out the diagnosis data is available via the SPI and this 3-state output. The output will remain in 3-state, if the chip is not selected by the input CSN (CSN = high)
24	CSN	SPI CSN chip select not (active low) this input is low active and requires CMOS logic levels. The serial data transfer between the L99MD02 and micro controller is enabled by pulling the input CSN to low level.
30	SCK	SPI serial clock input this input controls the internal shift register of the SPI and requires CMOS logic levels.

Figure 3. Pin connection (top view-not in scale)



4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0,3…28	V
	Single pulse t_{max} < 400 ms	40	V
V_{SA} V_{SB}	DC supply voltage	-0,3…38	V
	Single pulse t_{max} < 400 ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
EN DI DO SCK CSN	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
CURR1/2	Current monitor output	-0.3 to V_{CC} + 0.3	
OUT 1-6	Output current capability	±2	A

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit!

4.2 ESD protection

Table 5. ESD protection

Parameter	Value	Unit
All pins	±2(1)	kV
Output pins: OUT1 – 6, V_S, V_{SA}, V_{SB},	±4(2)	kV

1. HBM according to EIA/JESD22-A114-E.
2. HBM with all unzapped pins grounded.

4.3 Thermal data

Table 6. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 7. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j increasing	-	-	150	°C
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing	-	-	170	°C

4.4 Electrical characteristics

V_S = 6 to 18 V, V_{CC} = 3.0 to 5.3 V, T_j = -40 to 150 °C, unless otherwise specified.
The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 8. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SA}/V_{SB}	Operating supply voltage range		6		38	V
I_S	V_{SA} / V_{SB} DC supply current	V_{Sx} = 13 V, V_{CC} = 5.0 V EN = high Outputs floating		0.5	2	mA
I_{VS}	V_S supply current	V_S = 13 V, V_{CC} = 5 V EN = high		1.5	4	mA
I_{VSX}	V_{Sx} (V_S, V_{SA}, V_{SB}) quiescent supply current	V_{Sx} = 13 V, V_{CC} = 5 V EN = low T_{Test} = -40, 25 °C Outputs floating		3	10	µA
		T_{Test} = 130 °C		6	20	µA
V_{CC}	Operating supply voltage range		3,0		5,3	V
I_{CC}	V_{CC} DC supply current	V_{Sx} = 13 V, V_{CC} = 5.0 V EN = high		1	3	mA
	V_{CC} quiescent supply current	V_S = 13 V, V_{CC} = 5.0 V CSN = V_{CC} EN = low Outputs floating		5	20	µA

Table 9. Over and undervoltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{POR\ OFF}$	Power-on-reset threshold	V_{CC} increasing			3.0	V
$V_{POR\ ON}$	Power-on-reset threshold	V_{CC} decreasing	2.3			V
$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.2		V
$V_{SUV\ OFF}$	V_S UV-threshold voltage	V_S increasing	6.0		6.7	V

Table 9. Over and undervoltage detection (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	V_S UV-threshold voltage	V_S decreasing	5.4		6	V
$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ OFF}$ - $V_{SUV\ ON}$	0.35	0.5		V
$V_{SAUV\ OFF}$	V_{SA} UV-threshold voltage	V_{SA} increasing	5.95		6.7	V
$V_{SAUV\ ON}$	V_{SA} UV-threshold voltage	V_{SA} decreasing	5.4		6	V
$V_{SAUV\ hyst}$	V_{SA} UV-hysteresis	$V_{SAUV\ OFF}$ - $V_{SAUV\ ON}$	0.35	0.5		V
$V_{SBUV\ OFF}$	V_{SB} UV-threshold voltage	V_{SB} increasing	6.0		6.7	V
$V_{SBUV\ ON}$	V_{SB} UV-threshold voltage	V_{SB} decreasing	5.4		6	V
$V_{SBUV\ hyst}$	V_{SB} UV-hysteresis	$V_{SBUV\ OFF}$ - $V_{SBUV\ ON}$	0.35	0.5		V
$V_{SOV\ ON}$	V_S OV-threshold voltage	V_S increasing			24	V
$V_{SOV\ OFF}$	V_S OV-threshold voltage	V_S decreasing	18			V
$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ ON}$ - $V_{SOV\ OFF}$	0.75	1		V

Table 10. Switches

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$r_{ON\ HS\ 1\text{-}6}$	On resistance V_{SA} / V_{SB} to OUT 1-6	T_j = 25 °C, I_{OUT}1-6 = -0.25 A		900	1200	m
		T_j = 125 °C, I_{OUT}1-6 = -0.25 A		1300	1800	m
$r_{ONLSHC\ 1\text{-}6}$	On resistance OUT 1-6 to GND in HC mode	T_j = 25 °C, HC = 1 I_{OUT}1-6 = 0.25A		700	1000	m
		T_j = 125 °C, HC = 1 I_{OUT}1-6 = 0.25 A		1000	1500	m
$r_{ONLSLC\ 1\text{-}6}$	On resistance OUT 1-6 to GND in LC mode	T_j = 25 °C, HC = 0 I_{OUT}1-6 = 0.125 A		1200	1800	m
		T_j = 125 °C, HC = 0 I_{OUT}1-6 = 0.125 A		2000	2800	m
$I_{SCHS1\text{-}6}$	HS overcurrent protection	V_S = 13.5 V	0.8		1.4	A
$I_{SCLSHC1\text{-}6}$	LS overcurrent protection in HC mode	V_S = 13.5 V, HC=1	0.8		1.4	A
$I_{SCLSLC1\text{-}6}$	LS overcurrent protection in LC mode	V_S = 13.5 V, HC=0	0.4		0.7	A
$t_{d\ ON1\text{-}6\ H}$	Output delay time, HS switch on	V_S = 13.5 V, R_{load} = 52	10	25	80	µs
$t_{d\ OFF1\text{-}6\ H}$	Output delay time, HS switch off	V_S = 13.5 V, R_{load} = 52	50	100	300	µs
$t_{d\ ON1\text{-}6\ L}$	Output delay time, LS switch on	V_S = 13.5 V, R_{load} = 52	5	15	80	µs
$t_{d\ OFF1\text{-}6\ L}$	Output delay time, LS switch off	V_S = 13.5 V, R_{load} = 52	50	100	300	µs

Table 10. Switches (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{D\ LH}/t_{D\ HL}$	Cross current protection time		20	200	400	µs
I_{QLH}	Switched-off output current HS OUT 1-6	$V_{OUT1-6} = 0$ V	-2			µA
I_{QLL}	Switched-off output current LS OUT 1-6	$V_{OUT1-6} = V_S$			2	µA
$I_{OLDHS1-6}$	Open-load detection current HS OUT 1-6	T_{amb} = -40 °C	8	30	60	mA
		T_{amb} = 25 °C to 125 °C	10	30	60	mA
$I_{OLDLSHC1-6}$	Open-load detection current LS OUT 1-6 in HC mode	HC bit set to 1; T_{amb} = -40 °C	4.5	30	65	mA
		HC bit set to 1; T_{amb} = 25 °C to 125 °C	8	30	60	mA
$I_{OLDLSLC1-6}$	Open-load detection current LS OUT 1-6 in LC mode	HC bit set to 0; T_{amb} = -40 °C	1.8	15	35	mA
		HC bit set to 0; T_{amb} = 25 °C to 125 °C	4	15	30	mA
t_{dOL}	Minimum duration of open-load condition to set the status bit		500	2000	3000	µs
t_{ISC}	Minimum duration of overcurrent condition to switch off the driver		10	32	100	µs
dV_{OUT1-6}/dt	Slew rate of OUT 1-6	V_S = 13.5 V, R_{load} = 52	0.1	0.25	0.5	V/µs

Figure 4. Output turn-on/off delays and slew rates

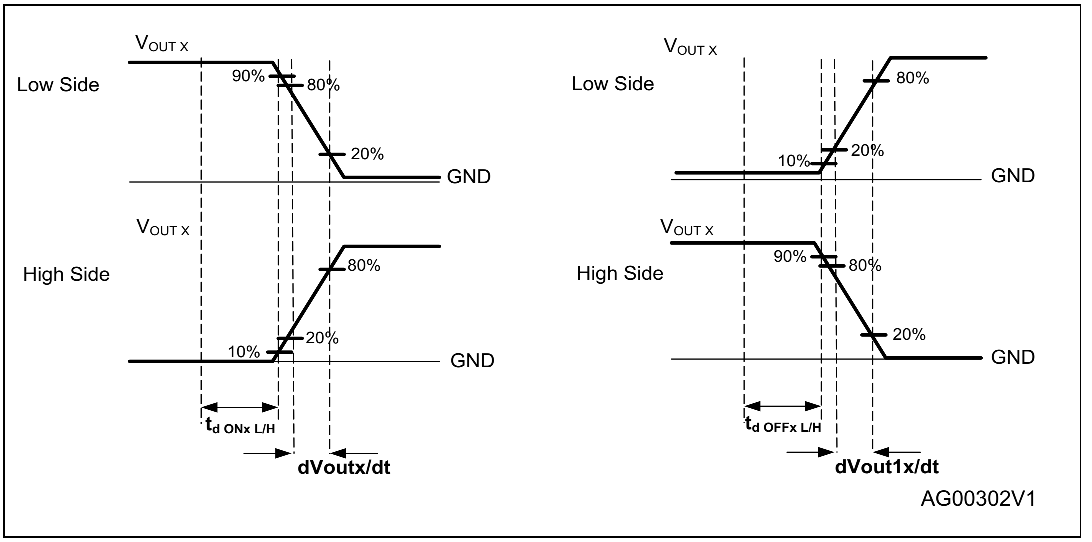


Table 11. **Current monitor output**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CURR1/2}$	Functional voltage range	V_{CC} = 5 V	0		V_{CC} -1	V
$I_{CURRHSLS250}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V, V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA		1/250		
$I_{CURRHSLS500}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA		1/500		
$I_{CURRHSLS750}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA		1/750		
$I_{CURRHSLS1000}$	HS/LS current monitor output ratio: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5 V; prog. via SPI, I_{max} = 800 mA		1/1000		
$I_{CURRLSLC125}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5 V; prog. via SPI, HC=0; I_{max} = 400 mA		1/125		
$I_{CURRLSLC250}$	LS current monitor output ratio in LC mode: $I_{CURRLSLC1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5 V; prog. via SPI, HC=0; I_{max} = 400 mA		1/250		
$I_{CURRLSLC375}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5V; prog. via SPI, HC = 0; I_{max} = 400mA		1/375		
$I_{CURRLSLC500}$	LS current monitor output ratio in LC mode: $I_{CURR1/2}$ / $I_{OUT\ 1\text{-}6}$	0 V <= $V_{CURR1/2}$ <= V_{CC} - 1V V_{CC} = 5V; prog. via SPI, HC = 0; I_{max} = 400 mA		1/500		
$I_{CURRHS1/2\ acc}$	HS current monitor accuracy	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; $I_{OUT\ 1\text{-}6\ max}$ = 0.8 A; (FS = full scale = 800 mA*current ratio); T_j = -40 °C		4% + 1%FS	10% + 3%FS	-
		0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V, V_{CC} = 5 V; $I_{OUT\ 1\text{-}6\ max}$ = 0.8 A; (FS = full scale = 800 mA*current ratio); T_j = 25 °C to 125 °C		4% + 1%FS	8% + 2%FS	
$I_{CURRLSHC1/2\ acc}$	LS current monitor accuracy in HC mode	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V; V_{CC} = 5 V; 0.4 A ≤ $I_{OUT1\text{-}6}$ ≤ 0.8 A; (FS = full scale = 800 mA*current ratio)		4% + 1%FS	10% + 3%FS	-
$I_{CURRLSLC1/2\ acc}$	LS current monitor accuracy in LC mode	0 V ≤ $V_{CURR1/2}$ ≤ V_{CC} - 1 V; V_{CC} = 5 V; $I_{OUT\ 1\text{-}6\ max}$ = 0.4 A; (FS = full scale = 800 mA*current ratio)		4% + 1%FS	10% + 3%FS	-

Table 12. Current monitor dynamic characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\text{-}CM}$	Output to current monitor delau time	I_{OUT} from 100 mA to 200 mA; $t_{d\text{-}CM}$ measured from 50% I_{OUT} to 50% ICM	—	2	—	µs

Table 13. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK}	Internal clock frequency		2.8	4	5.2	MHz

5 SPI electrical characteristics

V_S = 6 to 18 V, V_{CC} = 3.0 to 5.3 V, T_j = -40 to 150 °C, unless otherwise specified.
The voltages are referred to GND and currents are assumed positive, when the current flows into the pin

Table 14. DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SDI, SCK, CSN, EN						
V_{IL}	Input low voltage				0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}			V
$I_{CSN\ in}$	Pull up current at input CSN	V_{CSN} = 1.5 V; V_{CC} = 5 V	8	20	40	µA
$I_{SCK\ in}$	Pull down current at input SCK	V_{SCK} = 1.5 V; V_{CC} = 5 V	10	25	50	µA
$I_{DI\ in}$	Pull down current at input DI	V_{DI} = 1.5 V; V_{CC} = 5 V	10	25	50	µA
$R_{EN\ in}$	Pull down resistor at input EN	V_{EN} = 1.5 V; V_{CC} = 5 V	25	50	115	k
SDO						
V_{OL}	Output low voltage	I_{out} = 2 mA		0.2	0.4	V
V_{OH}	Output high voltage	I_{out} = +2 mA	V_{CC} - 0.4	V_{CC} - 0.2		V
I_{DOLK}	3-state leakage current	$V_{CSN} = V_{CC}$, 0 V < V_{CC}	-10		10	µA

Table 15. AC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SDO, SDI, SCK, CSN, EN						
C_{OUT}(1)	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	-	-	10	pF
C_{IN}	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	-	-	10	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	-	-	10	pF

1. Guaranteed by design.

Table 16. Dynamic characteristics(1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{EN}	EN high setup time				100	µs
t_{SCSN}	CSN setup time before SCK rising		400			ns
t_{HCSN}	CSN high time		2			µs

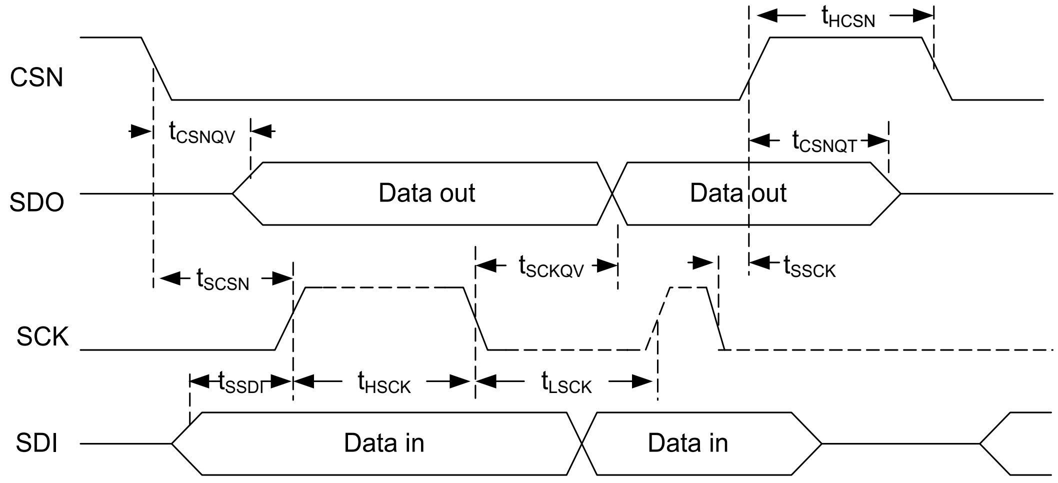
Table 16. Dynamic characteristics[1] (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CSNQV}	CSN falling until SDO valid	C_{OUT} = 100 pF			100	ns
t_{CSNQT}	CSN rising until SDO 3-state	C_{OUT} = 100 pF			150	ns
t_{SSCK}	SCK setup time before CSN rising		50			ns
t_{SSDI}	SDI setup time before SCK rising		40			ns
t_{HSCK}	SCK high time		200			ns
t_{LSCK}	SCK low time		200			ns
t_{SCKQV}	SCK falling until SDO valid	C_{out} = 100 pF			150	ns
t_{QLQH}	Output rise time	C_{out} = 100 pF 20 % - 80 % V_{CC}			110	ns
t_{QHQL}	Output fall time	C_{out} = 100 pF 20 % - 80 % V_{CC}			110	ns
f_{SPI}	SPI frequency				1	MHz

1. See *Section 5.1: SPI timing parameter definition*

5.1 SPI timing parameter definition

Figure 5. SPI timing



t_{CSNQV} : CSN falling until SDO valid
t_{CSNQT} : CSN rising until SDO tristate
t_{SCKQV} : SCK rising until SDO valid
t_{SCSN} : CSN setup time before SCK rising
t_{SSDI} : SDI setup time before SCK rising
t_{HSCK} : minimum SCK high time
t_{LSCK} : minimum SCK low time
t_{HCSN} : minimum CSN high time
t_{SSCK} : SCK setup time before NCS rising

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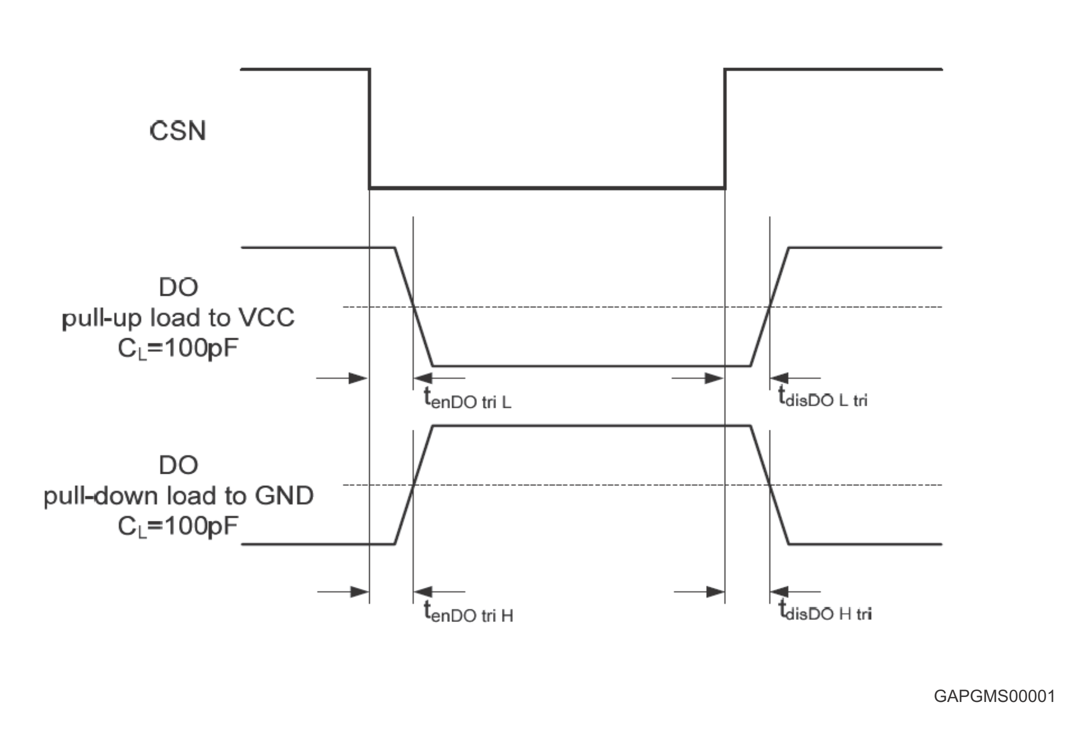
Figure 6. Serial output timing



6 Functional description of the SPI

6.1 Signal description

6.1.1 Serial clock (SCK)

This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK). Data on Serial Data Out (SDO) is shifted out at the falling edge of serial clock (see *Figure 7*). The SPI can be driven by a microcontroller with its SPI peripherals running in following mode: CPOL = 0 and CPHA = 0 (see *Figure 7*).

6.1.2 Serial data input (SDI)

This input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of Serial Clock (SCK).

6.1.3 Serial data output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK). SDO also reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>) while CSN is low and no clock signal is present

6.1.4 Chip select not (CSN)

When this input signal is High, the device is deselected and Serial Data Output (SDO) is high impedance (3-state). Driving this input low enables the communication. The communication must start and stop on a low level of Serial Clock (SCK).

Figure 7. Clock polarity and clock phase

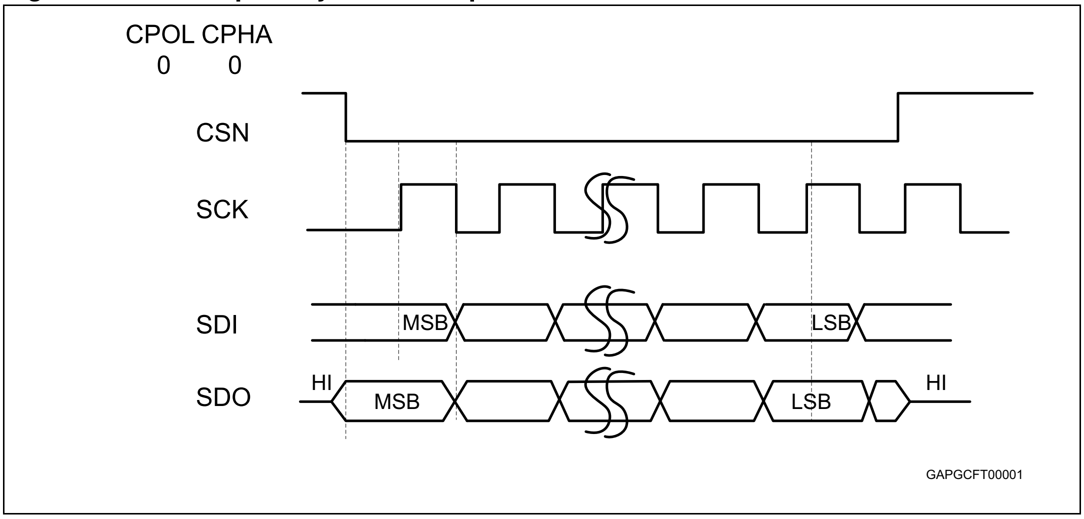
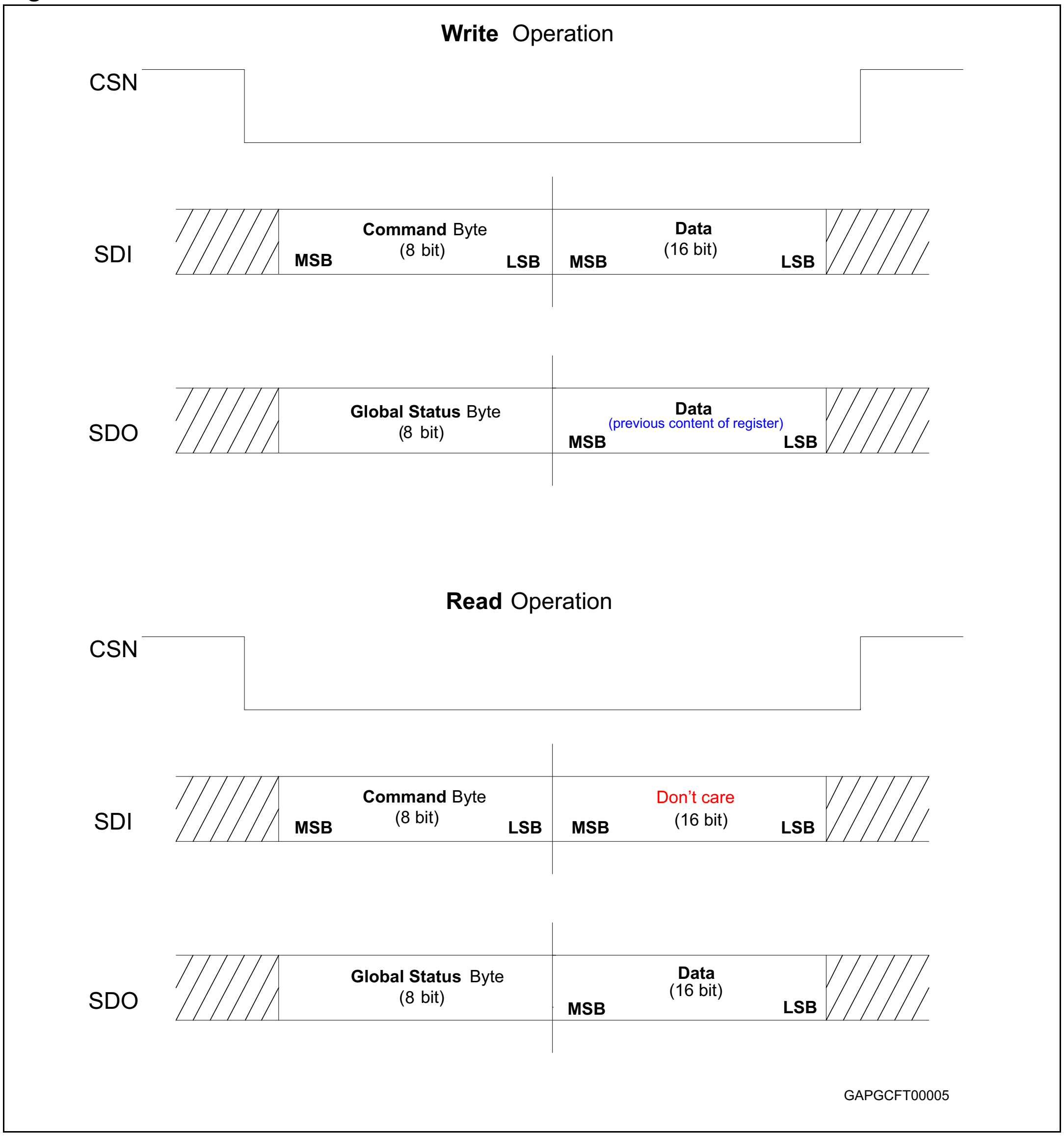


Figure 8. SPI frame structure



6.2 SPI communication flow

6.2.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines. Maximum SPI frequency is 1 MHz.

At the beginning of each communication the master reads the <SPI-frame-ID> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (24 bit for the L99MD02) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by 2 data bytes (*Figure 8*).

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 2bytes (i.e. 'In-frame-response', *Figure 8*).

For write cycles the <Global Status> register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

Table 17. Command byte (8 bit)

	Operating code		Address					
Bit	23	22	21	20	19	18	17	16
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

Table 18. Data byte

	Data Byte 1								Data Byte 0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

6.2.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear Status>, <Read Device Information>) and a 6 bit address.

Table 19. Operating code definition

OC1	OC0	Meaning
0	0	<Write mode>
0	1	<Read mode>
1	0	<Read and clear status>
1	1	<Read device information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device, i.e. write to control registers or read status information.

A <Read and Clear Status> Operation addressed to a device specific status register will read back and subsequently clear this status register. A <Read and Clear Status> Operation with address 3FH clears all status registers at a time and reads back the <Configuration> register.

A <Read and Clear Status> operation addressed to an unused RAM address register will be identical to a <Read Mode> operation (in case of unused RAM address, the second byte will be equal to 00H).

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version and register width.