Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

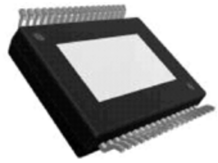
We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

L99PM62GXP

Power management IC with LIN and high speed CAN



PowerSSO-36

Features

- Two 5V voltage regulators for microcontroller and peripheral supply
- No electrolytic capacitor required on regulator outputs
- Ultra low quiescent current in standby modes
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog and fail safe output
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Advanced HS CAN transceiver (ISO 11898-2/-5 and SAE J2284 compliant) with local failure and bus failure diagnosis
- HS CAN transceiver supports partial networking
- Complete 3-channel contact monitoring interface with programmable cyclic sense functionality
- Programmable periodic system wake-up feature
- ST SPI interface for mode control and diagnosis
- 5 fully protected high-side drivers with internal 4-channel PWM generator
- 2 low-side drivers with active Zener clamping
- 4 internal PWM timers
- 2 operational amplifiers with rail-to-rail outputs (V_S) and low voltage inputs
- Temperature warning and thermal shutdown

Applications

- Automotive ECU's such as door zone and body control modules

Description

The L99PM62GXP is a power management system IC that provides electronic control units with enhanced system power supply functionality, including various standby modes, as well as LIN and HS CAN physical communication layers. The device's two low-drop voltage regulators supply the system microcontroller and external peripheral loads such as sensors and provide enhanced system standby functionality with programmable local and remote wake-up capability.

In addition, five high-side drivers, two low-side drivers and two operational amplifiers increase the system integration level.

The ST standard SPI interface (3.0) allows control and diagnosis of the device and enables generic software development.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99PM62GXP	L99PM62GXPTR

Contents

1 Block diagram and pin descriptions 9

2 Detailed description 12

2.1 Voltage regulators 12

2.1.1 Voltage regulator: V_1 12

2.1.2 Voltage regulator: V_2 13

2.1.3 Increased output current capability for voltage regulator V_2 13

2.1.4 Voltage regulator failure 15

2.1.5 Voltage regulator behaviour 16

2.2 Operating modes 16

2.2.1 Active mode 16

2.2.2 Flash mode 17

2.2.3 V1 standby mode 17

2.2.4 VBAT standby mode 18

2.2.5 Wake up from standby modes 18

2.2.6 Wake-up inputs 19

2.2.7 Cyclic contact supply 19

2.2.8 Timer interrupt / wake-up of microcontroller by timer 19

2.3 Functional overview (truth table) 20

2.4 Configurable window watchdog 21

2.4.1 Change watchdog timing 23

2.5 Fail safe mode 25

2.5.1 Single failures 25

2.5.2 Multiple failures – entering forced V_{BAT} standby mode 27

2.6 Reset output (NRESET) 28

2.7 Operational amplifiers 28

2.8 LIN bus interface 28

2.8.1 Error handling 29

2.8.2 Wake up (from LIN) 29

2.8.3 LIN pull-up 30

2.9 High speed CAN bus transceiver 30

2.9.1 CAN error handling 31

2.9.2 Wake up (from CAN) 31

2.9.3 CAN sleep mode 33
2.9.4 CAN receive only mode 33
2.9.5 CAN looping mode 33
2.10 Serial peripheral interface (ST SPI standard) 33

3 Protection and diagnosis 35
3.1 Power supply fail 35
3.1.1 V_S overvoltage 35
3.1.2 Vs undervoltage 35
3.2 Temperature warning and thermal shutdown 37
3.3 High-side driver outputs 38
3.4 Low-side driver outputs REL1, REL2 39
3.5 SPI diagnosis 40

4 Typical application 41

5 Electrical specifications 42
5.1 Absolute maximum rating 42
5.2 ESD protection 43
5.3 Thermal data 43
5.4 Package and PCB thermal data 45
5.4.1 PowerSSO-36 thermal data 45
5.5 Electrical characteristics 48
5.5.1 Supply and supply monitoring 48
5.5.2 Oscillator 49
5.5.3 Power-on reset (VS) 49
5.5.4 Voltage regulator V_1 49
5.5.5 Voltage regulator V_2 50
5.5.6 Reset output 51
5.5.7 Watchdog 51
5.5.8 High-side outputs 53
5.5.9 Relay drivers 54
5.5.10 Wake up inputs (WU1... WU3) 55
5.5.11 High speed CAN transceiver 55
5.5.12 LIN transceiver 58
5.5.13 Operational amplifier 61

5.5.14 SPI 62
5.5.15 Inputs TxD_C and TxD_L for Flash mode 65

6 ST SPI 69

6.1 SPI communication flow 69
6.1.1 General description 69
6.1.2 Operating code definition 69
6.1.3 Global status register 70
6.1.4 Configuration register 70
6.1.5 Address mapping 72
6.1.6 Write operation 72
6.1.7 Format of data shifted out at SDO during write cycle 73
6.1.8 Read operation 74
6.1.9 Format of data shifted out at SDO during read cycle 75
6.1.10 Read and clear status operation 76
6.1.11 Read device information 77
6.2 SPI registers 79
6.2.1 Overview 79
6.2.2 Control registers 81
6.2.3 Status registers 93

7 Package and packing information 99

7.1 ECOPACK® 99
7.2 PowerSSO-36 package information 99

8 Revision history 101

List of tables

Table 1. Device summary 1
Table 2. Pin definition 10
Table 3. Wake up sources 18
Table 4. Functional overview (truth table). 20
Table 5. Fail safe conditions and exit modes 26
Table 6. Persisting fail safe conditions and exit modes 27
Table 7. PWM configuration for high-side outputs 38
Table 8. Absolute maximum rating 42
Table 9. ESD protection 43
Table 10. Operating junction temperature 43
Table 11. Temperature warning and thermal shutdown 43
Table 12. Thermal parameter 47
Table 13. Supply and supply monitoring. 48
Table 14. Oscillator. 49
Table 15. Power-on reset (Vs) 49
Table 16. Voltage regulator V_1 49
Table 17. Voltage regulator V_2 50
Table 18. Reset output 51
Table 19. Watchdog 51
Table 20. Output (OUT_HS) 53
Table 21. Outputs (OUT1...4) 54
Table 22. Relay drivers. 54
Table 23. Wake up inputs (WU1... WU3) 55
Table 24. CAN communication operating range. 55
Table 25. CAN transmit data input: pin TXDC 55
Table 26. CAN receive data output: pin RXDC. 56
Table 27. CAN bus common mode stabilization output termination: pin SPLIT 56
Table 28. CAN transmitter and receiver: pins CANH and CANL 56
Table 29. CAN transceiver timing 58
Table 30. LIN transmit data input: pin TXD. 58
Table 31. LIN receive data output: pin RXD 58
Table 32. LIN transmitter and receiver: pin LIN 58
Table 33. LIN transceiver timing 60
Table 34. LIN pull-up: pin LINPU 61
Table 35. Operational amplifier. 61
Table 36. Input: CSN 62
Table 37. Input CLK, DI 62
Table 38. DI timing 63
Table 39. DO output pin 63
Table 40. DO timing 64
Table 41. CSN timing 64
Table 42. RXDL/NINT timing 65
Table 43. Inputs TxD_C and TxD_L for Flash mode 65
Table 44. Command byte 69
Table 45. Operating code definition 69
Table 46. Global status register 70
Table 47. Configuration register 70
Table 48. Address mapping 72

Table 49. Write command format: command byte . . . 72
Table 50. Write command format: data byte 1 . . . 73
Table 51. Write command format: data byte 2 . . . 73
Table 52. Format of data shifted out at SDO during write cycle: global status register . . . 73
Table 53. Format of data shifted out at SDO during write cycle: data byte 1 . . . 73
Table 54. Format of data shifted out at SDO during write cycle: data byte 2 . . . 73
Table 55. Read command format: command byte . . . 74
Table 56. Read command format: data byte 1 . . . 74
Table 57. Read command format: data byte 2 . . . 74
Table 58. Format of data shifted out at SDO during read cycle: global status register. . . . 75
Table 59. Format of data shifted out at SDO during read cycle: data byte 1 . . . 75
Table 60. Format of data shifted out at SDO during read cycle: data byte 2 . . . 75
Table 61. Read and clear status command format: command byte . . . 76
Table 62. Read and clear status command format: data byte 1 . . . 76
Table 63. Read and clear status command format: data byte 2 . . . 76
Table 64. Format of data shifted out at SDO during read and clear status: global status register . . . 76
Table 65. Format of data shifted out at SDO during read and clear status: data byte 1 . . . 76
Table 66. Format of data shifted out at SDO during read and clear status: data byte 2 . . . 77
Table 67. Read device information . . . 77
Table 68. ID-header . . . 78
Table 69. Family identifier. . . . 78
Table 70. Silicon version identifier . . . 78
Table 71. SPI-frame-ID . . . 79
Table 72. SPI register: command byte . . . 79
Table 73. SPI register: mode selection . . . 79
Table 74. SPI register: CTRL register selection . . . 79
Table 75. SPI register: STAT register selection . . . 80
Table 76. Overview of control registers data bytes. . . . 81
Table 77. Control register 1: command and data bytes . . . 82
Table 78. Control register 1, data bytes . . . 82
Table 79. Control register 1, bits. . . . 82
Table 80. Control register 2: command and data bytes . . . 84
Table 81. Control register 2, data bytes . . . 84
Table 82. Control register 2, bits. . . . 85
Table 83. Control register 3: command data bytes. . . . 85
Table 84. Control register 3, data bytes . . . 85
Table 85. Control register 3, bits. . . . 86
Table 86. Control register 4: command and data bytes . . . 87
Table 87. Control register 4, data bytes . . . 88
Table 88. Control register 4, bits. . . . 88
Table 89. Control register 5: command and data bytes . . . 90
Table 90. Control register 5, data bytes . . . 90
Table 91. Control register 5, bits. . . . 90
Table 92. Control register 6: command and data bytes . . . 91
Table 93. Control register 6, data bytes . . . 91
Table 94. Control register 6, bits. . . . 92
Table 95. Overview of status register data bytes . . . 93
Table 96. Global status register . . . 93
Table 97. Status register 1: command and data bytes . . . 94
Table 98. Status register 1, data bytes . . . 94
Table 99. Status register 1, bits . . . 95
Table 100. Status register 2: command and data bytes . . . 96

Table 101. Status register 2, data bytes . . . 96
Table 102. Status register 2, bits . . . 96
Table 103. Status register 3: command and data bytes . . . 97
Table 104. Status register 3, data bytes . . . 97
Table 105. Status register 3, bits . . . 97
Table 106. PowerSSO-36 mechanical data . . . 100
Table 107. Document revision history . . . 101

List of figures

Figure 1. Block diagram 9
Figure 2. Pin connection (top view) 11
Figure 3. Voltage source with external PNP 13
Figure 4. Voltage source with external PNP and current limitation 13
Figure 5. Voltage source with external NPN 14
Figure 6. Voltage source with external NPN and current limitation 14
Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions 16
Figure 8. Operating modes 21
Figure 9. Watchdog in normal operating mode (no errors) 22
Figure 10. Watchdog with error conditions 23
Figure 11. Watchdog in Flash mode 23
Figure 12. Change watchdog timing within long open window 24
Figure 13. Change watchdog timing within window mode 24
Figure 14. General procedure to change watchdog timing out of fail safe mode 25
Figure 15. Change watchdog timing out of fail safe mode (watchdog failure) 25
Figure 16. Example: exit fail safe mode from watchdog failure 27
Figure 17. LIN master node configuration using LIN_PU (optional) 30
Figure 18. CAN wake up capabilities 32
Figure 19. Over voltage and under voltage protection and diagnosis 36
Figure 20. Thermal shutdown protection and diagnosis 37
Figure 21. Phase shifted PWM 39
Figure 22. Typical application diagram 41
Figure 23. Thermal data of PowerSSO-36 44
Figure 24. PowerSSO-36 PC board 45
Figure 25. PowerSSO-36 Thermal Resistance junction to ambient vs PCB copper area (V1 ON) . . . 46
Figure 26. PowerSSO-36 Thermal Impedance junction to ambient vs PCB copper area (single pulse with V1 ON) 46
Figure 27. PowerSSO-36 thermal fitting model (V1 ON) 47
Figure 28. Watchdog timing (long, early, late and safe window) 52
Figure 29. Watchdog early, late and safe windows 53
Figure 30. LIN transmit, receive timing 61
Figure 31. SPI – transfer timing diagram 65
Figure 32. SPI - input timing 66
Figure 33. SPI output timing (part 1) 67
Figure 34. SPI output timing (part 2) 68
Figure 35. SPI – CSN low to high transition and global status bit access 68
Figure 36. Read configuration register(1) 71
Figure 37. Write configuration register(1) 71
Figure 38. Format of data shifted out at SDO during write cycle 74
Figure 39. Format of data shifted out at SDO during read cycle 75
Figure 40. Format of data shifted out at SDO during read and clear status operation 77
Figure 41. PowerSSO-36 package dimensions 99

1 Block diagram and pin descriptions

Figure 1. Block diagram

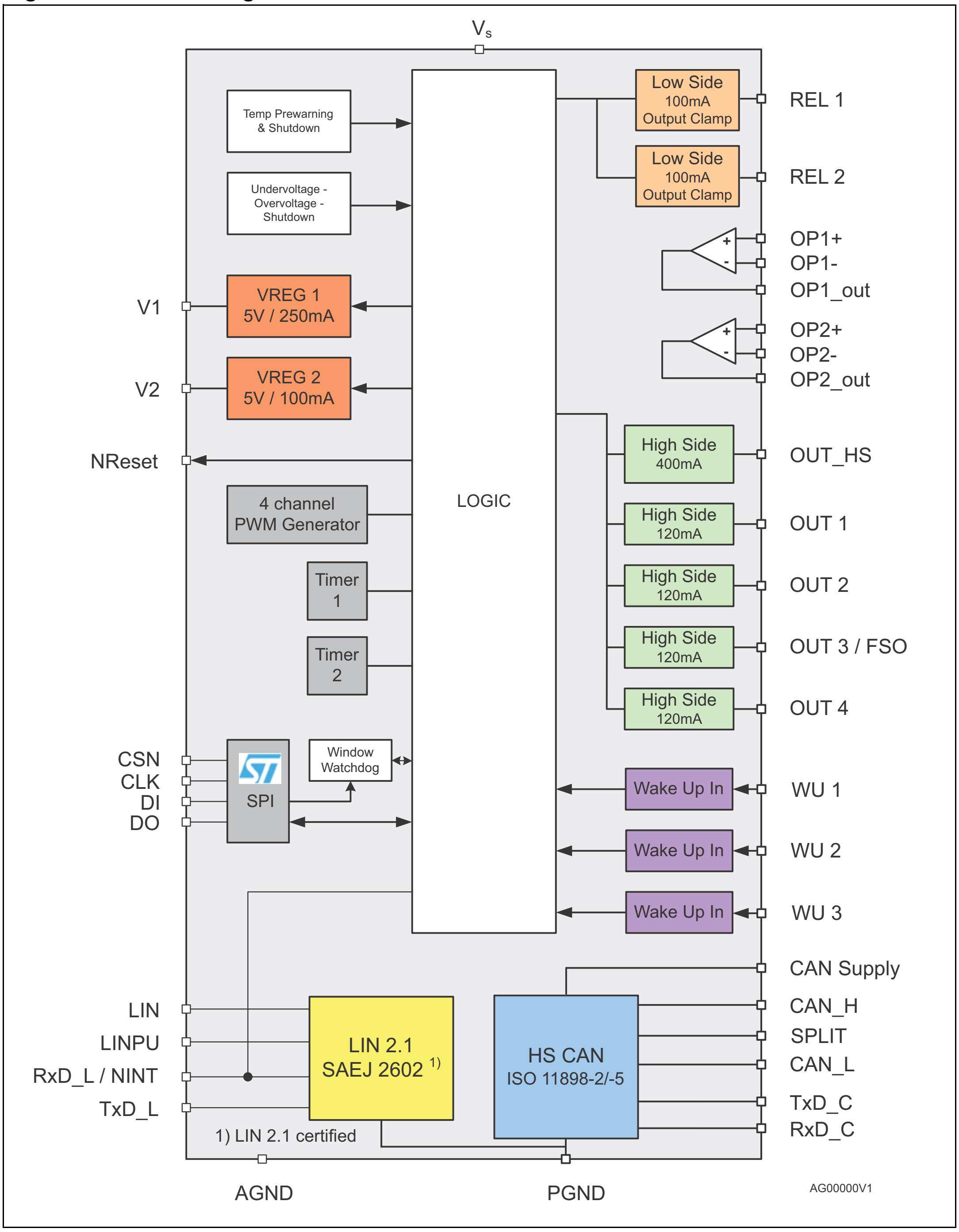


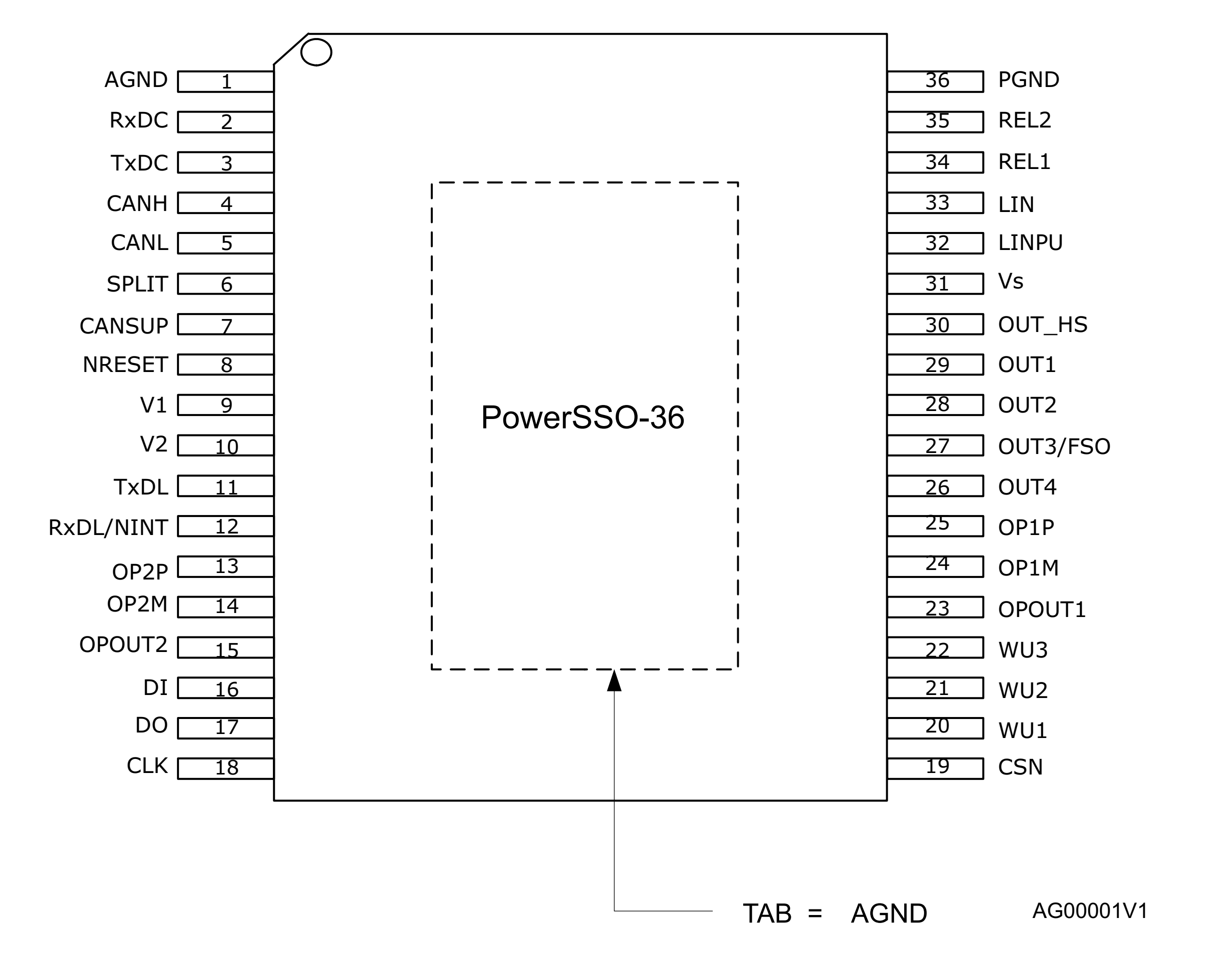
Table 2. Pin definition

Pin	Symbol	Function
1	AGND	Analog ground
2	RxDC	CAN receive data output
3	TxDC	CAN transmit data input
4	CANH	CAN high level voltage I/O
5	CANL	CAN low level voltage I/O
6	SPLIT	CAN reference voltage output, CAN termination
7	CANSUP	CAN supply input; to allow external CAN supply from V_1 or V_2 regulator.
8	NRESET	NReset output to micro controller; Internal pull-up of typical 100 KΩ (reset state = LOW)
9	V_1	Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver
10	V_2	Voltage regulator 2 output: 5 V supply for external loads (IR receiver, potentiometer, sensors) or CAN Transceiver. V_2 is protected against reverse supply.
11	TxDL	LIN Transmit data input
12	RxDL/NINT	RxDL -> LIN receive data output NINT -> indicates local/remote wake-up events or provides a programmable timer interrupt signal
13	OP2+	Non inverting input of operational amplifier 2
14	OP2-	Inverting input of operational amplifier 2
15	OP2_OUT	Output of operational amplifier 2
16	DI	SPI: serial data input
17	DO	SPI: serial data output
18	CLK	SPI: serial clock input
19	CSN	SPI: chip select not input
20…22	WU1…3	Wake-up Inputs 1to 3: Input pins for static or cyclic monitoring of external contacts
23	OP1_OUT	Output of operational amplifier 1
24	OP1-	Inverting input of operational amplifier 1
25	OP1+	Non inverting input of operational amplifier 1
26	OUT4	High-side driver output (7 Ω, typ)
27	OUT3/FSO	Configurable as high-side driver output (7 Ω, typ) or fail safe output pin (default)
28	OUT2	High-side driver output (7 Ω, typ)
29	OUT1	High-side driver output (7 Ω, typ)
30	OUT_HS	High-side driver (1 Ω, typ)
31	V_S	Power supply voltage
32	LINPU	High-side driver output to switch off LIN master pull up resistor
33	LIN	LIN bus line
34	REL1	Low-side driver output (2 Ω typ)

Table 2. Pin definition (continued)

Pin	Symbol	Function
35	REL2	Low-side driver output (2 Ω typ)
36	PGND	Power ground (REL1/2, LIN and CAN GND), to be externally connected to AGND

Figure 2. Pin connection (top view)



Note: It is recommended to connect the PGND and AGND pins directly to the TAB.

2 Detailed description

2.1 Voltage regulators

The L99PM62GXP contains two independent and fully protected low drop voltage regulators, which are designed for very fast transient response and don't require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors $\geq$ 220 nF.

2.1.1 Voltage regulator: V_1

The V_1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current and is mainly intended for supply of the system microcontroller. The V_1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode.

It can be used to supply the internal HS CAN Transceiver via the CANSUP pin externally. In case of a short circuit condition on the CAN bus, the output current of the transmitter is limited to 100 mA and the transceiver is turned off in order to ensure continued supply of the microcontroller.

In addition the regulator V_1 drives the L99PM62GXP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors $\geq$ 220 nF.

If the device temperature exceeds the TSD1 threshold, all outputs (OUTx, RELx, V_2, LIN) is deactivated except V_1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2>TSD1), also V_1 is deactivated (see state chart in *Chapter 3: Protection and diagnosis*). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1sec. During this time, all other wake up sources (CAN, LIN, WU1 to3 and wake up of µC by timer) are disabled. After 1 sec, the voltage regulator tries to restart automatically. If the restart fails 7 times, within one minute, without clearing and thermal shutdown condition still exists, the L99PM62GXP enters the forced V_{BAT} standby Mode.

In case of short to GND at "V_1" after initial turn on (V_1 < 2V for t > $t_{V1short}$) the L99PM62GXP enters the forced V_{BAT} standby Mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..3 or *periodic wake by timer* (see *Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer*).

2.1.2 Voltage regulator: V_2

The voltage regulator V_2 can supply additional 5 V loads (e.g. logic components or the integrated HS CAN transceiver or external loads such as sensors or potentiometers). The maximum continuous load current is 100 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.1.3 Increased output current capability for voltage regulator V_2

For applications which require high output currents, the output current capability of the regulator can be increased my means of the integrated operational amplifiers and an external pass transistor.

Figure 3. Voltage source with external PNP

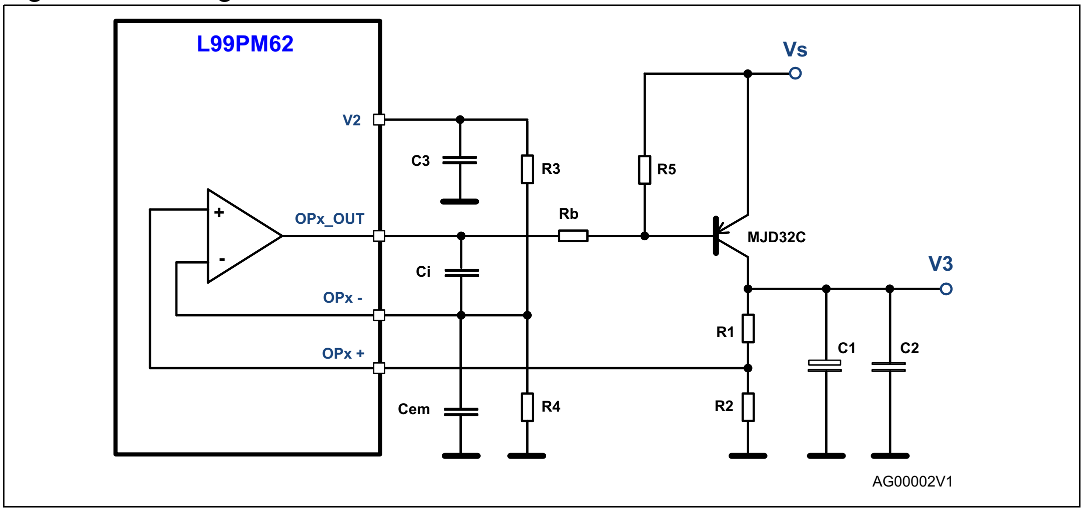


Figure 4. Voltage source with external PNP and current limitation

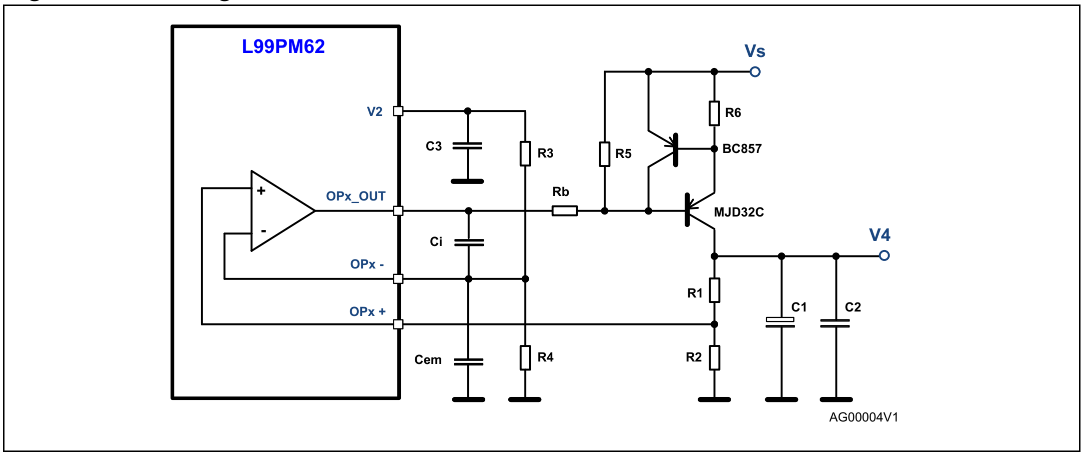


Figure 3 shows a possible configuration with a PNP pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3.

The Vs operating range for this circuit is 5.5 V to 18 V. It is important the respect the input common mode range specified for the operational amplifiers.

The output voltage V3 can be calculated using the following formula:

$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 4* provides additional current limitation using an additional PNP transistor and R6 which allows setting the current limit.

Figure 5. Voltage source with external NPN

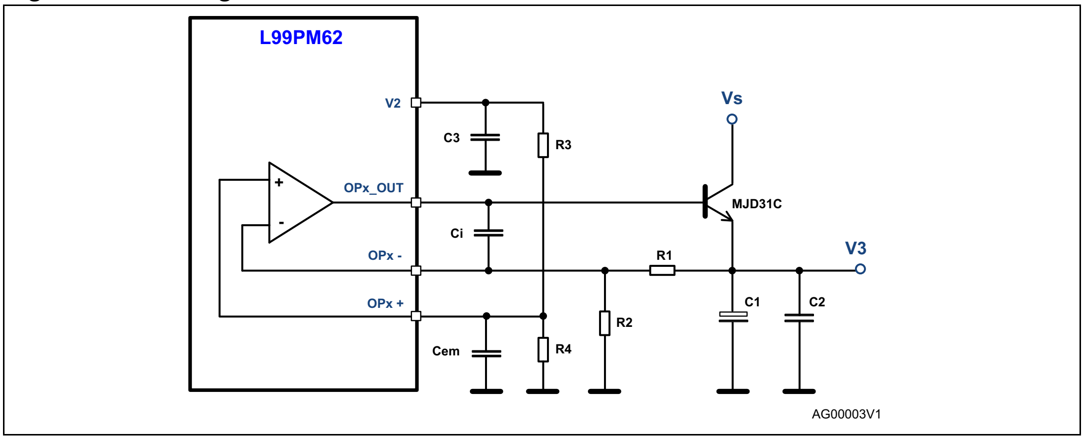


Figure 6. Voltage source with external NPN and current limitation

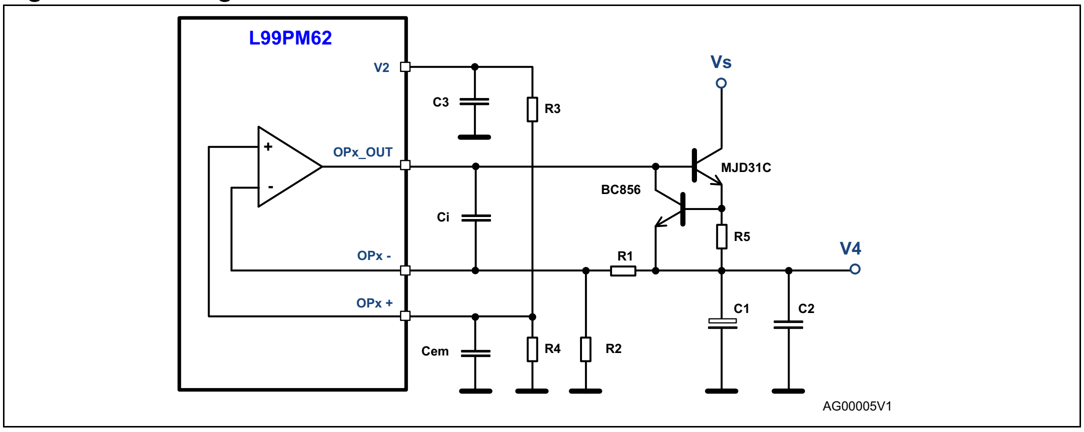


Figure 5 shows a possible configuration with an NPN pass element using voltage regulator 2 to provide the voltage reference for the regulated output voltage V3. This circuit requires fewer components compared to the configuration in *Figure 3* but has a limited V_S operating range (6 V to 18 V).

The output voltage V3 can be calculated using the following formula:

$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 6* provides additional current limitation using an additional NPN transistor and R5 which allows setting the current limit.

Alternatively, voltage regulator 1 can be used to provide the 5 V reference for this topology. However, the additional current consumption through R3 and R4 has to be considered in V_1standby mode.

2.1.4 Voltage regulator failure

The $V_{1,}$ and V_2 regulator output voltages are monitored.

In case of a drop below the $V_{1,}$ V_2 – fail thresholds ($V_{1,2}$ < 2 V, typ for t > 2 µs), the $V_{1,2}$-fail bits are latched. The fail bits can be cleared by a dedicated SPI command.

Short to ground detection

If 4 ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for $V_{1,2}$), the L99PM62GXP identifies a short circuit condition at the related regulator output and the regulator is switched off.

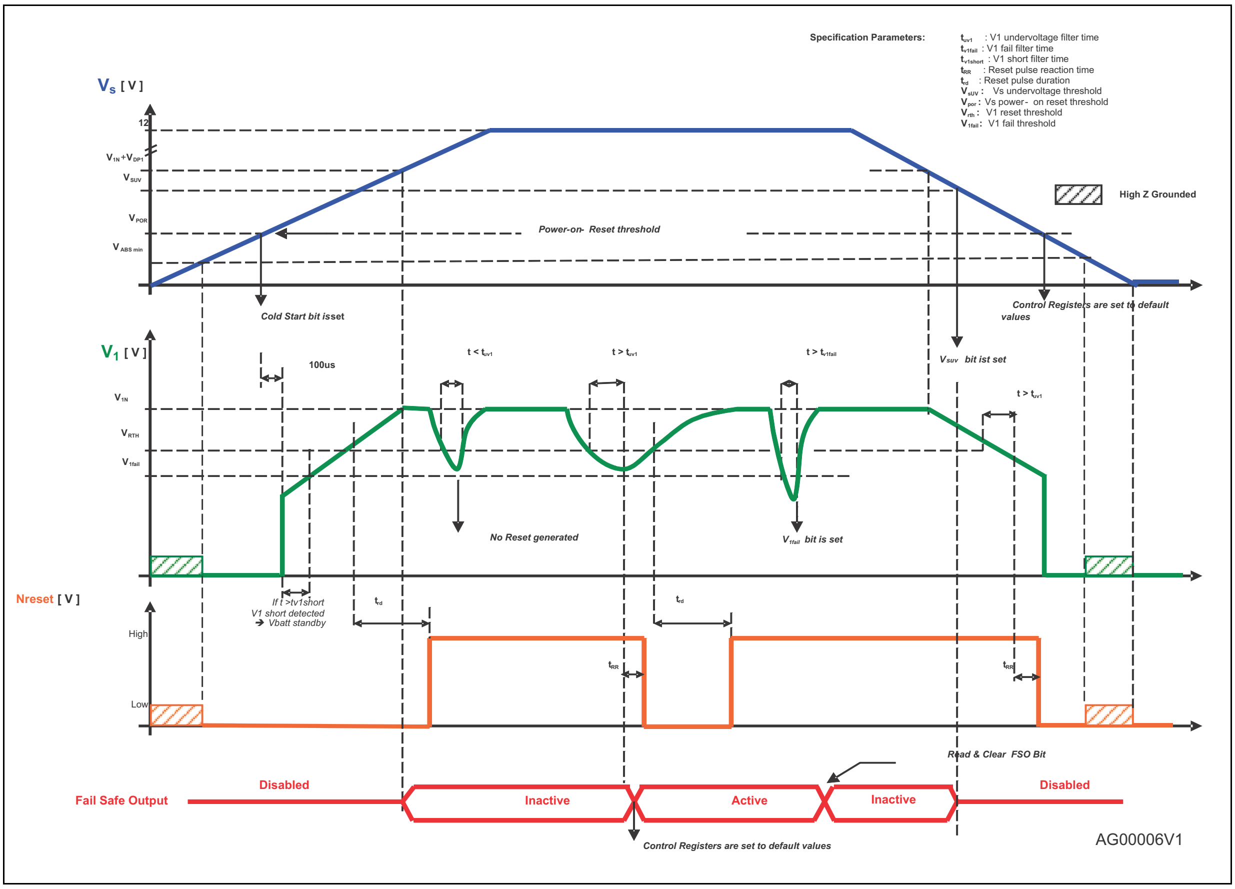
In case of V_1 short to GND failure the device enters V_{BAT} standby mode automatically. Bits Forced V_{BAT} STD2/SHTV$_1$ and V_1 fail were set.

In case of a V_2 short to GND failure the V_2short and V_2 fail bit is set.

If the output voltage of the corresponding regulator once exceeded the $V_{1,2}$ fail thresholds the short to ground detection is disabled. If a short to ground condition occurs the regulator outputs switches off due to thermal shutdown (V_1 at TSD2; V_2 at TSD1).

2.1.5 Voltage regulator behaviour

Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions



2.2 Operating modes

The L99PM62GXP can be operated in 4 different operating modes:

- Active
- Flash
- V_1 standby
- V_{BAT} standby

A cyclic monitoring of wake-up inputs and a periodic interrupt/wake-up by timer is available in standby modes.

2.2.1 Active mode

All functions are available and the device is controlled by the ST SPI Interface.

2.2.2 Flash mode

To program the system microcontroller, the L99PM62 can be operated in Flash mode where the internal watchdog is disabled. This mode can also be used for software debugging.

Except for the disabled watchdog, the Flash mode is identical to active mode and all device features are available.

A transition from Flash mode to V_{1stby} or $V_{batstby}$ is not possible.

The mode can be entered if one of the following conditions is applied:

- $V_{TxDL} \geq V_{Flash}$
- $V_{TxDC} \geq V_{Flash}$

At exit from Flash mode ($V_{TxD} < V_{Flash}$) no NReset pulse is generated and the watchdog starts with a long open window.

Note: *Setting both TxDL and TxDC to high voltage levels (> V_{Flash}) is not allowed.*

Communication at the respective TxD pin is not possible.

2.2.3 V_1 standby mode

The transition from active mode to V_1 standby mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 (V_1) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the I_{cmp} current threshold. At this transition, the L99PM62 also deactivates the internal watchdog.

Relay outputs, LIN and CAN transmitters is switched off in V_1 standby mode. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

A cyclic supply of external contacts and a synchronized monitoring of the contact state can be activated and configured by SPI.

In V_1 standby mode various wake up sources can be individually programmed. Each wake up event puts the device into active mode and forces the RxDL/NINT pin to a low level indicating the wake-up condition to the microcontroller.

After power ON reset (POR) all wake up sources are activated by default except the periodic interrupt/wake timer.

With the interrupt timer the micro controller can be forced from ‘stop’ to ‘run’ after a programmable period. The RxDL/NINT pin is forced low after the timer is elapsed. The L99PM62GXP enters active mode and is awaiting a valid watchdog trigger.

Both internal timers can be used for this feature.

The interrupt timer (T_{INT}) at pin RxDL/NINT is only available in V_1 standby mode.

Note: *Inputs TxDL, TxDC and CSN must be at high level or at high impedance in order to achieve minimum standby current in* V_1 *standby mode.*

Inputs DI and CLK must be at GND or at high impedance to achieve minimum standby current in V_1 standby mode.

Interrupt

The interrupt signal (linked to RxDL/NINT internally) indicates a wake-up event from V_1 standby mode. In case of a wake-up by Wake-up Inputs, activity on LIN or CAN, SPI access or timer-interrupt the NINT pin is pulled low for 56 µs.

In case of V_1 standby mode and ($I_{V1} > I_{cmp}$), the device remains in standby mode, the V_1 regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

2.2.4 V_{BAT} standby mode

The transition from active mode to V_{BAT} standby mode is initiated by an SPI command.

In V_{BAT} standby mode, the V_1 voltage regulator, relay outputs, LIN and CAN transmitters are switched off. High-side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

In V_{BAT} standby mode the current consumption of the L99PM62GXP is reduced to a minimum level.

Note: Inputs TXDL, TXDC and CSN must be terminated to GND in V_{BAT} standby to achieve minimum standby current.

This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V_1 is pulled to GND).

2.2.5 Wake up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 3. Wake up sources

Wake up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI
Level change of WU1 - 3	Can be individually configured or disabled by SPI
$I_{V1} > I_{cmp}$	Device remains in V_1 standby mode but watchdog is enabled (If I_{cmp} = 0) and the V_1 regulator goes into high current mode (increased current consumption). No interrupt is generated.
Timer interrupt / wake up of µC by TIMER	Programmable by SPI – V_1 standby mode: device wakes up and Interrupt signal is generated at RxDL/NINT when programmable time-out has elapsed – V_{BAT} standby mode: device wakes up, V_1 regulator is turned on and NReset signal is generated when programmable time-out has elapsed
SPI access	Always active (except in V_{BAT} standby mode) Wake up event: CSN is low and first rising edge on CLK

To prevent the system from a deadlock condition (no wake up possible) a configuration where the periodic timer interrupt and wake up by LIN and HS CAN are disabled, is not allowed. The default configuration is entered for all wake-up sources in case of such an invalid setting.

All wake-up events from V_1 standby mode (except $I_{V1} > I_{cmp}$) are indicated to the microcontroller by a low-pulse at RxDL/NINT (duration: 56 µs).

Wake-up from V_1 standby by SPI Access might be used to check the interrupt service handler.

2.2.6 Wake-up inputs

The de-bounced digital inputs WU1 to WU3 can be used to wake up the L99PM62GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 µs is implemented at WU1-3. The filter is started when the input voltage passes the specified threshold.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic sense functionality is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer1 or Timer2 (see *Section 2.2.7: Cyclic contact supply*). The input signal is filtered with a filter time of 16 µs after a programmable delay (80 µs or 800 µs) according to the configured timer on-time. A wake-up is processed if the status has changed versus the previous cycle.

The outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode the input filter timing and input filter delay (*WUx_filt* in control register 2) must correspond to the setting of the high-side output which supplies the external contact switches (OUTx in control register 0).

In standby mode, the inputs WU1-3 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external. In active mode the inputs have a pull down resistor.

In active mode, the input status can be read by SPI (Status Register 2). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

2.2.7 Cyclic contact supply

In V_1 standby and V_{BAT} standby modes, any high-side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X s. The on-time is 10 ms resp. 20 ms: With $X \in \{1, 2, 3, 4\ s\}$

Timer 2: period is X ms. The on-time is 100 µs resp. 1ms: With $X \in \{10, 20, 50, 200\ ms\}$

2.2.8 Timer interrupt / wake-up of microcontroller by timer

During standby modes the cyclic wake up feature, configured via SPI, allows waking up the µC after a programmable timeout according to timer1 or timer2.

From V_1 standby mode, the L99PM62GXP wakes up (after the selected timer has elapsed) and sends an interrupt signal (via RxDL/NINT pin) to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_1 standby after finishing its tasks.

From V_{BAT} standby mode, the L99PM62GXP wakes up (after the selected timer has elapsed), turns on the V_1 regulator and provides an NReset signal to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into V_{BAT} standby after finishing its tasks.

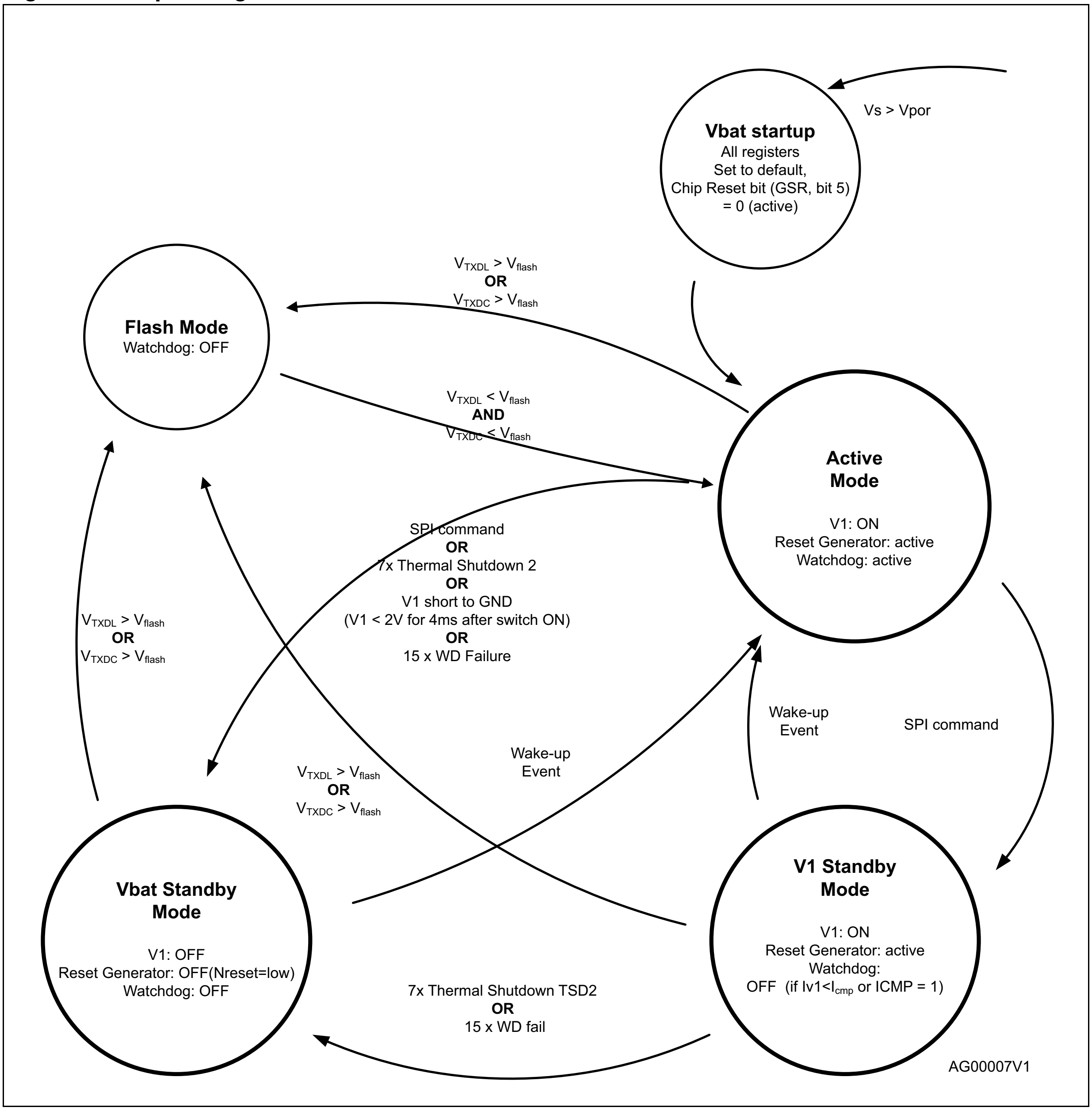
2.3 Functional overview (truth table)

Table 4. Functional overview (truth table)

Function	Comments	Operating modes		
		Active mode	V_1-standby static mode (cyclic sense)	V_{BAT}-standby static mode (cyclic sense)
Voltage-regulator, V_1	V_{OUT} = 5 V	On	On(1)	Off
Voltage-regulator, V_2	V_{OUT} = 5 V	On/ Off (2)	On(2) / Off	On(2) / Off
Reset-generator		On	On	Off
Window watchdog	V_1 monitor	On	Off (On: $I\_V_1 > I_{cmp}$-threshold and I_{cmp} = 0)	Off
Wake up		Off	Active(3)	Active(3)
HS-cyclic supply	Oscillator time base	On / Off	On(2) / Off	On(2) / Off
Relay driver		On	Off	Off
Operational amplifiers		On	Off	Off
LIN	LIN 2.1	On	Off(4)	Off(4)
HS_CAN		On	Off(4)	Off(4)
FSO (if configured by SPI), active by default	Fail safe output	OUT3/FSO Off(5)	OUT3/FSO Off(5)	OUT3/FSO Off(5)
Oscillator		On	(6)	(6)
Vs-monitor		On	(7)	(7)

1. Supply the processor in low current mode.
2. Only active when selected via SPI.
3. Unless disabled by SPI.
4. The bus state is internally stored when going to standby mode. A change of bus state leads a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI).
5. ON in fail-safe condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
6. Activation = ON if cyclic sense is selected.
7. cyclic activation = pulsed ON during cyclic sense.

Figure 8. Operating modes



2.4 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle: (10 ms, 50 ms, 100 ms, 200 ms)

In V_{BAT} standby and Flash program modes, the watchdog circuit is automatically disabled. In V_1 standby mode a wake up by timer is programmable in order to wake up the µC (see *Section 2.2.8: Timer interrupt / wake-up of microcontroller by timer*). After wake-up, the watchdog starts with a long open window. After serving the watchdog, the µC may send the device back to V_1 standby mode.

After power-on or standby mode, the watchdog is started with a long open window (65 ms nominal). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is processed when the CSN input becomes HIGH after the transmission of the SPI word.

Writing ‘1’ to the watchdog trigger bit terminates the long open window and start the window watchdog (the timing is programmable by SPI). Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to *Figure 29*). A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the V_1 regulator is switched off for 200ms. If subsequently, 7 additional watchdog failures occur, the V_1 regulator is completely turned off and the device goes into V_{BAT} standby mode until a wakeup occurs.

In case of a watchdog failure, the outputs (RELx, OUTx, V_2) are switched off and the device enters fail-safe mode (i.e. all control registers are set to default values except the ‘OUT3 control bit’).

The following diagrams illustrate the watchdog behavior of the L99PM62. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of Flash mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and Flash mode.

Figure 9. Watchdog in normal operating mode (no errors)

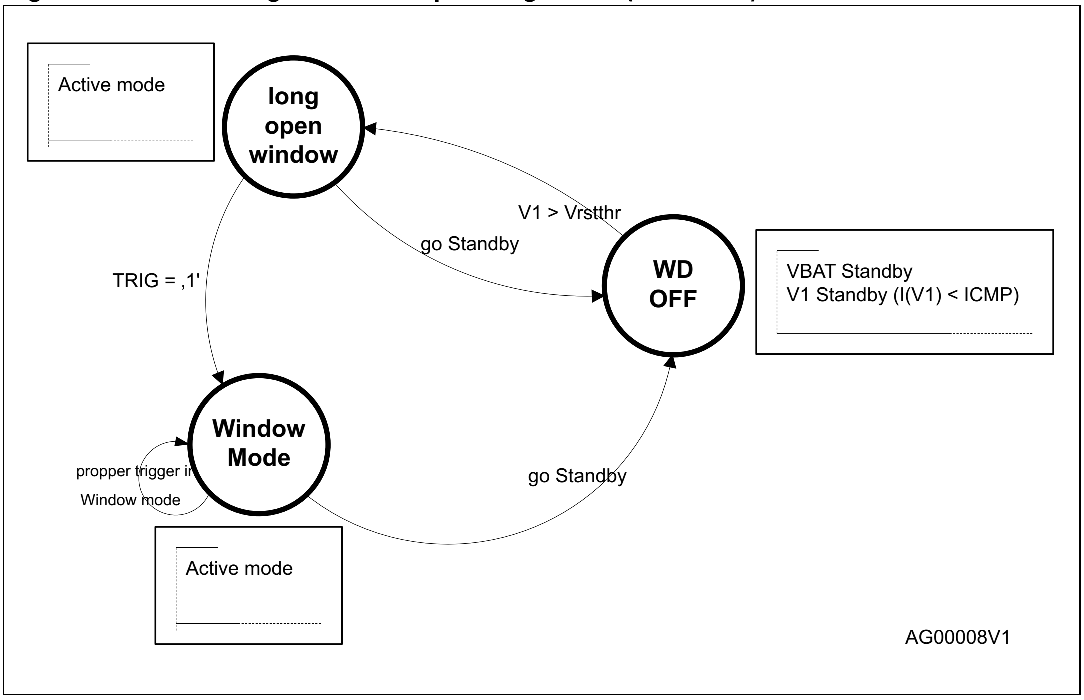


Figure 10. Watchdog with error conditions

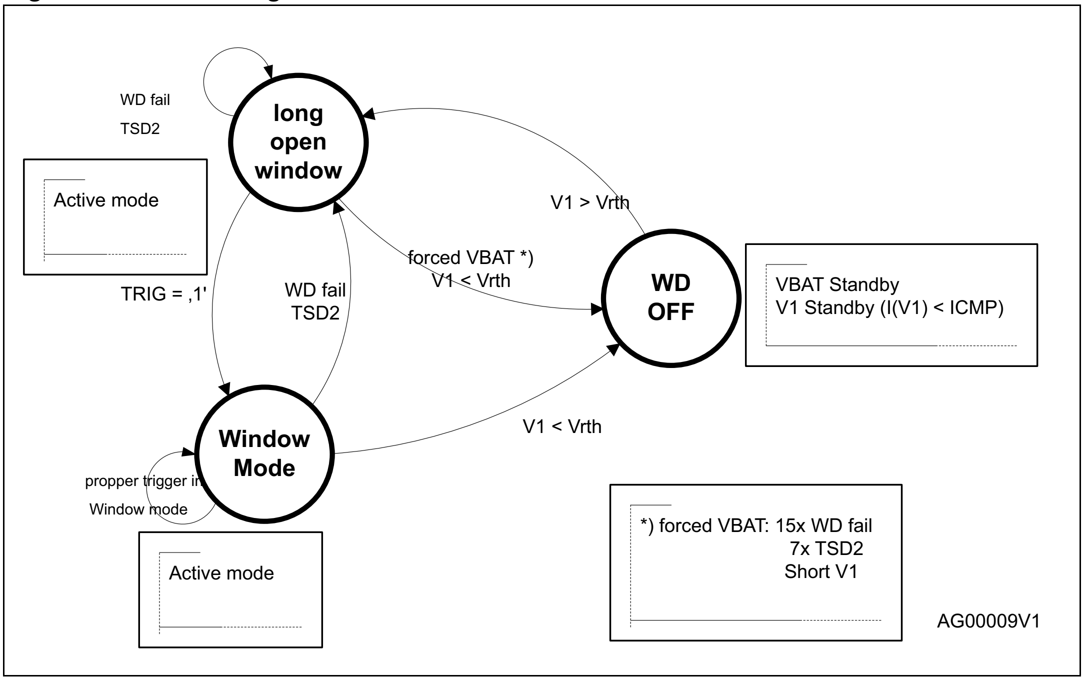
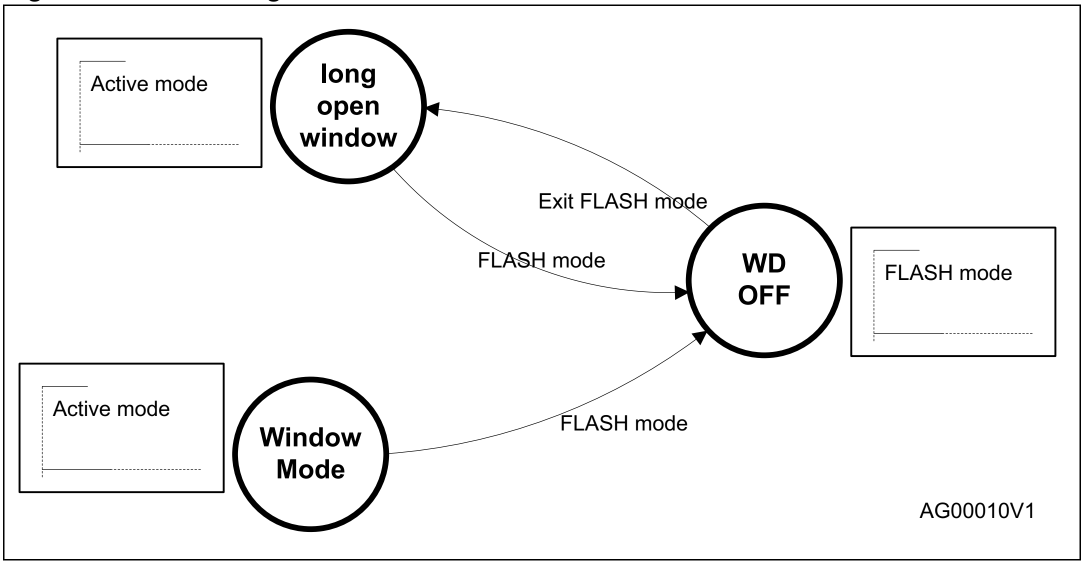


Figure 11. Watchdog in Flash mode



2.4.1 Change watchdog timing

There are 4 programmable watchdog timings available, which represent the nominal trigger time in window mode. To change the watchdog timing, a new timing has to be written by SPI. The new timing gets active with the next valid watchdog trigger. The following figures illustrate the sequence, which is recommended to use, changing the timing within long open window and within window mode.

Figure 12. Change watchdog timing within long open window

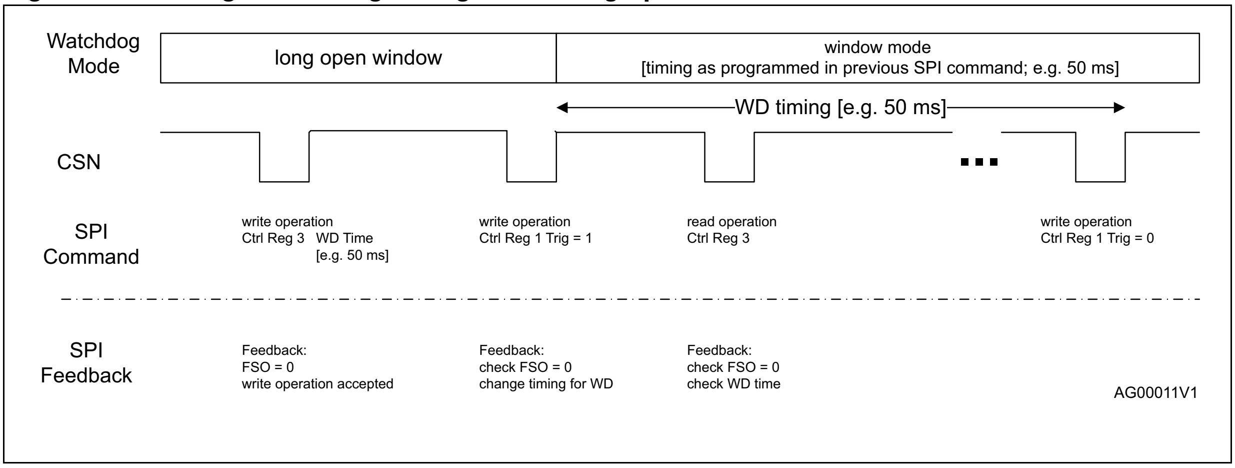
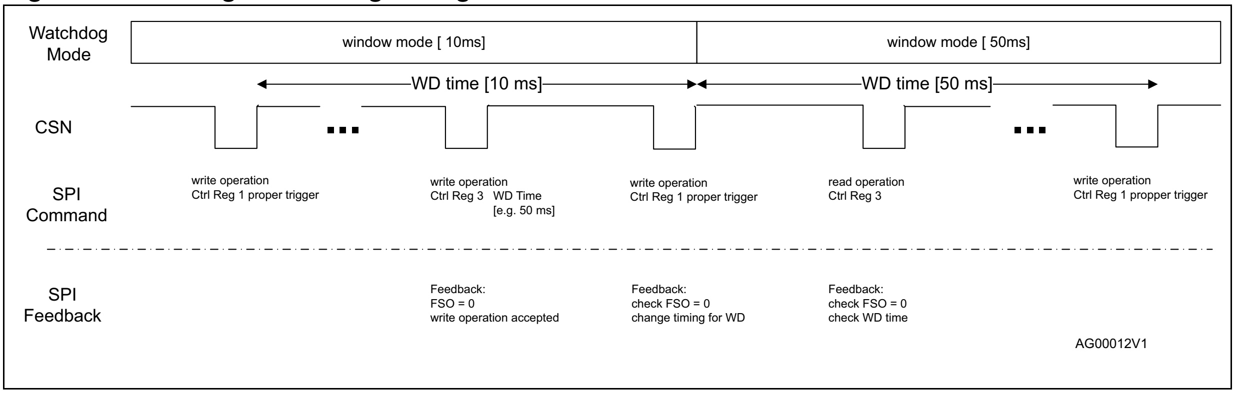


Figure 13. Change watchdog timing within window mode



If the device is in fail-safe mode, the control registers are locked for writing. To change the watchdog timing out of fail-safe mode, first the fail-safe condition must be solved, respective confirmed from the microcontroller. Afterwards the new watchdog timing can be programmed using the sequence from *Figure 14*. Since the actions to remove, a fail-safe condition can differ from the root cause of the fail safe the following diagram shows the general procedure how to change the watchdog timing out of fail-safe mode. *Figure 15* shows the procedure to change watchdog timing with a previous watchdog failure, since this is a special fail-safe scenario.

Figure 14. General procedure to change watchdog timing out of fail safe mode

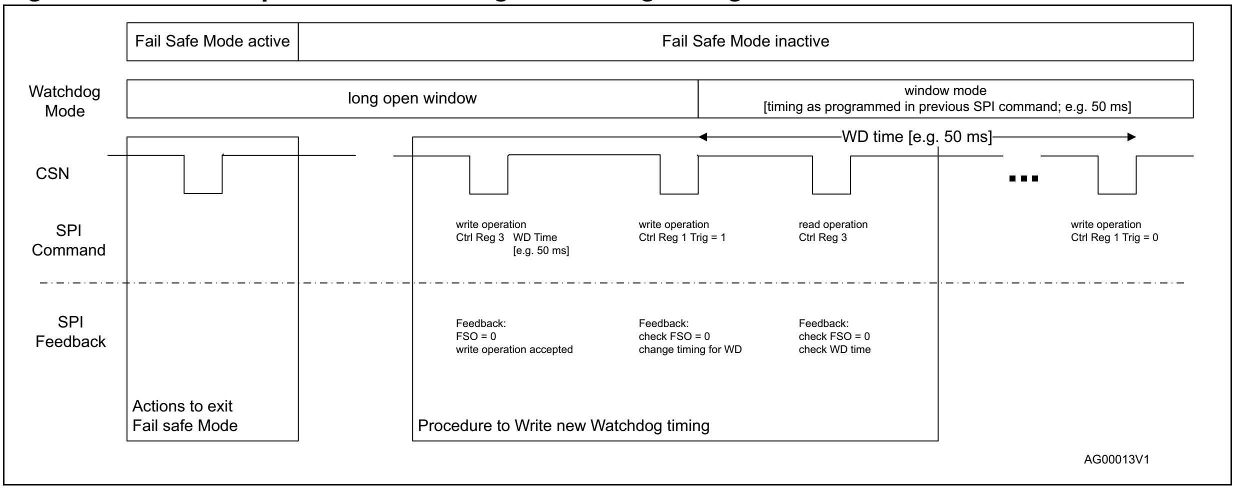
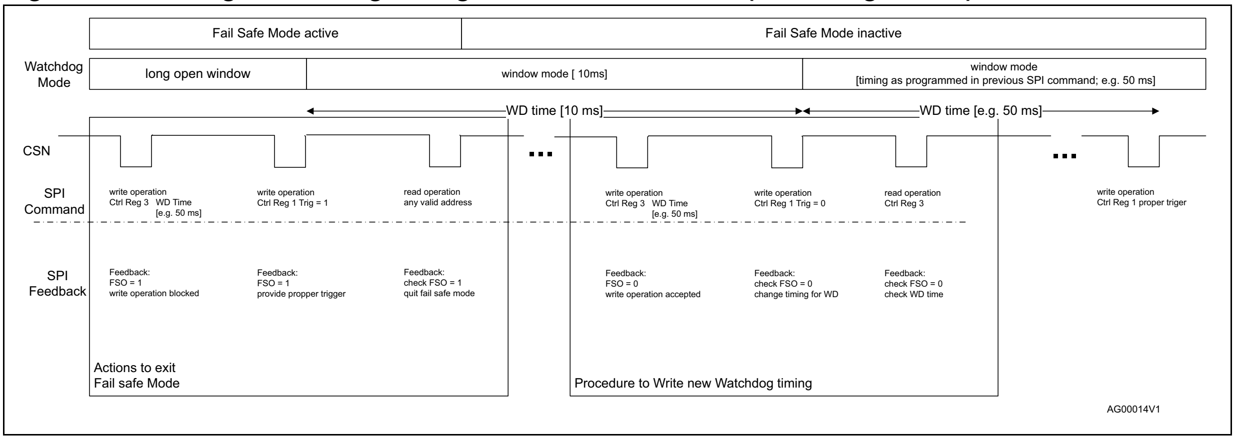


Figure 15. Change watchdog timing out of fail safe mode (watchdog failure)



2.5 Fail safe mode

2.5.1 Single failures

L99PM62GXP enters fail safe mode in case of:

- Watchdog failure
- V_1 turn on failure
  - V_1 short ($V_1 < V_{1fail}$ for $t > t_{V1short}$)
- V_1 undervoltage ($V_1 <$ Vrth for $t > t_{UV1}$)
- Thermal shutdown TSD2
- SPI failure
  - DI stuck to GND or V_{CC} (SPI frame = '00 00 00' or 'FF FF FF')