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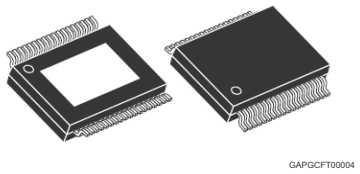
L99PM72PXP

Advanced power management system IC with embedded LIN and high speed CAN transceiver supporting CAN Partial Networking

Datasheet – production data

Features

- Two 5 V voltage regulators for microcontroller and peripheral supply
- No electrolytic capacitor required on regulator outputs
- Ultra low quiescent current in standby modes
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog and fail safe output
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Advanced high speed CAN transceiver (ISO 11898-2/-5 and SAE J2284 compliant) with local failure and bus failure diagnosis and selective wake-up functionality according to ISO 11898-6
- Complete 3 channel contact monitoring interface with programmable cyclic sense functionality
- Programmable periodic system wake-up feature
- ST SPI interface for mode control and diagnosis
- 5 fully protected high-side drivers with internal 4-channel PWM generator
- 2 low-side drivers with active Zener clamping
- 4 Internal PWM timers
- 2 operational amplifiers with rail-to-rail outputs (V_S) and low voltage inputs
- Temperature warning and thermal shutdown



PowerSSO-36

Applications

- Automotive ECU's such as door zone and body control modules description

Description

The L99PM72PXP is a power management system IC providing electronic control units with enhanced system power supply functionality including various standby modes as well as LIN and HS CAN physical communication layers. It contains two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake up capability.

In addition, five high-side drivers, two low-side drivers and two operational amplifiers increase the system integration level.

The ST standard SPI Interface (3.0) allows control and diagnosis of the device and enables generic software development.

Table 1. Device summary

Package	Order code	
	Tube	Tape and reel
PowerSSO-36	L99PM72PXP	L99PM72PXPTR

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1 Block diagram and pin description

Figure 1. Block diagram

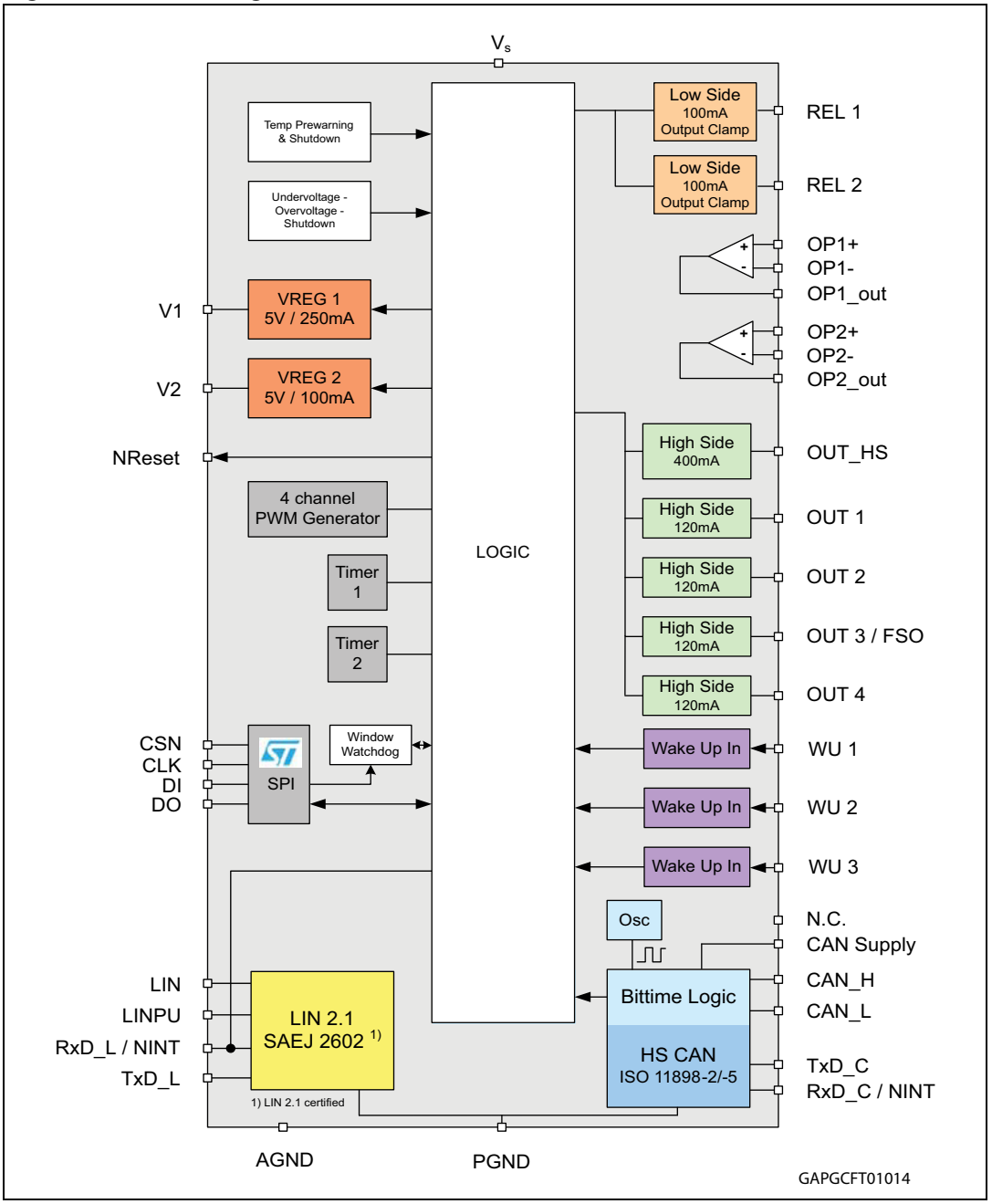


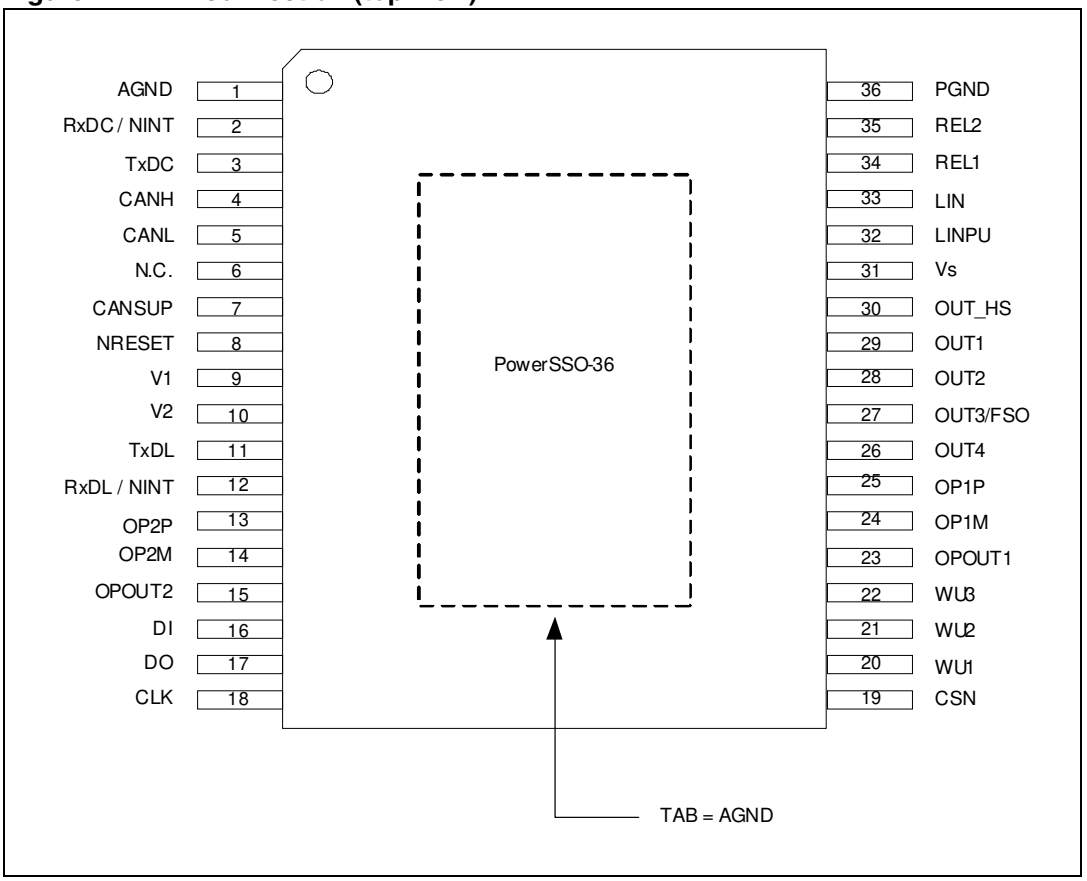
Table 2. Pin definitions and functions

Pin	Symbol	Function
1	AGND	Analog ground
2	RxDC/NINT	RxDC -> CAN receive data output NINT -> indicates remote CAN wake-up events in Active Mode (transceiver in TRX_STBY; CAN_ACT = 0)
3	TxDC	CAN transmit data Input
4	CANH	CAN high level voltage I/O
5	CANL	CAN low level voltage I/O
6	N.C.	TBC
7	CANSUP	CAN supply input; to allow external CAN supply from V_1 or V_2 regulator.
8	NRESET	N_{reset} output to microcontroller; Internal pull-up of typ. 100 KΩ (reset state = LOW)
9	V1	Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver
10	V2	Voltage regulator 2 output: 5 V supply for external loads (IR receiver, potentiometer, sensors) or CAN transceiver. V_2 is protected against reverse supply.
11	TxDL	LIN transmit data input
12	RxDL/NINT	RxDL -> LIN receive data output NINT -> indicates local/remote wake-up events except CAN wake-up in Active Mode provides a programmable timer interrupt signal
13	OP2+	Non inverting input of operational amplifier 2
14	OP2-	Inverting input of operational amplifier 2
15	OP2_OUT	Output of operational amplifier 2
16	DI	SPI: serial data input
17	DO	SPI: serial data output
18	CLK	SPI: serial clock input
19	CSN	SPI: chip select not input
20…22	WU1…3	Wake-up Inputs 1…3: Input pins for static or cyclic monitoring of external contacts
23	OP1_OUT	Output of operational amplifier 1
24	OP1-	Inverting input of operational amplifier 1
25	OP1+	Non inverting input of operational amplifier 1
26	OUT4	High side driver output (7Ω, typ)
27	OUT3/FSO	Configurable as: – High-side driver output (7Ω, typ) – Fail safe output pin (default)
28	OUT2	High side driver output (7Ω, typ)
29	OUT1	High side driver output (7Ω, typ)
30	OUT_HS	High side driver (1 Ω, typ)

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
31	V_S	Power supply voltage
32	LINPU	High side driver output to switch off LIN master pull up resistor
33	LIN	LIN bus line
34	REL1	Low side driver output (2 Ω typ)
35	REL2	Low side driver output (2 Ω typ)
36	PGND	Power ground (REL1/2, LIN and CAN GND), to be connected to AGND externally

Figure 2. Pin connection (top view)



2 Detailed description

2.1 Voltage regulators

The L99PM72PXP contains two independent and fully protected low drop voltage regulators, which are designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors ≥ 220 nF.

2.1.1 Voltage regulator: V_1

The V_1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current and is mainly intended for supply of the system microcontroller. The V_1 regulator is embedded in the power management and Fail_safe functionality of the device and operates according to the selected operating mode.

It can be used to supply the internal HS CAN Transceiver via the CANSUP pin externally. In case of a short circuit condition on the CAN bus, the output current of the transmitter is limited to 100 mA and the transceiver is turned off in order to ensure continued supply of the microcontroller.

In addition the regulator V_1 drives the L99PM72PXP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors ≥ 220 nF.

If the device temperature exceeds the TSD1 threshold, all outputs (OUTx, RELx, V2, LIN) are deactivated except V_1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2 > TSD1), also V_1 is deactivated (see *Figure 23: Thermal shutdown protection and diagnosis*). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1 sec. During this time, all other wakeup sources (CAN, LIN, WU1...3 and wake up of µC by timer) are disabled. After 1 sec, the voltage regulator tries to restart automatically. If the restart fails 7 times, within one minute, without clearing and thermal shutdown condition still exists, the L99PM72PXP enters the Forced $V_{Bat\_standby}$ Mode.

In case of short to GND at "V_1" after initial turn on (V_1 < 2 V for t > $t_{V1\ short}$) the L99PM72PXP enters the Forced $V_{Bat\_standby}$ Mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..3 or periodic wake by timer.

2.1.2 Voltage regulator: V_2

The voltage regulator V_2 can supply additional 5 V loads (e.g. logic components or the integrated HS CAN transceiver or external loads such as sensors or potentiometers. The maximum continuous load current is 100 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.1.3 Increased output current capability for voltage regulator V_2

For applications, which require high output currents, the output current capability of the regulator can be increased my means of the integrated operational amplifiers and an external pass transistor.

Figure 3. Voltage source with external PNP

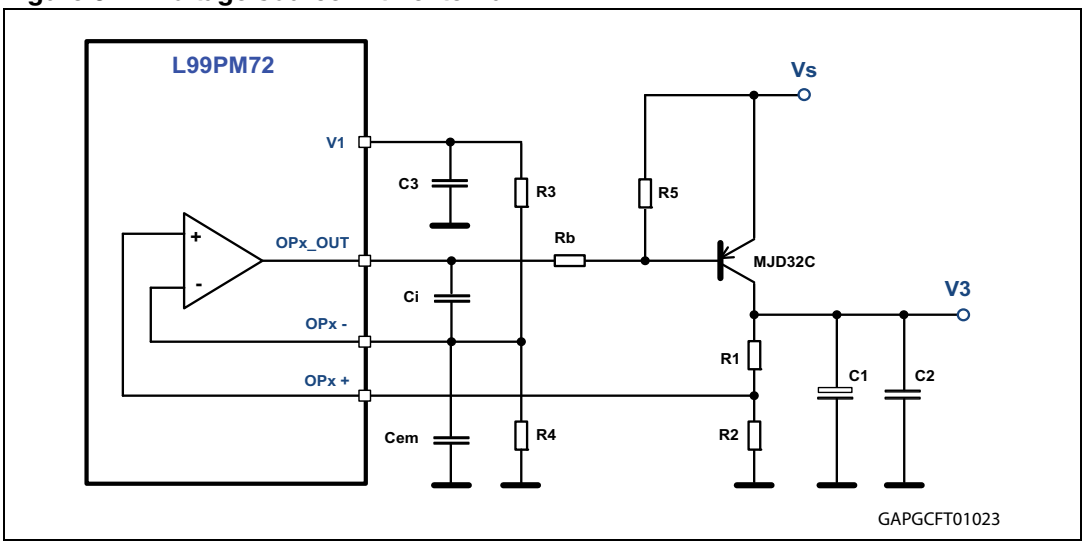


Figure 4. Voltage source with external PNP and current limitation

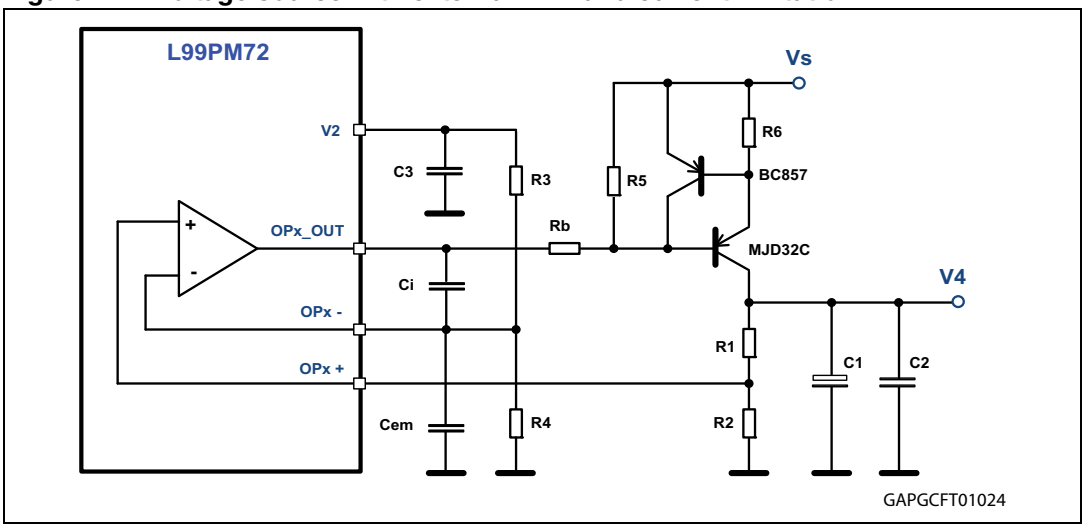


Figure 3 shows a possible configuration with a PNP pass element using Voltage Regulator 2 to provide the voltage reference for the regulated output voltage V3.

The V_S operating range for this circuit is 5.5 V to 18 V. It is important respect the input common mode range specified for the operational amplifiers.

The output voltage V3 can be calculated using the following formula (for R3 = R4):

$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2}[V]$$

The circuit in *Figure 4* provides additional current limitation using an additional PNP transistor and R6, which allows setting the current limit.

Figure 5. Voltage source with external NPN

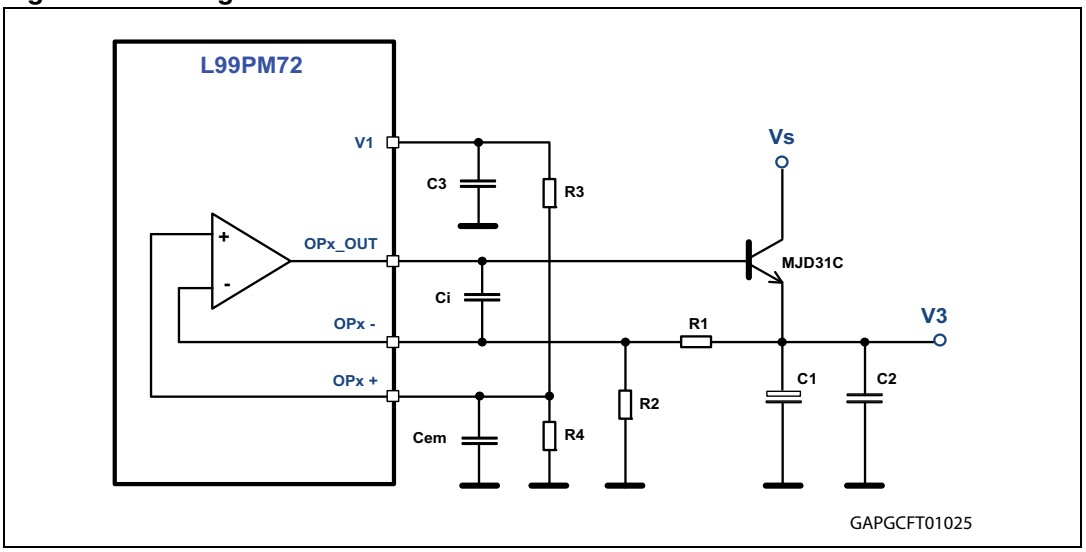


Figure 6. Voltage source with external NPN and current limitation

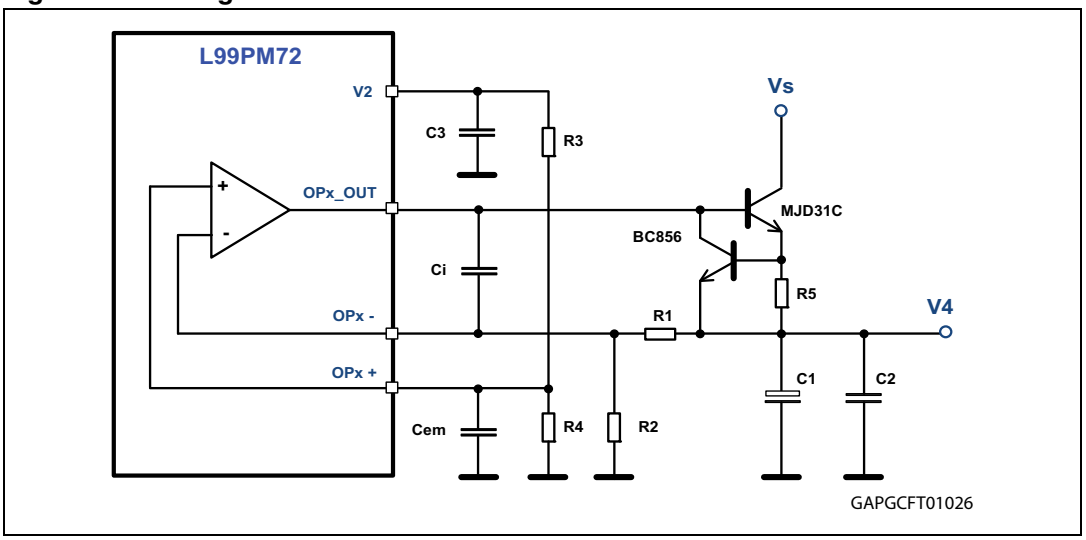


Figure 5 shows a possible configuration with an NPN pass element using Voltage Regulator 2 to provide the voltage reference for the regulated output voltage V3. This circuit requires fewer components compared to the configuration in *Figure 3* but has a limited V_S operating range (6 V to 18 V).

The output voltage V3 can be calculated using the following formula (for R3 = R4):

$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2}[V]$$

The circuit in *Figure 6* provides additional current limitation using an additional NPN transistor and R5 which allows setting the current limit.

Alternatively, Voltage Regulator 1 can be used to provide the 5 V reference for this topology. However, the additional current consumption through R3 and R4 has to be considered in $V_{1\_standby}$ Mode.

2.1.4 Voltage regulator failure

The V_1 and V_2 regulator output voltages are monitored.

In case of a drop below the V_1, V_2 - fail thresholds ($V_{1,2}$ < 2 V, typ for t > 2 µs), the $V_{1,2}$ -fail bits are latched. The fail bits can be cleared by a dedicated SPI command.

Short to ground detection

If 4 ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for $V_{1,2}$), the L99PM72PXP identifies a short circuit condition at the related regulator output and the regulator are switched off.

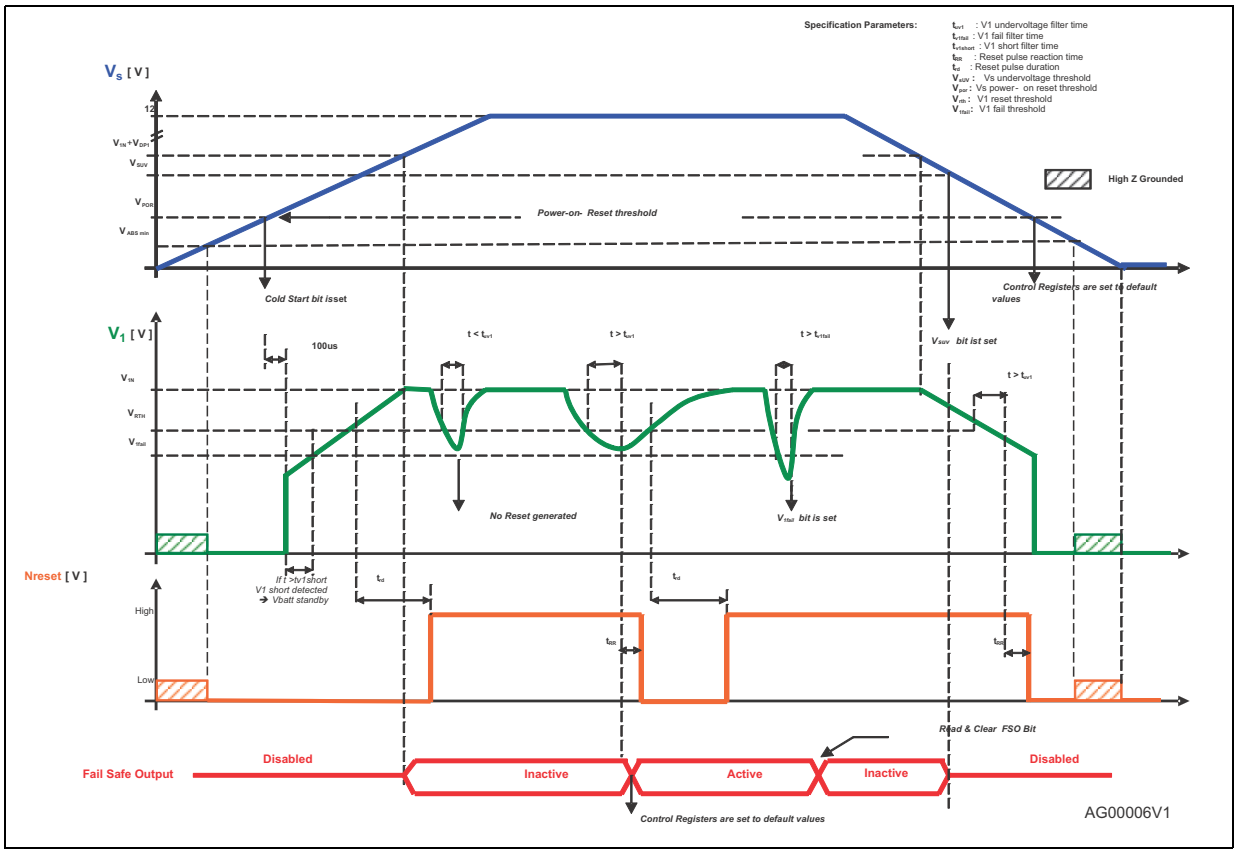
In case of V_1 short to GND failure the device enters $V_{Bat\_standby}$ mode automatically. Bits Forced VBAT TSD2/SHTV1 and V_{1_fail} were set.

In case of a V_2 short to GND failure the V_2 short and V_2 fail bit is set.

If the output voltage of the corresponding regulator once exceeded the $V_{1,2\_fail}$ thresholds the short to ground detection is disabled. If a short to ground condition occurs the regulator outputs switch of due to Thermal shutdown (V_1 at TSD2; V_2 at TSD1).

2.1.5 Voltage regulator behavior

Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions



2.2 Operating modes

The L99PM72PXP can be operated in 4 different operating modes:

- Active
- FLASH
- $V_{1\_standby}$
- $V_{Bat\_standby}$

A cyclic monitoring of wake-up inputs and a periodic interrupt / wake-up by timer is available in stand-by modes.

2.2.1 Active Mode

All functions are available and the device is controlled by the ST SPI Interface.

2.2.2 Flash Mode

To program the system microcontroller via LIN or HS CAN bus signals, the device can be operated in LIN Flash Mode or CAN Flash Mode where the internal watchdog is disabled.

Moreover, in Flash Mode the DO-output is a test output and cannot be used for device communication. All other device features in Flash Mode are available as in Active Mode.

The CAN-Receiver is enabled in CAN Flash Mode by default; the CAN Transmitter has to be enabled by setting the CAN_ACT bit to '1'.

A transition from Flash Modes to $V_{1\_standby}$ or $V_{bat\_standby}$ is not possible.

The modes can be entered by applying an external voltage at the respective pin:

- $V_{TxDL} \geq V_{flash}$ (CAN Flash Mode)
- $V_{TxDC} \geq V_{flash}$ (LIN Flash Mode)

At exit from Flash Modes ($V_{TxD} < V_{flash}$) no N_{Reset} pulse is generated and the watchdog starts with a long open window.

Note: Setting both TxDL and TxDC to high voltage levels (> V_{flash}) is not allowed Communication at the respective TxD pin is not possible

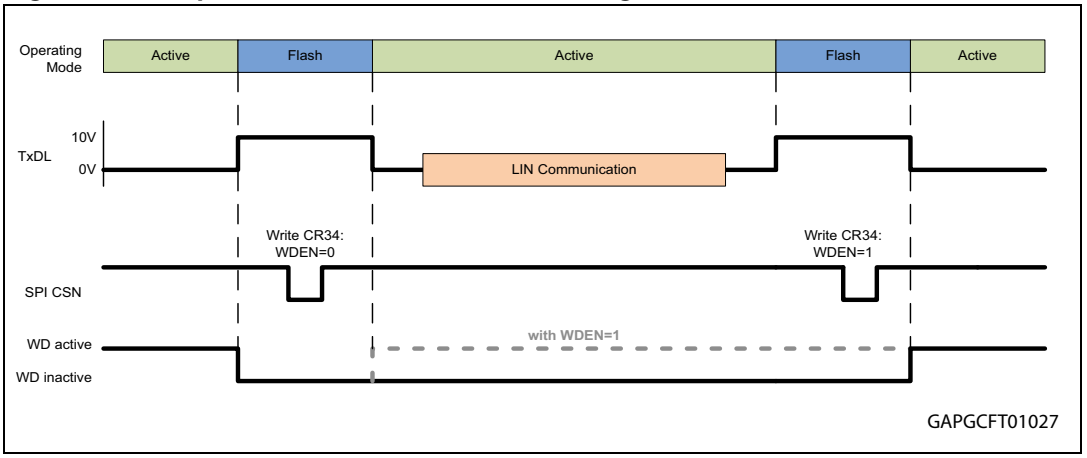
2.2.3 SW-Debug Mode

To allow software debugging, the watchdog can be deactivated by setting CR34: WDEN = 0.

Write access to this bit is only possible during CAN Flash Mode in order to prevent accidental deactivation of the watchdog. After setting the WDEN bit the CAN Flash Mode can be left ($V_{TxDL} < V_{Flash}$) and the Watchdog remains deactivated (see *Figure 8*)

In SW-Debug Mode, the full device functionality is available.

Figure 8. Sequence to enter and exit SW Debug Mode



2.2.4 $V_{1\_standby}$ mode

The transition from Active Mode to $V_{1\_standby}$ mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 (V_1) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the I_{CMP} current threshold. At this transition, the L99PM72PXP also deactivates the internal watchdog.

Relay outputs, LIN and CAN Transmitters are switched off in $V_{1\_standby}$ Mode. High side outputs and the V_2 regulator remain in the configuration programmed prior to the standby command.

A cyclic supply of external contacts and a synchronized monitoring of the contact state can be activated and configured by SPI.

In $V_{1\_standby}$ mode various wake-up sources can be individually programmed. Each wake-up event puts the device into Active Mode and forces the RxDL/NINT pin to a low level indicating the wake-up condition to the microcontroller.

After Power ON Reset (POR) all wake up sources are activated by default except the periodic interrupt / wake timer.

With the interrupt timer the micro controller can be forced from 'stop' to 'run' after a programmable period. The RxDL/NINT pin is forced low after the timer is elapsed. The L99PM72PXP enters active mode and is awaiting a valid watchdog trigger.

Both internal timers can be used for this feature.

The interrupt timer (TINT) at pin RxDL/NINT is only available in $V_{1\_standby}$ mode.

Note: Inputs TxDL, TxDC must be at recessive (high) level and CSN must be at high level or at high impedance in order to achieve minimum standby current in $V_{1\_standby}$ Mode. Inputs DI and CLK must be at GND or at high impedance to achieve minimum standby current in $V_{1\_standby}$ Mode.

2.2.5 Interrupt

The interrupt signal (linked to RxDL/NINT) indicates a wake-up event from $V_{1\_standby}$ mode. In case of a wake-up by Wake-up Inputs, activity on LIN or CAN, SPI access or Timer-Interrupt the RxDL/NINT pin is pulled low for t = $t_{interrupt}$.

When CAN_ACT = 0 (during $V_{1\_standby}$ Mode or Active Mode) a WUP (SW_EN = 0) or a WUF (SW_EN = 1) generates an interrupt on RxDC/NINT to signalize CAN communication on the bus to the µC.

In case of a CAN communication timeout an interrupt at RxDC /NINT is generated and the CAN_TO flag is set.

In case of $V_{1\_standby}$ mode and ($I_{V1} > I_{CMP}$), the device remains in standby mode, the V_1 regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

Table 3. CAN wake-up signalization

Operating mode	Event	Wake-up transition to active	Status flag	Interrupt	Transceiver state
Active	WUP or WUF(1)	Not applicable	Wake_CAN WUP or WUP/WUF	RxDC	TRX_STBY
	CAN timeout		CAN_TO	RxDC	TRX_STBY
$V_{1\_standby}$	WUP or WUF(1)	Yes	Wake_CAN WUP or WUP/WUF	RxDL	TRX_STBY
	CAN timeout	No	CAN_TO	RxDC	TRX_STBY

Table 3. CAN wake-up signalization (continued)

Operating mode	Event	Wake-up transition to active	Status flag	Interrupt	Transceiver state
$V_{bat\_standby}$	WUP or WUP/WUF(2)	Yes	Wake_CAN WUP/WUF	Not applicable	TRX_STBY
	CAN timeout	Transition to TRX_SLEEP	CAN_TO		TRX_SLEEP

1. SW_EN = 0:
   — wake-up according ISO 11898-5 (WUP)
   — Flags: Wake_CAN, WUP
   SW_EN = 1:
   — wake-up according ISO 11898-6 (WUP)
   — Flags: Wake_CAN, WUP, WUF (the WUP flag is set only if the received WUF also contained a WUP)
2. SW_EN = 0:
   — wake-up according ISO 11898-5 (on WUP)
   — Flags: Wake_CAN, WUP
   SW_EN = 1:
   — wake-up according ISO 11898-6 (on WUP/WUF combination)
   — After the reception of a wake-up pattern (WUP) the CAN Enhanced Voltage Biasing is turned on until a CAN timeout is detected
   — Flags: Wake_CAN, WUP, WUF

2.2.6 $V_{Bat\_standby}$ mode

The transition from Active Mode to $V_{Bat\_standby}$ mode is initiated by an SPI command.

In $V_{Bat\_standby}$ Mode, the V_1 voltage regulator, relay outputs, LIN and CAN Transmitters are switched off. High side Outputs and the V_2 Regulator remain in the configuration programmed prior to the standby command.

In $V_{Bat\_standby}$ mode the current consumption of the L99PM72PXP is reduced to a minimum level.

An N_{Reset} pulse is generated upon wake-up from $V_{bat\_standby}$ Mode.

Note: Inputs TXDL, TXDC and CSN must be terminated to GND in $V_{bat\_standby}$ to achieve minimum standby current.
This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V_1 is pulled to GND).

2.2.7 Wake up from Standby Modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 4. Wake up from Standby Modes

Wake up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI Selective Wake-up can be configured by SPI
Level change of WU1 - 3	Can be individually configured or disabled by SPI

Table 4. Wake up from Standby Modes (continued)

Wake up source	Description
$I_{V1} > I_{CMP}$	Device remains in $V_{1\_standby}$ mode but watchdog is enabled (If $I_{CMP} = 0$) and the V_1 regulator goes into High Current Mode (Increased Current Consumption). No interrupt is generated.
Timer Interrupt / Wake up of µC by TIMER	programmable by SPI – $V_{1\_standby}$ Mode: device wakes up and Interrupt signal is generated at RxDL/NINT when programmable timeout has elapsed – $V_{Bat\_standby}$ Mode: device wakes up, V_1 regulator is turned on and N_{Reset} signal is generated when programmable timeout has elapsed
SPI Access	Always active (except in $V_{Bat\_standby}$ mode) Wake up event: CSN is low and first rising edge on CLK

To prevent the system from a deadlock condition (no wake up possible) a configuration where the periodic timer interrupt and wake up by LIN and HS CAN are disabled, is not allowed. The default configuration is entered for all wake-up sources in case of such an invalid setting.

All wake-up events from $V_{1\_standby}$ mode (except $I_{V1} > I_{CMP}$) are indicated to the microcontroller by a low-pulse (duration: 56 µs) at RxDL/NINT or RxDC/NINT (see *Table 3: CAN wake-up signalization*)

Wake-up from $V_{1\_standby}$ by SPI Access might be used to check the interrupt service handler.

2.2.8 Wake up inputs

The de-bounced digital inputs WU1...WU3 can be used to wake up the L99PM72PXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64µs is implemented at WU1-3. The filter is started when the input voltage passes the specified threshold.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic sense functionality is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer 1 or Timer 2 (see *Section 2.2.9*). The input signal is filtered with a filter time of 16 µs after a programmable delay (80 µs or 800 µs) according to the configured Timer On-time. A wake-up is processed if the status has changed versus the previous cycle.

The Outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode the input filter timing and input filter delay (*WUx_filt* in control register 2) must correspond to the setting of the High Side Output which supplies the external contact switches (OUTx in control register 0).

In Standby Mode, the inputs WU1-3 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external. In active mode the inputs have a pull down resistor.

In Active Mode, the input status can be read by SPI (Status Register 2). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense

configuration, the input status is updated according to the cyclic sense timing; therefore, reading the input status in this mode may not reflect the actual status).

2.2.9 Cyclic contact supply

In $V_{1\_standby}$ and $V_{Bat\_standby}$ modes, any high side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X s. The on-time is 10 ms resp. 20 ms: with X ∈ {1, 2, 3, 4s}

Timer 2: period is X ms. The on-time is 100 µs resp. 1 ms: with X ∈ {10, 20, 50, 200 ms}

Timer 1 and Timer 2 are re-started with every valid write command to CR3 (CSN low to high transition). The timers start with the off-phase.

2.2.10 Timer interrupt / wake-up of microcontroller by timer

During standby modes the cyclic wake up feature, configured via SPI, allows waking up the µC after a programmable timeout according to timer1 or timer 2.

From $V_{1\_standby}$ mode, the L99PM72PXP wakes up (after the selected timer has elapsed) and sends an interrupt signal (via RxDL/NINT pin) to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into $V_{1\_standby}$ after finishing its tasks.

From $V_{bat\_standby}$ mode, the L99PM72PXP wakes up (after the selected timer has elapsed), turns on the V_1 regulator and provides an N_{Reset} signal to the µC. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into $V_{bat\_standby}$ after finishing its tasks.

2.3 Functional overview (truth table)

Table 5. Functional overview (truth table)

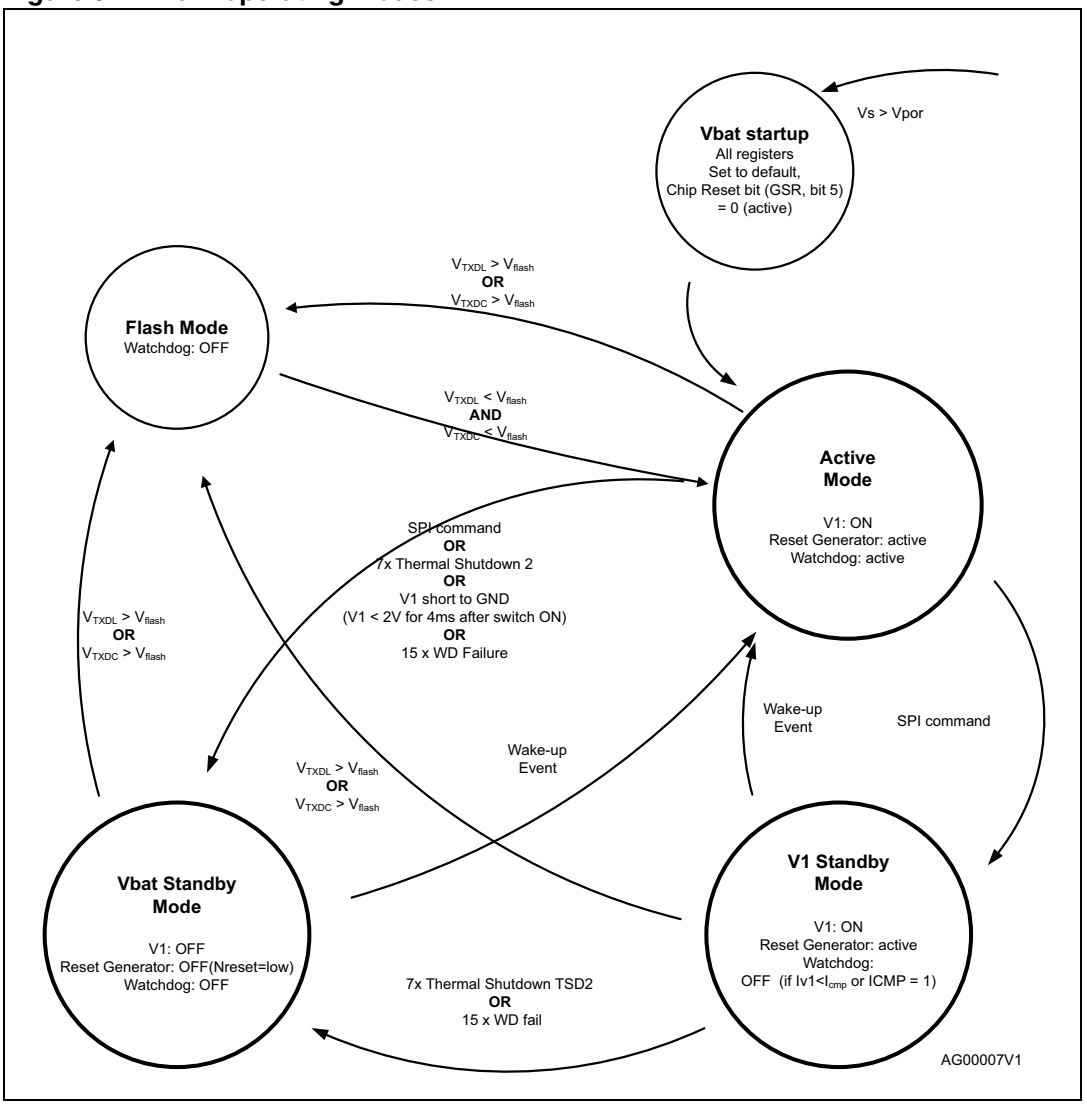
Function	Comments	Operating modes		
		Active Mode	$V_{1\_standby}$ static mode (cyclic sense)	$V_{Bat\_standby}$ static mode (cyclic sense)
Voltage regulator, V_1	VOUT=5V	On	On(1)	Off
Voltage regulator, V_2	VOUT=5V	On/ Off(2)	On(2) / Off	On(2) / Off
Reset generator		On	On	Off
Window watchdog	V_1 monitor	On	Off (ON: $I_{V1} > I_{CMP}$-threshold and $I_{CMP} = 0$)	Off
Wake up		Off	Active(3)	Active(3)
HS-cyclic supply	Oscillator time base	On / Off	On(2) / Off	On(2) / Off
Relay driver		On	Off	Off

Table 5. Functional overview (truth table) (continued)

Function	Comments	Operating modes		
		Active Mode	$V_{1\_standby}$ static mode (cyclic sense)	$V_{Bat\_standby}$ static mode (cyclic sense)
Operational amplifiers		On	Off	Off
LIN	LIN 2.1	On	Off(4)	Off(4)
HS_CAN		On / Off(5)	Off(4)	Off(4)
FSO (if configured by SPI), active by default	Fail safe output	OUT3/FSO OFF (6)	OUT3/FSO OFF(6)	OUT3/FSO OFF(6)
Oscillator		On	Off(7)	Off(7)
V_S-Monitor		On	(8)	(8)

1. Supply the processor in low current mode.
2. Only active when selected via SPI.
3. Unless disabled by SPI
4. The bus state is internally stored when going to standby mode. A change of bus state leads to a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI). Selective Wake functionality if enabled by SPI
5. After power-on, the HS CAN transceiver is in ‘CAN Trx Standby’ Mode. It is activated by SPI command (CAN_ACT = 1)
6. ON in Failsafe Condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
7. ON, if cyclic sense is enabled.
8. Cyclic activation = pulsed ON during cyclic sense

Figure 9. Main operating modes



2.4 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle: (10 ms, 50 ms, 100 ms, 200 ms)

In $V_{Bat\_standby}$ and Flash program modes, the watchdog circuit is automatically disabled. In $V_{1\_standby}$ mode a wake up by timer is programmable in order to wake up the µC (see *Section 2.2.10*). After wake-up, the Watchdog starts with a long open window. After serving the watchdog, the microcontroller may send the device back to $V_{1\_standby}$ mode.

After power-on or Standby mode, the watchdog is started with a long open window (65 ms nominal). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is processed when the CSN input becomes HIGH after the transmission of the SPI word.

Writing '1' to the watchdog trigger bit terminates the long open window and start the window watchdog (the timing is programmable by SPI). Subsequently, the micro controller has to

serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to *Figure 32*).

A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the V_1 regulator is switched off for 200 ms. If subsequently, 7 additional watchdog failures occur, the V_1 regulator is completely turned off and the device goes into $V_{Bat\_standby}$ mode until a wakeup occurs.

In case of a Watchdog failure, the outputs (RELx, OUTx, V2) are switched off and the device enters Fail_safe mode (i. e. all control registers are set to default values except the 'OUT3 control bit').

The following diagrams illustrate the Watchdog behavior of the L99PM72PXP. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of FLASH mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and flash mode.

Figure 10. Watchdog in normal operating mode (no errors)