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LA-ispPAC®-POWR1014/A Automotive Family

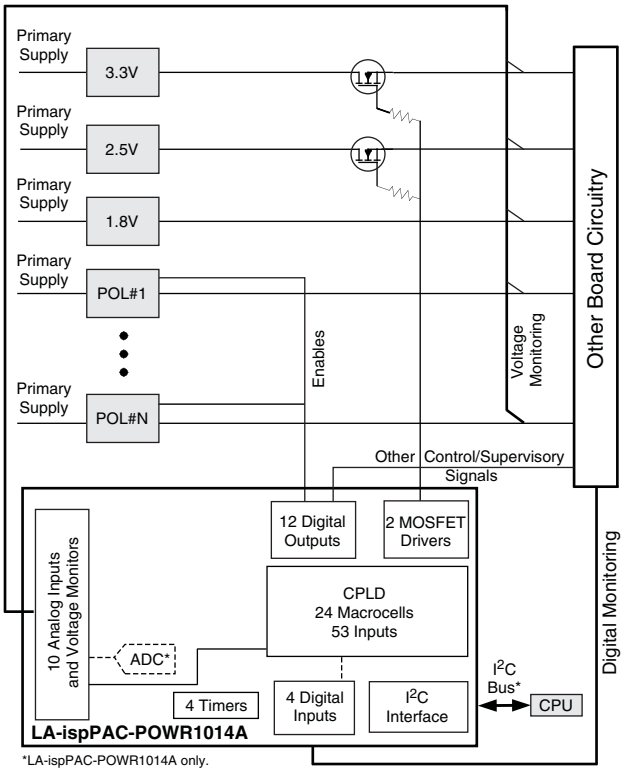
In-System Programmable Power Supply Supervisor, Reset Generator and Sequencing Controller

September 2013 **Data Sheet DS1018**

Features

- **Monitor and Control Multiple Power Supplies**
  - Simultaneously monitors up to 10 power supplies
  - Provides up to 14 output control signals
  - Programmable digital and analog circuitry
- **AEC-Q100 Tested and Qualified**
- **Embedded PLD for Sequence Control**
  - 24-macrocell CPLD implements both state machines and combinatorial logic functions
- **Embedded Programmable Timers**
  - Four independent timers
  - 32µs to 2 second intervals for timing sequences
- **Analog Input Monitoring**
  - 10 independent analog monitor inputs
  - Two programmable threshold comparators per analog input
  - Hardware window comparison
  - 10-bit ADC for I²C monitoring (LA-ispPAC-POWR1014A only)
- **High-Voltage FET Drivers**
  - Power supply ramp up/down control
  - Programmable current and voltage output
  - Independently configurable for FET control or digital output
- **2-Wire (I²C/SMBus™ Compatible) Interface**
  - Comparator status monitor
  - ADC readout
  - Direct control of inputs and outputs
  - Power sequence control
  - Only available with LA-ispPAC-POWR1014A
- **3.3V Operation, Wide Supply Range 2.8V to 3.96V**
  - Automotive temperature range: -40°C to +105°C
  - 48-pin TQFP package, lead-free option
- **Multi-Function JTAG Interface**
  - In-system programming
  - Access to all I²C registers
  - Direct input control

Application Block Diagram



Description

Lattice's Power Manager II LA-ispPAC-POWR1014/A is a general-purpose power-supply monitor and sequence controller, incorporating both in-system programmable logic and in-system programmable analog functions implemented in non-volatile E²CMOS® technology. The LA-ispPAC-POWR1014/A device provides 10 independent analog input channels to monitor up to 10 power supply test points. Each of these input channels has two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. Four general-purpose digital inputs are also provided for miscellaneous control functions.

The LA-ispPAC-POWR1014/A provides 14 open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general-purpose logic interface functions. Two of these outputs (HVOUT1-HVOUT2) may be configured as high-voltage

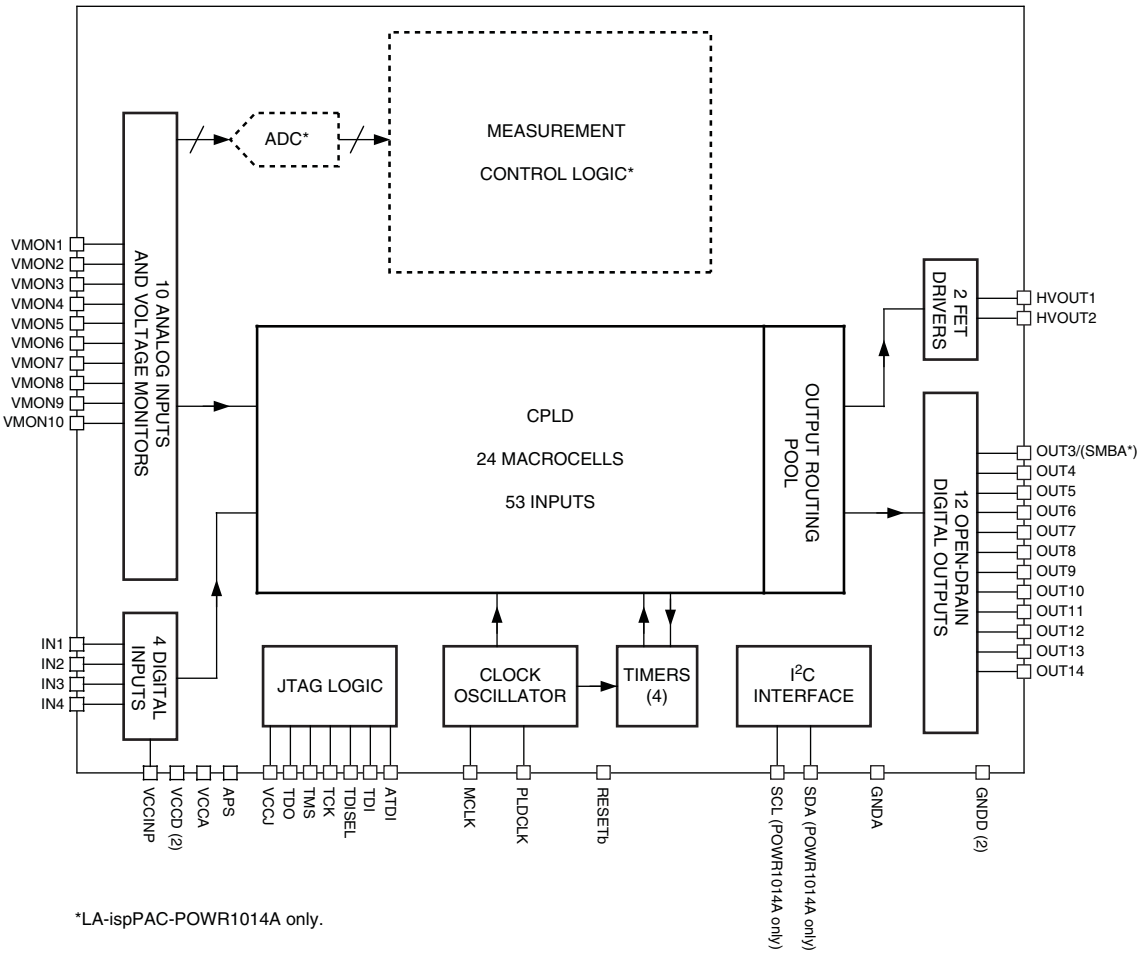
MOSFET drivers. In high-voltage mode these outputs can provide up to 8V for driving the gates of n-channel MOSFETs so that they can be used as high-side power switches controlling the supplies with a programmable ramp rate for both ramp up and ramp down.

The LA-ispPAC-POWR1014/A incorporates a 24-macrocell CPLD that can be used to implement complex state machine sequencing for the control of multiple power supplies as well as combinatorial logic functions. The status of all of the comparators on the analog input channels as well as the general purpose digital inputs are used as inputs by the CPLD array, and all digital outputs may be controlled by the CPLD. Four independently programmable timers can create delays and time-outs ranging from 32µs to 2 seconds. The CPLD is programmed using Logi-Builder™, an easy-to-learn language integrated into the PAC-Designer® software. Control sequences are written to monitor the status of any of the analog input channel comparators or the digital inputs.

The on-chip 10-bit A/D converter is used to monitor the V_{MON} voltage through the I^2C bus or JTAG interface of the LA-ispPAC-POWR1014A device.

The I^2C bus/SMBus interface allows an external microcontroller to measure the voltages connected to the V_{MON} inputs, read back the status of each of the V_{MON} comparator and PLD outputs, control logic signals IN2 to IN4 and control the output pins (LA-ispPAC-POWR1014A only). The JTAG interface can be used to read out all I^2C registers during manufacturing.

Figure 5-1. LA-ispPAC-POWR1014/A Block Diagram



Pin Descriptions

Number	Name	Pin Type	Voltage Range	Description
44	IN1	Digital Input	VCCINP[1, 2]	PLD Logic Input 1 Registered by MCLK
46	IN2	Digital Input	VCCINP[1, 3]	PLD Logic Input 2 Registered by MCLK
47	IN3	Digital Input	VCCINP[1, 3]	PLD Logic Input 3 Registered by MCLK
48	IN4	Digital Input	VCCINP[1, 3]	PLD Logic Input 4 Registered by MCLK
25	VMON1	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 1 Input
26	VMON2	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 2 Input
27	VMON3	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 3 Input
28	VMON4	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 4 Input
32	VMON5	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 5 Input
33	VMON6	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 6 Input
34	VMON7	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 7 Input
35	VMON8	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 8 Input
36	VMON9	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 9 Input
37	VMON10	Analog Input	-0.3V to 5.87V[4]	Voltage Monitor 10 Input
7, 31	GNDD[5]	Ground	Ground	Digital Ground
30	GNDA[5]	Ground	Ground	Analog Ground
41, 23	VCCD[6]	Power	2.8V to 3.96V	Core VCC, Main Power Supply
29	VCCA[6]	Power	2.8V to 3.96V	Analog Power Supply
45	VCCINP	Power	2.25V to 5.5V	VCC for IN[1:4] Inputs
20	VCCJ	Power	2.25V to 3.6V	VCC for JTAG Logic Interface Pins
24	APS[10]	Alternate Programming Supply	3.0V to 3.6V	Alternate E^2 Programming Supply; use only when the Device is Not Powered by V_{CCD} and V_{CCA}
15	HVOUT1	Open Drain Output[7]	0V to 8V	Open-Drain Output 1
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 1
14	HVOUT2	Open Drain Output[7]	0V to 8V	Open-Drain Output 2
		Current Source/Sink	12.5µA to 100µA Source 100µA to 3000µA Sink	High-voltage FET Gate Driver 2
13	SMBA_OUT3	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 3, (SMBUS Alert Active Low, LA-ispPAC-POWR1014A only).
12	OUT4	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 4
11	OUT5	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 5
10	OUT6	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 6
9	OUT7	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 7
8	OUT8	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 8
6	OUT9	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 9
5	OUT10	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 10
4	OUT11	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 11
3	OUT12	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 12
2	OUT13	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 13
1	OUT14	Open Drain Output[7]	0V to 5.5V	Open-Drain Output 14
40	RESETb[8]	Digital I/O	0V to 3.96V	Device Reset (Active Low) - Internal pull-up
42	PLDCLK	Digital Output	0V to 3.96V	250kHz PLD Clock Output (Tristate), CMOS Output - Internal pull-up

Pin Descriptions (Cont.)

Number	Name	Pin Type	Voltage Range	Description
43	MCLK	Digital I/O	0V to 3.96V	8MHz Clock I/O (Tristate), CMOS Drive - Internal Pull-up
21	TDO	Digital Output	0V to 5.5V	JTAG Test Data Out
22	TCK	Digital Input	0V to 5.5V	JTAG Test Clock Input
16	TMS	Digital Input	0V to 5.5V	JTAG Test Mode Select - Internal Pull-up
18	TDI	Digital Input	0V to 5.5V	JTAG Test Data In, TDISEL pin = 1 - Internal Pull-up
17	ATDI	Digital Input	0V to 5.5V	JTAG Test Data In (Alternate), TDISEL Pin = 0 - Internal Pull-up
19	TDISEL	Digital Input	0V to 5.5V	Select TDI/ATDI Input - Internal Pull-up
39	SCL[9, 11]	Digital Input	0V to 5.5V	I^2C Serial Clock Input (LA-ispPAC-POWR1014A Only)
38	SDA[9, 11]	Digital I/O	0V to 5.5V	I^2C Serial Data, Bi-directional Pin, Open Drain (LA-ispPAC-POWR1014A Only)

1. [IN1...IN4] are inputs to the PLD. The thresholds for these pins are referenced by the voltage on VCCINP. Unused INx inputs should be tied to GNDD.
2. IN1 pin can also be controlled through JTAG interface.
3. [IN2..IN4] can also be controlled through I^2C/SMBus interface (LA-ispPAC-POWR1014A only).
4. The VMON inputs can be biased independently from VCCA. Unused VMON inputs should be tied to GNDD.
5. GNDA and GNDD pins must be connected together on the circuit board.
6. VCCD and VCCA pins must be connected together on the circuit board.
7. Open-drain outputs require an external pull-up resistor to a supply.
8. The RESETb pin should only be used for cascading two or more LA-ispPAC-POWR1014/A devices.
9. These pins should be connected to GNDD (LA-ispPAC-POWR1014 device only).
10. The APS pin MUST be left floating when V_{CCD} and V_{CCA} are powered.
11. SCL should be tied high and SDA is don't care when I^2C registers are accessed through the JTAG interface.

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}	Core supply		-0.5	4.5	V
V_{CCA}	Analog supply		-0.5	4.5	V
V_{CCINP}	Digital input supply (IN[1:4])		-0.5	6	V
V_{CCJ}	JTAG logic supply		-0.5	6	V
APS	Alternate E^2 programming supply		-0.5	4	V
V_{IN}	Digital input voltage (all digital I/O pins)		-0.5	6	V
V_{MON}	V_{MON} input voltage		-0.5	6	V
V_{TRI}	Voltage applied to tri-stated pins	HVOUT[1:2]	-0.5	13.3	V
		OUT[3:14]	-0.5	6	V
$I_{SINKMAXTOTAL}$	Maximum sink current on any output			23	mA
T_S	Storage temperature		-65	150	°C
T_A	Ambient temperature		-65	125	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CCD}, V_{CCA}	Core supply voltage at pin		2.8	3.96	V
V_{CCINP}	Digital input supply for IN[1:4] at pin		2.25	5.5	V
V_{CCJ}	JTAG logic supply voltage at pin		2.25	3.6	V
APS	Alternate E^2 programming supply at pin	V_{CCD} and V_{CCA} powered	No connect Must be left floating		V
		V_{CCD} and V_{CCA} not powered	3.0	3.6	V
V_{IN}	Input voltage at digital input pins		-0.3	5.5	V
V_{MON}	Input voltage at V_{MON} pins		-0.3	5.9	V
V_{OUT}	Open-drain output voltage	OUT[3:14] pins	-0.3	5.5	V
		HVOUT[1:2] pins in open-drain mode	-0.3	13.0	V
T_{APROG}	Ambient temperature during programming		-40	85	°C
T_A[1]	Ambient temperature	Power applied	-40	105	°C
T_J	Junction temperature	Power applied	-40	110	°C

1. Device functionality guaranteed up to 125°C.

Analog Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}[1]	Core and analog supply current				20	mA
I_{CCINP}	V_{CCINP} supply current				5	mA
I_{CCJ}	JTAG supply current				1	mA
I_{CCPROG}	Core and analog supply current	During programming cycle			20	mA

1. Includes currents on V_{CCD} and V_{CCA} supplies.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input resistance		55	65	75	kΩ
C_{IN}	Input capacitance			8		pF
V_{MON} Range	Programmable trip-point range		0.075		5.867	V
V_Z Sense	Near-ground sense threshold		70	75	80	mV
V_{MON} Accuracy	Absolute accuracy of any trip-point[1]	-40<T_A<105°C		0.3	1.1	%
		-40<T_A<125°C			1.2	%
HYST	Hysteresis of any trip-point (relative to setting)			1		%

1. Guaranteed by characterization across V_{CCA} range, operating temperature, process.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP}	Gate driver output voltage	8V setting	7.6	8	8.4	V
		6V setting	5.7	6	6.3	
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software		12.5		µA
				25		
				50		
				100		
$I_{OUTSINK}$	Gate driver sink current (LOW state)	FAST OFF mode	1500	3000		µA
		Controlled ramp settings		100		
				250		
				500		

ADC Characteristics[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	ADC resolution			10		Bits
$T_{CONVERT}$	Conversion time	Time from I^2C request			100	µs
V_{IN}	Input range full scale	Programmable attenuator = 1	0		2.048	V
		Programmable attenuator = 3	0		5.9[2]	V
ADC Step Size	LSB	Programmable attenuator = 1		2		mV
		Programmable attenuator = 3		6		mV
Eattenuator	Error due to attenuator	Programmable attenuator = 3		+/- 0.1		%

1. LA-ispPAC-POWR1014A only.
2. Maximum voltage is limited by V_{MONX} pin (theoretical maximum is 6.144V).

ADC Error Budget Across Entire Operating Temperature Range[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
TADC Error	Total Measurement Error at Any Voltage[2]	Measurement Range 600 mV - 2.048V, Attenuator =1	-10	+/-4	10	mV
		Measurement Range Zero to 600mV, Attenuator = 1		+/-12		mV

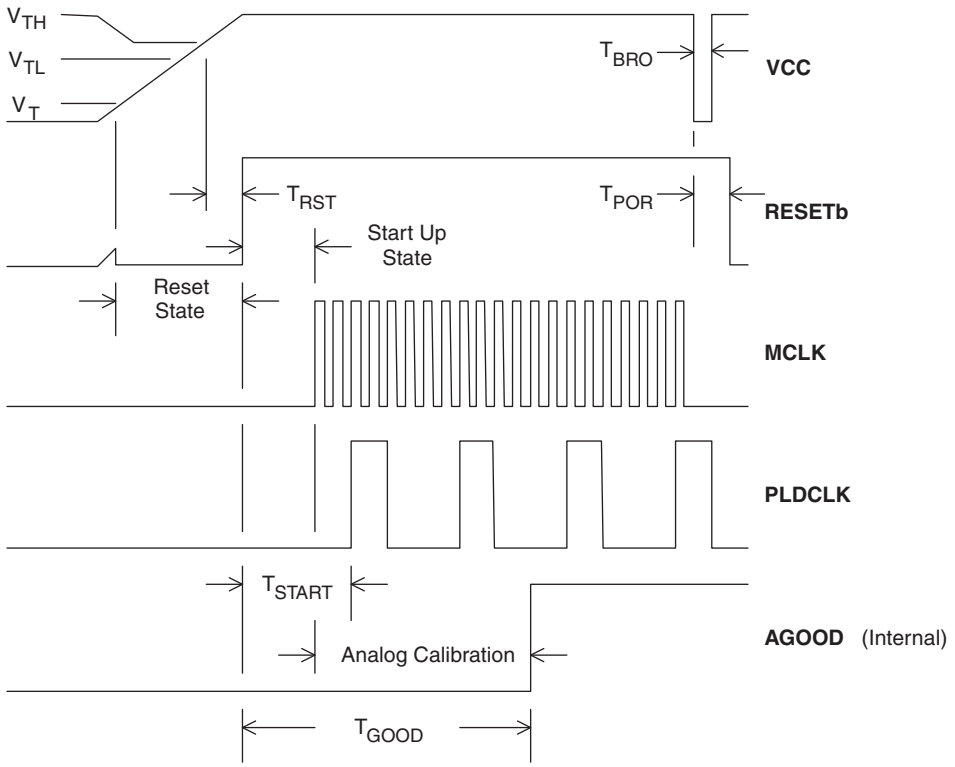
1. LA-ispPAC-POWR1014A only.
2. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specifications of the ADC.

Power-On Reset

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{RST}	Delay from V_{TH} to start-up state				100	µs
T_{START}	Delay from RESETb HIGH to PLDCLK rising edge			5	10	µs
T_{GOOD}	Power-on reset to valid VMON comparator output and AGOOD is true.				500	µs
T_{BRO}	Minimum duration brown out required to trigger RESETb		1		5	µs
T_{POR}	Delay from brown out to reset state.				11	µs
V_{TL}	Threshold below which RESETb is LOW[1]				2.3	V
V_{TH}	Threshold above which RESETb is HIGH[1]		2.7			V
V_T	Threshold above which RESETb is valid[1]		0.8			V
C_L	Capacitive load on RESETb for master/slave operation				200	pF

1. Corresponds to VCCA and VCCD supply voltages.

Figure 5-2. LA-ispPAC-POWR1014/A Power-On Reset



AC/Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Monitors						
t_{PD16}	Propagation delay input to output glitch filter OFF			16		µs
t_{PD64}	Propagation delay input to output glitch filter ON			64		µs
Oscillators						
f_{CLK}	Internal master clock frequency (MCLK)		7.6	8	8.4	MHz
f_{CLKEXT}	Externally applied master clock (MCLK)		7.2		8.8	MHz
f_{PLDCLK}	PLDCLK output frequency	f_{CLK} = 8MHz		250		kHz
Timers						
Timeout Range	Range of programmable timers (128 steps)	f_{CLK} = 8MHz	0.032		1966	ms
Resolution	Spacing between available adjacent timer intervals				13	%
Accuracy	Timer accuracy	f_{CLK} = 8MHz	-6.67		-12.5	%

Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL},I_{IH}	Input leakage, no pull-up/pull-down				+/-10	µA
$I_{OH-HVOUT}$	Output leakage current	HVOUT[1:2] in open drain mode and pulled up to 8V		35	100	µA
I_{PU}	Input pull-up current (TMS, TDI, TDISEL, ATDI, MCLK, PLDCLK, RESETb)			70		µA
V_{IL}	Voltage input, logic low[1]	TDI, TMS, ATDI, TDISEL, 3.3V supply			0.8	V
		TDI, TMS, ATDI, TDISEL, 2.5V supply			0.7	
		SCL, SDA			30% V_{CCD}	
		IN[1:4]			30% V_{CCINP}	
V_{IH}	Voltage input, logic high[1]	TDI, TMS, ATDI, TDISEL, 3.3V supply	2.0			V
		TDI, TMS, ATDI, TDISEL, 2.5V supply	1.7			
		SCL, SDA	70% V_{CCD}		V_{CCD}	
		IN[1:4]	70% V_{CCINP}		V_{CCINP}	
V_{OL}	HVOUT[1:2] (open drain mode),	I_{SINK} = 10mA			0.8	V
	OUT[3:14]	I_{SINK} = 20mA			0.8	
	TDO, MCLK, PLDCLK, SDA	I_{SINK} = 4mA			0.4	
V_{OH}	TDO, MCLK, PLDCLK	I_{SRC} = 4mA			V_{CCD} - 0.4	V
$I_{SINKTOTAL}$[2]	All digital outputs				67	mA

1. IN[1:4] referenced to V_{CCINP}; TDO, TDI, TMS, ATDI, TDISEL referenced to V_{CCJ}; SCL, SDA referenced to V_{CCD}.
2. Sum of maximum current sink from all digital outputs combined. Reliable operation is not guaranteed if this value is exceeded.

I²C Port Characteristics[1]

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I²C clock/data rate		100[2]		400[2]	kHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7	10	1.3	10	us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

1. Applies to LA-ispPAC-POWR1014A only.
2. If F_{I^2C} is less than 50kHz, then the ADC DONE status bit is not guaranteed to be set after a valid conversion request is completed. In this case, waiting for the $T_{CONVERT}$ minimum time after a convert request is made is the only way to guarantee a valid conversion is ready for readout. When F_{I2C} is greater than 50kHz, ADC conversion complete is ensured by waiting for the DONE status bit.

Timing for JTAG Operations

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{ISPEN}	Program enable delay time		10	—	—	µs
t_{ISPDIS}	Program disable delay time		30	—	—	µs
t_{HVDIS}	High voltage discharge time, program		30	—	—	µs
t_{HVDIS}	High voltage discharge time, erase		200	—	—	µs
t_{CEN}	Falling edge of TCK to TDO active		—	—	10	ns
t_{CDIS}	Falling edge of TCK to TDO disable		—	—	10	ns
t_{SU1}	Setup time		5	—	—	ns
t_H	Hold time		10	—	—	ns
t_{CKH}	TCK clock pulse width, high		20	—	—	ns
t_{CKL}	TCK clock pulse width, low		20	—	—	ns
f_{MAX}	Maximum TCK clock frequency		—	—	25	MHz
t_{CO}	Falling edge of TCK to valid output		—	—	10	ns
t_{PWV}	Verify pulse width		30	—	—	µs
t_{PWP}	Programming pulse width		20	—	—	ms

Figure 5-3. Erase (User Erase or Erase All) Timing Diagram

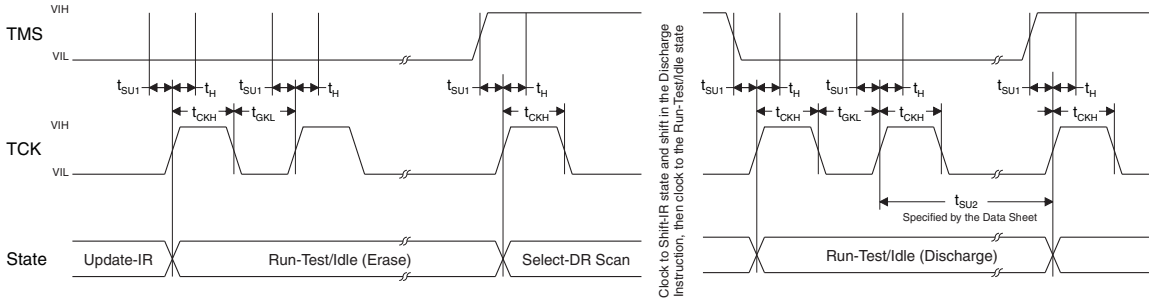


Figure 5-4. Programming Timing Diagram

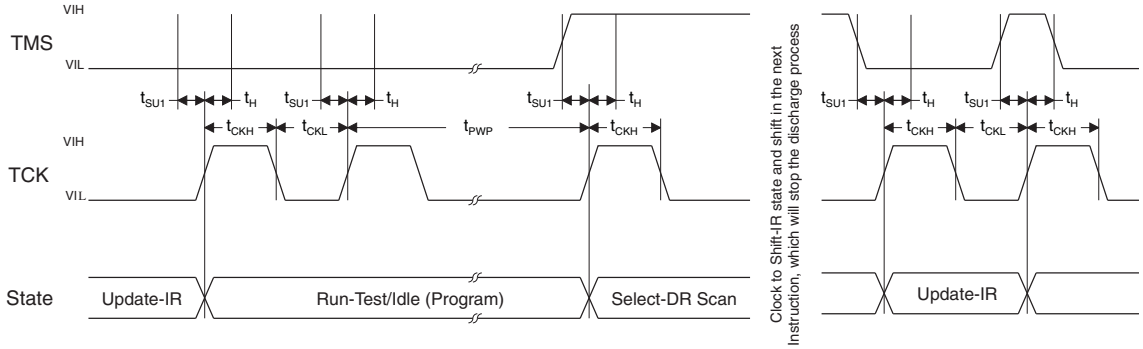


Figure 5-5. Verify Timing Diagram

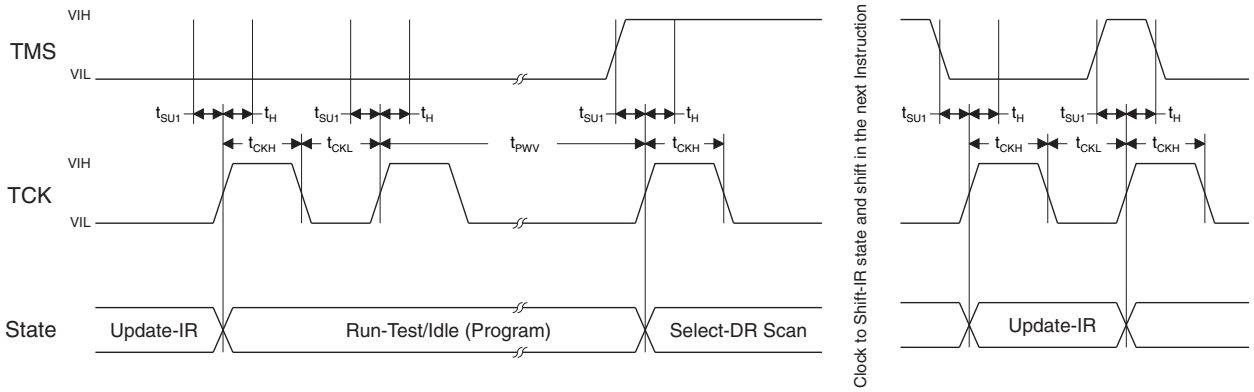
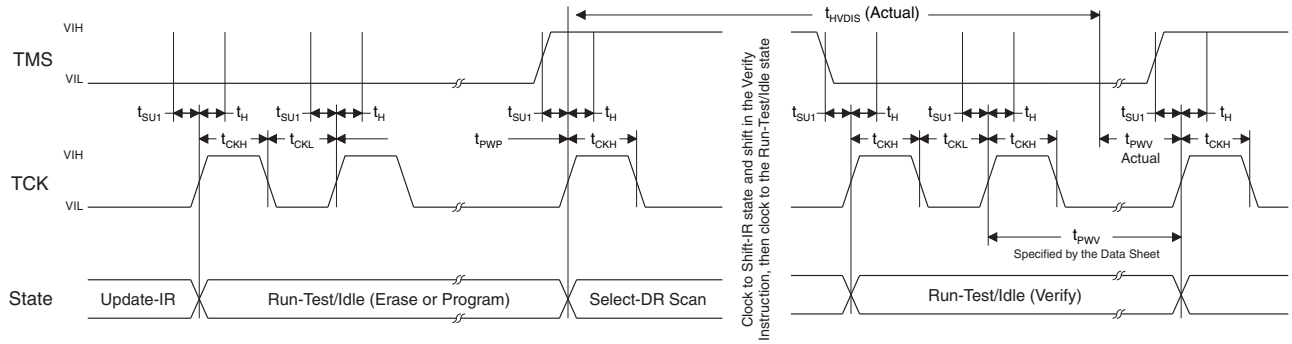


Figure 5-6. Discharge Timing Diagram



Theory of Operation

Analog Monitor Inputs

The LA-ispPAC-POWR1014/A provides 10 independently programmable voltage monitor input circuits as shown in Figure 5-7. Two individually programmable trip-point comparators are connected to an analog monitoring input. Each comparator reference has 372 programmable trip points over the range of 0.672V to 5.867V. Additionally, a 75mV 'zero-detect' threshold is selectable which allows the voltage monitors to determine if a monitored signal has dropped to ground level. This feature is especially useful for determining if a power supply's output has decayed to a substantially inactive condition after it has been switched off.

Figure 5-7. LA-ispPAC-POWR1014/A Voltage Monitors

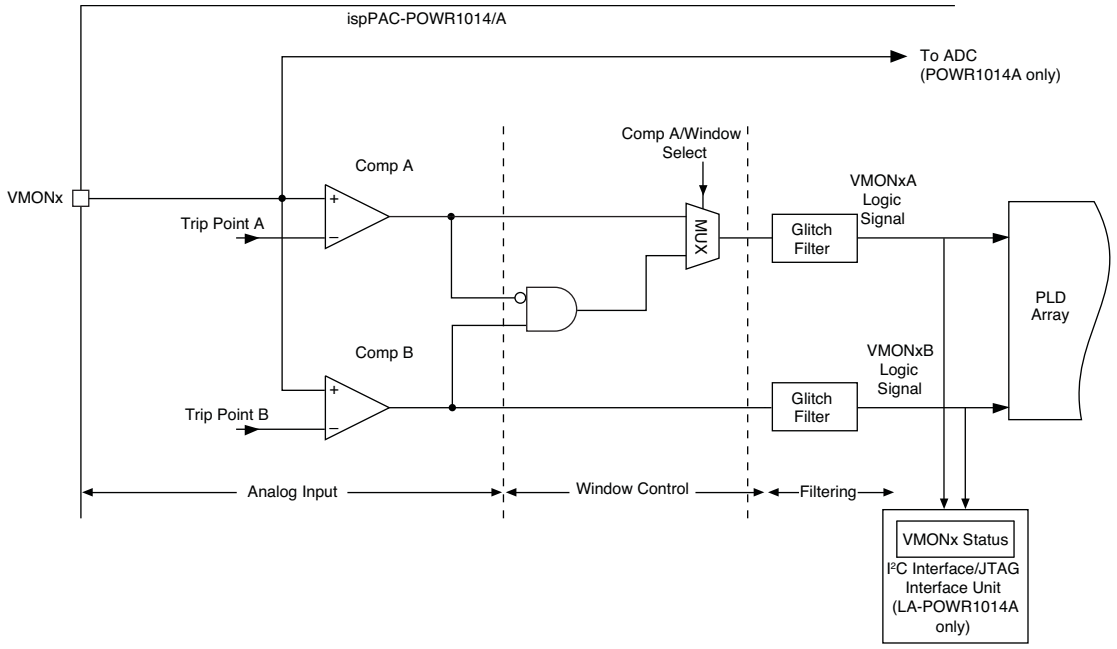


Figure 5-7 shows the functional block diagram of one of the 10 voltage monitor inputs - 'x' (where x = 1...10). Each voltage monitor can be divided into three sections: Analog Input, Window Control, and Filtering.

The voltage input is monitored by two individually programmable trip-point comparators, shown as CompA and CompB. Table 5-1 shows all trip points and the range to which any comparator's threshold can be set.

Each comparator outputs a HIGH signal to the PLD array if the voltage at its positive terminal is greater than its programmed trip point setting, otherwise it outputs a LOW signal.

A hysteresis of approximately 1% of the setpoint is provided by the comparators to reduce false triggering as a result of input noise. The hysteresis provided by the voltage monitor is a function of the input divider setting. Table 5-3 lists the typical hysteresis versus voltage monitor trip-point.

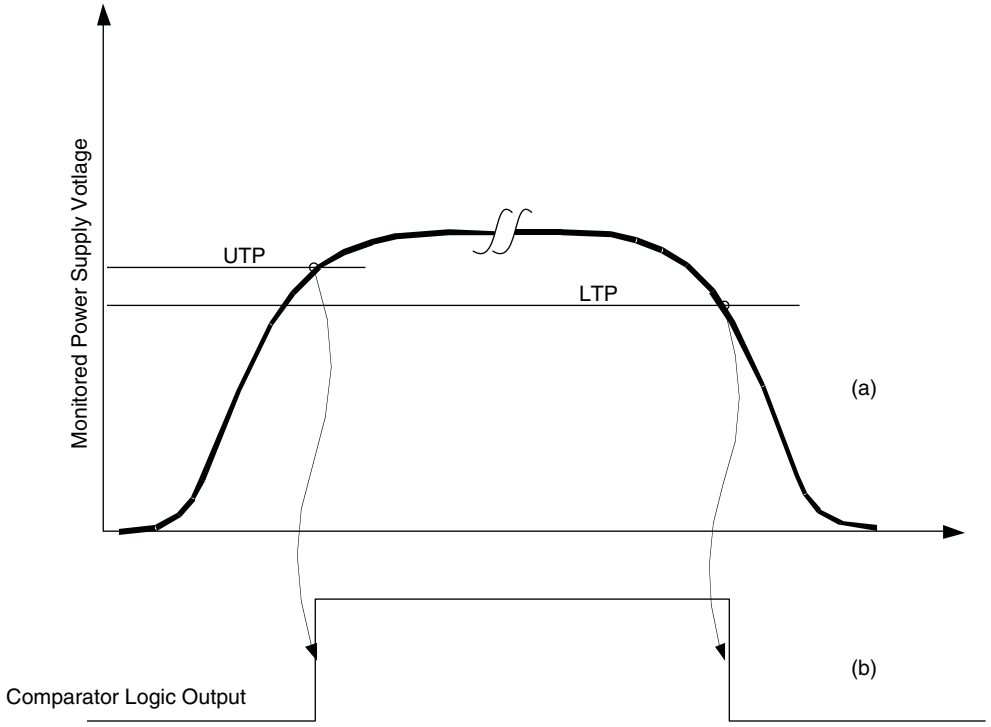
AGOOD Logic Signal

All the VMON comparators auto-calibrate immediately after a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signalled by an internally generated logic signal: AGOOD. All logic using the VMON comparator logic signals must wait for the AGOOD signal to become active.

Programmable Over-Voltage and Under-Voltage Thresholds

Figure 5-8 (a) shows the power supply ramp-up and ramp-down voltage waveforms. Because of hysteresis, the comparator outputs change state at different thresholds depending on the direction of excursion of the monitored power supply.

Figure 5-8. (a) Power Supply Voltage Ramp-up and Ramp-down Waveform and the Resulting Comparator Output, (b) Corresponding to Upper and Lower Trip Points



During power supply ramp-up the comparator output changes from logic 0 to 1 when the power supply voltage crosses the upper trip point (UTP). During ramp down the comparator output changes from logic state 1 to 0 when the power supply voltage crosses the lower trip point (LTP). To monitor for over voltage fault conditions, the UTP should be used. To monitor under-voltage fault conditions, the LTP should be used.

Tables 1 and 2 show both the under-voltage and over-voltage trip points, which are automatically selected in software depending on whether the user is monitoring for an over-voltage condition or an under-voltage condition.

Table 5-1. Trip Point Table Used For Over-Voltage Detection

Coarse Range Setting												
Fine Range Setting	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	0.806	0.960	1.143	1.360	1.612	1.923	2.290	2.719	3.223	3.839	4.926	5.867
2	0.802	0.955	1.137	1.353	1.603	1.913	2.278	2.705	3.206	3.819	4.900	5.836
3	0.797	0.950	1.131	1.346	1.595	1.903	2.266	2.691	3.190	3.799	4.875	5.806
4	0.793	0.945	1.125	1.338	1.586	1.893	2.254	2.677	3.173	3.779	4.849	5.775
5	0.789	0.940	1.119	1.331	1.578	1.883	2.242	2.663	3.156	3.759	4.823	5.745
6	0.785	0.935	1.113	1.324	1.570	1.873	2.230	2.649	3.139	3.739	4.798	5.714
7	0.781	0.930	1.107	1.317	1.561	1.863	2.219	2.634	3.122	3.719	4.772	5.683
8	0.776	0.925	1.101	1.310	1.553	1.853	2.207	2.620	3.106	3.699	4.746	5.653
9	0.772	0.920	1.095	1.303	1.544	1.843	2.195	2.606	3.089	3.679	4.721	5.622
10	0.768	0.915	1.089	1.296	1.536	1.833	2.183	2.592	3.072	3.659	4.695	5.592
11	0.764	0.910	1.083	1.289	1.528	1.823	2.171	2.578	3.055	3.639	4.669	5.561
12	0.760	0.905	1.077	1.282	1.519	1.813	2.159	2.564	3.038	3.619	4.644	5.531
13	0.755	0.900	1.071	1.275	1.511	1.803	2.147	2.550	3.022	3.599	4.618	5.500
14	0.751	0.895	1.065	1.268	1.502	1.793	2.135	2.535	3.005	3.579	4.592	5.470
15	0.747	0.890	1.059	1.261	1.494	1.783	2.123	2.521	2.988	3.559	4.567	5.439
16	0.743	0.885	1.053	1.254	1.486	1.773	2.111	2.507	2.971	3.539	4.541	5.408
17	0.739	0.880	1.047	1.246	1.477	1.763	2.099	2.493	2.954	3.519	4.515	5.378
18	0.734	0.875	1.041	1.239	1.469	1.753	2.087	2.479	2.938	3.499	4.490	5.347
19	0.730	0.870	1.035	1.232	1.460	1.743	2.075	2.465	2.921	3.479	4.464	5.317
20	0.726	0.865	1.029	1.225	1.452	1.733	2.063	2.450	2.904	3.459	4.438	5.286
21	0.722	0.860	1.024	1.218	1.444	1.723	2.052	2.436	2.887	3.439	4.413	5.256
22	0.718	0.855	1.018	1.211	1.435	1.713	2.040	2.422	2.871	3.419	4.387	5.225
23	0.713	0.850	1.012	1.204	1.427	1.703	2.028	2.408	2.854	3.399	4.361	5.195
24	0.709	0.845	1.006	1.197	1.418	1.693	2.016	2.394	2.837	3.379	4.336	5.164
25	0.705	0.840	1.000	1.190	1.410	1.683	2.004	2.380	2.820	3.359	4.310	5.133
26	0.701	0.835	0.994	1.183	1.402	1.673	1.992	2.365	2.803	3.339	4.284	5.103
27	0.697	0.830	0.988	1.176	1.393	1.663	1.980	2.351	2.787	3.319	4.259	5.072
28	0.692	0.825	0.982	1.169	1.385	1.653	1.968	2.337	2.770	3.299	4.233	5.042
29	0.688	0.820	0.976	1.161	1.377	1.643	1.956	2.323	2.753	3.279	4.207	5.011
30	0.684	0.815	0.970	1.154	1.368	1.633	1.944	2.309	2.736	3.259	4.182	4.981
31	0.680	0.810	0.964	1.147	—	1.623	1.932	2.295	—	3.239	4.156	4.950
Low-V Sense	75mV											

Table 5-2. Trip Point Table Used For Under-Voltage Detection

Fine Range Setting	1	2	3	4	5	6	7	8	9	10	11	12
1	0.797	0.950	1.131	1.346	1.595	1.903	2.266	2.691	3.190	3.799	4.875	5.806
2	0.793	0.945	1.125	1.338	1.586	1.893	2.254	2.677	3.173	3.779	4.849	5.775
3	0.789	0.940	1.119	1.331	1.578	1.883	2.242	2.663	3.156	3.759	4.823	5.745
4	0.785	0.935	1.113	1.324	1.570	1.873	2.230	2.649	3.139	3.739	4.798	5.714
5	0.781	0.930	1.107	1.317	1.561	1.863	2.219	2.634	3.122	3.719	4.772	5.683
6	0.776	0.925	1.101	1.310	1.553	1.853	2.207	2.620	3.106	3.699	4.746	5.653
7	0.772	0.920	1.095	1.303	1.544	1.843	2.195	2.606	3.089	3.679	4.721	5.622
8	0.768	0.915	1.089	1.296	1.536	1.833	2.183	2.592	3.072	3.659	4.695	5.592
9	0.764	0.910	1.083	1.289	1.528	1.823	2.171	2.578	3.055	3.639	4.669	5.561
10	0.760	0.905	1.077	1.282	1.519	1.813	2.159	2.564	3.038	3.619	4.644	5.531
11	0.755	0.900	1.071	1.275	1.511	1.803	2.147	2.550	3.022	3.599	4.618	5.500
12	0.751	0.895	1.065	1.268	1.502	1.793	2.135	2.535	3.005	3.579	4.592	5.470
13	0.747	0.890	1.059	1.261	1.494	1.783	2.123	2.521	2.988	3.559	4.567	5.439
14	0.743	0.885	1.053	1.254	1.486	1.773	2.111	2.507	2.971	3.539	4.541	5.408
15	0.739	0.880	1.047	1.246	1.477	1.763	2.099	2.493	2.954	3.519	4.515	5.378
16	0.734	0.875	1.041	1.239	1.469	1.753	2.087	2.479	2.938	3.499	4.490	5.347
17	0.730	0.870	1.035	1.232	1.460	1.743	2.075	2.465	2.921	3.479	4.464	5.317
18	0.726	0.865	1.029	1.225	1.452	1.733	2.063	2.450	2.904	3.459	4.438	5.286
19	0.722	0.860	1.024	1.218	1.444	1.723	2.052	2.436	2.887	3.439	4.413	5.256
20	0.718	0.855	1.018	1.211	1.435	1.713	2.040	2.422	2.871	3.419	4.387	5.225
21	0.713	0.850	1.012	1.204	1.427	1.703	2.028	2.408	2.854	3.399	4.361	5.195
22	0.709	0.845	1.006	1.197	1.418	1.693	2.016	2.394	2.837	3.379	4.336	5.164
23	0.705	0.840	1.000	1.190	1.410	1.683	2.004	2.380	2.820	3.359	4.310	5.133
24	0.701	0.835	0.994	1.183	1.402	1.673	1.992	2.365	2.803	3.339	4.284	5.103
25	0.697	0.830	0.988	1.176	1.393	1.663	1.980	2.351	2.787	3.319	4.259	5.072
26	0.692	0.825	0.982	1.169	1.385	1.653	1.968	2.337	2.770	3.299	4.233	5.042
27	0.688	0.820	0.976	1.161	1.377	1.643	1.956	2.323	2.753	3.279	4.207	5.011
28	0.684	0.815	0.970	1.154	1.368	1.633	1.944	2.309	2.736	3.259	4.182	4.981
29	0.680	0.810	0.964	1.147	1.360	1.623	1.932	2.295	2.719	3.239	4.156	4.950
30	0.676	0.805	0.958	1.140	1.352	1.613	1.920	2.281	2.702	3.219	4.130	4.919
31	0.672	0.800	0.952	1.133	-	1.603	1.908	2.267	-	3.199	4.105	4.889
Low-V Sense	75mV											

Table 5-3. Comparator Hysteresis vs. Trip-Point

Trip-point Range (V)		Hysteresis (mV)
Low Limit	High Limit	
0.672	0.806	8
0.800	0.960	10
0.952	1.143	12
1.133	1.360	14
1.346	1.612	17
1.603	1.923	20
1.908	2.290	24
2.267	2.719	28
2.691	3.223	34
3.199	3.839	40
4.105	4.926	51
4.889	5.867	61
75 mV		0 (Disabled)

The window control section of the voltage monitor circuit is an AND gate (with inputs: an inverted COMPA "ANDed" with COMPB signal) and a multiplexer that supports the ability to develop a 'window' function without using any of the PLD's resources. Through the use of the multiplexer, voltage monitor's 'A' output may be set to report either the status of the 'A' comparator, or the window function of both comparator outputs. The voltage monitor's 'A' output indicates whether the input signal is between or outside the two comparator thresholds. **Important:** This windowing function is only valid in cases where the threshold of the 'A' comparator is set to a value higher than that of the 'B' comparator. Table 5-4 shows the operation of window function logic.

Table 5-4. Voltage Monitor Windowing Logic

Input Voltage	Comp A	Comp B	Window (B and Not A)	Comment
V_{IN} < Trip-point B < Trip-point A	0	0	0	Outside window, low
Trip-point B < V_{IN} < Trip-point A	0	1	1	Inside window
Trip-point B < Trip-point A < V_{IN}	1	1	0	Outside window, high

Note that when the 'A' output of the voltage monitor circuit is set to windowing mode, the 'B' output continues to monitor the output of the 'B' comparator. This can be useful in that the 'B' output can be used to augment the windowing function by determining if the input is above or below the windowing range.

The third section in the LA-ispPAC-POWR1014/A's input voltage monitor is a digital filter. When enabled, the comparator output will be delayed by a filter time constant of 64 µs, and is especially useful for reducing the possibility of false triggering from noise that may be present on the voltages being monitored. When the filter is disabled, the comparator output will be delayed by 16µs. In both cases, enabled or disabled, the filters also provide synchronization of the input signals to the PLD clock. This synchronous sampling feature effectively eliminates the possibility of race conditions from occurring in any subsequent logic that is implemented in the LA-ispPAC-POWR1014/A's internal PLD logic.

The comparator status can be read from the I^2C interface or JTAG interface (LA-ispPAC-POWR1014A only). For details on the I^2C/JTAG interfaces, please refer to the I^2C/SMBUS Interface, and Accessing I^2C Registers Through JTAG sections of this data sheet.

VMON Voltage Measurement with the On-chip Analog to Digital Converter (ADC, LA-ispPAC-POWR1014A Only)

The LA-ispPAC-POWR1014A has an on-chip analog to digital converter that can be used for measuring the voltages at the VMON inputs.

Figure 5-9. ADC Monitoring VMON1 to VMON10

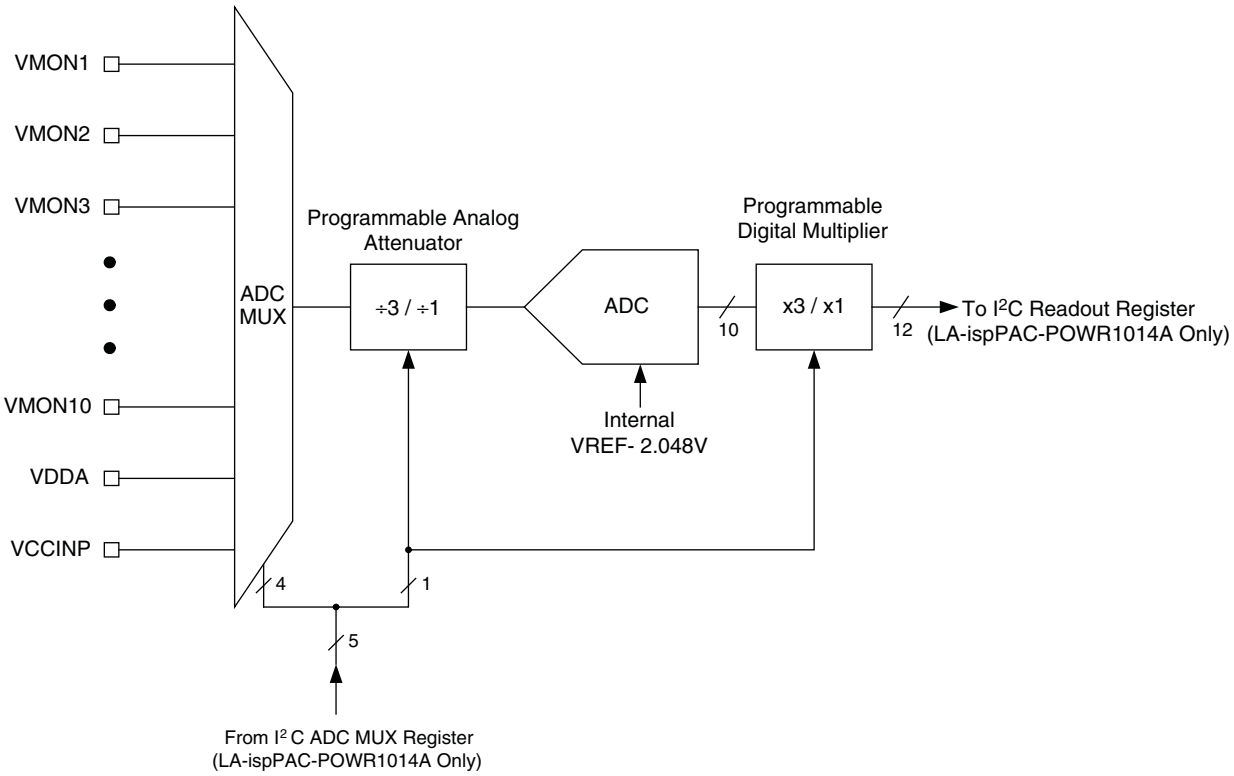


Figure 5-9 shows the ADC circuit arrangement within the LA-ispPAC-POWR1014A device. The ADC can measure all analog input voltages through the multiplexer, ADC MUX. The programmable attenuator between the ADC mux and the ADC can be configured as divided-by-3 or divided-by-1 (no attenuation). The divided-by-3 setting is used to measure voltages from 0V to 6V range and divided-by-1 setting is used to measure the voltages from 0V to 2V range.

A microcontroller can place a request for any VMON voltage measurement at any time through the I²C bus (LA-ispPAC-POWR1014A only). Upon the receipt of an I²C command, the ADC will be connected to the I²C selected VMON through the ADC MUX. The ADC output is then latched into the I²C readout registers.

Calculation

The algorithm to convert the ADC code to the corresponding voltage takes into consideration the attenuation bit value. In other words, if the attenuation bit is set, then the 10-bit ADC result is automatically multiplied by 3 to calculate the actual voltage at that VMON input. Thus, the I²C readout register is 12 bits instead of 10 bits. The following formula can always be used to calculate the actual voltage from the ADC code.

Voltage at the VMONx Pins

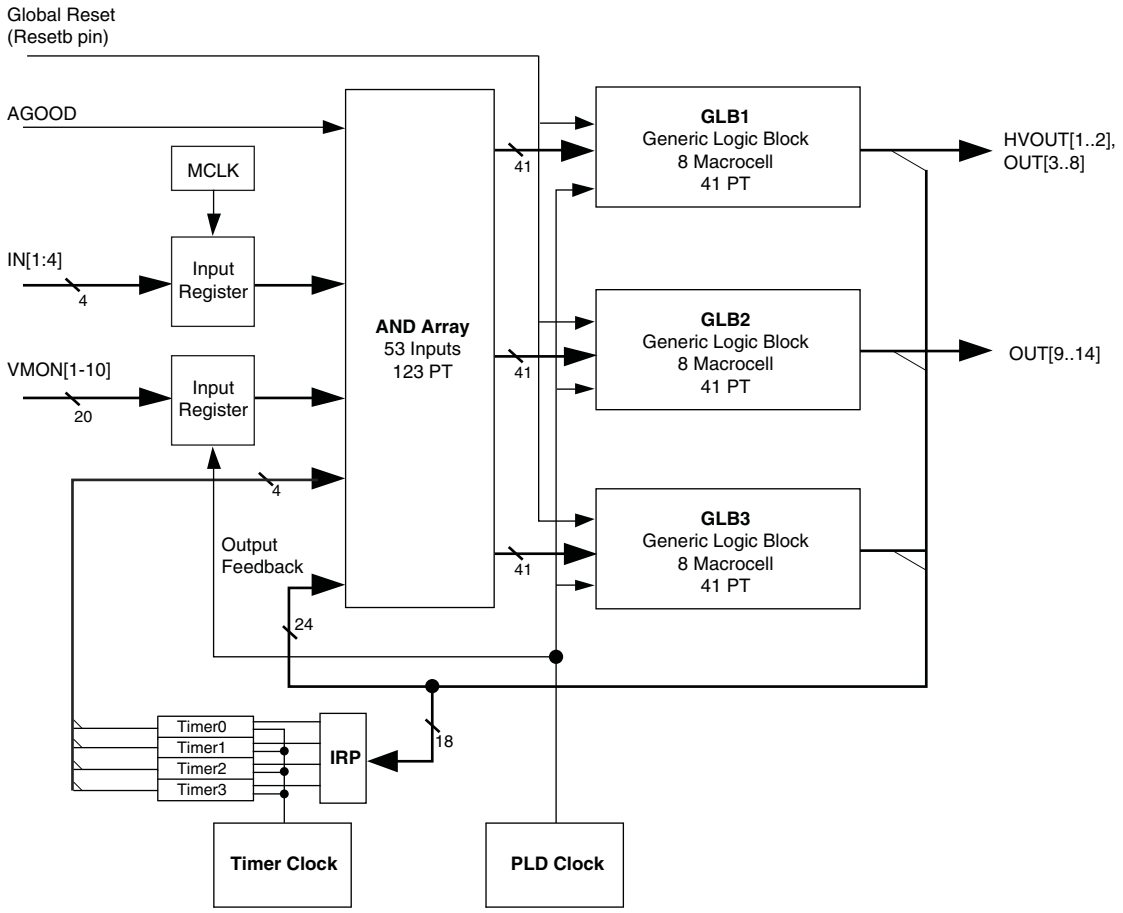
VMON = I²C Readout Register (12 bits[1], converted to decimal) * 2mV

[1]Note: ADC_VALUE_HIGH (8 bits), ADC_VALUE_LOW (4 bits) read from I²C/SMBUS interface (LA-ispPAC-POWR1014A only).

PLD Block

Figure 5-10 shows the LA-ispPAC-POWR1014/A PLD architecture, which is derived from the Lattice's ispMACH™ 4000 CPLD. The PLD architecture allows the flexibility in designing various state machines and control functions used for power supply management. The AND array has 53 inputs and generates 123 product terms. These 123 product terms are divided into three groups of 41 for each of the generic logic blocks, GLB1, GLB2, and GLB3. Each GLB is made up of eight macrocells. In total, there are 24 macrocells in the LA-ispPAC-POWR1014/A device. The output signals of the LA-ispPAC-POWR1014/A device are derived from GLBs as shown in Figure 5-10. GLB3 generates timer control.

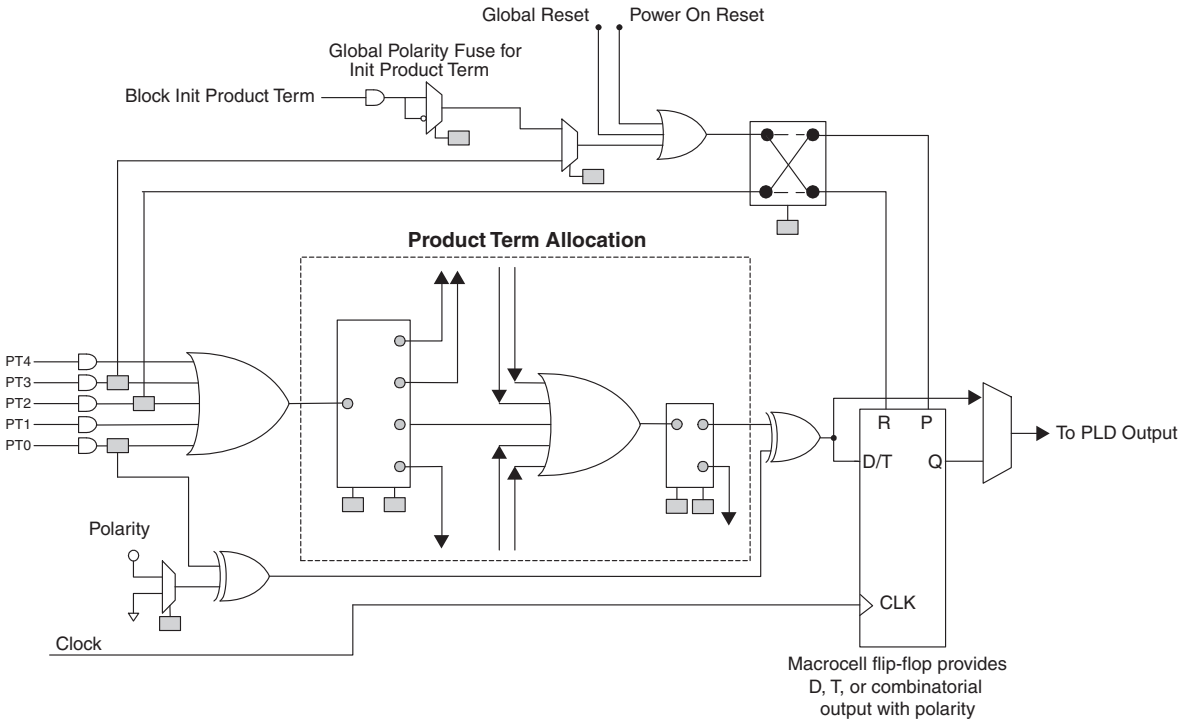
Figure 5-10. LA-ispPAC-POWR1014/A PLD Architecture



Macrocell Architecture

The macrocell shown in Figure 5-11 is the heart of the PLD. The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. Combinatorial functions are realized by bypassing the flip-flop. The polarity control and XOR gates provide additional flexibility for logic synthesis. The flip-flop's clock is driven from the common PLD clock that is generated by dividing the 8 MHz master clock by 32. The macrocell also supports asynchronous reset and preset functions, derived from either product terms, the global reset input, or the power-on reset signal. The resources within the macrocells share routing and contain a product term allocation array. The product term allocation array greatly expands the PLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions. All the digital inputs are registered by MCLK and the VMON comparator outputs are registered by the PLD Clock to synchronize them to the PLD logic.

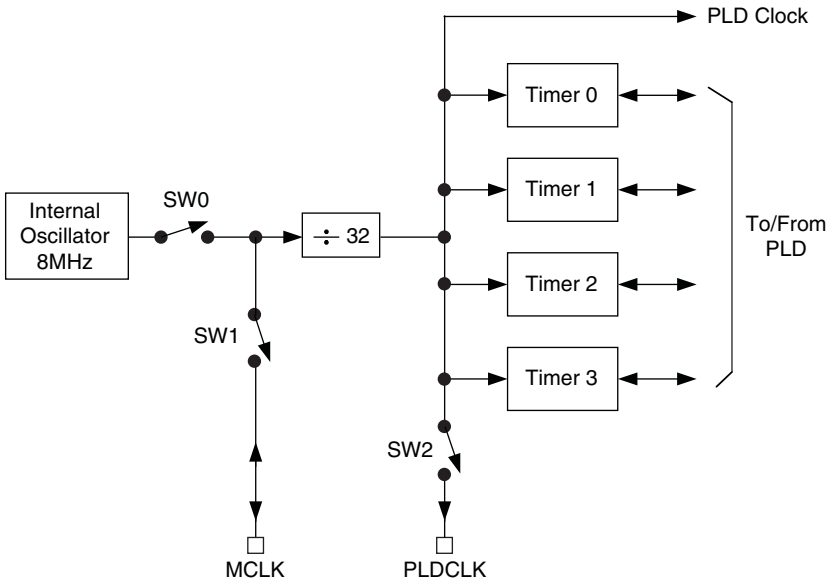
Figure 5-11. LA-ispPAC-POWR1014/A Macrocell Block Diagram



Clock and Timer Functions

Figure 5-12 shows a block diagram of the LA-ispPAC-POWR1014/A's internal clock and timer systems. The master clock operates at a fixed frequency of 8MHz, from which a fixed 250kHz PLD clock is derived.

Figure 5-12. Clock and Timer System



The internal oscillator runs at a fixed frequency of 8 MHz. This signal is used as a source for the PLD and timer clocks. It is also used for clocking the comparator outputs and clocking the digital filters in the voltage monitor circuits and ADC. The LA-ispPAC-POWR1014/A can be programmed to operate in three modes: Master mode,

Standalone mode and Slave mode. Table 5-5 summarizes the operating modes of LA-ispPAC-POWR1014/A.

Table 5-5. LA-ispPAC-POWR1014/A Operating Modes

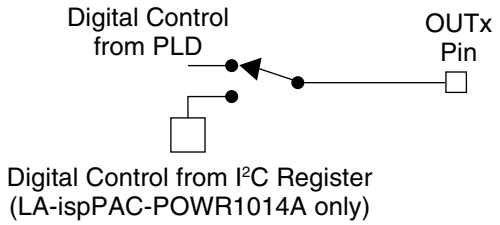
Timer Operating Mode	SW0	SW1	Condition	Comments
Standalone	Closed	Open	When only one LA-ispPAC-POWR1014/A is used.	MCLK pin tristated
Master	Closed	Closed	When more than one LA-ispPAC-POWR1014/A is used in a board, one of them should be configured to operate in this mode.	MCLK pin outputs 8MHz clock
Slave	Open	Closed	When more than one LA-ispPAC-POWR1014/As is used in a board. Other than the master, the rest of the LA-ispPAC-POWR1014/As should be programmed as slaves.	MCLK pin is input

A divide-by-32 prescaler divides the internal 8MHz oscillator (or external clock, if selected) down to 250kHz for the PLD clock and for the programmable timers. This PLD clock may be made available on the PLDCLK pin by closing SW2. Each of the four timers provides independent timeout intervals ranging from 32µs to 1.96 seconds in 128 steps.

Digital Outputs

The LA-ispPAC-POWR1014/A provides 14 digital outputs, HVOUT[1:2] and OUT[3:14]. Outputs OUT[3:14] are permanently configured as open drain to provide a high degree of flexibility when interfacing to logic signals, LEDs, opto-couplers, and power supply control inputs. The HVOUT[1:2] pins can be configured as either high voltage FET drivers or open drain outputs. Each of these outputs may be controlled either from the PLD or from the I^2C bus (LA-ispPAC-POWR1014A only). The determination whether a given output is under PLD or I^2C control may be made on a pin-by-pin basis (see Figure 5-13). For further details on controlling the outputs through I^2C, please see the I^2C/SMBUS Interface section of this data sheet.

Figure 5-13. Digital Output Pin Configuration



High-Voltage Outputs

In addition to being usable as digital open-drain outputs, the LA-ispPAC-POWR1014/A's HVOUT1-HVOUT2 output pins can be programmed to operate as high-voltage FET drivers. Figure 5-14 shows the details of the HVOUT gate drivers. Each of these outputs may be controlled from the PLD, or with the LA-ispPAC-POWR1014A, from the I^2C bus/JTAG interface (see Figure 5-14). For further details on controlling the outputs through I^2C, please see the I^2C/SMBUS Interface, and Accessing I^2C Registers Through JTAG sections of this data sheet.

Figure 5-14. Basic Function Diagram for an Output in High Voltage MOSFET Gate Driver Mode

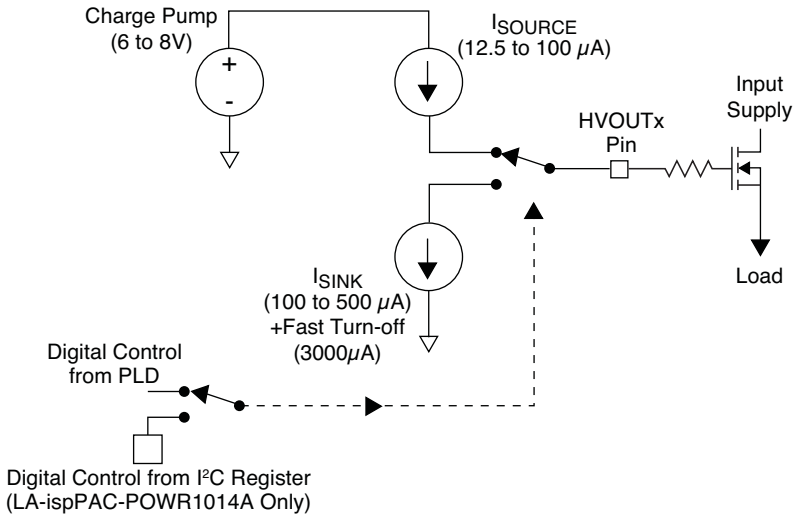


Figure 5-14 shows the HVOUT circuitry when programmed as a FET driver. In this mode the output either sources current from a charge pump or sinks current. The maximum voltage that the output level at the pin will rise to is also programmable. The HVOUT pin source current, which is programmable between 12.5 µA and 100 µA, is used to control the FET turn-on rate. Similarly, the HVOUT sink current, which is programmable between 3000 µA and 100 µA, is used to control the turn-off rate.

Programmable Output Voltage Levels for HVOUT1- HVOUT2

There are four selectable steps for the output voltage of the FET drivers when in FET driver mode. The voltage that the pin is capable of driving to can be programmed from 6V to 8V in 2V steps.

RESETb Signal, RESET Command via JTAG or I²C

Activating the RESETb signal (Logic 0 applied to the RESETb pin) or issuing a reset instruction via JTAG, or with the LA-ispPAC-POWR1014A, I²C will force the outputs to the following states independent of how these outputs have been configured in the PINS window:

- OUT3-14 will go high-impedance.
- HVOUT pins programmed for open drain operation will go high-impedance.
- HVOUT pins programmed for FET driver mode operation will pull down.

At the conclusion of the RESET event, these outputs will go to the states defined by the PINS window, and if a sequence has been programmed into the device, it will be re-started at the first step. The analog calibration will be re-done and consequently, the VMONs, and ADCs will not be operational until 500 microseconds (max.) after the conclusion of the RESET event.

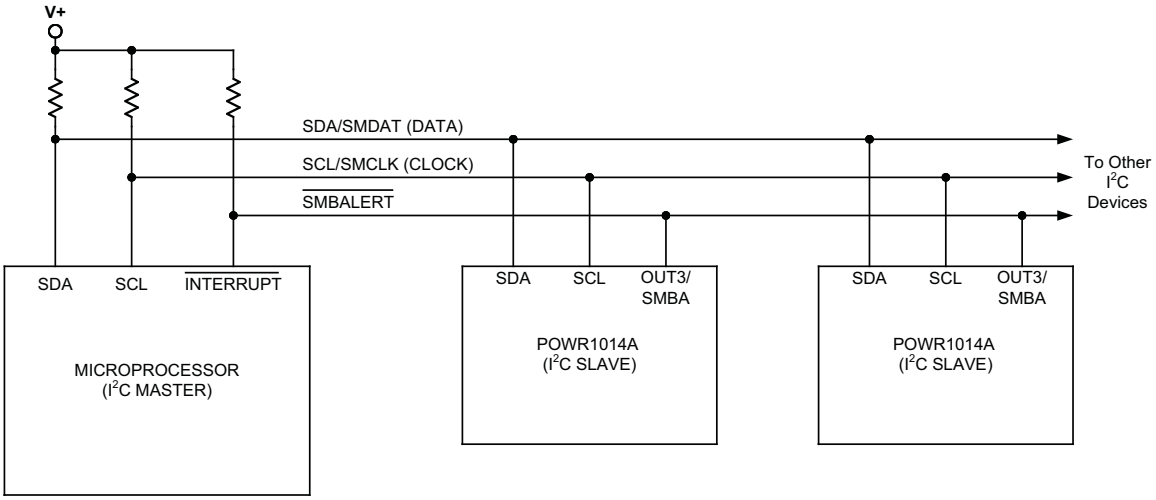
CAUTION: Activating the RESETb signal or issuing a RESET command through I2C or JTAG during the LA-ispPAC-POWR1014/A device operation, results in the device aborting all operations and returning to the power-on reset state. The status of the power supplies which are being enabled by the LA-ispPAC-POWR1014/A will be determined by the state of the outputs shown above.

I²C/SMBUS Interface (LA-ispPAC-POWR1014A Only)

I²C and SMBus are low-speed serial interface protocols designed to enable communications among a number of devices on a circuit board. The LA-ispPAC-POWR1014A supports a 7-bit addressing of the I²C communications protocol, as well as SMBTimeout and SMBAlert features of the SMBus, enabling it to easily integrated into many types of modern power management systems. Figure 5-15 shows a typical I²C configuration, in which one or more LA-ispPAC-POWR1014As are slaved to a supervisory microcontroller. SDA is used to carry data signals, while

SCL provides a synchronous clock signal. The SMBAlert line is only present in SMBus systems. The 7-bit I²C address of the POWR1014A is fully programmable through the JTAG port.

Figure 5-15. LA-ispPAC-POWR1014A in I²C/SMBUS System



In both the I²C and SMBus protocols, the bus is controlled by a single MASTER device at any given time. This master device generates the SCL clock signal and coordinates all data transfers to and from a number of slave devices. The LA-ispPAC-POWR1014A is configured as a slave device, and cannot independently coordinate data transfers. Each slave device on a given I²C bus is assigned a unique address. The LA-ispPAC-POWR1014A implements the 7-bit addressing portion of the standard. Any 7-bit address can be assigned to the LA-ispPAC-POWR1014A device by programming through JTAG. When selecting a device address, one should note that several addresses are reserved by the I²C and/or SMBus standards, and should not be assigned to LA-ispPAC-POWR1014A devices to assure bus compatibility. Table 5-6 lists these reserved addresses.

Table 5-6. I²C/SMBus Reserved Slave Device Addresses

Address	R/W bit	I²C function Description	SMBus Function
0000 000	0	General Call Address	General Call Address
0000 000	1	Start Byte	Start Byte
0000 001	x	CBUS Address	CBUS Address
0000 010	x	Reserved	Reserved
0000 011	x	Reserved	Reserved
0000 1xx	x	HS-mode master code	HS-mode master code
0001 000	x	NA	SMBus Host
0001 100	x	NA	SMBus Alert Response Address
0101 000	x	NA	Reserved for ACCESS.bus
0110 111	x	NA	Reserved for ACCESS.bus
1100 001	x	NA	SMBus Device Default Address
1111 0xx	x	10-bit addressing	10-bit addressing
1111 1xx	x	Reserved	Reserved

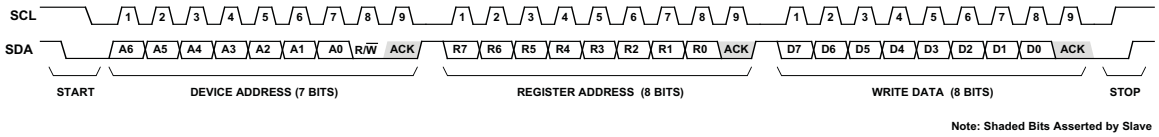
The LA-ispPAC-POWR1014A's I²C/SMBus interface allows data to be both written to and read from the device. A data write transaction (Figure 5-16) consists of the following operations:

1. Start the bus transaction
2. Transmit the device address (7 bits) along with a low write bit

3. Transmit the address of the register to be written to (8 bits)
4. Transmit the data to be written (8 bits)
5. Stop the bus transaction

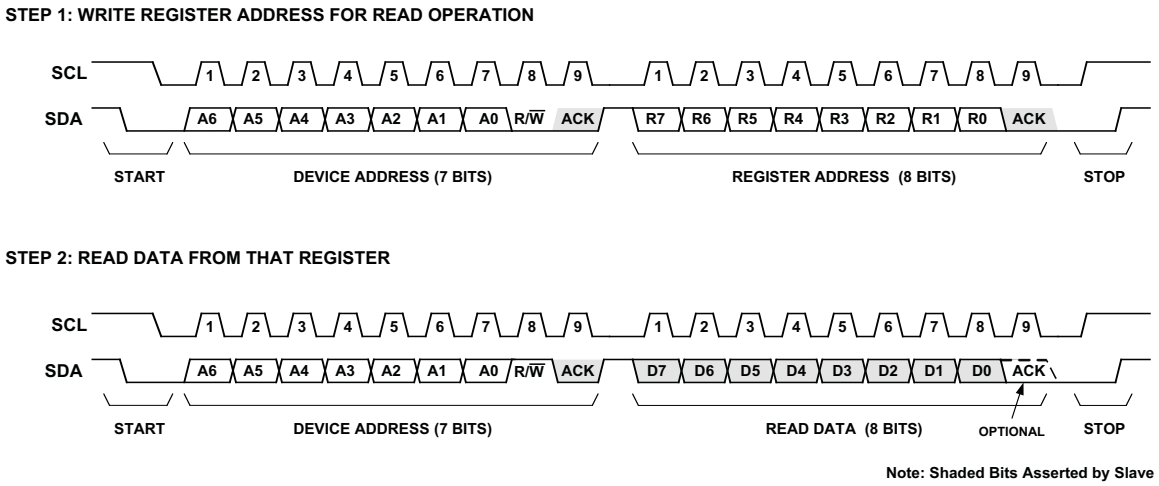
To start the transaction, the master device holds the SCL line high while pulling SDA low. Address and data bits are then transferred on each successive SCL pulse, in three consecutive byte frames of 9 SCL pulses. Address and data are transferred on the first 8 SCL clocks in each frame, while an acknowledge signal is asserted by the slave device on the 9th clock in each frame. Both data and addresses are transferred in a most-significant-bit-first format. The first frame contains the 7-bit device address, with bit 8 held low to indicate a write operation. The second frame contains the register address to which data will be written, and the final frame contains the actual data to be written. Note that the SDA signal is only allowed to change when the SCL is low, as raising SDA when SCL is high signals the end of the transaction.

Figure 5-16. I²C Write Operation



Reading a data byte from the LA-ispPAC-POWR1014A requires two separate bus transactions (Figure 5-17). The first transaction writes the register address from which a data byte is to be read. Note that since no data is being written to the device, the transaction is concluded after the second byte frame. The second transaction performs the actual read. The first frame contains the 7-bit device address with the R/W bit held High. In the second frame the LA-ispPAC-POWR1014A asserts data out on the bus in response to the SCL signal. Note that the acknowledge signal in the second frame is asserted by the master device and not the LA-ispPAC-POWR1014A.

Figure 5-17. I²C Read Operation



The LA-ispPAC-POWR1014ALA-ispPAC-POWR1014A provides 17 registers that can be accessed through its I²C interface. These registers provide the user with the ability to monitor and control the device's inputs and outputs, and transfer data to and from the device. Table 5-7 provides a summary of these registers.