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## **LA-MachXO Automotive Family Data Sheet**

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DS1003 Version 01.5, November 2007

## Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - Single chip, no external configuration memory required
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through JTAG port
  - Supports background programming of non-volatile memory
- **AEC-Q100 Tested and Qualified**
- **Sleep Mode**
  - Allows up to 100x static current reduction
- **TransFR™ Reconfiguration (TFR)**
  - In-field logic update while system operates
- **High I/O to Logic Density**
  - 256 to 2280 LUT4s
  - 73 to 271 I/Os with extensive package options
  - Density migration supported
  - Lead free/RoHS compliant packaging
- **Embedded and Distributed Memory**
  - Up to 27.6 Kbits sysMEM™ Embedded Block RAM
  - Up to 7.5 Kbits distributed RAM
  - Dedicated FIFO control logic
- **Flexible I/O Buffer**

- Programmable sysIO™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTTL
  - PCI
  - LVDS, Bus-LVDS, LVPECL, RSDS
- **sysCLOCK™ PLLs**
  - Up to two analog PLLs per device
  - Clock multiply, divide, and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan
  - Onboard oscillator
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply
  - IEEE 1532 compliant in-system programming

## Introduction

The LA-MachXO automotive device family is optimized to meet the requirements of applications traditionally addressed by CPLDs and low capacity FPGAs: glue logic, bus bridging, bus interfacing, power-up control, and control logic. These devices bring together the best features of CPLD and FPGA devices on a single chip in AEC-Q100 tested and qualified versions.

The devices use look-up tables (LUTs) and embedded block memories traditionally associated with FPGAs for flexible and efficient logic implementation. Through non-volatile technology, the devices provide the single-chip,

**Table 1-1. LA-MachXO Automotive Family Selection Guide**

Device	LAMXO256E/C	LAMXO640E/C	LAMXO1200E	LAMXO2280E
LUTs	256	640	1200	2280
Dist. RAM (Kbits)	2.0	6.0	6.25	7.5
EBR SRAM (Kbits)	0	0	9.2	27.6
Number of EBR SRAM Blocks (9 Kbits)	0	0	1	3
V <sub>CC</sub> Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2	1.2
Number of PLLs	0	0	1	2
Max. I/O	78	159	211	271
<b>Packages</b>				
100-pin Lead-Free TQFP (14x14 mm)	78	74	73	73
144-pin Lead-Free TQFP (20x20 mm)		113	113	113
256-ball Lead-Free ftBGA (17x17 mm)		159	211	211
324-ball Lead-Free ftBGA (19x19 mm)				271

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high-security, instant-on capabilities traditionally associated with CPLDs. Finally, advanced process technology and careful design will provide the high pin-to-pin performance also associated with CPLDs.

The ispLEVER® design tools from Lattice allow complex designs to be efficiently implemented using the LA-MachXO automotive family of devices. Popular logic synthesis tools provide synthesis library support for LA-MachXO. The ispLEVER tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LA-MachXO device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.



## Architecture Overview

The LA-MachXO family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). Some devices in this family have sysCLOCK PLLs and blocks of sysMEM™ Embedded Block RAM (EBRs). Figures 2-1, 2-2, and 2-3 show the block diagrams of the various family members.

The logic blocks are arranged in a two-dimensional grid with rows and columns. The EBR blocks are arranged in a column to the left of the logic array. The PIO cells are located at the periphery of the device, arranged into Banks. The PIOs utilize a flexible I/O buffer referred to as a sysIO interface that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

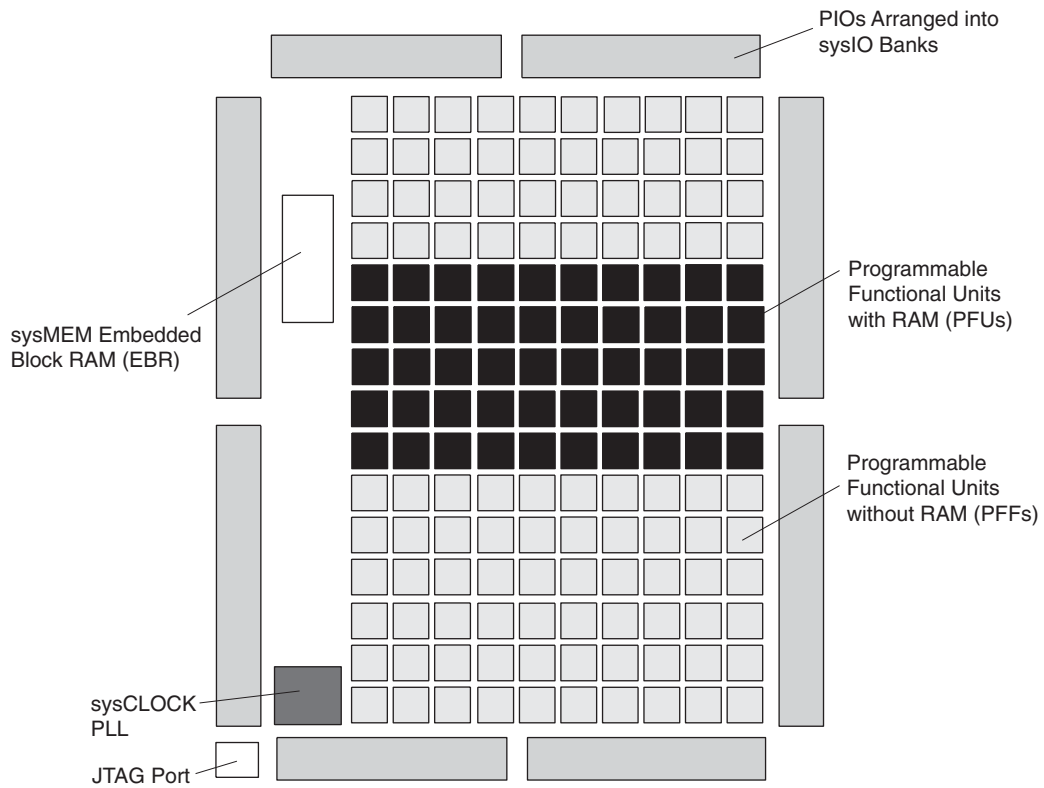
There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and the Programmable Functional unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PFF block contains building blocks for logic, arithmetic, ROM, and register functions. Both the PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and effectively. Logic blocks are arranged in a two-dimensional array. Only one type of block is used per row.

In the LA-MachXO family, the number of sysIO Banks varies by device. There are different types of I/O Buffers on different Banks. See the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks; these blocks are found only in the larger devices. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT use.

The LA-MachXO architecture provides up to two sysCLOCK™ Phase Locked Loop (PLL) blocks on larger devices. These blocks are located at either end of the memory blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a JTAG Port that supports programming and configuration of the device as well as access to the user logic. The LA-MachXO devices are available for operation from 3.3V, 2.5V, 1.8V, and 1.2V power supplies, providing easy integration into the overall system.

Figure 2-1. Top View of the LA-MachXO1200 Device<sup>1</sup>



1. Top view of the LA-MachXO2280 device is similar but with higher LUT count, two PLLs, and three EBR blocks.

Figure 2-2. Top View of the LA-MachXO640 Device

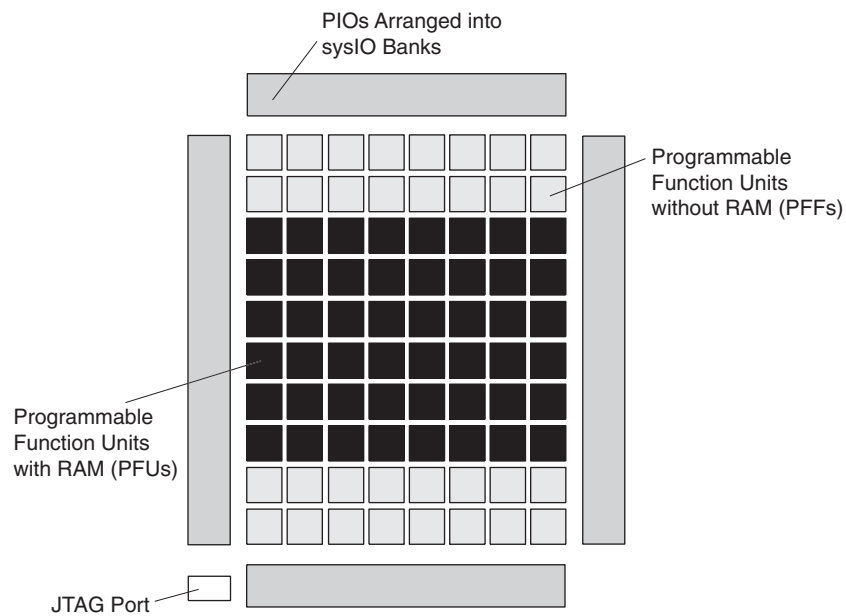
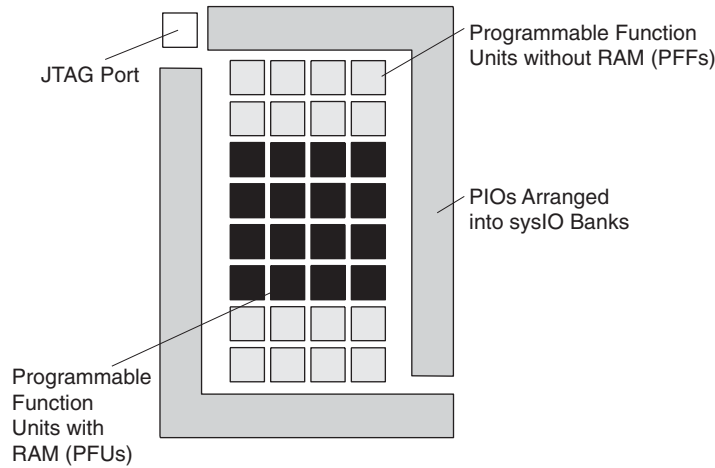


Figure 2-3. Top View of the LA-MachXO256 Device

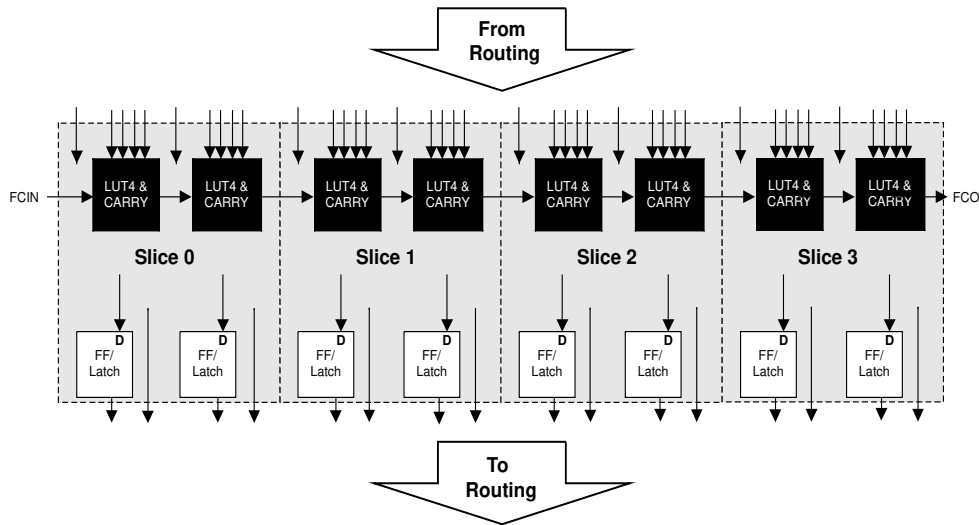


**PFU Blocks**

The core of the LA-MachXO devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM, and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic, and Distributed ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected Slices, numbered 0-3 as shown in Figure 2-4. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-4. PFU Diagram

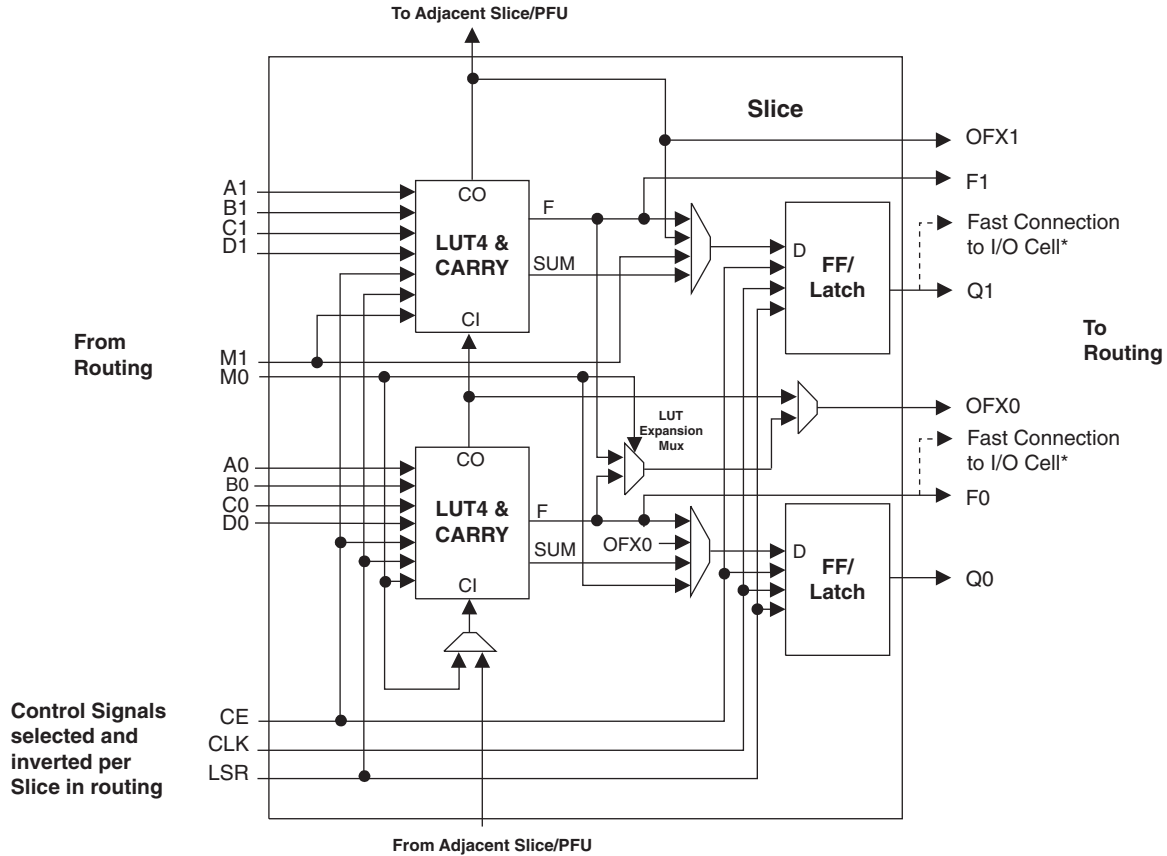


**Slice**

Each Slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select, and wider RAM/ROM functions. Figure 2-5 shows an overview of the internal logic of the Slice. The registers in the Slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent Slice/PFU). There are 7 outputs: 6 to the routing and one to the carry-chain (to the adjacent Slice/PFU). Table 2-1 lists the signals associated with each Slice.

Figure 2-5. Slice Diagram



Notes:  
Some inter-Slice signals are not shown.  
\* Only PFUs at the edges have fast connections to the I/O cell.

Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In <sup>1</sup>
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 <sup>2</sup> MUX depending on the Slice
Output	Inter-PFU signal	FCO	Fast Carry Out <sup>1</sup>

1. See Figure 2-4 for connection details.  
2. Requires two PFUs.



**Modes of Operation**

Each Slice is capable of four modes of operation: Logic, Ripple, RAM, and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

**Table 2-2. Slice Modes**

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

**Logic Mode:** In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables (LUT4). A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other Slices.

**Ripple Mode:** Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals, Carry Generate and Carry Propagate, are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

**RAM Mode:** In this mode, distributed RAM can be constructed using each LUT block as a 16x2-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

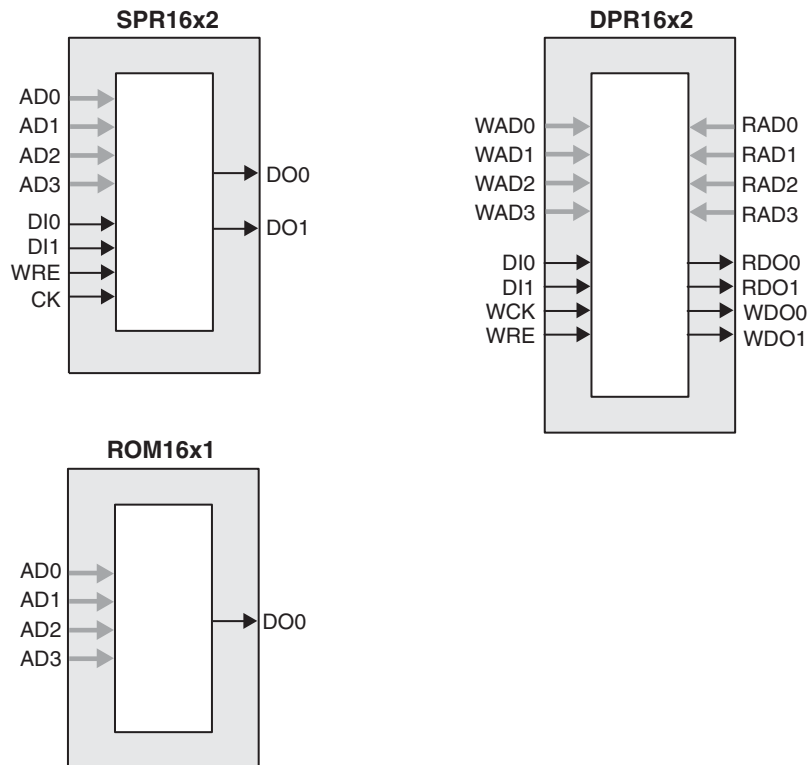
The ispLEVER design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-6 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices. One Slice functions as the read-write port, while the other companion Slice supports the read-only port. For more information on RAM mode in LA-MachXO devices, please see details of additional technical documentation at the end of this data sheet.

**Table 2-3. Number of Slices Required For Implementing Distributed RAM**

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-6. Distributed Memory Primitives



**ROM Mode:** The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

**PFU Modes of Operation**

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

**Routing**

There are many resources provided in the LA-MachXO devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

## Clock/Control Distribution Network

The LA-MachXO automotive family of devices provides global signals that are available to all PFUs. These signals consist of four primary clocks and four secondary clocks. Primary clock signals are generated from four 16:1 muxes as shown in Figure 2-7 and Figure 2-8. The available clock sources for the LA-MachXO256 and LA-MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the LA-MachXO1200 and LA-MachXO2280 devices are four dual function clock pins, up to nine internal routing signals and up to six PLL outputs.

**Figure 2-7. Primary Clocks for LA-MachXO256 and LA-MachXO640 Devices**

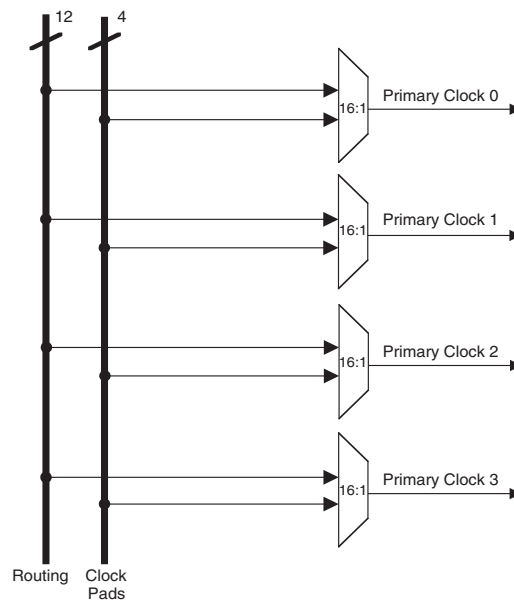
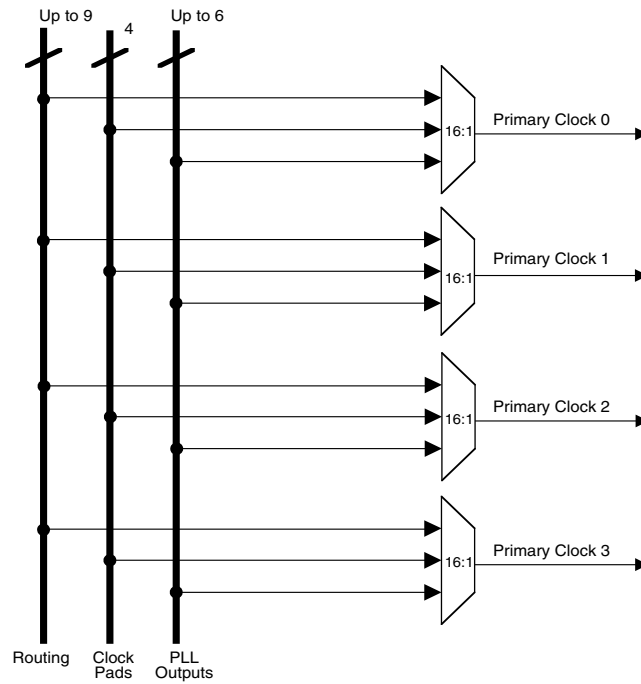
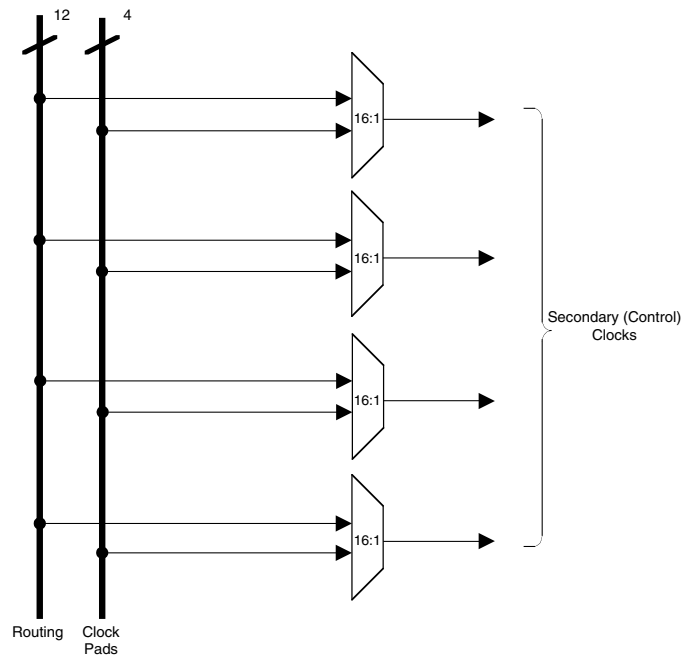


Figure 2-8. Primary Clocks for LA-MachXO1200 and LA-MachXO2280 Devices



Four secondary clocks are generated from four 16:1 muxes as shown in Figure 2-9. Four of the secondary clock sources come from dual function clock pins and 12 come from internal routing.

Figure 2-9. Secondary Clocks for LA-MachXO Devices



### sysCLOCK Phase Locked Loops (PLLs)

The LA-MachXO1200 and LA-MachXO2280 provide PLL support. The source of the PLL input divider can come from an external pin or from internal routing. There are four sources of feedback signals to the feedback divider: from CLKINTFB (internal feedback port), from the global clock nets, from the output of the post scalar divider, and from the routing (or from an external pin). There is a PLL\_LOCK signal to indicate that the PLL has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the  $t_{LOCK}$  parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider, and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

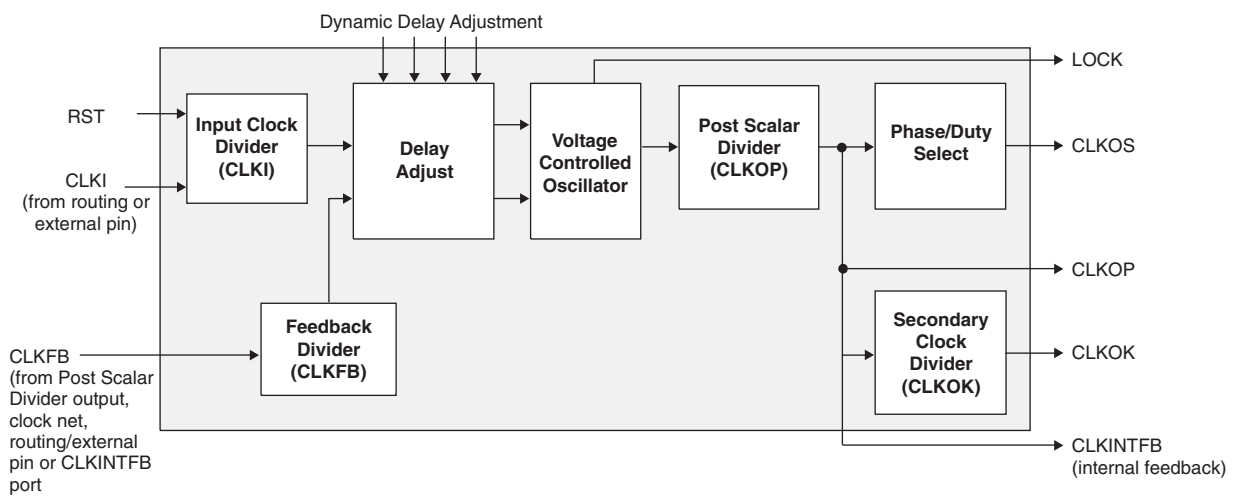
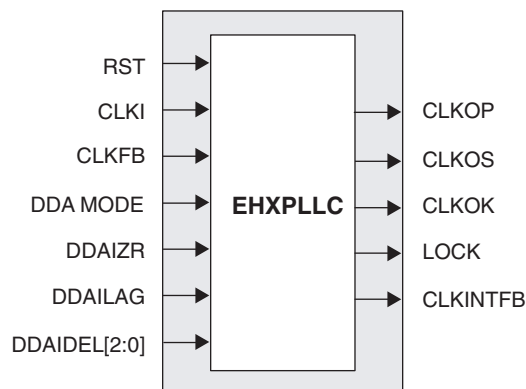


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive



**Table 2-5. PLL Signal Descriptions**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clock net, routing/external pin or internal feedback from CLKINTFB port
RST	I	“1” to reset the input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	“1” indicates PLL LOCK to CLKI
CLKINTFB	O	Internal feedback source, CLKOP divider output before CLOKRTREE
DDAMODE	I	Dynamic Delay Enable. “1”: Pin control (dynamic), “0”: Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead
DDAIDEL[2:0]	I	Dynamic Delay Input

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## sysMEM Memory

The LA-MachXO1200 and LA-MachXO2280 devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

**Table 2-6. sysMEM Block Configurations**

Memory Mode	Configurations
Single Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36
True Dual Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
Pseudo Dual Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36
FIFO	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18
	256 x 36



**Bus Size Matching**

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

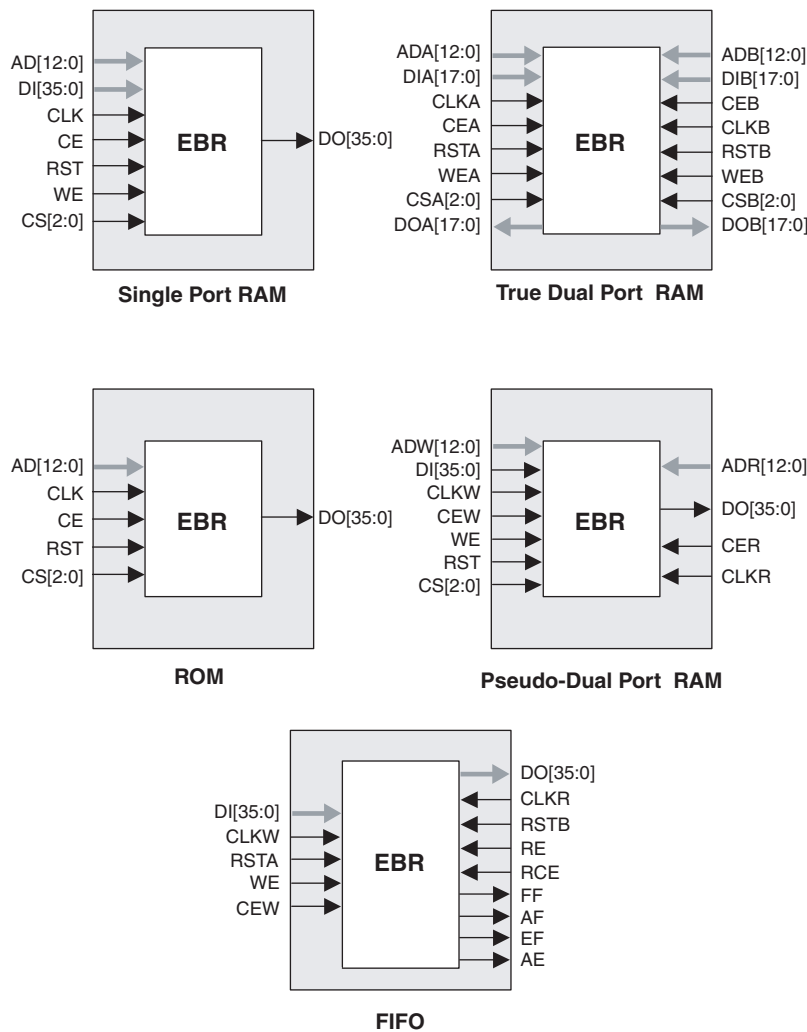
**Memory Cascading**

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

**Single, Dual, Pseudo-Dual Port and FIFO Modes**

Figure 2-12 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

**Figure 2-12. sysMEM Memory Primitives**



The EBR memory supports three forms of write behavior for single or dual port operation:

1. **Normal** – data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – a copy of the input data appears at the output of the same port. This mode is supported for all data widths.
3. **Read-Before-Write** – when new data is being written, the old contents of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

### FIFO Configuration

The FIFO has a write port with Data-in, CEW, WE and CLKW signals. There is a separate read port with Data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. The range of programming values for these flags are in Table 2-7.

**Table 2-7. Programmable FIFO Flag Ranges**

Flag Name	Programming Range
Full (FF)	1 to (up to $2^N-1$ )
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

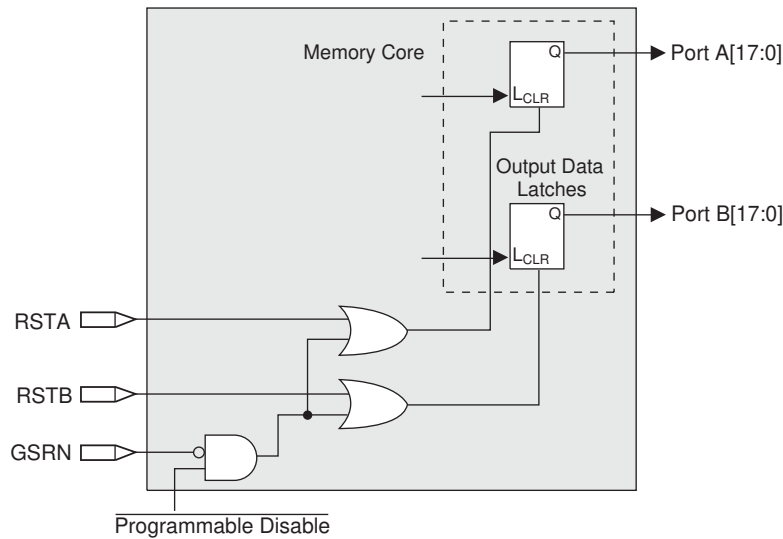
N = Address bit width

The FIFO state machine supports two types of reset signals: RSTA and RSTB. The RSTA signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RSTB signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

### Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-13.

Figure 2-13. Memory Core Reset

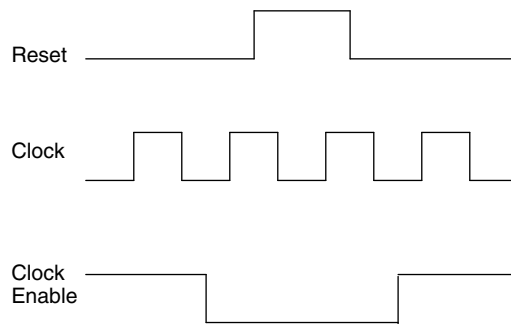


For further information on the sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

**EBR Asynchronous Reset**

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-14. The GSR input to the EBR is always asynchronous.

Figure 2-14. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of  $1/f_{MAX}$  (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-14. The reset timing rules apply to the RPRreset input vs the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

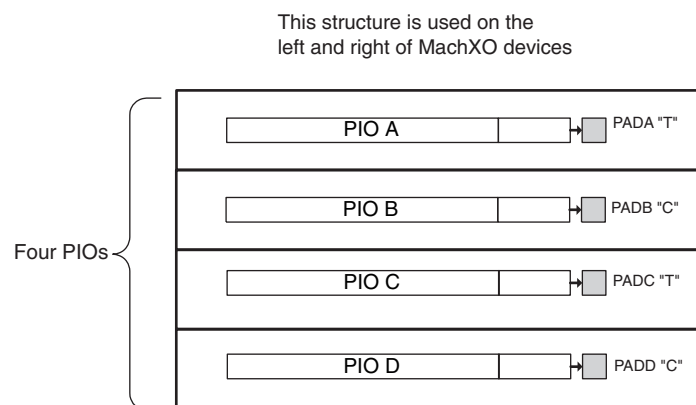
## PIO Groups

On the LA-MachXO devices, PIO cells are assembled into two different types of PIO groups, those with four PIO cells and those with six PIO cells. PIO groups with four IOs are placed on the left and right sides of the device while PIO groups with six IOs are placed on the top and bottom. The individual PIO cells are connected to their respective sysIO buffers and PADS.

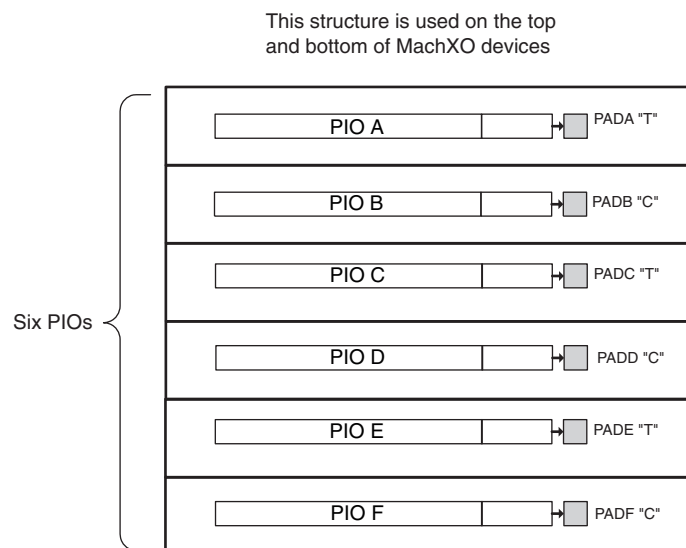
On all LA-MachXO devices, two adjacent PIOs can be joined to provide a complementary Output driver pair. The I/O pin pairs are labeled as "T" and "C" to distinguish between the true and complement pins.

The LA-MachXO1200 and LA-MachXO2280 devices contain enhanced I/O capability. All PIO pairs on these larger devices can implement differential receivers. In addition, half of the PIO pairs on the left and right sides of these devices can be configured as LVDS transmit/receive pairs. PIOs on the top of these larger devices also provide PCI support.

**Figure 2-15. Group of Four Programmable I/O Cells**



**Figure 2-16. Group of Six Programmable I/O Cells**



## PIO

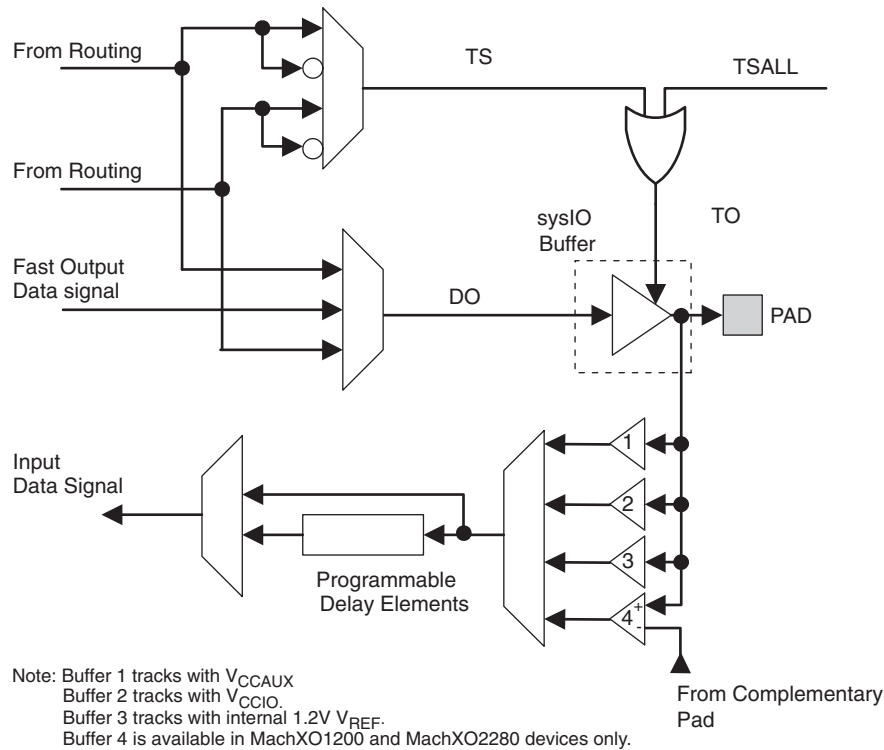
The PIO blocks provide the interface between the sysIO buffers and the internal PFU array blocks. These blocks receive output data from the PFU array and a fast output data signal from adjacent PFUs. The output data and fast

output data signals are multiplexed and provide a single signal to the I/O pin via the sysIO buffer. Figure 2-17 shows the LA-MachXO PIO logic.

The tristate control signal is multiplexed from the output data signals and their complements. In addition a global signal (TSALL) from a dedicated pad can be used to tristate the sysIO buffer.

The PIO receives an input signal from the pin via the sysIO buffer and provides this signal to the core of the device. In addition there are programmable elements that can be utilized by the design tools to avoid positive hold times.

Figure 2-17. LA-MachXO PIO Block Diagram



## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today’s systems including LVCMOS, TTL, BLVDS, LVDS and LVPECL.

In the LA-MachXO devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS and PCI) are powered using  $V_{CCIO}$ . In addition to the Bank  $V_{CCIO}$  supplies, the LA-MachXO devices have a  $V_{CC}$  core logic power supply, and a  $V_{CCAUX}$  supply that powers up a variety of internal circuits including all the differential and referenced input buffers.

LA-MachXO256 and LA-MachXO640 devices contain single-ended input buffers and single-ended output buffers with complementary outputs on all the I/O Banks.

LA-MachXO1200 and LA-MachXO2280 devices contain two types of sysIO buffer pairs.

### 1. Top and Bottom sysIO Buffer Pairs

The sysIO buffer pairs in the top and bottom Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (for ratioed or absolute input levels). The I/O pairs on the top and bottom

of the devices also support differential input buffers. PCI clamps are available on the top Bank I/O buffers. The PCI clamp is enabled after  $V_{CC}$ ,  $V_{CCAUX}$ , and  $V_{CCIO}$  are at valid operating levels and the device has been configured.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

## 2. Left and Right sysIO Buffer Pairs

The sysIO buffer pairs in the left and right Banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (supporting ratioed and absolute input levels). The devices also have a differential driver per output pair. The referenced input buffer can also be configured as a differential input buffer. In these Banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$  and  $V_{CCAUX}$  have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  Banks are active with valid input logic levels to properly control the output logic states of all the I/O Banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-up to  $V_{CCIO}$ . The I/O pins will maintain the blank configuration until  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCIO}$  have reached satisfactory levels at which time the I/Os will take on the user-configured settings.

The  $V_{CC}$  and  $V_{CCAUX}$  supply the power to the FPGA core fabric, whereas the  $V_{CCIO}$  supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, the I/O buffers should be powered up along with the FPGA core fabric. Therefore,  $V_{CCIO}$  supplies should be powered up before or together with the  $V_{CC}$  and  $V_{CCAUX}$  supplies

### Supported Standards

The LA-MachXO sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTTL. The buffer supports the LVTTTL, LVCMOS 1.2, 1.5, 1.8, 2.5, and 3.3V standards. In the LVCMOS and LVTTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS and LVPECL output emulation is supported on all devices. The LA-MachXO1200 and LA-MachXO2280 support on-chip LVDS output buffers on approximately 50% of the I/Os on the left and right Banks. Differential receivers for LVDS, BLVDS and LVPECL are supported on all Banks of LA-MachXO1200 and LA-MachXO2280 devices. PCI support is provided in the top Banks of the LA-MachXO1200 and LA-MachXO2280 devices. Table 2-8 summarizes the I/O characteristics of the devices in the LA-MachXO family.

Tables 2-9 and 2-10 show the I/O standards (together with their supply and reference voltages) supported by the LA-MachXO devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.



**Table 2-8. I/O Support Device by Device**

	LA-MachXO256	LA-MachXO640	LA-MachXO1200	LA-MachXO2280
Number of I/O Banks	2	4	8	8
Type of Input Buffers	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)	Single-ended (all I/O Banks)  Differential Receivers (all I/O Banks)	Single-ended (all I/O Banks)  Differential Receivers (all I/O Banks)
Types of Output Buffers	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)	Single-ended buffers with complementary outputs (all I/O Banks)  Differential buffers with true LVDS outputs (50% on left and right side)	Single-ended buffers with complementary outputs (all I/O Banks)  Differential buffers with true LVDS outputs (50% on left and right side)
Differential Output Emulation Capability	All I/O Banks	All I/O Banks	All I/O Banks	All I/O Banks
PCI Support	No	No	Top side only	Top side only

**Table 2-9. Supported Input Standards**

Input Standard	VCCIO (Typ.)				
	3.3V	2.5V	1.8V	1.5V	1.2V
<b>Single Ended Interfaces</b>					
LVTTTL	√	√	√	√	√
LVC MOS33	√	√	√	√	√
LVC MOS25	√	√	√	√	√
LVC MOS18			√		
LVC MOS15				√	
LVC MOS12	√	√	√	√	√
PCI <sup>1</sup>	√				
<b>Differential Interfaces</b>					
BLVDS <sup>2</sup> , LVDS <sup>2</sup> , LVPECL <sup>2</sup> , RSDS <sup>2</sup>	√	√	√	√	√

1. Top Banks of LA-MachXO1200 and LA-MachXO2280 devices only.

2. LA-MachXO1200 and LA-MachXO2280 devices only.

Table 2-10. Supported Output Standards

Output Standard	Drive	V <sub>CCIO</sub> (Typ.)
<b>Single-ended Interfaces</b>		
LVTTTL	4mA, 8mA, 12mA, 16mA	3.3
LVC MOS33	4mA, 8mA, 12mA, 14mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 14mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 14mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA, 14mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33 <sup>3</sup>	N/A	3.3
<b>Differential Interfaces</b>		
LVDS <sup>1,2</sup>	N/A	2.5
BLVDS, RSDS <sup>2</sup>	N/A	2.5
LVPECL <sup>2</sup>	N/A	3.3

1. LA-MachXO1200 and LA-MachXO2280 devices have dedicated LVDS buffers.
2. These interfaces can be emulated with external resistors in all devices.
3. Top Banks of LA-MachXO1200 and LA-MachXO2280 devices only.

## sysIO Buffer Banks

The number of Banks vary between the devices of this family. Eight Banks surround the two larger devices, the LA-MachXO1200 and LA-MachXO2280 (two Banks per side). The LA-MachXO640 has four Banks (one Bank per side). The smallest member of this family, the LA-MachXO256, has only two Banks.

Each sysIO buffer Bank is capable of supporting multiple I/O standards. Each Bank has its own I/O supply voltage (V<sub>CCIO</sub>) which allows it to be completely independent from the other Banks. Figure 2-18, Figure 2-18, Figure 2-20 and Figure 2-21 shows the sysIO Banks and their associated supplies for all devices.

Figure 2-18. LA-MachXO2280 Banks

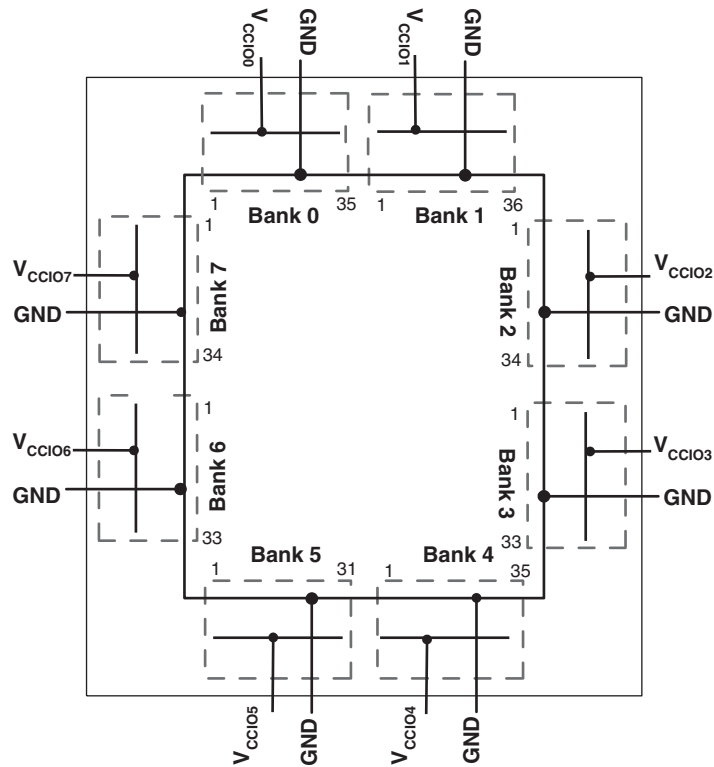


Figure 2-19. LA-MachXO1200 Banks

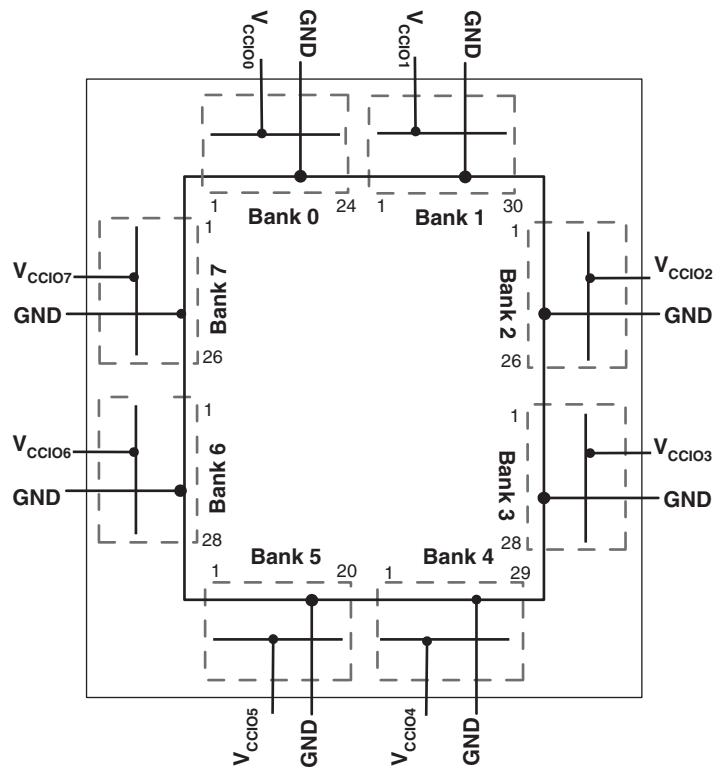


Figure 2-20. LA-MachXO640 Banks

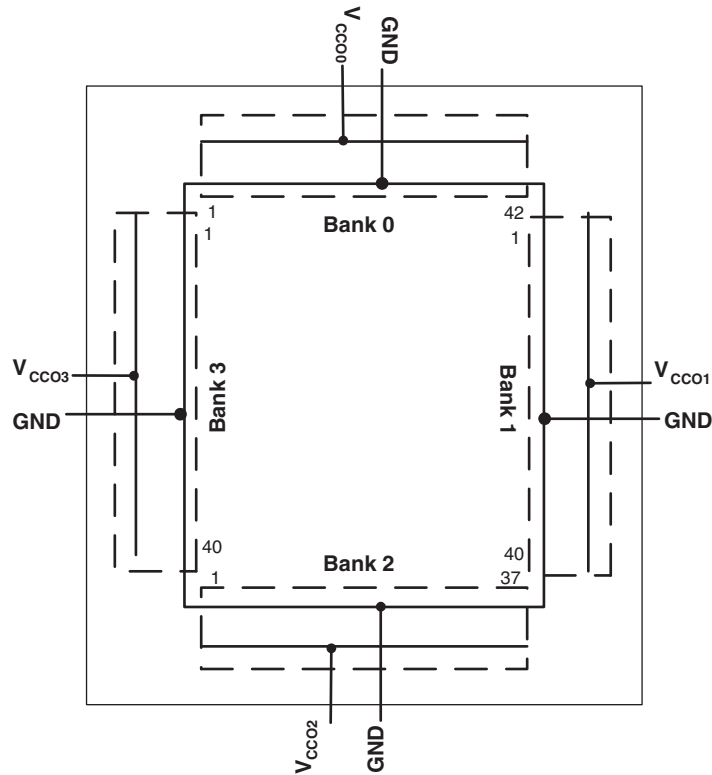
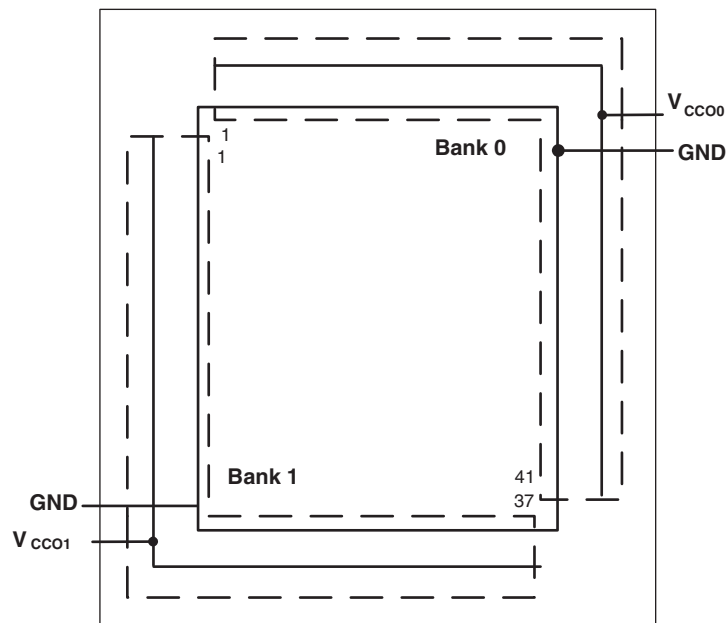


Figure 2-21. LA-MachXO256 Banks



## Hot Socketing

The LA-MachXO automotive devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration

with the rest of the system. These capabilities make the LA-MachXO ideal for many multiple power supply and hot-swap applications.

## Sleep Mode

The LA-MachXO “C” devices ( $V_{CC} = 1.8/2.5/3.3V$ ) have a sleep mode that allows standby current to be reduced dramatically during periods of system inactivity. Entry and exit to Sleep mode is controlled by the SLEEPN pin.

During Sleep mode, the logic is non-operational, registers and EBR contents are not maintained, and I/Os are tri-stated. Do not enter Sleep mode during device programming or configuration operation. In Sleep mode, power supplies are in their normal operating range, eliminating the need for external switching of power supplies. Table 2-11 compares the characteristics of Normal, Off and Sleep modes.

**Table 2-11. Characteristics of Normal, Off and Sleep Modes**

Characteristic	Normal	Off	Sleep
SLEEPN Pin	High	—	Low
Static $I_{cc}$	Typical <10mA	0	Typical <100uA
I/O Leakage	<10 $\mu$ A	<1mA	<10 $\mu$ A
Power Supplies VCC/VCCIO/VCCAUX	Normal Range	0	Normal Range
Logic Operation	User Defined	Non Operational	Non operational
I/O Operation	User Defined	Tri-state	Tri-state
JTAG and Programming circuitry	Operational	Non-operational	Non-operational
EBR Contents and Registers	Maintained	Non-maintained	Non-maintained

## SLEEPN Pin Characteristics

The SLEEPN pin behaves as an LVCMOS input with the voltage standard appropriate to the VCC supply for the device. This pin also has a weak pull-up, along with a Schmidt trigger and glitch filter to prevent false triggering. An external pull-up to VCC is recommended when Sleep Mode is not used to ensure the device stays in normal operation mode. Typically, the device enters sleep mode several hundred nanoseconds after SLEEPN is held at a valid low and restarts normal operation as specified in the Sleep Mode Timing table. The AC and DC specifications portion of this data sheet shows a detailed timing diagram.

## Oscillator

Every LA-MachXO device has an internal CMOS oscillator. The oscillator can be routed as an input clock to the clock tree or to general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit to enable/disable the oscillator. The oscillator frequency ranges from 16MHz to 26MHz.

## Configuration and Testing

The following section describes the configuration and testing features of the LA-MachXO automotive family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All LA-MachXO devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port shares its power supply with one of the VCCIO Banks (LA-MachXO256:  $V_{CCIO1}$ ; LA-MachXO640:  $V_{CCIO2}$ ; LA-MachXO1200 and LA-MachXO2280:  $V_{CCIO5}$ ) and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

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## Device Configuration

All LA-MachXO devices contain a test access port that can be used for device configuration and programming.

The non-volatile memory in the LA-MachXO can be configured in two different modes:

- In IEEE 1532 mode via the IEEE 1149.1 port. In this mode, the device is off-line and I/Os are controlled by BSCAN registers.
- In background mode via the IEEE 1149.1 port. This allows the device to remain operational in user mode while reprogramming takes place.

The SRAM configuration memory can be configured in three different ways:

- At power-up via the on-chip non-volatile memory.
- After a refresh command is issued via the IEEE 1149.1 port.
- In IEEE 1532 mode via the IEEE 1149.1 port.

Figure 2-22 provides a pictorial representation of the different programming modes available in the LA-MachXO devices. On power-up, the SRAM is ready to be configured with IEEE 1149.1 serial TAP port using IEEE 1532 protocols.

### Leave Alone I/O

When using IEEE 1532 mode for non-volatile memory programming, SRAM configuration, or issuing a refresh command, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reconfiguration or reprogramming occurs on-the-fly.

### TransFR (Transparent Field Reconfiguration)

TransFR (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. See Lattice technical note #TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology*, for details.

### Security

The LA-MachXO automotive devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear the security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

## AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.