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LAN7500/LAN7500i

Hi-Speed USB 2.0 to 10/100/1000 Ethernet Controller

PRODUCT FEATURES

Datasheet

Highlights

- Single Chip Hi-Speed USB 2.0 to 10/100/1000 Ethernet Controller
- 10/100/1000 Ethernet MAC with Full-Duplex Support
- 10/100/1000 Ethernet PHY with HP Auto-MDIX
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated USB 2.0 Hi-Speed PHY
- Implements Reduced Power Operating Modes
- Supports EEPROM-less Operation for Reduced BOM
- NetDetach provides automatic USB attach/detach when Ethernet cable is connected/removed

Target Applications

- Embedded Systems / CE Devices
- Set-Top Boxes / PVR's
- Networked Printers
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Test Instrumentation / Industrial

Key Benefits

- USB Device Controller
  - Fully compliant with USB Specification Revision 2.0
  - Supports HS (480 Mbps) and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Integrated USB 2.0 PHY
  - Remote wakeup supported
- High-Performance 10/100/1000 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u/802.3ab
  - Integrated Ethernet MAC and PHY
  - 10BASE-T, 100BASE-TX, and 1000BASE-T support
  - Full- and half-duplex capability (only full-duplex operation at 1000Mbps)
  - Full-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - 9 KB jumbo frame support
  - Automatic payload padding and pad removal
  - Loop-back modes
  - Supports checksum offloads (IPv4, IPv6, TCP, UDP)
  - Supports Microsoft NDIS 6.2 large send offload
  - Supports IEEE 802.1q VLAN tagging
    - Ability to add and strip IEEE 802.1q VLAN tags
    - VLAN tag based packet filtering (all 4096 VIDs)
  - Flexible address filtering modes
    - 33 exact matches (unicast or multicast)
    - 512-bit hash filter for multicast frames
    - Pass all multicast
    - Promiscuous unicast/multicast modes
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
    - Perfect DA frame, wakeup frame, magic packet, broadcast frame, IPv6 & IPv4 TCP SYN
    - 8 programmable 128-bit wakeup frame filters
  - ARP and NS offload
  - PME pin support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for 5 status LEDs
  - Supports various statistical counters
- Power and I/Os
  - Various low power modes
  - 12 GPIOs
  - Supports bus-powered and self-powered operation
  - Variable voltage I/O supply (2.5V/3.3V)
- Miscellaneous Features
  - EEPROM Controller
  - IEEE 1149.1 (JTAG) Boundary Scan
  - Requires single 25 MHz crystal
- Software
  - Windows XP/ Vista / Windows 7 Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM/Manufacturing Utility for Windows/DOS
  - PXE Support
  - DOS ODI Driver
- Packaging
  - 56-pin QFN (8x8 mm), RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

Order Numbers:

LAN7500-ABZJ for 56 pin, QFN RoHS compliant package (0 to +70°C temp range)

LAN7500i-ABZJ for 56 pin, QFN RoHS compliant package (-40 to +85°C temp range)

This product meets the halogen maximum concentration values per IEC61249-2-21

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Chapter 1 Introduction

1.1 Block Diagram

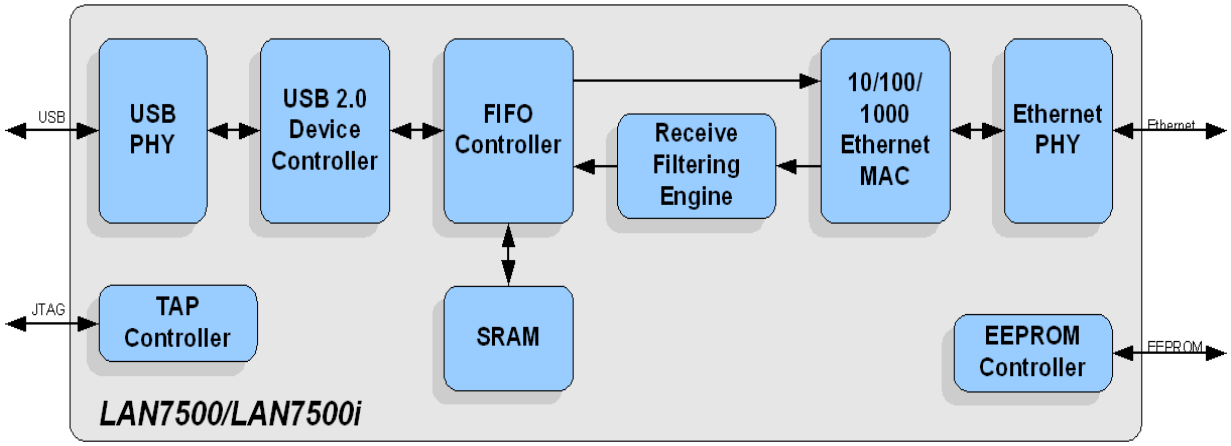


Figure 1.1 LAN7500/LAN7500i System Diagram

1.1.1 Overview

The LAN7500/LAN7500i is a high performance Hi-Speed USB 2.0 to 10/100/1000 Ethernet controller. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators, USB to Ethernet dongles, and test instrumentation, the device is a high performance and cost competitive USB to Ethernet connectivity solution.

The LAN7500/LAN7500i contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY, Hi-Speed USB 2.0 device controller, TAP controller, EEPROM controller, and a FIFO controller with a total of 32 KB of internal packet buffering.

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The device implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab standards. ARP and NS offload is also supported.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

1.1.2 USB

The USB portion of the LAN7500/LAN7500i integrates a Hi-Speed USB 2.0 device controller and USB PHY.

The USB device controller contains a USB low-level protocol interpreter which implements the USB bus protocol, packet generation/extraction, PID/Device ID parsing, and CRC coding/decoding, with autonomous error handling. The USB device controller is capable of operating in USB 2.0 Hi-Speed and Full-Speed compliant modes and contains autonomous protocol handling functions such as handling of suspend/resume/reset conditions, remote wakeup, and stall condition clearing on Setup packets. The USB device controller also autonomously handles error conditions such as retry for CRC and data toggle errors, and generates NYET, STALL, ACK and NACK handshake responses, depending on the endpoint buffer status.

The LAN7500/LAN7500i implements four USB endpoints: Control, Interrupt, Bulk-in, and Bulk-out. The Bulk-in and Bulk-out Endpoints allow for Ethernet reception and transmission respectively. Implementation of vendor-specific commands allows for efficient statistics gathering and access to the device's system control and status registers.

1.1.3 FIFO Controller

The FIFO controller uses two internal SRAMs to buffer RX and TX traffic. Bulk-Out packets from the USB controller are directly stored into the TX buffer. The FIFO Controller is responsible for extracting Ethernet frames from the USB packet data and passing the frames to the MAC. Received Ethernet Frames are filtered by the Receive Filtering Engine and frames meeting the filtering constraints are stored into the RX buffer and become the basis for bulk-in packets.

1.1.4 Ethernet

The LAN7500/LAN7500i integrates an IEEE 802.3/802.3u/802.3ab compliant PHY for twisted pair Ethernet applications and a 10/100/1000 Ethernet Media Access Controller (MAC).

The PHY can be configured for 1000 Mbps (1000BASE-T), 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) operation in Full-Duplex mode. It can be configured for 100 Mbps or 10 Mbps operation in Half Duplex mode. The PHY block includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the Integrated PHY.

The Ethernet MAC/PHY supports numerous power management wakeup features, including "Magic Packet", "Wake on LAN", and "Link Status Change". Microsoft NDIS 6.2 and Windows 7 compliant ARP and NS offload support is also provided.The device will respond to an NS or ARP request by generating and transmitting a response. When received in a SUSPEND state, an NS or ARP request will not result in the generation of a wake event. Additionally, five status LEDs are supported.

1.1.5 Frame Filtering

The LAN7500/LAN7500i Receive Filtering Engine performs frame filtering. It supports 33 perfect address filters. These can be used to filter either the Ethernet source address or destination address. Additional address filtering is available via a 512-bit hash filter. The hash filter can perform unicast or multicast filtering.

VLAN tagged frames can be filtered via the VLAN ID. A 4096-bit table exists to support all possible VLAN IDs. The VLAN type can be programmed. Double tagging is supported.

1.1.6 Host Offloading

The LAN7500/LAN7500i supports a variety of TCP/UDP/IP checksum offloads to reduce the burden on the host processor. For Ethernet receive frames, the device can be configured to validate the IP checksum and UDP/TCP checksum. Both IPv4 and IPv6 packets are supported. A raw checksum across the layer 3 packet can also be provided.

For Ethernet transmitted frames, the device can be configured to calculate the IP checksum and UDP/TCP checksum. Additionally, Large Send Offload (LSO) is supported to further reduce host CPU loading.

1.1.7 Power Management

The LAN7500/LAN7500i features four variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2, and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, “Wake On LAN”, “Magic Packet”, and “PHY Link Up” remote wakeup events. It, however, consumes the most power.
- **SUSPEND1:** Supports GPIO and “Link Status Change” for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** Supports GPIO, “Good Packet”, and “PHY Link Up” remote wakeup events. A “Good Packet” is a received frame that is free of errors and passes certain filtering constraints independent of those imposed on “Wake On LAN” and “Magic Packet” frames. This suspend state consumes power at a level similar to the NORMAL state, however, it allows for power savings in the Host CPU, which greatly exceeds that of the LAN7500/LAN7500i. The driver may place the device in this state after prolonged periods of not receiving any Ethernet traffic.

1.1.8 EEPROM Controller

The LAN7500/LAN7500i contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon pin reset, or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and MAC address.

Custom operation without EEPROM is also provided.

1.1.9 General Purpose I/O

Twelve GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN7500/LAN7500i is in a suspended state.

1.1.10 TAP Controller

IEEE 1149.1 compliant TAP Controller supports boundary scan and various test modes.

The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of four pins (TDO, TDI, TCK and TMS) and includes a state machine, data register array, and an instruction register. The JTAG pins are described in Table 2.3, “JTAG Pins,” on page 14. The JTAG interface conforms to the IEEE Standard 1149.1 - *1990 Standard Test Access Port (TAP) and Boundary-Scan Architecture*.

All input and output data is synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.

The JTAG logic is reset when the TMS and TDI pins are high for five TCK periods.

The implemented IEEE 1149.1 instructions and their op codes are shown in Table 1.1.

Table 1.1 IEEE 1149.1 Op Codes

INSTRUCTION	OP CODE	COMMENT
Bypass	111	Mandatory Instruction
Sample/Preload	010	Mandatory Instruction
EXTEST	000	Mandatory Instruction
Clamp	011	Optional Instruction
HIGHZ	100	Optional Instruction
IDCODE	001	Optional Instruction

Note: All digital I/O pins support IEEE 1149.1 operation. Analog pins and the XO pin do not support IEEE 1149.1 operation.

1.1.11 Test Features

Read/Write access to internal SRAMs is provided via the devices registers. JTAG based USB BIST is available.

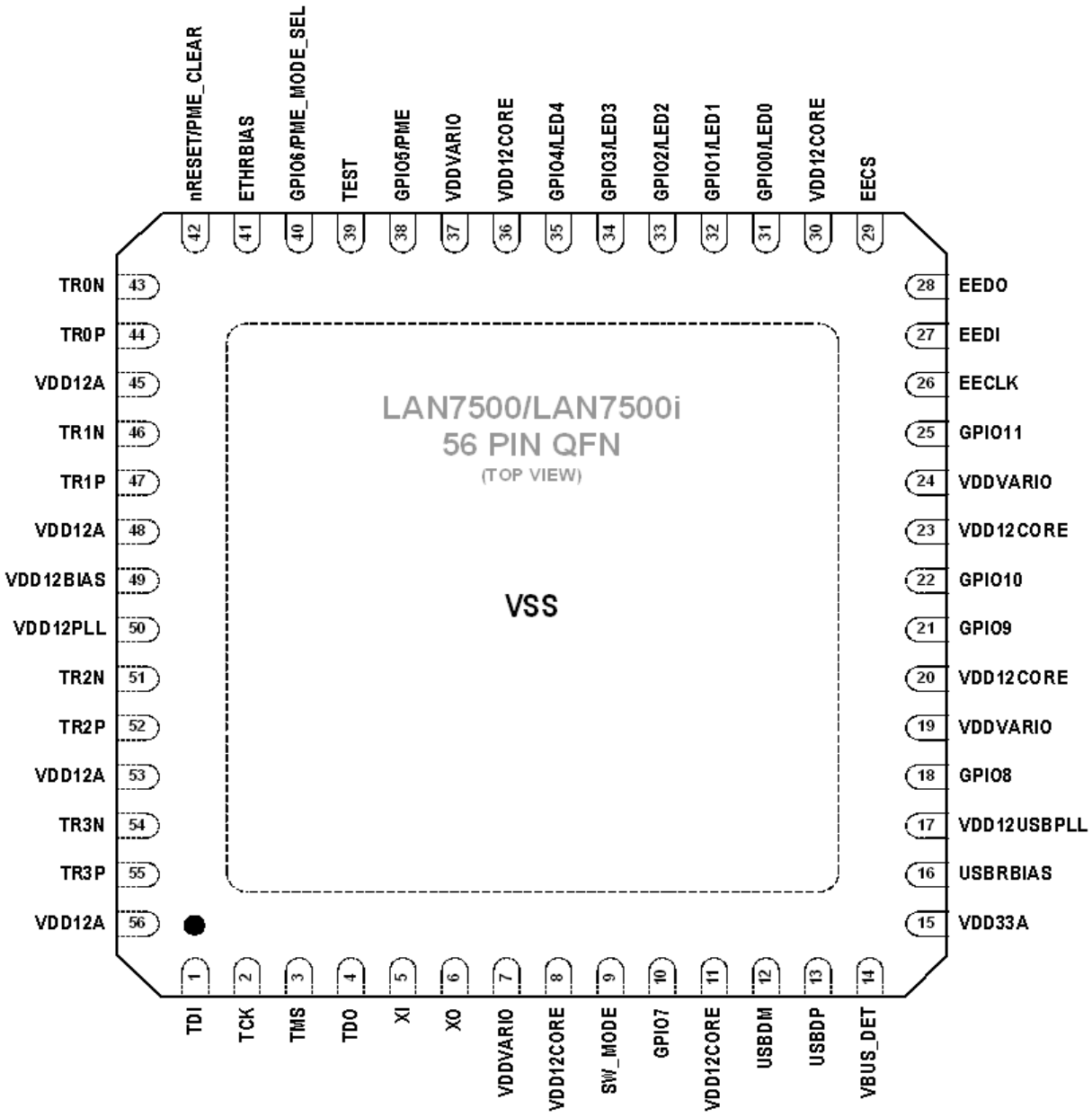
1.1.12 System Software

LAN7500/LAN7500i software drivers are available for the following operating systems:

- Windows XP/ Vista/ Windows 7
- Win CE
- Linux
- MAC OS
- DOS ODI

In addition, an EEPROM programming utility is available for configuring the external EEPROM. PXE Support is also available.

Chapter 2 Pin Description and Configuration



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 2.1 LAN7500/LAN7500i 56-QFN Pin Assignments (TOP VIEW)

Table 2.1 GPIO Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Indicator LED0	LED0	VOD8	Used in conjunction with LED1. May be programmed to indicate Link and Speed or Link and Speed and Activity.
	General Purpose I/O 0	GPIO0	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** This pin is configured as a GPIO by default.
1	Indicator LED1	LED1	VOD8	Used in conjunction with LED0. May be programmed to indicate Ethernet Link and Speed or Link and Speed and Activity.
	General Purpose I/O 1	GPIO1	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** This pin is configured as a GPIO by default.
1	Indicator LED2	LED2	VOD8	May be programmed to indicate Ethernet Link and Activity or just Activity.
	General Purpose I/O 2	GPIO2	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** This pin is configured as a GPIO by default.
1	Indicator LED3	LED3	VOD8	May be programmed for use as an Ethernet Link indicator.
	General Purpose I/O 3	GPIO3	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. **Note:** This pin is configured as a GPIO by default.
1	Indicator LED4	LED4	VOD8	May be programmed to indicate Ethernet Full Duplex operation.
	General Purpose I/O 4	GPIO4	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	PME	PME	VO8/ VOD8	This pin may be used to signal PME when PME mode of operation is in effect. Refer to Chapter 4, "PME Operation," on page 30 for additional information.
	General Purpose I/O 5	GPIO5	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.

Table 2.1 GPIO Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	PME Mode Select	PME_MODE_SEL	VIS (PU)	This pin may serve as the PME_MODE_SEL input when PME mode of operation is in effect. Refer to Chapter 4, "PME Operation," on page 30 for additional information.
	General Purpose I/O 6	GPIO6	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 7	GPIO7	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 8	GPIO8	VIS/VO6/ VOD6 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 9	GPIO9	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 10	GPIO10	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
1	General Purpose I/O 11	GPIO11	VIS/VO8/ VOD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.

Table 2.2 EEPROM Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	EEPROM Data In	EEDI	VIS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	VO8	This pin drives the EEDI input of the external EEPROM.
1	EEPROM Chip Select	EECS	VO8	This pin drives the chip select output of the external EEPROM. **Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's datasheet for additional information.
1	EEPROM Clock	EECLK	VO8	This pin drives the EEPROM clock of the external EEPROM.

Table 2.3 JTAG Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	JTAG Test Data Out	TDO	VO8	JTAG (IEEE 1149.1) data output.
1	JTAG Test Data Input	TDI	VIS (PU)	JTAG (IEEE 1149.1) data input. **Note:** When not used, tie this pin to VDDVARIO.
1	JTAG Test Clock	TCK	VIS (PD)	JTAG (IEEE 1149.1) test clock. **Note:** When not used, tie this pin to VSS.
1	JTAG Test Mode Select	TMS	VIS (PU)	JTAG (IEEE 1149.1) test mode select. **Note:** When not used, tie this pin to VDDVARIO.

Table 2.4 USB Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	USB DMINUS	USBDM	AIO	**Note:** The functionality of this pin may be swapped to USB DPLUS via the Port Swap bit of Configuration Flags 0.
1	USB DPLUS	USBDP	AIO	**Note:** The functionality of this pin may be swapped to USB DMINUS via the Port Swap bit of Configuration Flags 0.
1	External USB Bias Resistor.	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.

Table 2.5 Ethernet PHY Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.
1	Ethernet TX/RX Positive Channel 0	TR0P	AIO	Transmit/Receive Positive Channel 0.
1	Ethernet TX/RX Negative Channel 0	TR0N	AIO	Transmit/Receive Negative Channel 0.
1	Ethernet TX/RX Positive Channel 1	TR1P	AIO	Transmit/Receive Positive Channel 1.
1	Ethernet TX/RX Negative Channel 1	TR1N	AIO	Transmit/Receive Negative Channel 1.
1	Ethernet TX/RX Positive Channel 2	TR2P	AIO	Transmit/Receive Positive Channel 2.
1	Ethernet TX/RX Negative Channel 2	TR2N	AIO	Transmit/Receive Negative Channel 2.
1	Ethernet TX/RX Positive Channel 3	TR3P	AIO	Transmit/Receive Positive Channel 3.
1	Ethernet TX/RX Negative Channel 3	TR3N	AIO	Transmit/Receive Negative Channel 3.
1	External PHY Bias Resistor	ETHRBIAS	AI	Used for the internal bias circuits. Connect to an external 8.06K 1.0% resistor to ground.

Table 2.6 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	System Reset	nRESET	VIS (PU)	This active-low pin allows external hardware to reset the device. **Note:** Assertion of nRESET is required following power-on.
	PME Clear	PME_CLEAR	VIS (PU)	This pin may serve as the PME_CLEAR input when PME mode of operation is in effect. Refer to Chapter 4, "PME Operation," on page 30 for additional information.
1	Detect Upstream VBUS Power	VBUS_DET	IS_5V (PD)	Detects state of upstream bus power. For bus powered operation, this pin must be tied to VDD33A. For self powered operation, refer to the LAN7500/LAN7500i reference schematics.
1	Test	TEST	-	This pin must always be connected to VSS for proper operation.
1	Switching Regulator Mode	SW_MODE	VO6	When asserted, this pin places the external switching regulator into power saving mode. **Note:** The SW_MODE_POL and SW_MODE_SEL bits of Configuration Flags 1 control the polarity of the pin and when it is asserted, respectively.

Table 2.7 I/O Power Pins, Core Power Pins, and Ground Pad

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+3.3V Analog Power Supply Input	VDD33A	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for connection information.
4	+3.3V/+2.5V I/O Power Supply Input	VDDVARIO	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for connection information.
6	Digital Core +1.2V Power Supply Input	VDD12CORE	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for connection information.
1	USB PLL +1.2V Power Supply Input	VDD12USBPLL	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for additional connection information.
4	Ethernet +1.2V Port Power Supply Input For Channels 0-3	VDD12A	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for additional connection information.

Table 2.7 I/O Power Pins, Core Power Pins, and Ground Pad (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet +1.2V Bias Power Supply Input	VDD12BIAS	P	Refer to Chapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for additional connection information.
1	Ethernet PLL +1.2V Power Supply Input	VDD12PLL	P	Refer toChapter 6, "Application Diagrams," on page 36 and the LAN7500/LAN7500i reference schematics for additional connection information.
Exposed pad on package bottom (Figure 2.1)	Ground	VSS	P	Common Ground

2.1 Pin Assignments

Table 2.8 56-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	TDI	15	VDD33A	29	EECS	43	TR0N
2	TCK	16	USBRBIAS	30	VDD12CORE	44	TR0P
3	TMS	17	VDD12USBPLL	31	GPIO0/LED0	45	VDD12A
4	TDO	18	GPIO8	32	GPIO1/LED1	46	TR1N
5	XI	19	VDDVARIO	33	GPIO2/LED2	47	TR1P
6	XO	20	VDD12CORE	34	GPIO3/LED3	48	VDD12A
7	VDDVARIO	21	GPIO9	35	GPIO4/LED4	49	VDD12BIAS
8	VDD12CORE	22	GPIO10	36	VDD12CORE	50	VDD12PLL
9	SW_MODE	23	VDD12CORE	37	VDDVARIO	51	TR2N
10	GPIO7	24	VDDVARIO	38	GPIO5/PME	52	TR2P
11	VDD12CORE	25	GPIO11	39	TEST	53	VDD12A
12	USBDM	26	EECLK	40	GPIO6/ PME_MODE_SEL	54	TR3N
13	USBDP	27	EEDI	41	ETHRBIAS	55	TR3P
14	VBUS_DET	28	EEDO	42	nRESET/ PME_CLEAR	56	VDD12A
EXPOSED PAD MUST BE CONNECTED TO VSS							

2.2 Buffer Types

Table 2.9 Buffer Types

BUFFER TYPE	DESCRIPTION
VIS	Variable voltage Schmitt-triggered Input
IS_5V	5V Tolerant Schmitt-triggered Input
VO6	Variable voltage output with 6mA sink and 6mA source
VOD6	Variable voltage open-drain output with 6mA sink
VO8	Variable voltage output with 8mA sink and 8mA source
VOD8	Variable voltage open-drain output with 8mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN7500/LAN7500i. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to LAN7500/LAN7500i. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 3 EEPROM Controller (EPC)

LAN7500/LAN7500i may use an external EEPROM to store the default values for the USB descriptors and the MAC address. The EEPROM controller supports most “93C56 or 93C66” type 256/512 byte EEPROMs. A total of nine address bits are used for connection to the device.

Note: A 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation must be used.

The MAC address is used as the default Ethernet MAC address and is loaded into the device’s MAC address registers. If a properly configured EEPROM is not detected, it is the responsibility of the Host LAN Driver to set the IEEE addresses.

After a system-level reset occurs, the device will load the default values from a properly configured EEPROM. The device will not accept USB transactions from the Host until this process is completed.

The device’s EEPROM controller also allows the Host system to read, write and erase the contents of the Serial EEPROM.

3.1 EEPROM Format

Table 3.1 illustrates the format in which data is stored inside of the EEPROM.

Note the EEPROM offsets are given in units of 16-bit word offsets. A length field with a value of zero indicates that the field does not exist in the EEPROM. The device will use the field’s HW default value in this case.

Note: For the device descriptor, the only valid values for the length are 0 and 18.

Note: For the configuration and interface descriptor, the only valid values for the length are 0 and 18.

Note: The EEPROM programmer must ensure that if a string descriptor does not exist in the EEPROM, the referencing descriptor must contain 00h for the respective string index field.

Note: If all string descriptor lengths are zero, then a Language ID will not be supported.

Table 3.1 EEPROM Format

EEPROM ADDRESS	EEPROM CONTENTS
00h	A5h (EEPROM Programmed Indicator)
01h	MAC Address [7:0]
02h	MAC Address [15:8]
03h	MAC Address [23:16]
04h	MAC Address [31:24]
05h	MAC Address [39:32]
06h	MAC Address [47:40]
07h	Full-Speed Polling Interval for Interrupt Endpoint
08h	Hi-Speed Polling Interval for Interrupt Endpoint
09h	Configuration Flags 0
0Ah	Language ID Descriptor [7:0]

Table 3.1 EEPROM Format (continued)

0Bh	Language ID Descriptor [15:8]
0Ch	Manufacturer ID String Descriptor Length (bytes)
0Dh	Manufacturer ID String Descriptor EEPROM Word Offset
0Eh	Product Name String Descriptor Length (bytes)
0Fh	Product Name String Descriptor EEPROM Word Offset
10h	Serial Number String Descriptor Length (bytes)
11h	Serial Number String Descriptor EEPROM Word Offset
12h	Configuration String Descriptor Length (bytes)
13h	Configuration String Descriptor Word Offset
14h	Interface String Descriptor Length (bytes)
15h	Interface String Descriptor Word Offset
16h	Hi-Speed Device Descriptor Length (bytes)
17h	Hi-Speed Device Descriptor Word Offset
18h	Hi-Speed Configuration and Interface Descriptor Length (bytes)
19h	Hi-Speed Configuration and Interface Descriptor Word Offset
1Ah	Full-Speed Device Descriptor Length (bytes)
1Bh	Full-Speed Device Descriptor Word Offset
1Ch	Full-Speed Configuration and Interface Descriptor Length (bytes)
1Dh	Full-Speed Configuration and Interface Descriptor Word Offset
1Eh	GPIO[7:0] Wakeup Enables Bit x = 0 -> GPIOx Pin Disabled for Wakeup Use. Bit x = 1 -> GPIOx Pin Enabled for Wakeup Use.
1Fh	GPI0[11:8] Wakeup Enables Bit x = 0 -> GPIO(x+8) Pin Disabled for Wakeup Use. Bit x = 1 -> GPIO(x+8) Pin Enabled for Wakeup Use. **Note:** Bits 7:4 Unused.
20h	GPIO PME Flags
21h	Configuration Flags 1

Note: EEPROM byte addresses past 21h can be used to store data for any purpose assuming these addresses are not used for descriptor storage.

Table 3.2 describes the Configuration Flags 0 byte. If a configuration descriptor exists in the EEPROM, it will override the values in Configuration Flags 0.

Table 3.2 Configuration Flags 0

<table>
<tr><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>Port Swap
This bit facilitates swapping the mapping of USBDP and USBDM.

0 = USBDP maps to the USB D+ line and USBDM maps to the USB D- line.
1 = USBDP maps to the USB D- line. USBDM maps to the USB D+ line.</td></tr>
<tr><td>6:5</td><td>PHY Boost
This field provides the ability to boost the electrical drive strength of the HS output current to the upstream port.

00 = Normal electrical drive strength.
01 = Elevated electrical drive strength (+4% boost).
10 = Elevated electrical drive strength (+8% boost).
11 = Elevated electrical drive strength (+12% boost).</td></tr>
<tr><td>4</td><td>Duplex Detection
This bit determines whether duplex operational mode is detected automatically or manually set.

0 = Manual
1 = Automatic</td></tr>
<tr><td>3</td><td>Speed Detection
This bit determines whether operational speed is detected automatically or manually set.

0 = Manual
1 = Automatic</td></tr>
<tr><td>2</td><td>SPD_LED_FUNCTION
This bit specifies the functionality of speed LEDs (LED0 and LED1). The Speed LEDs’ behavior is determined by line speed and the setting of this bit, as indicated in following table:

<table>
<tr><th>SPD_LED_FUNCTION</th><th>SPEED (Mbps)</th><th>LED0</th><th>LED1</th></tr>
<tr><td>0</td><td>No Link</td><td>Off</td><td>Off</td></tr>
<tr><td>0</td><td>10</td><td>On</td><td>Off</td></tr>
<tr><td>0</td><td>100</td><td>Off</td><td>On</td></tr>
<tr><td>0</td><td>1000</td><td>On</td><td>On</td></tr>
<tr><td>1</td><td>No Link</td><td>Off</td><td>Off</td></tr>
<tr><td>1</td><td>10</td><td>Blink</td><td>Off</td></tr>
<tr><td>1</td><td>100</td><td>Off</td><td>Blink</td></tr>
<tr><td>1</td><td>1000</td><td>Blink</td><td>Blink</td></tr>
</table>
When SPD_LED_FUNCTION = 0, the LEDs function solely as Link and Speed LEDs. When SPD_LED_FUNCTION = 1, the LEDs function as Link and Speed and Activity LEDs. In those cases, the table entry “Blink” indicates the LED will remain on when no transmit or receive activity is detected and will blink at an 80 mS rate whenever TX or RX activity is detected.

Note: GPIOEN[1:0] in Configuration Flags 1 must be set in order to properly control speed LED operation. If only one of the bits is set, then untoward operation and unexpected results may occur. If both bits are clear, then SPD_LED_FUNCTION is ignored.</td></tr>
</table>

Table 3.2 Configuration Flags 0 (continued)

BITS	DESCRIPTION
1	**Remote Wakeup Support** 0 = Device does not support remote wakeup. 1 = Device supports remote wakeup.
0	**Power Method** 0 = Device is bus powered. 1 = Device is self powered.

Table 3.3 describes the Configuration Flags 1.

Table 3.3 Configuration Flags 1

BITS	DESCRIPTION
7	**LED2_FUNCTION** This bit specifies the functionality of LED2. 0 = Link and Activity LED. 1 = Activity LED. **Note:** This bit is ignored if GPIOEN2 is not set in this flag byte.
6:2	**GPIOEN[4:0]** This field specifies GPIO/LED functionality for GPIO[4:0]. 0 = GPIOn Pin Functions as GPIO pin. 1 = GPIOn Pin Functions as LED.
1	**SW_MODE_SEL** This bit specifies the modes of operation during which the SW_MODE pin will be asserted. 0 = SW_MODE asserted in SUSPEND2. 1 = SW_MODE asserted in SUSPEND2, SUSPEND1, and NetDetach.
0	**SW_MODE_POL** This bit selects the polarity of the SW_MODE pin. 0 = Active low. 1 = Active high.

Table 3.4 describes the GPIO PME flags.

Table 3.4 GPIO PME Flags

BITS	DESCRIPTION
7	**GPIO PME Enable** Setting this bit enables the assertion of the GPIO5 pin, as a result of a Wakeup (GPIO) pin, Magic Packet, or PHY Link Up. The host processor may use the GPIO5 pin to asynchronously wake up, in a manner analogous to a PCI PME pin. 0 = The device does not support GPIO PME signaling. 1 = The device supports GPIO PME signaling. **Note:** When this bit is 0, the remaining GPIO PME parameters in this flag byte are ignored.
6	**GPIO PME Configuration** This bit selects whether the GPIO PME is signaled on the GPIO5 pin as a level or a pulse. If pulse is selected, the duration of the pulse is determined by the setting of the GPIO PME Length bit of this flag byte. The level of the signal or the polarity of the pulse is determined by the GPIO PME Polarity bit of this flag byte. 0 = GPIO PME is signaled via a level. 1 = GPIO PME is signaled via a pulse. **Note:** If GPIO PME Enable is 0, this bit is ignored.
5	**GPIO PME Length** When the GPIO PME Configuration bit of this flag byte indicates that the GPIO PME is signaled by a pulse on the GPIO5 pin, this bit determines the duration of the pulse. 0 = GPIO PME pulse length is 1.5 mS. 1 = GPIO PME pulse length is 150 mS. **Note:** If GPIO PME Enable is 0, this bit is ignored.
4	**GPIO PME Polarity** Specifies the level of the signal or the polarity of the pulse used for GPIO PME signaling. 0 = GPIO PME signaling polarity is low. 1 = GPIO PME signaling polarity is high. **Note:** If GPIO PME Enable is 0, this bit is ignored.
3	**GPIO PME Buffer Type** This bit selects the output buffer type for GPIO5. 0 = Open drain driver / open source 1 = Push-Pull driver **Note:** Buffer Type = 0, Polarity = 0 implies Open Drain Buffer Type = 0, Polarity = 1 implies Open Source **Note:** If GPIO PME Enable is 0, this bit is ignored.
2	**GPIO PME WOL Select** Four types of wakeup events are supported; Magic Packet, Perfect DA, PHY Link Up, and Wakeup Pin(s) assertion. Wakeup Pin(s) are selected via the GPIO Wakeup Enables specified in bytes 1Eh and 1Fh of the EEPROM. This bit selects whether WOL events or Link Up wakeup events are supported. 0 = WOL event wakeup supported. 1 = PHY linkup wakeup supported. **Note:** If WOL is selected, the PME Magic Packet Enable and PME Perfect DA Enable bits determine the WOL event(s) that will cause a wakeup. **Note:** If GPIO PME Enable is 0, this bit is ignored.

Table 3.4 GPIO PME Flags (continued)

BITS	DESCRIPTION
1	**PME Magic Packet Enable** When GPIO PME WOL Select indicates WOL is selected, this bit enables/disables Magic Packet detection and wakeup. 0 = Magic Packet event wakeup disabled. 1 = Magic Packet event wakeup enabled. **Note:** This bit is ignored if GPIO PME WOL Select indicates WOL event wakeup not supported.
0	**PME Perfect DA Enable** When GPIO PME WOL Select indicates WOL is selected, this bit enables/disables Perfect DA detection and wakeup. 0 = Perfect DA event wakeup disabled. 1 = Perfect DA event wakeup enabled. **Note:** This bit is ignored if GPIO PME WOL Select indicates WOL event wakeup not supported.

3.2 EEPROM Defaults

The signature value of 0xA5 is stored at address 0. A different signature value indicates to the EEPROM controller that no EEPROM or an un-programmed EEPROM is attached to the device. In this case, the hardware default values are used, as shown in Table 3.5.

Table 3.5 EEPROM Defaults

FIELD	DEFAULT VALUE
MAC Address	FFFFFFFFFFFFh
Full-Speed Polling Interval (mS)	01h
Hi-Speed Polling Interval (mS)	04h
Configuration Flags 0	1Bh
Maximum Power (mA)	FAh
Vendor ID	0424h
Product ID	7500h

Note: Refer to the LAN7500/LAN7500i Vendor/Product ID application note for details on proper usage of these fields.

3.3 EEPROM Auto-Load

Certain system level resets (USB reset, nRESET, and SRST) cause the EEPROM contents to be loaded into the device. After a reset, the EEPROM controller attempts to read the first byte of data from the EEPROM. If the value A5h is read from the first address, then the EEPROM controller will assume that a programmed external Serial EEPROM is present.

Note: The USB reset only loads the MAC address.

3.4 An Example of EEPROM Format Interpretation

Table 3.6 and Table 3.7 provide an example of how the contents of a EEPROM are formatted. Table 3.6 is a dump of the EEPROM memory (256-byte EEPROM), while Table 3.7 illustrates, byte by byte, how the EEPROM is formatted. The industrial version of the device is used in the example.

Table 3.6 Dump of EEPROM Memory

OFFSET BYTE	VALUE (HEX)
0000h	A5 12 34 56 78 9A BC 01
0008h	04 1E 09 04 0A 0F 12 14
0010h	10 1D 00 00 00 00 12 25
0018h	12 2E 12 37 12 40 00 04
0020h	8A 7C 0A 03 53 00 4D 00
0028h	53 00 43 00 12 03 4C 00
0030h	41 00 4E 00 37 00 35 00
0038h	30 00 30 00 69 00 10 03
0040h	30 00 30 00 30 00 35 00
0048h	31 00 32 00 33 00 12 01
0050h	00 02 FF 00 FF 40 24 04
0058h	00 75 00 01 01 02 03 01
0060h	09 02 27 00 01 01 00 A0
0068h	FA 09 04 00 00 03 FF 00
0070h	FF 00 12 01 00 02 FF 00
0078h	FF 40 24 04 00 75 00 01
0080h	01 02 03 01 09 02 27 00
0088h	01 01 00 A0 FA 09 04 00
0090h - 00FFh	00 03 FF 00 FF 00 .....