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LAN7800

SuperSpeed USB 3.1 Gen 1 to 10/100/1000 Ethernet Controller

Highlights

- Single Chip SuperSpeed (SS) USB 3.1 Gen 1 to 10/100/1000 Ethernet Controller
  - Integrated Gigabit PHY with HP Auto-MDIX
  - Integrated 10/100/1000 Ethernet MAC (Full-Duplex Support)
  - Integrated USB 3.1 Gen 1 SS Device Controller and PHY
- Low Power Consumption
  - Compliant with Energy Efficient Ethernet IEEE 802.3az
  - Wake on LAN support (WoL)
- Configuration via One Time Programmable (OTP) Memory
- Cable Diagnostic Support
- NetDetach provides automatic USB attach/detach when Ethernet cable is connected/removed

Target Applications

- Automotive Infotainment
- Notebook/Tablet Docking Stations
- Detachable Laptops
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Embedded Systems / CE Devices
- Set-Top Boxes / Video Recorders
- Test Instrumentation / Industrial

System Considerations

- Power and I/Os
  - Multiple power management features
  - 8 GPIOs
  - Supports bus and self-powered operation
  - Variable voltage I/O supply (1.8V-3.3V)
- Software Support
  - Windows 7, 8, 8.1, and 10 driver
  - Linux driver
  - Mac OS driver
  - UEFI support
  - PXE support
  - Windows line command OTP/EEPROM programming and testing utility
- Packaging
  - Pb-free RoHS compliant 48-pin SQFN (6 x 6 mm)
  - Pb-free RoHS compliant 48-pin SQFN (7 x 7 mm)
- Environmental
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

Key Benefits

- USB 3.1 Gen 1 Device Controller
  - Supports SS (5 Gbps), HS (480 Mbps), and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Remote wakeup supported
- 10/100/1000 Ethernet Controller
  - Compliant with IEEE802.3/802.3u/802.3ab/802.3az
    - -10BASE-T/100BASE-TX/1000BASE-T support
    - -Full- and half-duplex capability (only full-duplex operation at 1000 Mbps)
  - Controller Modes
    - -Microsoft AOAC support (Always On Always Connected)
    - -Supports Microsoft NDIS 6.2 large send offload
    - -Full-duplex flow control
    - -Loop-back modes
    - -Supports IEEE 802.1q VLAN tagging
    - -VLAN tag based packet filtering (all 4096 tags)
    - -Flexible address filtering modes
      - -33 exact matches (unicast or multicast)
      - -512-bit hash filter for multicast frames
      - -Pass all multicast
      - -Promiscuous unicast/multicast modes
      - -Inverse filtering
      - -Pass all incoming with status report
    - -Supports various statistical counters
    - -PME pin support
  - Integrated Ethernet PHY
    - -Auto-negotiation
    - -Automatic polarity detection and correction
    - -Link status change wake-up detection
    - -Low EMI drivers with integrated line side termination resistor
  - Frame Features
    - -Supports 32 wake-up frame patterns
    - -Preamble generation and removal
    - -Automatic 32-bit CRC generation and checking
    - -9 KB jumbo frame support
    - -Automatic payload padding and pad removal
    - -Supports Rx/Tx checksum offloads (IPv4, IPv6, TCP, UDP, IGMP, ICMP)
    - -Ability to add and strip IEEE 802.1q VLAN tags

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
10BASE-T	10 Mbps Ethernet, IEEE 802.3 compliant
100BASE-TX	100 Mbps Fast Ethernet, IEEE802.3u compliant
1000BASE-T	100 Mbps Fast Ethernet, IEEE802.3ab compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
ALR	Address Logic Resolution
AN	Auto-Negotiation
AOAC	Always on Always Connected
ARP	Address Resolution Protocol
BELT	Best Effort Latency Tolerance
BLW	Baseline Wander
Byte	8 bits
CPM	Clocks and Power Management
CSMA/CD	Carrier Sense Multiple Access/Collision Detect
CSR	Control and Status Registers
CTR	Counter
DA	Destination Address
DWORD	32 bits
EC	Embedded Controller
EEE	Energy Efficient Ethernet
EP	USB Endpoint
EPC	EEPROM Controller
FCS	Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction.
FCT	FIFO Controller
FIFO	First In First Out buffer
FS	Full Speed
FSM	Finite State Machine
FW	Firmware
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O
GPHY	Gigabit Ethernet Physical Layer
Host	External system (Includes processor, application software, etc.)
HS	High Speed
HW	Hardware. Refers to function implemented by digital logic.
IGMP	Internet Group Management Protocol
Inbound	Refers to data input to the device from the host
LDO	Linear Drop-Out Regulator
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writ-ing a zero.

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
LFPS	Low Frequency Periodic Signal
LFSR	Linear Feedback Shift Register
LPM	Link Power Management
lsb	Least Significant Bit
LSB	Least Significant Byte
LTM	Latency Tolerance Messaging
MAC	Media Access Controller
MDI	Medium Dependent Interface
MDIX	Media Dependent Interface with Crossover
MEF	Multiple Ethernet Frames
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MIL	MAC Interface Layer
MLD	Multicast Listening Discovery
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
msb	Most Significant Bit
MSB	Most Significant Byte
NRZI	Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0”
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
OUI	Organizationally Unique Identifier
Outbound	Refers to data output from the device to the host
PCS	Physical Coding Sublayer
PHY	Physical Layer
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PMD	Physical Medium Dependent
PME	Power Management Event
PMIC	Power Management IC
POR	Power on Reset
PTP	Precision Time Protocol
QWORD	64 bits
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RFE	Receive Filtering Engine
RGMII	Reduced Gigabit Media Independent Interface
RMON	Remote Monitoring
RMII	Reduced Media Independent Interface
RST	Reset
RTC	Real-Time Clock

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
SA	Source Address
SCSR	System Control and Status Registers
SEF	Single Ethernet Frame
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame.
SIPO	Serial In Parallel Out
SMI	Serial Management Interface
SMNP	Simple Network Management Protocol
SQE	Signal Quality Error (also known as “heartbeat”)
SS	SuperSpeed
SSD	Start of Stream Delimiter
TMII	Turbo Media Independent Interface
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks
URX	USB Bulk-Out Receiver
USB	Universal Serial Bus
UTX	USB Bulk-In Transmitter
UUID	Universally Unique IDentifier
VSM	Vendor Specific Messaging
WORD	16 bits
ZLP	Zero Length USB Packet

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
VIS	Variable voltage Schmitt-triggered input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog Input
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
RS	**Read to Set:** This bit is set on read.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
WC	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect
WAC	**Write Anything to Clear:** Writing anything clears the value.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After it is read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition.
NALR	**Not Affected by Lite Reset.** The state of NASR bits do not change on assertion of a lite reset.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

2.0 INTRODUCTION

2.1 General Description

The LAN7800 is a high performance SuperSpeed USB 3.1 Gen 1 to 10/100/1000 Ethernet controller with an integrated 10/100/1000 Ethernet PHY. With applications ranging from notebook/tablet docking stations, set-top boxes, and PVRs, to USB port replicators, USB to Ethernet dongles, embedded systems, and test instrumentation, the LAN7800 is a high performance and cost effective USB to Ethernet connectivity solution.

The LAN7800 contains an integrated 10/100/1000 Ethernet MAC and PHY, Filtering Engine, USB PHY, SuperSpeed USB 3.1 Gen 1 device controller, EEPROM controller, and a FIFO controller with internal packet buffering.

The internal USB 3.1 Gen 1 device controller and USB PHY are compliant with the USB 3.1 Gen 1 SuperSpeed standard. The LAN7800 implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

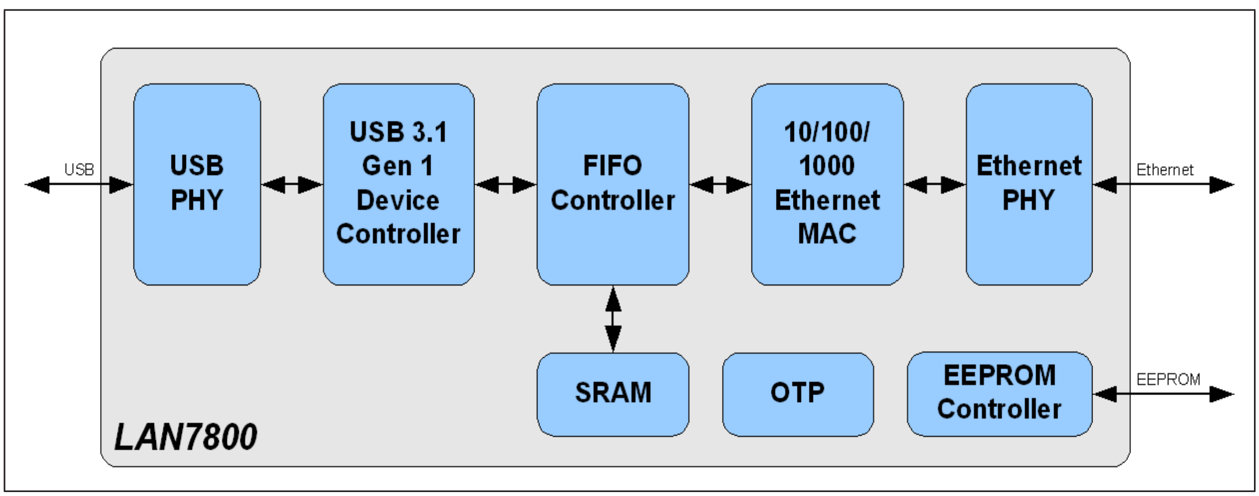
The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab, and 802.3az (Energy Efficient Ethernet) standards. ARP and NS offload are also supported.

Multiple power management features are provided, including Energy Efficient Ethernet (IEEE 802.3az), support for Microsoft's Always On Always Connected (AOAC), and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. Wake events can be programmed to initiate a USB remote wakeup. Up to 32 different AOAC wake-up frame patterns are supported along with Microsoft's WPD (Whole Packet Detection).

An internal EEPROM controller exists to load various USB and Ethernet configuration parameters. For EEPROM-less applications, the LAN7800 provides 1K Bytes of OTP memory that can be used to preload this same configuration data before enumeration.

The LAN7800 is available in commercial and industrial temperature range versions. An internal block diagram of the LAN7800 is shown in Figure 2-1.

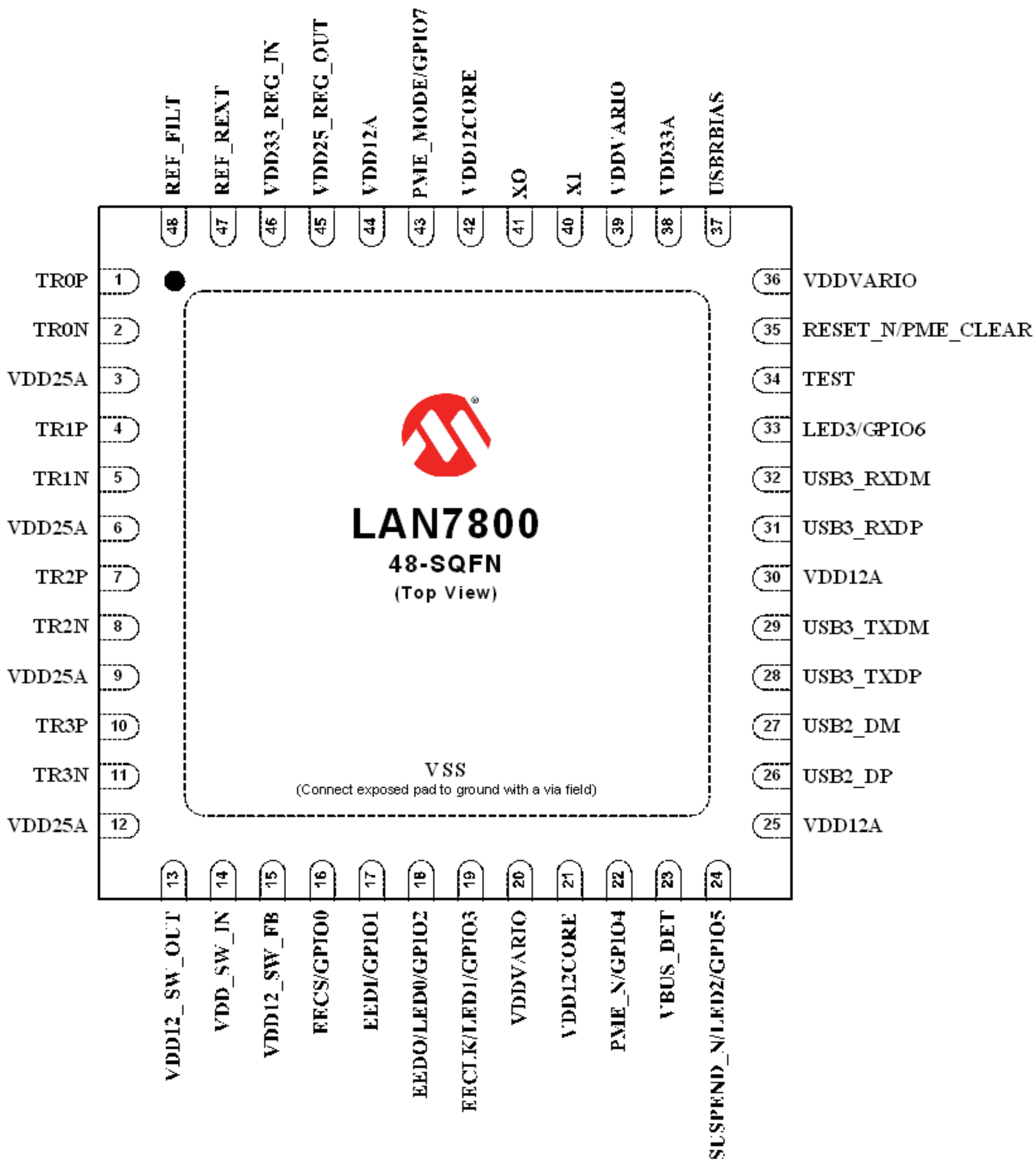
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note: When an "_N" is used at the end of the signal name, it indicates that the signal is active low. For example, **RESET_N** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.2, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

TABLE 3-1: PIN ASSIGNMENTS

Pin Number	Pin Name	Pin Number	Pin Name
1	**TR0P**	25	**VDD12A**
2	**TR0N**	26	**USB2_DP**
3	**VDD25A**	27	**USB2_DM**
4	**TR1P**	28	**USB3_TXDP**
5	**TR1N**	29	**USB3_TXDM**
6	**VDD25A**	30	**VDD12A**
7	**TR2P**	31	**USB3_RXDP**
8	**TR2N**	32	**USB3_RXDM**
9	**VDD25A**	33	**LED3/GPIO6**
10	**TR3P**	34	**TEST**
11	**TR3N**	35	**RESET_N/PME_CLEAR**
12	**VDD25A**	36	**VDDVARIO**
13	**VDD12_SW_OUT**	37	**USBRBIAS**
14	**VDD_SW_IN**	38	**VDD33A**
15	**VDD12_SW_FB**	39	**VDDVARIO**
16	**EECS/GPIO0**	40	**XI**
17	**EEDI/GPIO1**	41	**XO**
18	**EEDO/LED0/GPIO2**	42	**VDD12CORE**
19	**EECLK/LED1/GPIO3**	43	**PME_MODE/GPIO7**
20	**VDDVARIO**	44	**VDD12A**
21	**VDD12CORE**	45	**VDD25_REG_OUT**
22	**PME_N/GPIO4**	46	**VDD33_REG_IN**
23	**VBUS_DET**	47	**REF_REXT**
24	**SUSPEND_N/LED2/GPIO5**	48	**REF_FILT**
Exposed Pad (**VSS**) must be connected to ground			

3.2 Pin Descriptions

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Gigabit Ethernet Pins			
Ethernet TX/RX Positive Channel 0	**TR0P**	AIO	Transmit/Receive Positive Channel 0.
Ethernet TX/RX Negative Channel 0	**TR0N**	AIO	Transmit/Receive Negative Channel 0.
Ethernet TX/RX Positive Channel 1	**TR1P**	AIO	Transmit/Receive Positive Channel 1.
Ethernet TX/RX Negative Channel 1	**TR1N**	AIO	Transmit/Receive Negative Channel 1.
Ethernet TX/RX Positive Channel 2	**TR2P**	AIO	Transmit/Receive Positive Channel 2.
Ethernet TX/RX Negative Channel 2	**TR2N**	AIO	Transmit/Receive Negative Channel 2.
Ethernet TX/RX Positive Channel 3	**TR3P**	AIO	Transmit/Receive Positive Channel 3.
Ethernet TX/RX Negative Channel 3	**TR3N**	AIO	Transmit/Receive Negative Channel 3.
External PHY Reference Filter	**REF_FILT**	AI	External PHY Reference Filter. Connect to an external 1uF capacitor to ground.
External PHY Reference Resistor	**REF_REXT**	AI	External PHY Reference Resistor. Connect to an external 2K 1.0% resistor to ground.
USB Pins			
USB 3.1 Gen 1 DPLUS TX	**USB3_TXDP**	AIO	SuperSpeed USB transmit data plus.
USB 3.1 Gen 1 DMINUS TX	**USB3_TXDM**	AIO	SuperSpeed USB transmit data minus.
USB 3.1 Gen 1 DPLUS RX	**USB3_RXDP**	AIO	SuperSpeed USB receive data plus.
USB 3.1 Gen 1 DMINUS RX	**USB3_RXDM**	AIO	SuperSpeed USB receive data minus.
USB 2.0 DPLUS	**USB2_DP**	AIO	Hi-Speed USB data plus.
USB 2.0 DMINUS	**USB2_DM**	AIO	Hi-Speed USB Speed data minus.
External USB Bias Resistor	**USBRBIAS**	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12K 1.0% resistor to ground.
Miscellaneous Pins			
Detect Upstream VBUS Power	**VBUS_DET**	VIS (PD)	Detects the state of the upstream bus power. For bus powered operation, this pin must be tied to **VDD33A**. Refer to Section 4.0, "Power Connections" for additional information.
PME	**PME_N**	O8/OD8	This pin is used to signal PME when the PME mode of operation is in effect.

TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PME Mode Select	**PME_MODE**	VIS	This pin serves as the PME mode selection input when the PME mode of operation is in effect.
PME Clear	**PME_CLEAR**	VIS	This pin may serves as PME clear input when the PME mode of operation is in effect.
USB Suspend	**SUSPEND_N**	O12	This pin is asserted when the device is in one of the suspend states as defined in Section 12.3, "Suspend States". This pin may be configured to place an external switcher into a low power state such as when the device is in SUSPEND2.
General Purpose I/O 0-7	**GPIO[0:7]**	VIS/O8/ OD8 (PU)	These general purpose I/O pins are each fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input. A programmable pull-up may optionally be enabled.
Indicator LEDs 0-3	**LED[0:3]**	OD12	These LEDs can be configured to indicate Ethernet link, activity, duplex, and collision. Refer to Section 9.6, "LED Interface," on page 126 for additional information.
System Reset	**RESET_N**	VIS	System reset. This pin is active low. If this signal is unused it must be pulled-up to VDD.
Test Pin	**TEST**	VIS	Test pin. This pin is used for internal purposes only and must be connected to ground for proper operation.
EEPROM			
EEPROM Chip Select	**EECS**	O12	This pin drives the chip select output of the external EEPROM.
EEPROM Data In	**EEDI**	VIS	This pin is driven by the EEDO output of the external EEPROM.
EEPROM Data Out	**EEDO**	O12	This pin drives the EEDI input of the external EEPROM.
EEPROM Clock	**EECLK**	O12	This pin drives the EEPROM clock of the external EEPROM.
Clock Interface			
Crystal Input	**XI**	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
Crystal Output	**XO**	OCLK	External 25 MHz crystal output.
I/O Power pins, Core Power Pins, and Ground Pad			
Variable I/O Power Supply Input	**VDDVARIO**	P	+1.8V - +3.3V variable supply for I/Os. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
+3.3V Analog Power Supply Input	**VDD33A**	P	+3.3V analog power supply for USB 2.0 AFE. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
+2.5V Analog Power Supply Input	**VDD25A**	P	+2.5V analog power supply input for Gigabit Ethernet PHY. Refer to Section 4.0, "Power Connections," on page 15 for connection information.

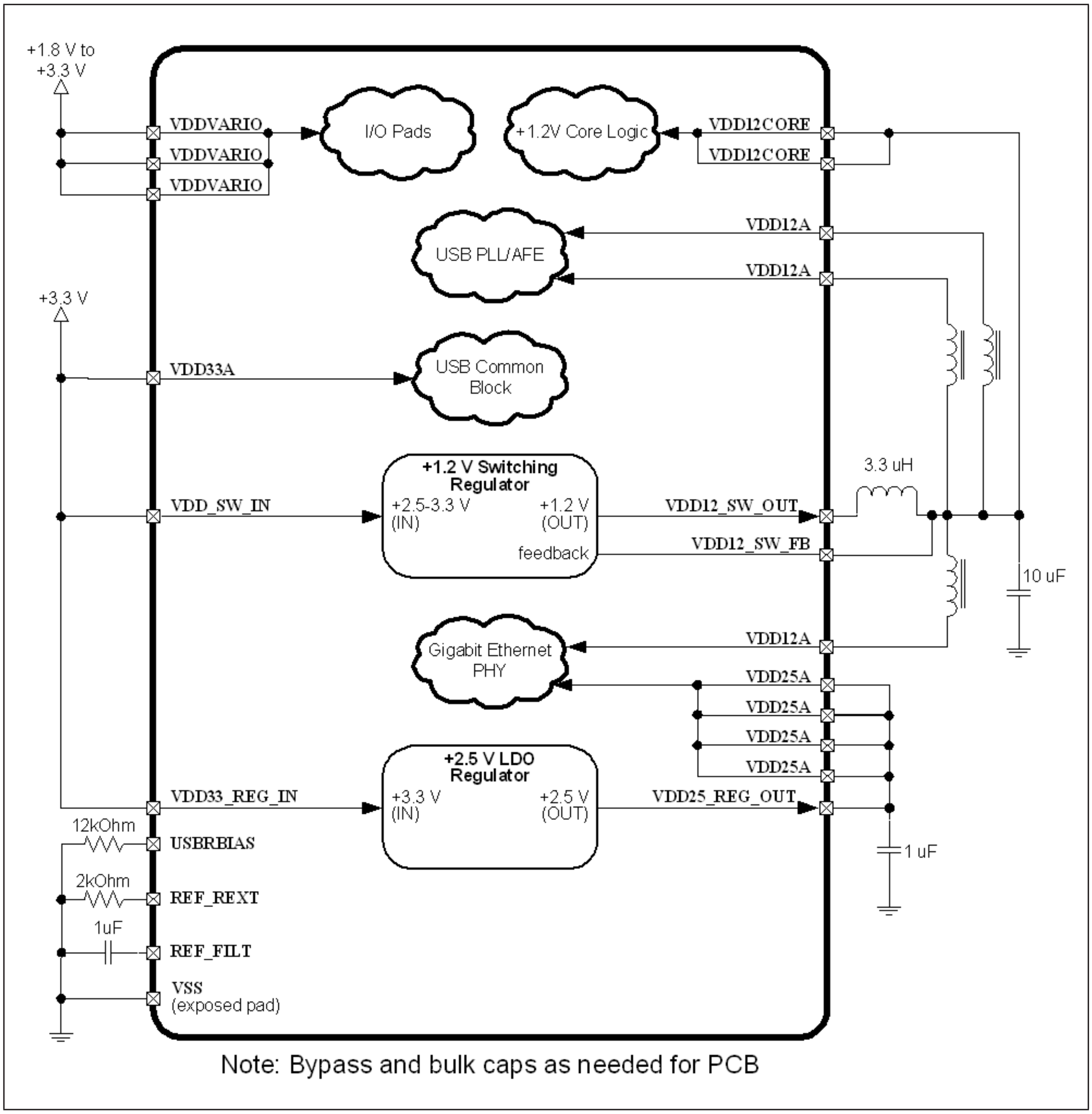
TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.2V Ethernet Port Power Supply Input	**VDD12A**	P	+1.2V analog power supply input for USB PLL/AFE. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
+1.2V Digital Core Power Supply Input	**VDD12CORE**	P	+1.2V digital core power supply input. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
+3.3V LDO Input Voltage	**VDD33_REG_IN**	P	+3.3V power supply input to the integrated LDO. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
+2.5V LDO Output	**VDD25_REG_OUT**	P	+2.5V power supply output from the integrated LDO. This is used to supply power to Gigabit Ethernet PHY AFE. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
Switcher Input Voltage	**VDD_SW_IN**	P	+2.5V-+3.3V input voltage for switching regulator. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
Switcher Feedback	**VDD12_SW_FB**	P	Feedback pin for the integrated switching regulator. Refer to Section 4.0, "Power Connections," on page 15 for connection information. **Note:** To disable the switcher, tie this pin to **VDD_SW_IN**.
+1.2V Switcher Output Voltage	**VDD12_SW_OUT**	P	+1.2V power supply output voltage for switching regulator. Refer to Section 4.0, "Power Connections," on page 15 for connection information.
Ground	**VSS**	P	Common Ground

4.0 POWER CONNECTIONS

Figure 4-1 illustrates the device power connections in a typical application. Refer to the device reference schematic for additional information. Refer to Section 3.0, "Pin Descriptions and Configuration," on page 10 for additional pin information.

FIGURE 4-1: POWER CONNECTION DIAGRAM



Note:	For 3.3V I/O operation, the **VDDVARIO** and +3.3V supplies may be connected together. To disable the internal switcher, tie the **VDD12_SW_FB** pin to **VDD_SW_IN**.

5.0 USB DEVICE CONTROLLER

5.1 Overview

The USB functionality consists of five major parts. The USB PHY, UDC (USB Device Controller), URX (USB Bulk Out Receiver), UTX (USB Bulk In Transmitter), and CTL (USB Control Block).

The UDC is configured to support one configuration, one interface, one alternate setting, and four endpoints. Streams are not supported in this device. The URX and UTX implement the Bulk-Out and Bulk-In endpoints respectively. The CTL manages Control and Interrupt endpoints.

Each USB Controller endpoint is unidirectional with even numbered endpoints handling the OUT (from the host, actually RX into the device) direction and odd numbered endpoints handling the IN (to the host, actually TX from the device) direction.

The UDC endpoint numbers start at 0 and increment. Endpoint numbers are not skipped and have a fixed mapping to the USB endpoint numbers. The corresponding USB endpoint is obtained by dividing the UDC endpoint number by 2 (rounding down). For example, single directional endpoint 0 indicates USB OUT endpoint 0, and single directional endpoint 1 corresponds to USB IN endpoint 0.

The mapping of the device's USB endpoints to the UDC endpoints is shown in Table 5-1. As can be seen, one IN and two OUT endpoints on the UDC are not utilized.

TABLE 5-1: DEVICE TO UDC ENDPOINT MAPPING

Endpoint Function	USB EP number
Control OUT	0
Control IN	0
unused	NA
Bulk IN	1
Bulk OUT	2
unused	NA
unused	NA
Interrupt IN	3

5.2 Control Endpoint

The Control endpoint is handled by the CTL (USB Control) module. The CTL module is responsible for handling standard USB requests, as well as USB vendor commands. The UDC does not handle USB commands. These commands are passed to the CTL for completion.

5.2.1 USB STANDARD COMMAND PROCESSING

This section lists the supported USB standard device requests. The basic format of a device request is shown in section 9.3 of the USB 2.0 and 3.1 Gen 1 specifications and the standard device requests are described in section 9.4. Valid values of the parameters are given below.

Per the USB specifications, if an unsupported or invalid request is made to a USB device, the device responds by returning STALL in the Data or Status stage of the request. Receipt of an unsupported or invalid request does NOT cause the optional Halt feature on the control pipe to be set.

For each request supported, the USB specifications provide details on the device behavior during the various configuration states and on the conditions which will return a Request Error. Some requests affect the state of the hardware. Table 9-9 of the USB 3.1 Gen 1 specification lists the events that affect the various parameters.

In order to implement the Get Descriptor command, the CTL manages a 128x32 Descriptor RAM. The RAMs contents are initialized via the EEPROM or OTP, after a system reset occurs. The Descriptor RAM may also be programmed by the device driver to support EEPROM-Less mode.

TABLE 5-2: STRING DESCRIPTOR INDEX MAPPINGS

INDEX	STRING NAME
0	Language ID
1	Manufacturer ID
2	Product ID
3	Serial Number
4	Configuration String
5	Interface String

When the UDC decodes a Get Descriptor command, it will pass a pointer to the CTL. The CTL uses this pointer to determine what the command is and how to fill it.

5.2.1.1 Clear Feature

This request varies between USB2.0 (HS, FS) and USB3.1 Gen 1 (SS) modes.

5.2.1.1.1 USB 2.0

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 1=Device_Remote_Wakeup and 0=Endpoint_Halt.

wIndex - Always 0 when the device is selected, specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (0, 80h, 81h, 2 or 83h) when an endpoint is selected.

A ClearFeature(Endpoint_Halt) request will clear the USB 2.0 data toggle for the specified endpoint.

5.2.1.1.2 USB 3.1 Gen 1

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 0=Endpoint_Halt (for endpoints), 0=Function_Suspend (for interfaces), 48=U1_Enable, 49=U2_Enable and 50=LTM_Enable.

wIndex - Always 0 when the device is selected, specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (0, 80h, 81h, 2 or 83h) when an endpoint is selected.

A ClearFeature(Endpoint_Halt) request will reset the USB 3.1 Gen 1 sequence number for the specified endpoint.

5.2.1.2 Get Configuration

All parameters are fixed per the USB specifications.

5.2.1.3 Get Descriptor

wValue - The high byte selects the descriptor type. The supported descriptors for this command are 1=Device, 2=Configuration (including Interface, Endpoint descriptors and Endpoint Companion descriptors (USB 2.1 LPM/USB 3.1 Gen 1)), 3=String, 6=Device Qualifier (HS/FS), 7=Other Speed Configuration (USB2.0) and 15=BOS (USB3.1 Gen 1 only). The low byte selects the descriptor index and must be 0.

> **Note:** Direct access to the Interface, Endpoint and Endpoint Companion (USB 2.1 LPM/USB3.1 Gen 1) descriptors are not supported by this command and will cause a USB stall. Access to USB 3.1 Gen 1 only descriptors while in USB 2.0 mode and access to HS and FS descriptors while in USB 3.1 Gen 1 mode are not supported by this command and will cause a USB stall.

wIndex - Specifies the Language ID for string descriptors or is 0 for other descriptors.

wLength - Specifies the number of bytes to return. If the descriptor is longer than the wLength field, only the initial bytes of the descriptor are returned. If the descriptor is shorter than the wLength field, the device indicates the end of the control transfer by sending a short packet when further data is requested. A short packet is defined as a packet shorter than the maximum payload size or a zero length data packet.

5.2.1.4 Get Interface

wIndex - Specifies the interface, always 0 for this device.

5.2.1.5 Get Status

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wIndex - Always 0 when the device is selected, specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (0, 80h, 81h, 2 or 83h) when an endpoint is selected.

Note: In USB 3.1 Gen 1 (SS) mode, only the lower byte of wIndex is used for the endpoint number.

The returned data for a device varies between USB 2.0 (FS, HS) and USB 3.1 Gen 1 (SS) modes, with USB 3.1 Gen 1 mode also returning LTM Enable, U2 Enabled and U1 Enabled. Also, the Remote Wakeup field is reserved and must return 0 for USB 3.1 Gen 1 (SS) mode.

The returned data for the first interface varies between USB 2.0 (FS, HS) and USB 3.1 Gen 1 (SS) modes, with USB 3.1 Gen 1 (SS) mode returning Function Remote Wakeup and Function Remote Wakeup Capable.

Note: Power Method (PWR_SEL) in Hardware Configuration Register (HW_CFG) is used as the source for the Self-Power bit (D0).

5.2.1.6 Set Address

wValue - Specifies the new device address.

Per the USB specification, the USB device does not change its device address until after the Status stage of this request is completed successfully. This is a difference between this request and all other requests. For all other requests, the operation indicated must be completed before the Status stage.

5.2.1.7 Set Configuration

wValue - The lower byte specifies the configuration value.

The device supports only one configuration. A value of 1 places the device into the Configured state while a value of 0 places the device into the Address state.

The Halt feature is reset for *all* endpoints upon the receipt of this request with a valid configuration value.

The USB 2.0 data toggle and the USB 3.1 Gen 1 sequence numbers for *all* endpoints are initialized upon the receipt of this request with a valid configuration value.

5.2.1.8 Set Descriptor

This optional request is not supported and the device responds by returning STALL.

5.2.1.9 Set Feature

This request varies between USB 2.0 (HS, FS) and USB 3.1 Gen 1 (SS) modes.

5.2.1.9.1 USB 2.0

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 1=Device_Remote_Wakeup, 2=device Test_Mode, 0=Endpoint_Halt.

Note: Endpoint_Halt is not implemented for Endpoint 0.

wIndex - Specifies the interface number (always 0) when an interface is selected or the direction/endpoint number (81h, 2 or 83h) when an endpoint is selected. When the device is selected, this field is always 0 unless device Test_Mode is selected via wValue, in which case the upper byte is the Test Selector and the lower byte a 0.

5.2.1.9.2 USB 3.1 Gen 1

bmRequestType - 00h for the device, 01h for interfaces and 02h for endpoints.

wValue - Specifies the feature, 0=Endpoint_Halt (for endpoints), 0=Function_Suspend (for interfaces), 48=U1_Enabe, 49=U2_Enable and 50=LTM_Enable.

Note:	Endpoint_Halt is not implemented for Endpoint 0.

wIndex - When an endpoint is selected, the lower byte specifies the direction/endpoint number (81h, 2 or 83h), when the device is selected this field is always 0 and when an interface the lower byte specifies the interface (always 0). For the Function_Suspend feature, the upper byte specifies the suspend options. Bit 0=Low power suspend state and bit 1=Function Remote Wake Enable.

5.2.1.10 Set Interface

wValue - Specifies the alternate setting (must be 0).

wIndex - Specifies the interface (always 0).

Only one interface with one setting is supported by the device. If the command is issued with an interface other than 00h, the device responds with a Request Error. If the command is issued with an interface setting of 00h but with an alternative setting other than 00h, the device responds with a STALL.

The Halt feature is reset for *all* endpoints upon the receipt of this request with valid interface and alternate setting values.

The USB 2.0 data toggle and the USB 3.1 Gen 1 sequence numbers for *all* endpoints are initialized upon the receipt of this request with valid interface and alternate setting values.

5.2.1.11 Set Isochronous Delay

All parameters are fixed per the USB 3.1 Gen 1 specification.

Although there are no isochronous endpoints the device must accept this request and silently discard it.

Note:	This command is only supported for USB 3.1 Gen 1. When not operating in super-speed mode the device will Stall this request.

5.2.1.12 Set SEL

All parameters are fixed per the USB 3.1 Gen 1 specification.

This command is accepted by the device. The U1 Exit Latency Register (U1_LATENCY) and U2 Exit Latency Register (U2_LATENCY) are updated accordingly. SET Select (SET_SEL) in USB Status Register (USB_STATUS) and USB Status Interrupt (USB_STS_INT) in Interrupt Status Register (INT_STS) are also asserted. USB_STS_INT is asserted in the Interrupt EP if configured.

Note:	This command is only supported for USB 3.1 Gen 1. When not operating in super-speed mode the device will Stall this command.

5.2.1.13 Sync Frame

There are no isochronous endpoints in this device. The device will respond with a Stall to this request.

5.2.2 USB VENDOR COMMANDS

The device implements several vendor specific commands in order to directly access CSRs and efficiently gather statistics. The memory map utilized by the address field is defined in Table 14-1, "Memory Map," on page 139.

5.2.2.1 Write Command

This command allows the Host to write a memory location. Burst writes are not supported. All writes are 32-bits.

TABLE 5-3: FORMAT OF WRITE SETUP STAGE

Offset	Field	Value
0h	bmRequestType	40h
1h	bRequest	A0h
2h	wValue	00h
4h	wIndex	{Address[12:0]}
6h	wLength	04h

TABLE 5-4: FORMAT OF WRITE DATA STAGE

Offset	Field
0h	Register Write Data [31:0]

5.2.2.2 Read Command

This command allows the Host to read a memory location. Burst reads are not supported. All reads return 32-bits.

TABLE 5-5: FORMAT OF READ SETUP STAGE

Offset	Field	Value
0h	bmRequestType	C0h
1h	bRequest	A1h
2h	wValue	00h
4h	wIndex	{Address[12:0]}
6h	wLength	04h

TABLE 5-6: FORMAT OF READ DATA STAGE

Offset	Field
0h	Register Read Data [31:0]

5.2.2.3 Get Statistics Command

The Get Statistics Command returns the entire contents of the RX and TX statistics counters. The statistics counters are snapshot when fulfilling the command request. The statistics counters rollover.

Note: TX statistics counters are not affected by frames sent in response to NS/ARP requests when the device is suspended.

Good byte and received frame counters will count all frames that are delivered to the Host. If Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL) any bad frames received will be counted as well.

The statistics counters are cleared by all reset events including LRST.

TABLE 5-7: FORMAT OF GET STATISTICS SETUP STAGE

Offset	Field	Value
0h	bmRequestType	C0h
1h	bRequest	A2h
2h	wValue	00h
4h	wIndex	00h
6h	wLength	BCh

TABLE 5-8: FORMAT OF GET STATISTICS DATA STAGE

Offset	Field
00h	RX FCS Errors
04h	RX Alignment Errors
08h	Rx Fragment Errors
0Ch	RX Jabber Errors
10h	RX Undersize Frame Errors
14h	RX Oversize Frame Errors
18h	RX Dropped Frames
1Ch	RX Unicast Byte Count
20h	RX Broadcast Byte Count
24h	RX Multicast Byte Count
28h	RX Unicast Frames
2Ch	RX Broadcast Frames
30h	RX Multicast Frames
34h	RX Pause Frames
38h	RX 64 Byte Frames
3Ch	RX 65 - 127 Byte Frames

TABLE 5-8: FORMAT OF GET STATISTICS DATA STAGE (CONTINUED)

Offset	Field
40h	RX 128 - 255 Byte Frames
44h	RX 256 - 511 Bytes Frames
48h	RX 512 - 1023 Byte Frames
4Ch	RX 1024 - 1518 Byte Frames
50h	RX Greater 1518 Byte Frames
54h	EEE RX LPI Transitions
58h	EEE RX LPI Time
5Ch	TX FCS Errors
60h	TX Excess Deferral Errors
64h	TX Carrier Errors
68h	TX Bad Byte Count
6Ch	TX Single Collisions
70h	TX Multiple Collisions
74h	TX Excessive Collision
78h	TX Late Collisions
7Ch	TX Unicast Byte Count
80h	TX Broadcast Byte Count
84h	TX Multicast Byte Count
88h	TX Unicast Frames
8Ch	TX Broadcast Frames
90h	TX Multicast Frames
94h	TX Pause Frames
98h	TX 64 Byte Frames
9Ch	TX 65 - 127 Byte Frames
A0h	TX 128 - 255 Byte Frames
A4h	TX 256 - 511 Bytes Frames
A8h	TX 512 - 1023 Byte Frames
ACh	TX 1024 - 1518 Byte Frames
B0h	TX Greater 1518 Byte Frames
B4h	EEE TX LPI Transitions
B8h	EEE TX LPI Time

TABLE 5-9: STATISTICS COUNTER DEFINITIONS

Name	Description	Size (Bits)
RX FCS Errors	Number of frames received with CRC-32 errors or RX errors. **Note:** If a frame has a Jabber Error and FCS error, only the RX Jabber Errors counter will be incremented **Note:** If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.	20
RX Alignment Errors	Number of RX frames received with alignment errors.	20
RX Fragment Errors	Number of frames received that are < 64 bytes in size and have an FCS error or RX error. **Note:** If a frame is less than 64 bytes in length and has an FCS error, only the RX Fragment Errors counter will be incremented.	20
RX Jabber Errors	Number of frames received with a length greater than Maximum Frame Size (MAX_SIZE) and have FCS errors or RX errors. **Note:** The existence of extra bits does not trigger a jabber error. A jabber error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received. **Note:** If a frame has a Jabber Error and FCS error, only the RX Jabber Errors counter will be incremented.	20
RX Undersize Frame Errors	Number of frames received with a length less than 64 bytes. No other errors have been detected in the frame.	20
RX Oversize Frame Errors	Number of frames received with a length greater than the programmed maximum Ethernet frame size (Maximum Frame Size (MAX_SIZE) field of the MAC Receive Register (MAC_RX)). No other errors have been detected in the frame. **Note:** The VLAN Frame Size Enforcement (FSE) bit allows for the maximum legal size to be increased by 4-bytes to account for a single VLAN tag or 8-bytes to account for stacked VLAN tags. **Note:** The MAC determines a VLAN tag is present if the type field is equal to 8100h or the value programmed in the VLAN Type Register (VLAN_TYPE). **Note:** The existence of extra bits does not trigger an oversize error. An oversize error requires at least one full byte beyond the value specified by the Maximum Frame Size (MAX_SIZE) to be received.	20
RX Dropped Frames	Number of RX frames dropped by the FCT due to insufficient room in the RX FIFO. **Note:** If a frame to be dropped has an Ethernet error, it will be counted in the relevant bad frame counter. The RX Dropped Frames counter will be incremented for the errored frame only if Store Bad Frames is set in the FIFO Controller RX FIFO Control Register (FCT_RX_CTL).	20

TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
RX Unicast Byte Count	Total number of bytes received from unicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32
RX Broadcast Byte Count	Total number of bytes received from broadcast frames without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is deasserted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32
RX Multicast Byte Count	Total number of bytes received from multicast frames without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted. **Note:** The per frame byte count does not include the VLAN TAG and VID if the Enable VLAN Tag Stripping bit is set in the Receive Filtering Engine Control Register (RFE_CTL). It does not include the FCS if the FCS Stripping bit is set in the MAC Receive Register (MAC_RX).	32
RX Unicast Frames	Number of unicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX Broadcast Frames	Number of broadcast frames received without errors. This counter does not count broadcast frames received when the Accept Broadcast Frames (AB) bit is deasserted. Frames that are discarded from FIFO overflow are not counted.	20
RX Multicast Frames	Number of multicast frames received without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX Pause Frames	Number of pause frames received without errors. **Note:** This counter records pause frames that failed address filtering.	20

TABLE 5-9: STATISTICS COUNTER DEFINITIONS (CONTINUED)

Name	Description	Size (Bits)
RX 64 Byte Frames	Number of frames received with a length of 64 bytes without errors. This counter does not count frames that fail address filtering. Pause frames filtered by Forward Pause Frames (FPF) are not counted. Frames that are discarded from FIFO overflow are not counted.	20
RX 65 - 127 Byte Frames	Number of frames received with a length between 65 bytes and 127 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 128 - 255 Byte Frames	Number of frames received with a length between 128 bytes and 255 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 256 - 511 Bytes Frames	Number of frames received with a length between 256 bytes and 511 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 512 - 1023 Byte Frames	Number of frames received with a length between 512 bytes and 1023 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX 1024 - 1518 Byte Frames	Number of frames received with a length between 1024 bytes and 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
RX Greater 1518 Byte Frames	Number of frames received with a length greater than 1518 bytes without errors. This counter does not count frames that fail address filtering. Frames that are discarded from FIFO overflow are not counted.	20
EEE RX LPI Transitions	Number of times that the LPI indication from the PHY changes from de-asserted to asserted. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32
EEE RX LPI Time	The amount of time, in micro-seconds, that the PHY indicates LPI. This counter is reset if Energy Efficient Ethernet Enable (EEEEN) in MAC Control Register (MAC_CR) is low. This counters is required to operate during SUSPEND0, SUSPEND3 and Normal Configured Power states.	32
TX FCS Errors	Number of frames transmitted with an FCS error. The MAC can be forced to transmit frames with FCS errors by setting the Bad FCS (BFCS) bit.	20