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High Performance Single Chip Low Power 10/100 Ethernet Physical Layer Transceiver (PHY)

PRODUCT FEATURES

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- Energy Detect power-down mode
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Table of Contents

Chapter 1	General Description	8
1.1	Architectural Overview	8
Chapter 2	Pin Configuration	9
Chapter 3	Pin Description	11
3.1	I/O Signals	11
Chapter 4	Architecture Details	16
4.1	Top Level Functional Architecture	16
4.2	100Base-TX Transmit	16
4.2.1	100M Transmit Data across the MII	16
4.2.2	4B/5B Encoding	16
4.2.3	Scrambling	18
4.2.4	NRZI and MLT3 Encoding	18
4.2.5	100M Transmit Driver	18
4.2.6	100M Phase Lock Loop (PLL)	18
4.3	100Base-TX Receive	19
4.3.1	100M Receive Input	19
4.3.2	Equalizer, Baseline Wander Correction and Clock and Data Recovery	19
4.3.3	NRZI and MLT-3 Decoding	19
4.3.4	Descrambling	20
4.3.5	Alignment	20
4.3.6	5B/4B Decoding	20
4.3.7	Receive Data Valid Signal	20
4.3.8	Receiver Errors	21
4.3.9	100M Receive Data across the MII	21
4.4	10Base-T Transmit	21
4.4.1	10M Transmit Data across the MII	21
4.4.2	Manchester Encoding	21
4.4.3	10M Transmit Drivers	21
4.5	10Base-T Receive	22
4.5.1	10M Receive Input and Squelch	22
4.5.2	Manchester Decoding	22
4.5.3	10M Receive Data across the MII	22
4.5.4	Jabber detection	22
4.6	MAC Interface	22
4.6.1	MII	23
4.7	Auto-negotiation	23
4.7.1	Parallel Detection	24
4.7.2	Re-starting Auto-negotiation	25
4.7.3	Disabling Auto-negotiation	25
4.7.4	Half vs. Full Duplex	25
4.8	PHY Management Control	25
4.8.1	Serial Management Interface (SMI)	25
Chapter 5	Registers	27
5.1	SMI Register Mapping	33
5.2	SMI Register Format	33
5.3	Management Interrupt	42
5.4	Miscellaneous Functions	42

5.4.1	Carrier Sense	42
5.4.2	Collision Detect	43
5.4.3	Isolate Mode	43
5.4.4	Link integrity Test	43
5.4.5	Power-Down modes	43
5.4.6	Reset	44
5.4.7	LED Description	44
5.4.8	Loopback Operation	45
5.4.9	Configuration Signals	45
5.5	Analog	46
5.5.1	ADC	46
5.5.2	100M PLL	47
5.5.3	MT_100	47
5.5.4	10M Squelch	47
5.5.5	10BT Filter	47
5.5.6	10M PLL - Data Recovery Clock	47
5.5.7	PLL 10M - Transmit Clock	48
5.5.8	XMT_10	48
5.5.9	Central Bias	48
5.6	DSP Block	49
5.6.1	General Description	49
5.6.2	ADC Gray code converting	49
<hr/>		
Chapter 6 Electrical Characteristics		50
6.1	Serial Management Interface (SMI) Timing	50
6.2	100Base-TX Timings	51
6.2.1	100M MII Receive Timing	51
6.2.2	100M MII Transmit Timing	51
6.3	10Base-T Timings	52
6.3.1	10M MII Receive Timing	52
6.3.2	10M MII Transmit Timing	52
6.4	Reset Timing	53
6.5	DC Characteristics	54
6.5.1	Operating Conditions	54
6.5.2	Power Consumption	54
6.5.3	DC Characteristics - Input and Output Buffers	56
<hr/>		
Chapter 7 Package Outline		60



Datasheet

List of Figures

Figure 1.1	LAN83C185 Architectural Overview	8
Figure 2.1	Package Pinout	9
Figure 4.1	100Base-TX Data Path	16
Figure 4.2	Receive Data Path	19
Figure 4.3	Relationship Between Received Data and Some MII Signals	20
Figure 4.4	MDIO Timing and Frame Structure - READ Cycle	26
Figure 4.5	MDIO Timing and Frame Structure - WRITE Cycle	26
Figure 5.1	PHY Address Strapping on LEDES	45
Figure 7.1	64 Pin TQFP Package Outline, 10X10X1.4 Body, 2 MM Footprint	60

List of Tables

Table 2.1	LAN83C185 64-PIN TQFP Pinout	10
Table 3.1	MII Signals	11
Table 3.2	LED Signals	12
Table 3.3	Management Signals	12
Table 3.4	Configuration Inputs	13
Table 3.5	General Signals	13
Table 3.6	10/100 Line Interface	14
Table 3.7	Analog References	14
Table 3.8	Analog Test Bus	14
Table 3.9	Power Signals	14
Table 4.1	4B/5B Code Table	17
Table 5.1	Control Register: Register 0 (Basic)	27
Table 5.2	Status Register: Register 1 (Basic)	27
Table 5.3	PHY ID 1 Register: Register 2 (Extended)	27
Table 5.4	PHY ID 2 Register: Register 3 (Extended)	27
Table 5.5	Auto-Negotiation Advertisement: Register 4 (Extended)	27
Table 5.6	Auto-Negotiation Link Partner Base Page Ability Register: Register 5 (Extended)	28
Table 5.7	Auto-Negotiation Expansion Register: Register 6 (Extended)	28
Table 5.8	Auto-Negotiation Link Partner Next Page Transmit Register: Register 7 (Extended)	28
Table 5.9	Register 8 (Extended)	28
Table 5.10	Register 9 (Extended)	28
Table 5.11	Register 10 (Extended)	29
Table 5.12	Register 11 (Extended)	29
Table 5.13	Register 12 (Extended)	29
Table 5.14	Register 13 (Extended)	29
Table 5.15	Register 14 (Extended)	29
Table 5.16	Register 15 (Extended)	29
Table 5.17	Silicon Revision Register 16: Vendor-Specific	30
Table 5.18	Mode Control/ Status Register 17: Vendor-Specific	30
Table 5.19	Special Modes Register 18: Vendor-Specific	30
Table 5.20	Reserved Register 19: Vendor-Specific	30
Table 5.21	TSTCNTL Register 20: Vendor-Specific	30
Table 5.22	TSTREAD2 Register 21: Vendor-Specific	31
Table 5.23	TSTREAD1 Register 22: Vendor-Specific	31
Table 5.24	TSTWRITE Register 23: Vendor-Specific	31
Table 5.25	Register 24: Vendor-Specific	31
Table 5.26	Register 25: Vendor-Specific	31
Table 5.27	Register 26: Vendor-Specific	31
Table 5.28	Special Control/Status Indications Register 27: Vendor-Specific	32
Table 5.29	Special Internal Testability Control Register 28: Vendor-Specific	32
Table 5.30	Interrupt Source Flags Register 29: Vendor-Specific	32
Table 5.31	Interrupt Mask Register 30: Vendor-Specific	32
Table 5.32	PHY Special Control/Status Register 31: Vendor-Specific	32
Table 5.33	SMI Register Mapping	33
Table 5.34	Register 0 - Basic Control	34
Table 5.35	Register 1 - Basic Status	34
Table 5.36	Register 2 - PHY Identifier 1	35
Table 5.37	Register 3 - PHY Identifier 2	35
Table 5.38	Register 4 - Auto Negotiation Advertisement	35
Table 5.39	Register 5 - Auto Negotiation Link Partner Ability	36
Table 5.40	Register 6 - Auto Negotiation Expansion	37
Table 5.41	Register 16 - Silicon Revision	37

**Datasheet**

Table 5.42 Register 17 - Mode Control/Status	37
Table 5.43 Register 18 - Special Modes	38
Table 5.44 Register 20 - TSTCNTL	39
Table 5.45 Register 21 - TSTREAD1	39
Table 5.46 Register 22 - TSTREAD2	39
Table 5.47 Register 23 - TSTWRITE	40
Table 5.48 Register 27 - Special Control/Status Indications	40
Table 5.49 Register 28 - Special Internal Testability Controls	40
Table 5.50 Register 29 - Interrupt Source Flags	40
Table 5.51 Register 30 - Interrupt Mask	41
Table 5.52 Register 31 - PHY Special Control/Status	41
Table 5.53 MODE[2:0] Bus	46
Table 6.1 Power Consumption Device Only	54
Table 6.2 Power Consumption Device and System Components	55
Table 6.3 MII Bus Interface Signals	56
Table 6.4 LAN Interface Signals	57
Table 6.5 LED Signals	57
Table 6.6 Configuration Inputs	57
Table 6.7 General Signals	58
Table 6.8 Analog References	58
Table 6.9 Internal Pull-Up / Pull-/Down Configurations	58
Table 6.10 100Base-TX Transceiver Characteristics	59
Table 6.11 10BASE-T Transceiver Characteristics	59
Table 7.1 64 Pin TQFP Package Parameters	60

Chapter 1 General Description

The SMSC LAN83C185 is a low-power, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN83C185 requires only a single +3.3V supply.

The LAN83C185 consists of an encoder/decoder, scrambler/descrambler, transmitter with wave-shaping and output driver, twisted-pair receiver with on-chip adaptive equalizer and baseline wander (BLW) correction, clock and data recovery, and Media Independent Interface (MII).

The LAN83C185 is fully compliant with IEEE 802.3/ 802.3u standards and supports both 802.3u-compliant and vendor-specific register functions. It contains a full-duplex 10-BASET/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

1.1 Architectural Overview

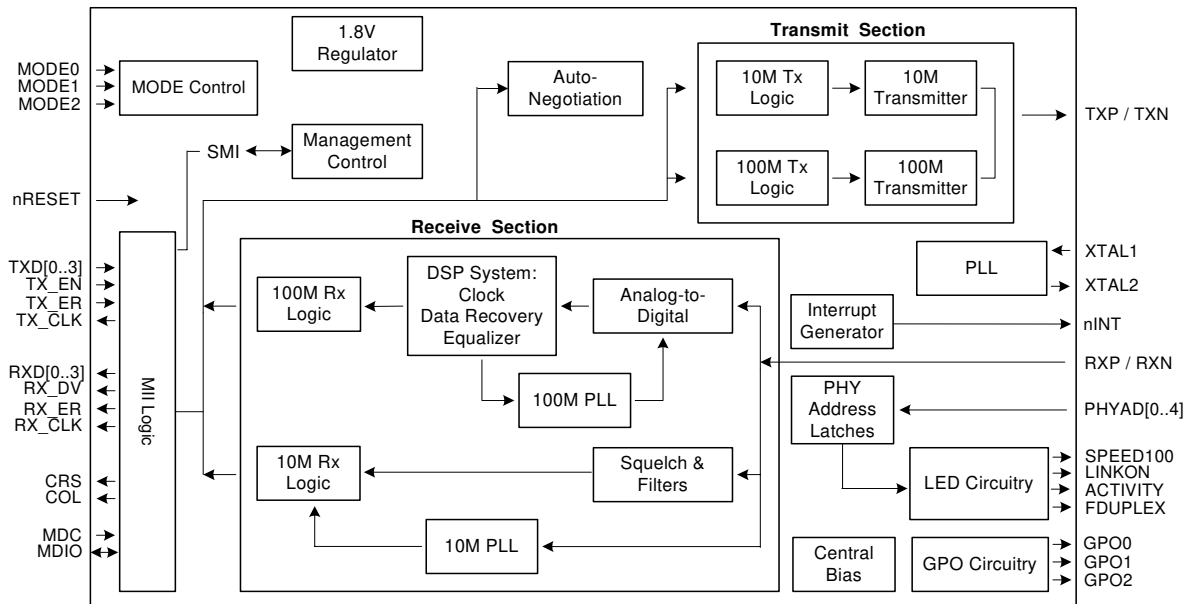


Figure 1.1 LAN83C185 Architectural Overview

Chapter 2 Pin Configuration

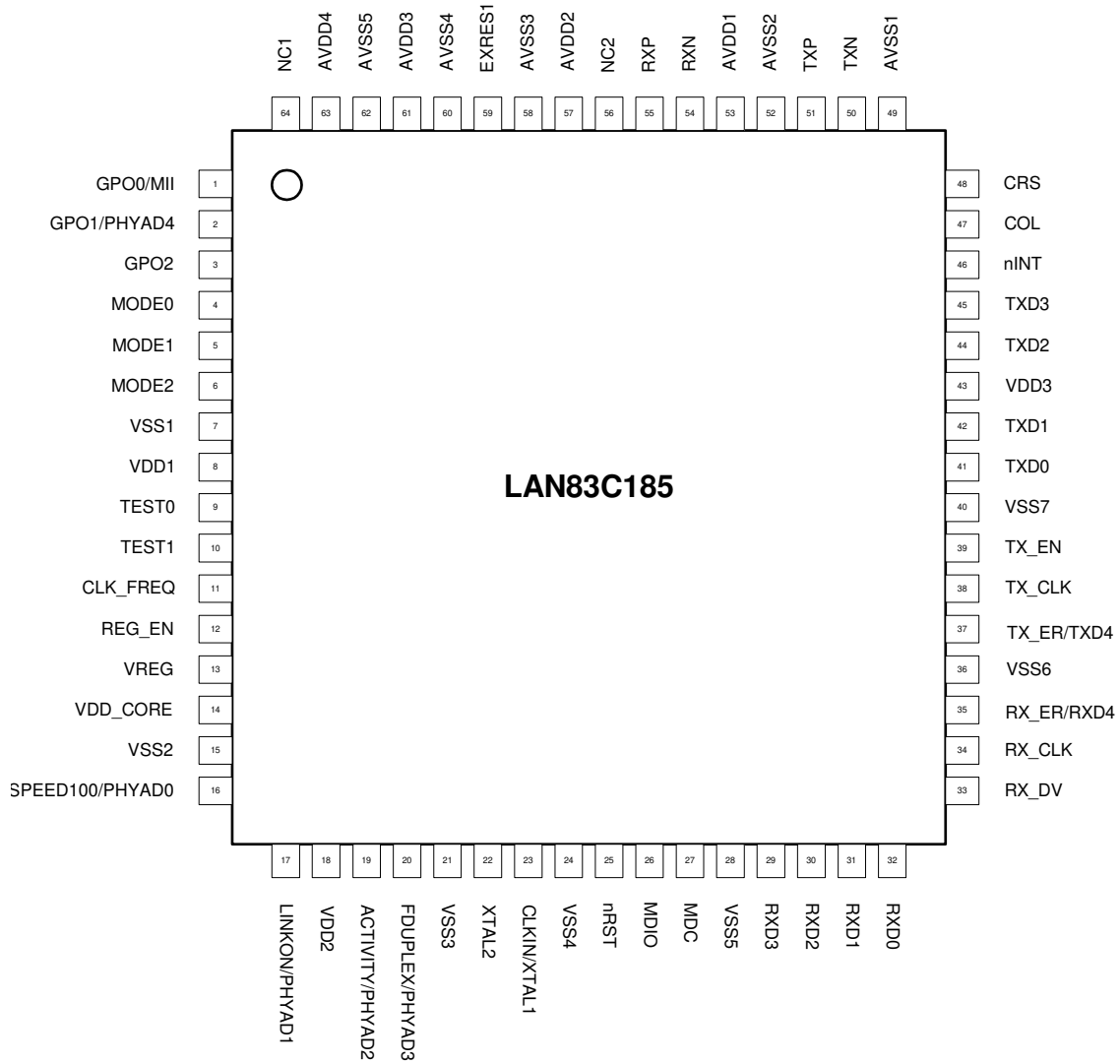


Figure 2.1 Package Pinout

Table 2.1 LAN83C185 64-PIN TQFP Pinout

PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GPO0/MII	33	RX_DV
2	GPO1/PHYAD4	34	RX_CLK
3	GPO2	35	RX_ER/RXD4
4	MODE0	36	VSS6
5	MODE1	37	TX_ER/TXD4
6	MODE2	38	TX_CLK
7	VSS1	39	TX_EN
8	VDD1	40	VSS7
9	TEST0	41	TXD0
10	TEST1	42	TXD1
11	CLK_FREQ	43	VDD3
12	REG_EN	44	TXD2
13	VREG	45	TXD3
14	VDD_CORE	46	nINT
15	VSS2	47	COL
16	SPEED100/PHYAD0	48	CRS
17	LINKON/PHYAD1	49	AVSS1
18	VDD2	50	TXN
19	ACTIVITY/PHYAD2	51	TXP
20	FDUPLEX/PHYAD3	52	AVSS2
21	VSS3	53	AVDD1
22	XTAL2	54	RXN
23	CLKIN/XTAL1	55	RXP
24	VSS4	56	NC2
25	nRST	57	AVDD2
26	MDIO	58	AVSS3
27	MDC	59	EXRES1
28	VSS5	60	AVSS4
29	RXD3	61	AVDD3
30	RXD2	62	AVSS5
31	RXD1	63	AVDD4
32	RXD0	64	NC1

Chapter 3 Pin Description

This chapter describes in detail the functionality of each of the five main architectural blocks.

The term “block” defines a stand-alone entity on the floor plan of the chip.

3.1 I/O Signals

I – Input. Digital TTL levels.

O – Output. Digital TTL levels.

AI – Input. Analog levels.

AO – Output. Analog levels.

AI/O – Input or Output. Analog levels.

Note: Reset as used in the signal descriptions is defined as nRST being active low.

Configuration inputs are listed in parenthesis.

Table 3.1 MII Signals

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
41	TXD0	I	Transmit Data 0: Bit 0 of the 4 data bits that are accepted by the PHY for transmission.
42	TXD1	I	Transmit Data 1: Bit 1 of the 4 data bits that are accepted by the PHY for transmission.
39	TX_EN	I	Transmit Enable: Indicates that valid data is presented on the TXD[3:0] signals, for transmission.
35	RX_ER (RXD4)	O O	Receive Error: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. In Symbol Interface (5B Decoding) mode, this signal is the MI1 Receive Data 4: the MSB of the received 5-bit symbol code-group.
47	COL	O	MI1 Collision Detect: Asserted to indicate detection of collision condition.
32	RXD0	O	Receive Data 0: Bit 0 of the 4 data bits that are sent by the PHY in the receive path.
31	RXD1	O	Receive Data 1: Bit 1 of the 4 data bits that are sent by the PHY in the receive path.
44	TXD2	I	Transmit Data 2: Bit 2 of the 4 data bits that are accepted by the PHY for transmission.
45	TXD3	I	Transmit Data 3: Bit 3 of the 4 data bits that are accepted by the PHY for transmission.

Table 3.1 MII Signals (continued)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
37	TX_ER (TXD4)	I	<p>MI1 Transmit Error: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10BaseT operation.</p> <p>In Symbol Interface (5B Decoding) mode, this signal becomes the MI1 Transmit Data 4: the MSB of the 5-bit symbol code-group.</p>
48	CRS	O	Carrier Sense: Indicate detection of carrier.
33	RX_DV	O	Receive Data Valid: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0].
30	RXD2	O	Receive Data 2: Bit 2 of the 4 data bits that sent by the PHY in the receive path.
29	RXD3	O	Receive Data 3: Bit 3 of the 4 data bits that sent by the PHY in the receive path.
38	TX_CLK	O	Transmit Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.
34	RX_CLK	O	Receive Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.

Table 3.2 LED Signals

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
16	SPEED100	O	LED1 – SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps.
17	LINKON	O	LED2 – LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on.
19	ACTIVITY	O	LED3 – ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD.
20	FDUPLEX	O	LED4 – DUPLEX indication. Active indicates that the PHY is in full-duplex mode.

Table 3.3 Management Signals

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
26	MDIO	IO	Management Data Input/OUTPUT: Serial management data input/output.
27	MDC	I	Management Clock: Serial management clock.

Table 3.4 Configuration Inputs

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
2	PHYAD4	I	PHY Address Bit 4: set the default address of the PHY.
20	PHYAD3	I	PHY Address Bit 3: set the default address of the PHY.
19	PHYAD2	I	PHY Address Bit 2: set the default address of the PHY.
17	PHYAD1	I	PHY Address Bit 1: set the default address of the PHY.
16	PHYAD0	I	PHY Address Bit 0: set the default address of the PHY.
6	MODE2	I	PHY Operating Mode Bit 2: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46 for the MODE options.
5	MODE1	I	PHY Operating Mode Bit 1: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46 for the MODE options.
4	MODE0	I	PHY Operating Mode Bit 0: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46 for the MODE options.
10	TEST1	I	Test Mode Select 1: Must be left floating.
9	TEST0	I	Test Mode Select 0: Must be left floating.
12	REG_EN	I	Internal +1.8V Regulator Enable: +3.3V – Enables internal regulator. 0V – Disables internal regulator.

Table 3.5 General Signals

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
46	nINT	OD	LAN Interrupt – Active Low output.
25	nRST	I	External Reset – input of the system reset. This signal is active LOW.
23	CLKIN/XTAL1	I	Clock Input – 25 MHz external clock or crystal input.
22	XTAL2	O	Clock Output – 25 MHz crystal output.
11	CLK_FREQ	I	Clock Frequency – define the frequency of the input clock CLKIN 0 – Clock frequency is 25 MHz. 1 – Reserved. This input needs to be held low continuously, during and after reset. This pin should be pulled-down to VSS via a pull-down resistor.
64	NC1		No Connect
3	GPO2	O	General Purpose Output 2 – General Purpose Output signal Driven by bits in registers 27 and 31.
2	GPO1	O	General Purpose Output 1 – General Purpose Output signal Driven by bits in registers 27 and 31. (Muxed with PHYAD4 signal)

Table 3.5 General Signals (continued)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
1	GPO0	O	General Purpose Output 0 – General Purpose Output signal. Driven by bits in registers 27 and 31. (Muxed with MII Select) This pin should be pulled-down or left floating – Do Not Pull Up.

Table 3.6 10/100 Line Interface

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
51	TXP	AO	Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
50	TXN	AO	Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
55	RXP	AI	Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics.
54	RXN	AI	Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics.

Table 3.7 Analog References

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
59	EXRES1	AI	Connects to reference resistor of value 12.4K-Ohm, 1% connected to digital GND.

Table 3.8 Analog Test Bus

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
56	NC2	AI/O	No Connect

Table 3.9 Power Signals

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
53	AVDD1	Power	+3.3V Analog Power
57	AVDD2	Power	+3.3V Analog Power
61	AVDD3	Power	+3.3V Analog Power
63	AVDD4	Power	+3.3V Analog Power
49	AVSS1	Power	Analog Ground
52	AVSS2	Power	Analog Ground
58	AVSS3	Power	Analog Ground

Table 3.9 Power Signals (continued)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
60	AVSS4	Power	Analog Ground
62	AVSS5	Power	Analog Ground
13	VREG	Power	+3.3V Internal Regulator Input Voltage
14	VDD_CORE	Power	+1.8V Ring (Core voltage) - required for capacitance connection.
8	VDD1	Power	+3.3V Digital Power
18	VDD2	Power	+3.3V Digital Power
43	VDD3	Power	+3.3V Digital Power
7	VSS1	Power	Digital Ground (GND)
15	VSS2	Power	Digital Ground (GND)
21	VSS3	Power	Digital Ground (GND)
24	VSS4	Power	Digital Ground (GND)
28	VSS5	Power	Digital Ground (GND)
36	VSS6	Power	Digital Ground (GND)
40	VSS7	Power	Digital Ground (GND)

Chapter 4 Architecture Details

4.1 Top Level Functional Architecture

Functionally, the PHY can be divided into the following sections:

- 100Base-TX transmit and receive
- 10Base-T transmit and receive
- MII interface to the controller
- Auto-negotiation to automatically determine the best speed and duplex possible
- Management Control to read status registers and write control registers

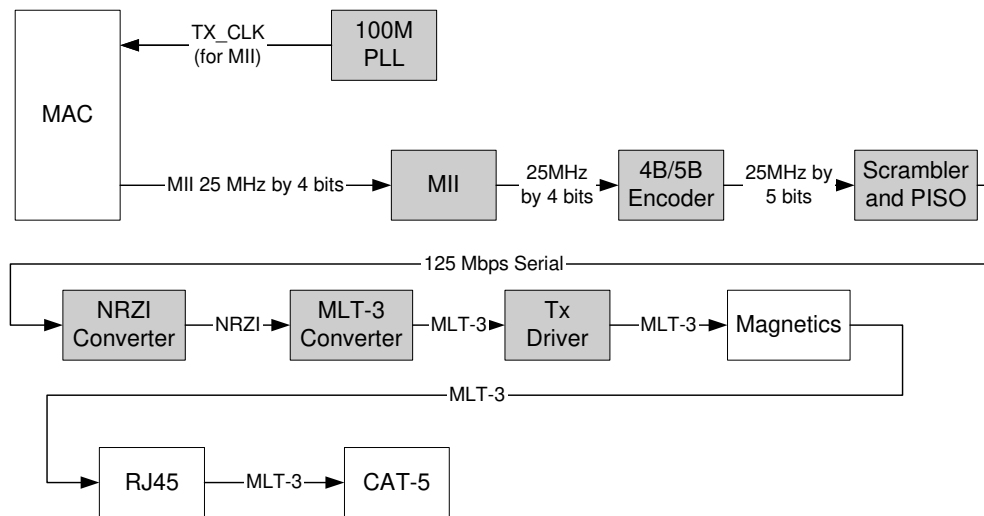


Figure 4.1 100Base-TX Data Path

4.2 100Base-TX Transmit

The data path of the 100Base-TX is shown in [Figure 4.1](#). Each major block is explained below.

4.2.1 100M Transmit Data across the MII

The MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 25MHz data.

4.2.2 4B/5B Encoding

The transmit data passes from the MII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to [Table 4.1](#). Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

Datasheet

The encoding process may be bypassed by clearing bit 6 of register 31. When the encoding is bypassed the 5th transmit data bit is equivalent to TX_ER.

Note that encoding can be bypassed only when the MAC interface is configured to operate in MII mode.

Table 4.1 4B/5B Code Table

CODE GROUP	SYM	RECEIVER INTERPRETATION			TRANSMITTER INTERPRETATION		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001		1	0001	
10100	2	2	0010		2	0010	
10101	3	3	0011		3	0011	
01010	4	4	0100		4	0100	
01011	5	5	0101		5	0101	
01110	6	6	0110		6	0110	
01111	7	7	0111		7	0111	
10010	8	8	1000		8	1000	
10011	9	9	1001		9	1001	
10110	A	A	1010		A	1010	
10111	B	B	1011		B	1011	
11010	C	C	1100		C	1100	
11011	D	D	1101		D	1101	
11100	E	E	1110		E	1110	
11101	F	F	1111		F	1111	
11111	I	IDLE			Sent after /T/R until TX_EN		
11000	J	First nibble of SSD, translated to "0101" following IDLE, else RX_ER			Sent for rising TX_EN		
10001	K	Second nibble of SSD, translated to "0101" following J, else RX_ER			Sent for rising TX_EN		
01101	T	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RX_ER			Sent for falling TX_EN		
00111	R	Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RX_ER			Sent for falling TX_EN		
00100	H	Transmit Error Symbol			Sent for rising TX_ER		
00110	V	INVALID, RX_ER if during RX_DV			INVALID		
11001	V	INVALID, RX_ER if during RX_DV			INVALID		
00000	V	INVALID, RX_ER if during RX_DV			INVALID		
00001	V	INVALID, RX_ER if during RX_DV			INVALID		

Table 4.1 4B/5B Code Table (continued)

CODE GROUP	SYM	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
00010	V	INVALID, RX_ER if during RX_DV	INVALID
00011	V	INVALID, RX_ER if during RX_DV	INVALID
00101	V	INVALID, RX_ER if during RX_DV	INVALID
01000	V	INVALID, RX_ER if during RX_DV	INVALID
01100	V	INVALID, RX_ER if during RX_DV	INVALID
10000	V	INVALID, RX_ER if during RX_DV	INVALID

4.2.3 Scrambling

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the PHY address, PHYAD[4:0], ensuring that in multiple-PHY applications, such as repeaters or switches, each PHY will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

4.2.4 NRZI and MLT3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT3 is a tri-level code where a change in the logic level represents a code bit "1" and the logic output remaining at the same level represents a code bit "0".

4.2.5 100M Transmit Driver

The MLT3 data is then passed to the analog transmitter, which launches the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media via a 1:1 ratio isolation transformer. The 10Base-T and 100Base-TX signals pass through the same transformer so that common "magnetics" can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

4.2.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100Base-Tx Transmitter.

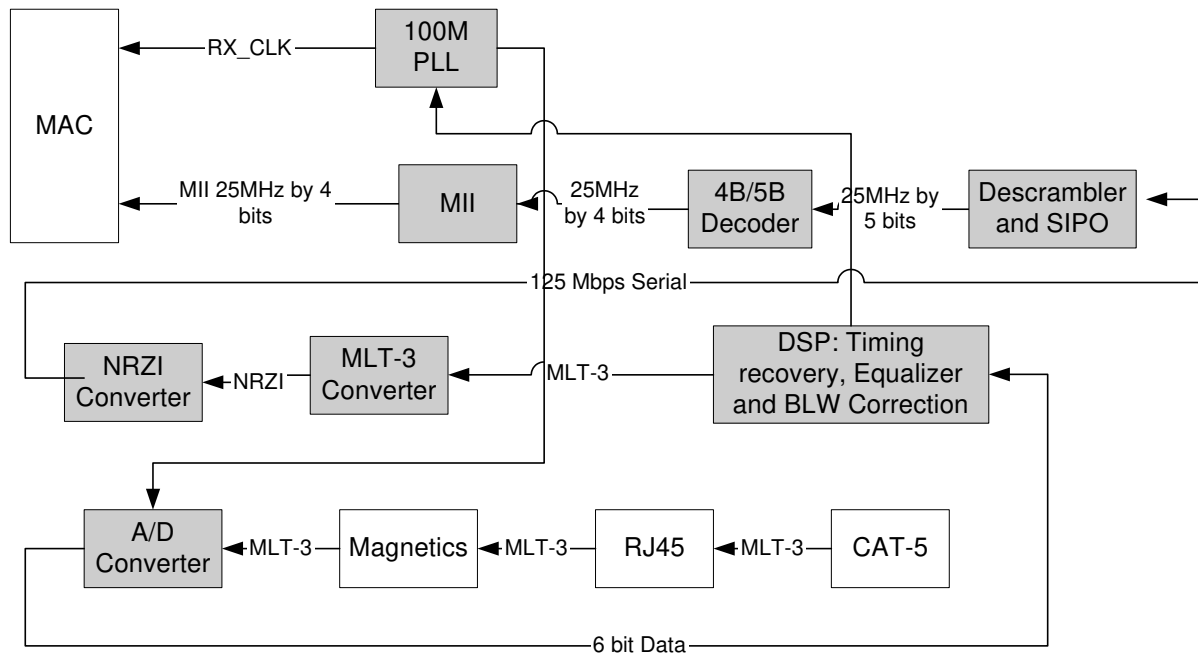


Figure 4.2 Receive Data Path

4.3 100Base-TX Receive

The receive data path is shown in [Figure 4.2](#). Detailed descriptions are given below.

4.3.1 100M Receive Input

The MLT-3 from the cable is fed into the PHY (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quantizer it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

4.3.2 Equalizer, Baseline Wander Correction and Clock and Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT-5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined "killer packet" with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

4.3.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

4.3.4 Descrambling

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols, the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The descrambler can be bypassed by setting bit 0 of register 31.

4.3.5 Alignment

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

4.3.6 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[3:0] signal lines. The SSD, /J/K/, is translated to "0101 0101" as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RX_DV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RX_DV.

These symbols are not translated into data.

The decoding process may be bypassed by clearing bit 6 of register 31. When the decoding is bypassed the 5th receive data bit is driven out on RX_ER/RXD4. Decoding may be bypassed only when the MAC interface is in MII mode.

4.3.7 Receive Data Valid Signal

The Receive Data Valid signal (RX_DV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RX_CLK. RX_DV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RX_DV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII).

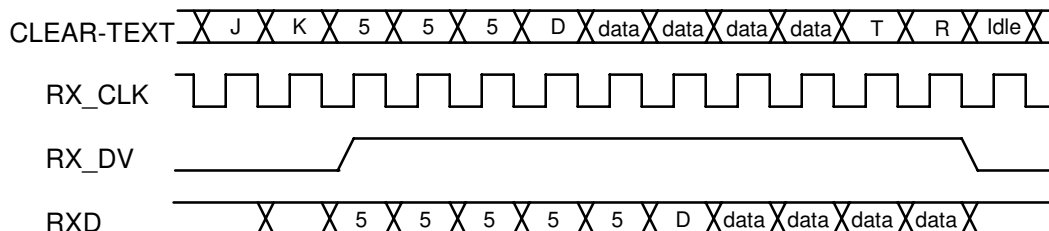


Figure 4.3 Relationship Between Received Data and Some MII Signals

4.3.8 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RX_ER signal is asserted and arbitrary data is driven onto the RXD[3:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RX_ER is asserted true and the value '1110' is driven onto the RXD[3:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

4.3.9 100M Receive Data across the MII

The 4-bit data nibbles are sent to the MII block. These data nibbles are clocked to the controller at a rate of 25MHz. The controller samples the data on the rising edge of RX_CLK. To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of RX_CLK. RX_CLK is the 25MHz output clock for the MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock (CLKIN).

When tracking the received data, RX_CLK has a maximum jitter of 0.8ns (provided that the jitter of the input clock, CLKIN, is below 100ps).

4.4 10Base-T Transmit

Data to be transmitted comes from the MAC layer controller. The 10Base-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

4.4.1 10M Transmit Data across the MII

The MAC controller drives the transmit data onto the TXD BUS. When the controller has driven TX_EN high to indicate valid data, the data is latched by the MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 2.5MHz data.

In order to comply with legacy 10Base-T MAC/Controllers, in Half-duplex mode the PHY loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The PHY also supports the SQE (Heartbeat) signal. See [Section 5.4.2, "Collision Detect," on page 43](#) for more details.

4.4.2 Manchester Encoding

The 4-bit wide data is sent to the TX10M block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TX_EN is low, the TX10M block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

4.4.3 10M Transmit Drivers

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

4.5 10Base-T Receive

The 10Base-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

4.5.1 10M Receive Input and Squelch

The Manchester signal from the cable is fed into the PHY (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

4.5.2 Manchester Decoding

The output of the SQUELCH goes to the RX10M block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition is indicated by the flag "XPOL", bit 4 in register 27. The 10M PLL is locked onto the received Manchester signal and from this, generates the received 20MHz clock. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

4.5.3 10M Receive Data across the MII

The 4 bit data nibbles are sent to the MII block. In MII mode, these data nibbles are valid on the rising edge of the 2.5 MHz RX_CLK.

4.5.4 Jabber detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TX_EN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TX_EN is deasserted, the logic resets the jabber condition.

Bit 1.1 indicates that a jabber condition was detected.

4.6 MAC Interface

The MII (Media Independent Interface) block is responsible for the communication with the controller. Special sets of hand-shake signals are used to indicate that valid received/transmitted data is present on the 4 bit receive/transmit bus.

Datasheet

4.6.1 MII

The MII includes 16 interface signals:

- transmit data - TXD[3:0]
- transmit strobe - TX_EN
- transmit clock - TX_CLK
- transmit error - TX_ER/TXD4
- receive data - RXD[3:0]
- receive strobe - RX_DV
- receive clock - RX_CLK
- receive error - RX_ER/RXD4
- collision indication - COL
- carrier sense - CRS

In MII mode, on the transmit path, the PHY drives the transmit clock, TX_CLK, to the controller. The controller synchronizes the transmit data to the rising edge of TX_CLK. The controller drives TX_EN high to indicate valid transmit data. The controller drives TX_ER high when a transmit error is detected.

On the receive path, the PHY drives both the receive data, RXD[3:0], and the RX_CLK signal. The controller clocks in the receive data on the rising edge of RX_CLK when the PHY drives RX_DV high. The PHY drives RX_ER high when a receive error is detected.

4.7 Auto-negotiation

The purpose of the Auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits in register 31, as well as the Link Partner Ability Register (Register 5).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The advertised capabilities of the PHY are stored in register 4 of the SMI registers. The default advertised by the PHY is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset

- Power-down reset
- Link status down
- Setting register 0, bit 9 high (auto-negotiation restart)

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in register 4 of the SMI registers.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex

If the full capabilities of the PHY are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of Half and Full duplex modes, then auto-negotiation selects Full Duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the PHY are initially determined by the logic levels latched on the MODE[2:0] bus after reset completes. This bus can also be used to disable auto-negotiation on power-up.

Writing register 4 bits [8:5] allows software control of the capabilities advertised by the PHY. Writing register 4 does not automatically re-start auto-negotiation. Register 0, bit 9 must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing register 0, bit 12.

The LAN83C185 does not support “Next Page” capability.

4.7.1 Parallel Detection

If the LAN83C185 is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be Half Duplex per the IEEE standard. This ability is known as “Parallel Detection. This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then bit 0 in register 6 is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register 6 is set.

Register 5 is used to store the Link Partner Ability information, which is coded in the received FLPs. If the Link Partner is not auto-negotiation capable, then register 5 is updated after completion of parallel detection to reflect the speed capability of the Link Partner.

4.7.2 Re-starting Auto-negotiation

Auto-negotiation can be re-started at any time by setting register 0, bit 9. Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to bit 9 of the control register, the LAN83C185 will respond by stopping all transmission/receiving operations. Once the `break_link_timer` is done, in the Auto-negotiation state-machine (approximately 1200ms) the auto-negotiation will re-start. The Link Partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

4.7.3 Disabling Auto-negotiation

Auto-negotiation can be disabled by setting register 0, bit 12 to zero. The device will then force its speed of operation to reflect the information in register 0, bit 13 (speed) and register 0, bit 8 (duplex). The speed and duplex bits in register 0 should be ignored when auto-negotiation is enabled.

4.7.4 Half vs. Full Duplex

Half Duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. In this mode, If data is received while the PHY is transmitting, a collision results.

In Full Duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

4.8 PHY Management Control

The Management Control module includes 3 blocks:

- Serial Management Interface (SMI)
- Management Registers Set
- Interrupt

4.8.1 Serial Management Interface (SMI)

The Serial Management Interface is used to control the LAN83C185 and obtain its status. This interface supports registers 0 through 6 as required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers 16 to 31 allowed by the specification. Non-supported registers (7 to 15) will be read as hexadecimal “FFFF”.

At the system level there are 2 signals, MDIO and MDC where MDIO is bi-directional open-drain and MDC is the clock.

A special feature (enabled by register 17 bit 3) forces the PHY to disregard the PHY-Address in the SMI packet causing the PHY to respond to any address. This feature is useful in multi-PHY applications and in production testing, where the same register can be written in all the PHYs using a single write transaction.

The MDC signal is an aperiodic clock provided by the station management controller (SMC). The MDIO signal receives serial data (commands) from the controller SMC, and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges.