Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LAN8700/LAN8700i

±15kV ESD Protected MII/RMII 10/100 Ethernet Transceiver with HP Auto-MDIX Support and flexPWR® Technology in a Small Footprint

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- ESD Protection levels of ±8kV HBM without external protection devices
- ESD protection levels of EN/IEC61000-4-2, ±8kV contact mode, and ±15kV for air discharge mode per independent test facility
- Comprehensive flexPWR® Technology
  - Flexible Power Management Architecture
- LVCMOS Variable I/O voltage range: +1.6V to +3.6V
- Integrated 3.3V to 1.8V regulator for optional single supply operation.
  - Regulator can be disabled if 1.8V system supply is available.
- Performs HP Auto-MDIX in accordance with IEEE 802.3ab specification
- Cable length greater than 150 meters
- Automatic Polarity Correction
- Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
- Energy Detect power-down mode
- Low Current consumption power down mode
- Low operating current consumption:
  - 39mA typical in 10BASE-T and
  - 79mA typical in 100BASE-TX mode
- Supports Auto-negotiation and Parallel Detection
- Supports the Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- Compliant with IEEE 802.3-2005 standards
  - MII Pins tolerant to 3.6V
- IEEE 802.3-2005 compliant register functions
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Vendor Specific register functions
- Low profile 36-pin QFN RoHS compliant package (6 x 6 x 0.9mm height)
- 4 LED status indicators
- Commercial Operating Temperature 0° C to 70° C
- Industrial Operating Temperature -40° C to 85° C version available (LAN8700i)

Applications

- Set Top Boxes
- Network Printers and Servers
- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- Personal Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- POS Terminals
- Automotive Networking
- Gaming Consoles
- Security Systems
- POE Applications
- Access Control

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 GENERAL DESCRIPTION

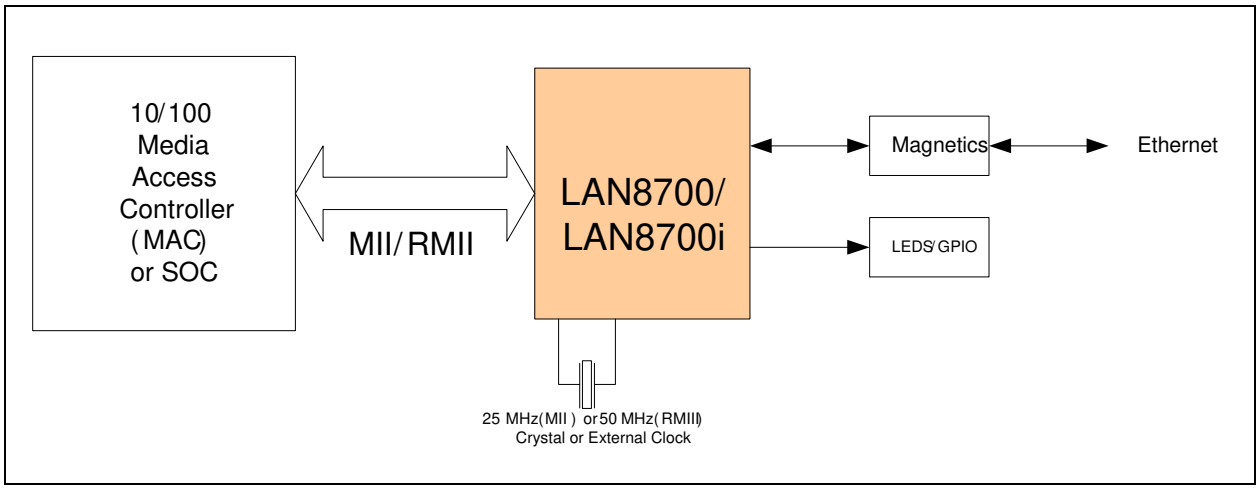
The Microchip LAN8700/LAN8700i is a low-power, industrial temperature (LAN8700i), variable I/O voltage, analog interface IC with HP Auto-MDIX support for high-performance embedded Ethernet applications. The LAN8700/LAN8700i can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.8V linear regulator. An option is available to disable the linear regulator to optimize system designs that have a 1.8V power plane available.

1.1 Architectural Overview

The LAN8700/LAN8700i consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions. The LAN8700/LAN8700i can be configured to support either the Media Independent Interface (MII) or the Reduced Media Independent Interface (RMII).

The LAN8700/LAN8700i is compliant with IEEE 802.3-2005 standards (MII Pins tolerant to 3.6V) and supports both IEEE 802.3-2005 compliant and vendor-specific register functions. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

FIGURE 1-1: LAN8700/LAN8700I SYSTEM BLOCK DIAGRAM



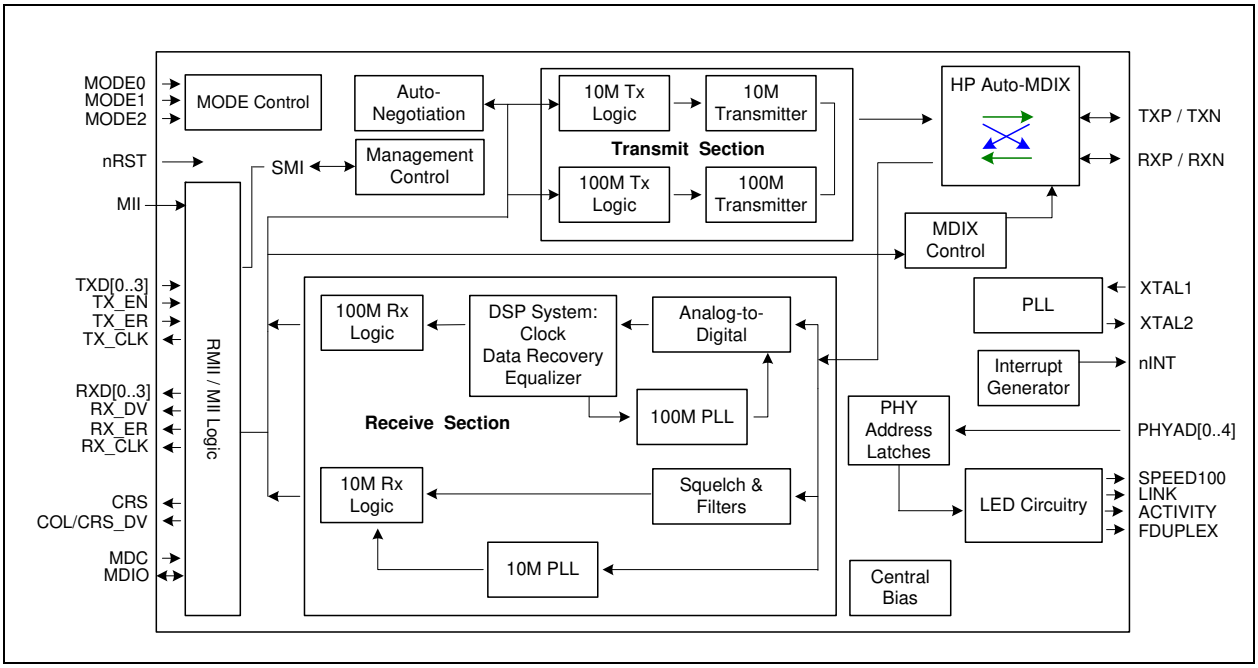
Hubs and switches with multiple integrated MACs and external PHYs can have a large pin count due to the high number of pins needed for each MII interface. An increasing pin count causes increasing cost.

The RMII interface is intended for use on Switch based ASICs or other embedded solutions requiring minimal pincount for ethernet connectivity. RMII requires only 6 pins for each MAC to PHY interface plus one common reference clock. The MII requires 16 pins for each MAC to PHY interface.

The Microchip LAN8700/LAN8700i is capable of running in RMII mode. Please contact your Microchip sales representative for the latest RMII specification.

The LAN8700/LAN8700i referenced throughout this document applies to both the commercial temperature and industrial temperature components. The LAN8700i refers to only the industrial temperature component.

FIGURE 1-2: LAN8700/LAN8700I ARCHITECTURAL OVERVIEW



2.0 PIN CONFIGURATION

2.1 Package Pin-out Diagram and Signal Table

FIGURE 2-1: PACKAGE PINOUT (TOP VIEW)

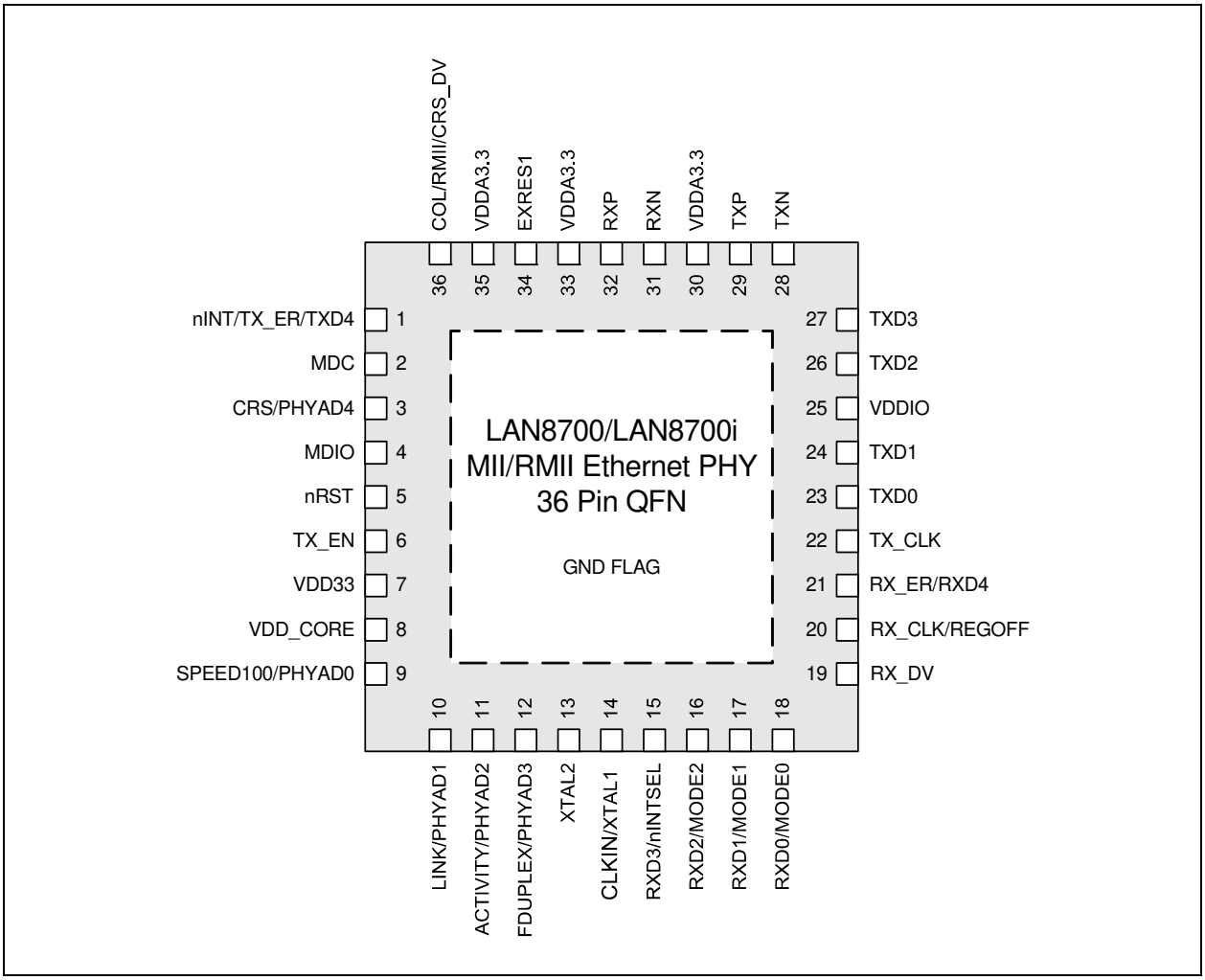


TABLE 2-1: LAN8700/LAN8700I 36-PIN QFN PINOUT

Pin No.	Pin Name	Pin No.	Pin Name
1	nINT/TX_ER/TXD4	19	RX_DV
2	MDC	20	RX_CLK/REGOFF
3	CRS/PHYAD4	21	RX_ER/RXD4
4	MDIO	22	TXCLK
5	nRST	23	TXD0
6	TX_EN	24	TXD1
7	VDD33	25	VDDIO
8	VDD_CORE	26	TXD2
9	SPEED100/PHYAD0	27	TXD3
10	LINK/PHYAD1	28	TXN
11	ACTIVITY/PHYAD2	29	TXP
12	FDUPLEX/PHYAD3	30	VDDA3.3
13	XTAL2	31	RXN
14	CLKIN/XTAL1	32	RXP
15	RXD3/nINTSEL	33	VDDA3.3
16	RXD2/MODE2	34	EXRES1
17	RXD1/MODE1	35	VDDA3.3
18	RXD0/MODE0	36	COL/RMII/CRS_DV

3.0 PIN DESCRIPTION

This chapter describes the signals on each pin. When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

3.1 I/O Signals

The following buffer types are shown in the TYPE column of the tables in this chapter.

- I Input. Digital LVCMOS levels.
- IPD Input with internal pull-down. Digital LVCMOS levels.
- O Output. Digital LVCMOS levels.
- OPD Output with internal pull-down. Digital LVCMOS levels.
- I/O Input or Output. Digital LVCMOS levels.
- IOPD Input or Output with internal pull-down. Digital LVCMOS levels.
- IOPU Input or Output with internal pull-up. Digital LVCMOS levels.

Note:	The digital signals are not 5V tolerant.They are variable voltage from +1.6V to +3.6V.

- AI Input. Analog levels.
- AO Output. Analog levels.

TABLE 3-1: MII SIGNALS

Signal Name	Type	Description
TXD0	I	**Transmit Data 0**: Bit 0 of the 4 data bits that are accepted by the PHY for transmission.
TXD1	I	**Transmit Data 1**: Bit 1 of the 4 data bits that are accepted by the PHY for transmission.
TXD2	I	**Transmit Data 2**: Bit 2 of the 4 data bits that are accepted by the PHY for transmission Note: This signal should be grounded in RMII Mode.
TXD3	I	**Transmit Data 3**: Bit 3 of the 4 data bits that are accepted by the PHY for transmission. Note: This signal should be grounded in RMII Mode
nINT/ TX_ER/ TXD4	IOPU	**MII Transmit Error**: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10Base-T operation. **MII Transmit Data 4:** In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line, the MSB of the 5-bit symbol code-group. • This signal is not used in RMII Mode. • This signal is mux’d with nINT • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional information on configuration/strapping options.
TX_EN	IPD	**Transmit Enable**: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. In RMII Mode, only TXD[1:0] have valid data.
TX_CLK	O	**Transmit Clock**: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. • This signal is not used in RMII Mode. • For proper TXCLK operation, RX_ER and RX_DV must NOT be driven high externally on a hardware reset or on a LAN8700 power up.

TABLE 3-1: MII SIGNALS (CONTINUED)

Signal Name	Type	Description
RXD0/ MODE0	IOPU	**Receive Data 0**: Bit 0 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 0:** set the default MODE of the PHY. Note: See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options
RXD1/ MODE1	IOPU	**Receive Data 1**: Bit 1 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 1:** set the default MODE of the PHY. Note: See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options.
RXD2/ MODE2	IOPU	**Receive Data 2**: Bit 2 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 2:** set the default MODE of the PHY. • RXD2 is not used in RMII Mode. • See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options.
RXD3/ nINTSEL	IOPU	**Receive Data 3**: Bit 3 of the 4 data bits that are sent by the PHY in the receive path. **nINTSEL**: On power-up or external reset, the mode of the nINT/TXER/TXD4 pin is selected. • When RXD3/nINTSEL is floated or pulled to VDDIO, nINT is selected for operation on pin nINT/TXER/TXD4 (default). • When RXD3/nINTSEL is pulled low to VSS through a resistor, (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25), TXER/TXD4 is selected for operation on pin nINT/TXER/TXD4. • RXD3 is not used in RMII Mode • If the nINT/TXER/TXD4 pin is configured for nINT mode, then a pull-up resistor is needed to VDDIO on the nINT/TXER/TXD4 pin. see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25. • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional information on configuration/strapping options.
RX_ER/ RXD4/	OPD	**Receive Error**: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. **MII Receive Data 4**: In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. Unless configured in this mode, the pin functions as RX_ER. Note: This pin has an internal pull-down resistor, and must not be high during reset. The RX_ER signal is optional in RMII Mode.
RX_DV	O	**Receive Data Valid**: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0]. Note: This pin has an internal pull-down resistor, and must not be high during reset. This signal is not used in RMII Mode.

TABLE 3-1: MII SIGNALS (CONTINUED)

Signal Name	Type	Description
RX_CLK/ REGOFF	IOPD	**Receive Clock**: In MII mode, this pin is the receive clock output. 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. Note: This signal is not used in RMII Mode. **Regulator Off**: This pin pulled up to configure the internal 1.8V regulator off. As described in Section 4.9, this pin is sampled during the power-on sequence to determine if the internal regulator should turn on. When the regulator is disabled, external 1.8V must be supplied to VDD_CORE, and the voltage at VDD33 must be at least 2.64V before voltage is applied to VDD_CORE.
COL/ RMII/ CRS_DV	IOPD	**MII Mode Collision Detect**: Asserted to indicate detection of collision condition. **RMII –** MII/RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the following strapping: • Float this pin for MII mode or pull-high with an external resistor to VDDIO (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25) to set the device in RMII mode. • See Section 4.6.3, "MII vs. RMII Configuration," on page 21 for more details. **RMII Mode CRS_DV (Carrier Sense/Receive Data Valid)** Asserted to indicate when the receive medium is non-idle. When a 10BT packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. In 10BT, half-duplex mode, transmitted data is not looped back onto the receive data pins, per the RMII standard.
CRS/ PHYAD4	IOPU	**Carrier Sense**: Indicates detection of carrier. Note: This signal is mux'd with PHYAD4

TABLE 3-2: LED SIGNALS

Signal Name	Type	Description
SPEED100/ PHYAD0	IOPU	**LED1 –** SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps. Note: This signal is mux'd with PHYAD0
LINK/ PHYAD1	IOPU	**LED2 –** LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on. Note: This signal is mux'd with PHYAD1
ACTIVITY/ PHYAD2	IOPU	**LED3 –** ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD. Note: This signal is mux'd with PHYAD2
FDUPLEX/ PHYAD3	IOPU	**LED4 –** DUPLEX indication. Active indicates that the PHY is in full-duplex mode. Note: This signal is mux'd with PHYAD3

TABLE 3-3: MANAGEMENT SIGNALS

Signal Name	Type	Description
MDIO	IOPD	**Management Data Input/OUTPUT**: Serial management data input/output.
MDC	IPD	**Management Clock**: Serial management clock.

TABLE 3-4: BOOT STRAP CONFIGURATION INPUTS (Note 3-1)

Signal Name	Type	Description
CRS/ PHYAD4	IOPU	**PHY Address Bit 4:** set the default address of the PHY. This signal is mux'd with CRS Note: This signal is mux'd with CRS
FDUPLEX/ PHYAD3	IOPU	**PHY Address Bit 3:** set the default address of the PHY. Note: This signal is mux'd with FDUPLEX
ACTIVITY/ PHYAD2	IOPU	**PHY Address Bit 2:** set the default address of the PHY. Note: This signal is mux'd with ACTIVITY
LINK/ PHYAD1	IOPU	**PHY Address Bit 1:** set the default address of the PHY. Note: This signal is mux'd with LINK
SPEED100/ PHYAD0	IOPU	**PHY Address Bit 0:** set the default address of the PHY. Note: This signal is mux'd with SPEED100
RXD2/ MODE2	IOPU	**PHY Operating Mode Bit 2:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD2
RXD1/ MODE1	IOPU	**PHY Operating Mode Bit 1:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD1
RXD0/ MODE0	IOPU	**PHY Operating Mode Bit 0:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD0
COL/ RMII/ CRS_DV	IOPD	**Digital Communication Mode:** set the digital communications mode of the PHY to RMII or MII. This signal is muxed with the Collision signal (MII mode) and Carrier Sense/ receive Data Valid (RMII mode) • Float for MII mode. • Pull up with a resistor to VDDIO for RMII mode (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25)
RXD3/ nINTSEL	IOPU	**nINT pin mode select:** set the mode of pin 1. • Default, left floating pin 1 is nINT, active low interrupt output. • For nINT mode, tie nINT/TXD4/TXER to VDDIO with a resistor (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25). • Pulled to VSS by a resistor, (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25) pin 1 is TX_ER/TXD4, Transmit Error or Transmit data 4 (5B mode). • For TXD4/TXER mode, do not tie nINT/TXD4/TXER to VDDIO or Ground.

Note 3-1 On nRST transition high, the PHY latches the state of the configuration pins in this table.

TABLE 3-5: GENERAL SIGNALS

Signal Name	Type	Description
nINT/ TX_ER/ TXD4	IOPU	**LAN Interrupt** – Active Low output. Place an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) pull-up to VCC 3.3V. • This signal is mux’d with TXER/TXD4 • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional details on Strapping options.
nRST	I	**External Reset** – input of the system reset. This signal is active LOW. When this pin is deasserted, the mode register bits are loaded from the mode pins as described in Section 5.4.9.2.
CLKIN/ XTAL1	I/O	**Clock Input** – 25 Mhz or 50 MHz external clock or crystal input. • In MII mode, this signal is the 25 MHz reference input clock • In RMII mode, this signal is the 50 MHz reference input clock which is typically also driven to the RMII compliant Ethernet MAC clock input. Note: See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional details on Strapping options.
XTAL2	O	**Clock Output** – 25 MHz crystal output. Note: Float this pin if using an external clock being driven through CLKIN/XTAL1

TABLE 3-6: 10/100 LINE INTERFACE

Signal Name	Type	Description
TXP	AO	**Transmit Data Positive**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
TXN	AO	**Transmit Data Negative**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
RXP	AI	**Receive Data Positive**: 100Base-TX or 10Base-T differential receive inputs from magnetics.
RXN	AI	**Receive Data Negative**: 100Base-TX or 10Base-T differential receive inputs from magnetics.

TABLE 3-7: ANALOG REFERENCES

Signal Name	Type	Description
EXRES1	AI	Connects to reference resistor of value 12.4K-Ohm, 1% connected as described in the Analog Layout Guidelines. The nominal voltage is 1.2V and therefore the resistor will dissipate approximately 1mW of power.

TABLE 3-8: POWER SIGNALS

Signal Name	Type	Description
VDDIO	POWER	+1.6V to +3.6V Variable I/O Pad Power
VDD33	POWER	+3.3V Core Regulator Input.
VDDA3.3	POWER	+3.3V Analog Power
VDD_CORE	POWER	+1.8V (Core voltage) - 1.8V for digital circuitry on chip. Supplied by the on-chip regulator unless configured for regulator off mode using the RX_CLK/REGOFF pin. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. When using the on-chip regulator, place a 4.7uF ±20% capacitor with ESR < 1ohm near this pin and connect the capacitor from this pin to ground. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1ohm at frequencies greater than 10kHz.
VSS	POWER	Exposed Ground Flag. The flag must be connected to the ground plane with an array of vias as described in the Analog Layout Guidelines

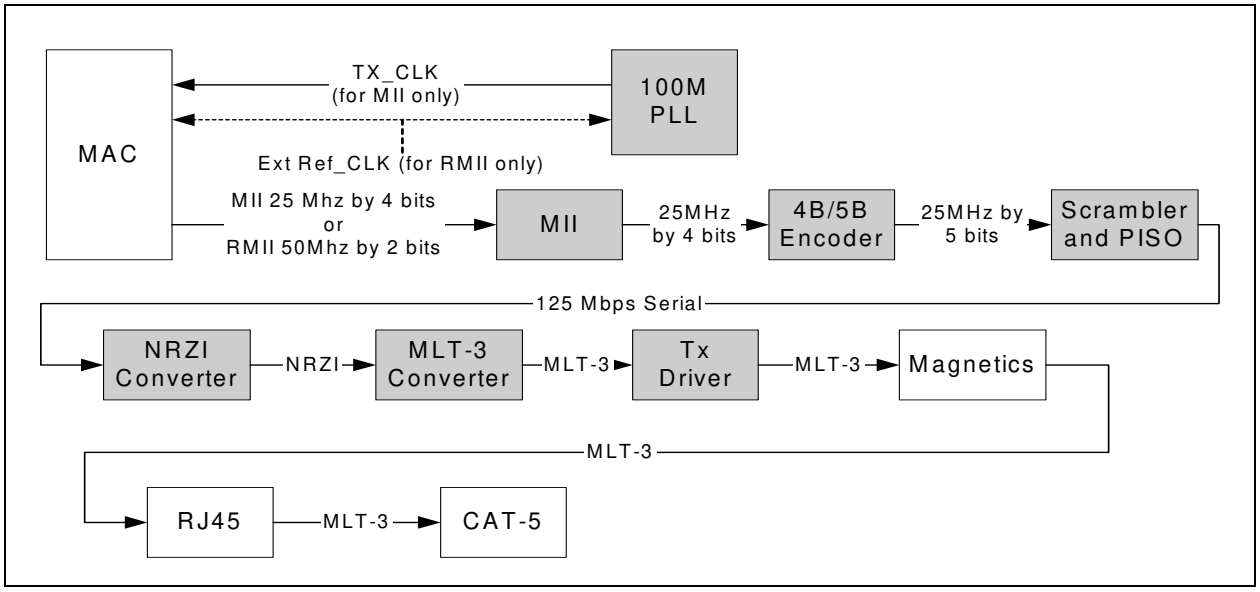
4.0 ARCHITECTURE DETAILS

4.1 Top Level Functional Architecture

Functionally, the PHY can be divided into the following sections:

- 100Base-TX transmit and receive
- 10Base-T transmit and receive
- MII or RMII interface to the controller
- Auto-negotiation to automatically determine the best speed and duplex possible
- Management Control to read status registers and write control registers

FIGURE 4-1: 100BASE-TX DATA PATH



4.2 100Base-TX Transmit

The data path of the 100Base-TX is shown in Figure 4-1. Each major block is explained below.

4.2.1 100M TRANSMIT DATA ACROSS THE MII/RMII INTERFACE

For MII, the MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 25MHz data.

The MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50MHz data.

4.2.2 4B/5B ENCODING

The transmit data passes from the MII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to Table 4-1. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

The encoding process may be bypassed by clearing bit 6 of register 31. When the encoding is bypassed the 5th transmit data bit is equivalent to TX_ER.

Note that encoding can be bypassed only when the MAC interface is configured to operate in MII mode.

TABLE 4-1: 4B/5B CODE TABLE

Code Group	SYM	Receiver Interpretation			Transmitter Interpretation		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001		1	0001	
10100	2	2	0010		2	0010	
10101	3	3	0011		3	0011	
01010	4	4	0100		4	0100	
01011	5	5	0101		5	0101	
01110	6	6	0110		6	0110	
01111	7	7	0111		7	0111	
10010	8	8	1000		8	1000	
10011	9	9	1001		9	1001	
10110	A	A	1010		A	1010	
10111	B	B	1011		B	1011	
11010	C	C	1100		C	1100	
11011	D	D	1101		D	1101	
11100	E	E	1110		E	1110	
11101	F	F	1111		F	1111	
11111	I	IDLE			Sent after /T/R until TX_EN		
11000	J	First nibble of SSD, translated to “0101” following IDLE, else RX_ER			Sent for rising TX_EN		
10001	K	Second nibble of SSD, translated to “0101” following J, else RX_ER			Sent for rising TX_EN		
01101	T	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RX_ER			Sent for falling TX_EN		
00111	R	Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RX_ER			Sent for falling TX_EN		
00100	H	Transmit Error Symbol			Sent for rising TX_ER		
00110	V	INVALID, RX_ER if during RX_DV			INVALID		
11001	V	INVALID, RX_ER if during RX_DV			INVALID		
00000	V	INVALID, RX_ER if during RX_DV			INVALID		
00001	V	INVALID, RX_ER if during RX_DV			INVALID		
00010	V	INVALID, RX_ER if during RX_DV			INVALID		
00011	V	INVALID, RX_ER if during RX_DV			INVALID		
00101	V	INVALID, RX_ER if during RX_DV			INVALID		
01000	V	INVALID, RX_ER if during RX_DV			INVALID		
01100	V	INVALID, RX_ER if during RX_DV			INVALID		
10000	V	INVALID, RX_ER if during RX_DV			INVALID		

4.2.3 SCRAMBLING

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the PHY address, PHYAD[4:0], ensuring that in multiple-PHY applications, such as repeaters or switches, each PHY will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

4.2.4 NRZI AND MLT3 ENCODING

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

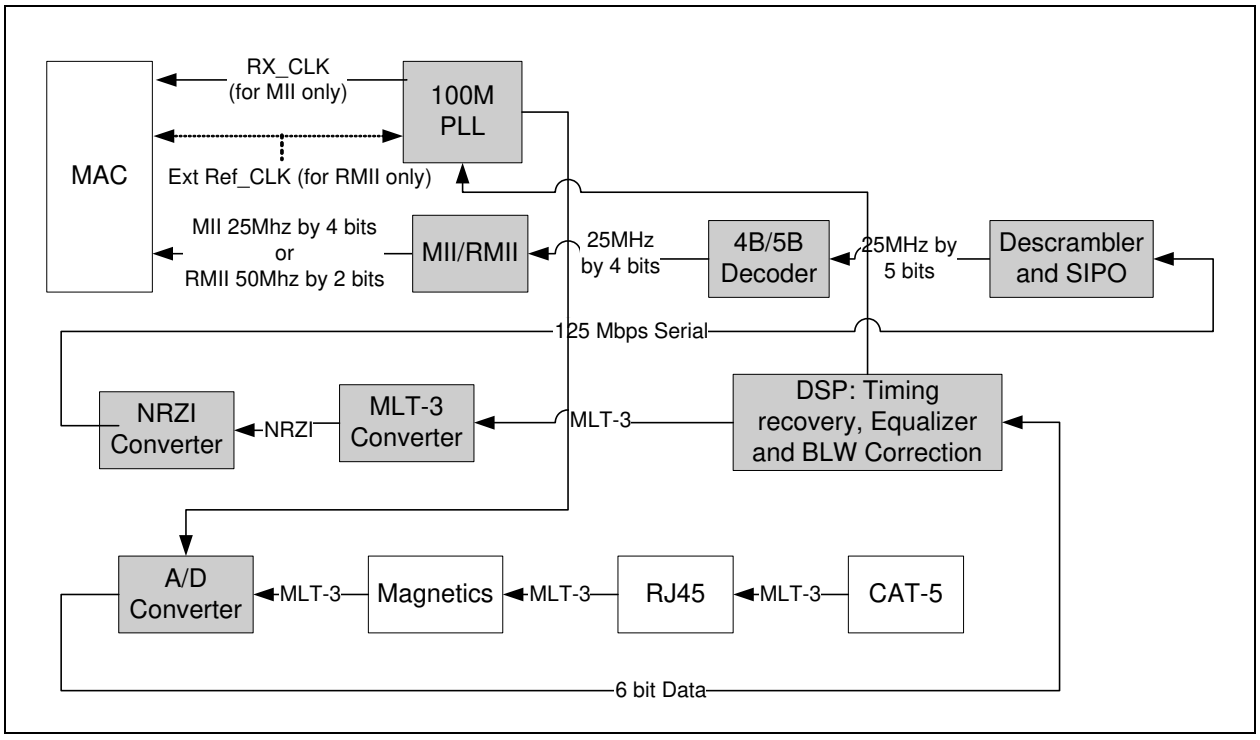
4.2.5 100M TRANSMIT DRIVER

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10Base-T and 100Base-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

4.2.6 100M PHASE LOCK LOOP (PLL)

The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100Base-Tx Transmitter.

FIGURE 4-2: RECEIVE DATA PATH



4.3 100Base-TX Receive

The receive data path is shown in Figure 4-2. Detailed descriptions are given below.

4.3.1 100M RECEIVE INPUT

The MLT-3 from the cable is fed into the PHY (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quanitizer it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

4.3.2 EQUALIZER, BASELINE WANDER CORRECTION AND CLOCK AND DATA RECOVERY

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT- 5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

4.3.3 NRZI AND MLT-3 DECODING

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

4.3.4 DESCRAMBLING

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The descrambler can be bypassed by setting bit 0 of register 31.

4.3.5 ALIGNMENT

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

4.3.6 5B/4B DECODING

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[3:0] signal lines. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RX_DV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RX_DV.

These symbols are not translated into data.

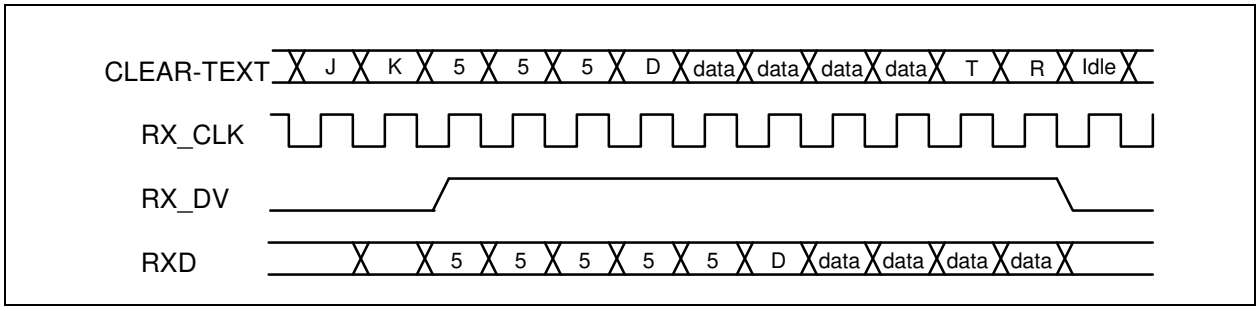
The decoding process may be bypassed by clearing bit 6 of register 31. When the decoding is bypassed the 5^{th} receive data bit is driven out on RX_ER/RXD4. Decoding may be bypassed only when the MAC interface is in MII mode.

4.3.7 RECEIVE DATA VALID SIGNAL

The Receive Data Valid signal (RX_DV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RX_CLK. RX_DV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RX_DV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII mode).

FIGURE 4-3: RELATIONSHIP BETWEEN RECEIVED DATA AND SPECIFIC MII SIGNALS



4.3.8 RECEIVER ERRORS

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RX_ER signal is asserted and arbitrary data is driven onto the RXD[3:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RX_ER is asserted true and the value '1110' is driven onto the RXD[3:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

4.3.9 100M RECEIVE DATA ACROSS THE MII/RMII INTERFACE

In MII mode, the 4-bit data nibbles are sent to the MII block. These data nibbles are clocked to the controller at a rate of 25MHz. The controller samples the data on the rising edge of RX_CLK. To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of RX_CLK. RX_CLK is the 25MHz output clock for the MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock (CLKIN).

When tracking the received data, RX_CLK has a maximum jitter of 0.8ns (provided that the jitter of the input clock, CLKIN, is below 100ps).

In RMII mode, the 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50MHz. The controller samples the data on the rising edge of CLKIN/XTAL1 (REF_CLK). To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of CLKIN/XTAL1 (REF_CLK).

4.4 10Base-T Transmit

Data to be transmitted comes from the MAC layer controller. The 10Base-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

4.4.1 10M TRANSMIT DATA ACROSS THE MII/RMII INTERFACE

The MAC controller drives the transmit data onto the TXD BUS. For MII, when the controller has driven TX_EN high to indicate valid data, the data is latched by the MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 2.5MHz data.

In order to comply with legacy 10Base-T MAC/Controllers, in Half-duplex mode the PHY loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The PHY also supports the SQE (Heartbeat) signal. See Section 5.4.2, "Collision Detect," on page 42, for more details.

For RMII, TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the LAN8700/LAN8700i. TXD[1:0] shall be “00” to indicate idle when TX_EN is deasserted. Values of TXD[1:0] other than “00” when TX_EN is deasserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TX_EN is deasserted shall be ignored by the LAN8700/LAN8700i.TXD[1:0] shall provide valid data for each REF_CLK period while TX_EN is asserted.

4.4.2 MANCHESTER ENCODING

The 4-bit wide data is sent to the TX10M block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TX_EN is low), the TX10M block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

4.4.3 10M TRANSMIT DRIVERS

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

4.5 10Base-T Receive

The 10Base-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

4.5.1 10M RECEIVE INPUT AND SQUELCH

The Manchester signal from the cable is fed into the PHY (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

4.5.2 MANCHESTER DECODING

The output of the SQUELCH goes to the RX10M block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition is indicated by the flag “XPOL“, bit 4 in register 27. The 10M PLL is locked onto the received Manchester signal and from this, generates the received 20MHz clock. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

4.5.3 10M RECEIVE DATA ACROSS THE MII/RMII INTERFACE

For MII, the 4 bit data nibbles are sent to the MII block. In MII mode, these data nibbles are valid on the rising edge of the 2.5 MHz RX_CLK.

For RMII, the 2bit data nibbles are sent to the RMII block. In RMII mode, these data nibbles are valid on the rising edge of the RMII REF_CLK.

4.5.4 JABBER DETECTION

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TX_EN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TX_EN is deasserted, the logic resets the jabber condition.

As shown in Table 5-31, bit 1.1 indicates that a jabber condition was detected.

4.6 MAC Interface

The MII/RMII block is responsible for the communication with the controller. Special sets of hand-shake signals are used to indicate that valid received/transmitted data is present on the 4 bit receive/transmit bus.

The device must be configured in MII or RMII mode. See Section 4.6.3, "MII vs. RMII Configuration," on page 21.

4.6.1 MII

The MII includes 16 interface signals:

- transmit data - TXD[3:0]
- transmit strobe - TX_EN
- transmit clock - TX_CLK
- transmit error - TX_ER/TXD4
- receive data - RXD[3:0]
- receive strobe - RX_DV
- receive clock - RX_CLK
- receive error - RX_ER/RXD4
- collision indication - COL
- carrier sense - CRS

In MII mode, on the transmit path, the PHY drives the transmit clock, TX_CLK, to the controller. The controller synchronizes the transmit data to the rising edge of TX_CLK. The controller drives TX_EN high to indicate valid transmit data. The controller drives TX_ER high when a transmit error is detected.

On the receive path, the PHY drives both the receive data, RXD[3:0], and the RX_CLK signal. The controller clocks in the receive data on the rising edge of RX_CLK when the PHY drives RX_DV high. The PHY drives RX_ER high when a receive error is detected.

4.6.2 RMII

The Microchip LAN8700/LAN8700i supports the low pin count Reduced Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch ASICs. Under IEEE 802.3, an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as switches, the number of pins can add significant cost as the port counts increase. The management interface (MDIO/MDC) is identical to MII. The RMII interface has the following characteristics:

- It is capable of supporting 10Mb/s and 100Mb/s data rates
- A single clock reference is sourced from the MAC to PHY (or from an external source)
- It provides independent 2 bit wide (di-bit) transmit and receive data paths
- It uses LVCMOS signal levels, compatible with common digital CMOS ASIC processes

The RMII includes 6 interface signals with one of the signals being optional:

- transmit data - TXD[1:0]
- transmit strobe - TX_EN
- receive data - RXD[1:0]
- receive error - RX_ER (Optional)
- carrier sense - CRS_DV
- Reference Clock - CLKIN/XTAL1 (RMII references usually define this signal as REF_CLK)

4.6.2.1 Reference Clock

The Reference Clock - CLKIN, is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. The Reference Clock is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device.

The “Reference Clock” frequency must be 50 MHz ± 50 ppm with a duty cycle between 40% and 60% inclusive. The Microchip LAN8700/LAN8700i uses the “Reference Clock” as the network clock such that no buffering is required on the transmit data path. The Microchip LAN8700/LAN8700i will recover the clock from the incoming data stream, the receiver will account for differences between the local REF_CLK and the recovered clock through use of sufficient elas-

ticity buffering. The elasticity buffer does not affect the Inter-Packet Gap (IPG) for received IPGs of 36 bits or greater. To tolerate the clock variations specified here for Ethernet MTUs, the elasticity buffer shall tolerate a minimum of ±10 bits.

4.6.2.2 CRS_DV - Carrier Sense/Receive Data Valid

The CRS_DV is asserted by the LAN8700/LAN8700i when the receive medium is non-idle. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected, carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (i.e. CRS_DV is deasserted only on nibble boundaries). If the LAN8700/LAN8700i has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the LAN8700/LAN8700i shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and de-assert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is: Starting on nibble boundaries CRS_DV toggles at 25 MHz in 100Mb/s mode and 2.5 MHz in 10Mb/s mode when CRS ends before RX_DV (i.e. the FIFO still has bits to transfer when the carrier event ends.) Therefore, the MAC can accurately recover RX_DV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place.

4.6.3 MII VS. RMII CONFIGURATION

The LAN8700/LAN8700i must be configured to support the MII or RMII bus for connectivity to the MAC. This configuration is done through the COL/RMII/CRS_DV pin. To select MII mode, float the COL/RMII/CRS_DV pin. To select RMII mode, pull the pin high with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to VDDIO. On the rising edge of the internal reset (nreset), the register bit 18.14 (MIIMODE) is loaded based on the strapping of the COL/RMII/CRS_DV pin.

Most of the MII and RMII pins are multiplexed. Table 4-2, "MII/RMII Signal Mapping", shown below, describes the relationship of the related device pins to what pins are used in MII and RMII mode.

TABLE 4-2: MII/RMII SIGNAL MAPPING

Signal Name	MII Mode	RMII Mode
TXD0	TXD0	TXD0
TXD1	TXD1	TXD1
TX_EN	TX_EN	TX_EN
RX_ER/ RXD4	RX_ER/ RXD4/	RX_ER Note 4-2
COL/RMII/ CRS_DV	COL	CRS_DV
RXD0	RXD0	RXD0
RXD1	RXD1	RXD1
TXD2	TXD2	Note 4-1
TXD3	TXD3	Note 4-1
TX_ER/ TXD4	TX_ER/ TXD4	
CRS	CRS	
RX_DV	RX_DV	
RXD2	RXD2	
RXD3/ nINTSEL	RXD3	
TX_CLK	TX_CLK	
RX_CLK	RX_CLK	
CLKIN/ XTAL1	CLKIN/ XTAL1	REF_CLK

Note 4-1 In RMII mode, this pin needs to tied to VSS.

Note 4-2 The RX_ER signal is optional on the RMII bus. This signal is required by the PHY, but it is optional for the MAC. The MAC can choose to ignore or not use this signal.

4.7 Auto-negotiation

The purpose of the Auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits in register 31, as well as the Link Partner Ability Register (Register 5).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The advertised capabilities of the PHY are stored in register 4 of the SMI registers. The default advertised by the PHY is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting register 0, bit 9 high (auto-negotiation restart)

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in register 4 of the SMI registers.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex

If the full capabilities of the PHY are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of Half and Full duplex modes, then auto-negotiation selects Full Duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the PHY are initially determined by the logic levels latched on the MODE[2:0] bus after reset completes. This bus can also be used to disable auto-negotiation on power-up.

Writing register 4 bits [8:5] allows software control of the capabilities advertised by the PHY. Writing register 4 does not automatically re-start auto-negotiation. Register 0, bit 9 must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing register 0, bit 12.

The LAN8700/LAN8700i does not support “Next Page” capability.

4.7.1 PARALLEL DETECTION

If the LAN8700/LAN8700i is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be Half Duplex per the IEEE standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then bit 0 in register 6 is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register 6 is set.

Register 5 is used to store the Link Partner Ability information, which is coded in the received FLPs. If the Link Partner is not auto-negotiation capable, then register 5 is updated after completion of parallel detection to reflect the speed capability of the Link Partner.

4.7.2 RE-STARTING AUTO-NEGOTIATION

Auto-negotiation can be re-started at any time by setting register 0, bit 9. Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to bit 9 of the control register, the LAN8700/LAN8700i will respond by stopping all transmission/receiving operations. Once the break_link_timer is done, in the Auto-negotiation state-machine (approximately 1200ms) the auto-negotiation will re-start. The Link Partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

4.7.3 DISABLING AUTO-NEGOTIATION

Auto-negotiation can be disabled by setting register 0, bit 12 to zero. The device will then force its speed of operation to reflect the information in register 0, bit 13 (speed) and register 0, bit 8 (duplex). The speed and duplex bits in register 0 should be ignored when auto-negotiation is enabled.

4.7.4 HALF VS. FULL DUPLEX

Half Duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. In this mode, If data is received while the PHY is transmitting, a collision results.

In Full Duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

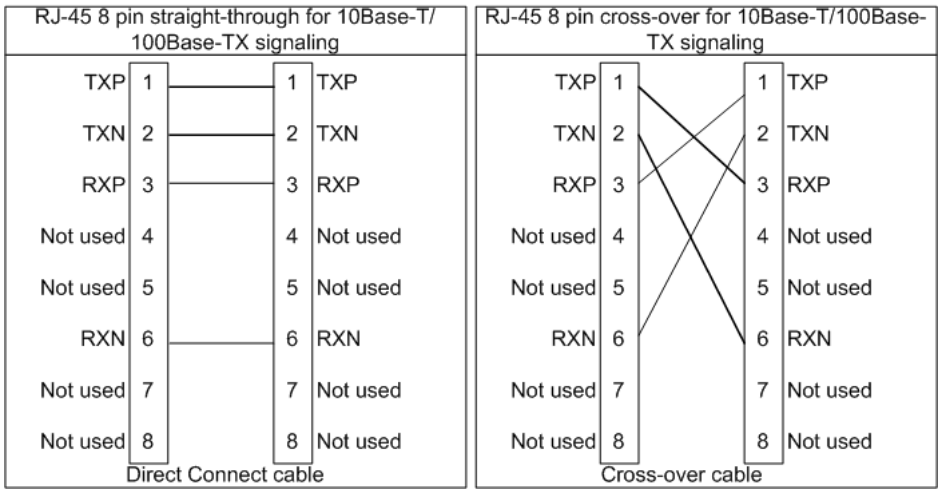
4.8 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-3 (10 Base-T) or CAT-5 (100 Base-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a cross-over patch cable, as shown in FIGURE 4-4: on page 24, the Microchip LAN8700/LAN8700i Auto-MDIX PHY is capable of configuring the TXP/TXN and RXP/RXN pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled through an internal register.

FIGURE 4-4: DIRECT CABLE CONNECTION VS. CROSS-OVER CABLE CONNECTION



4.9 Internal +1.8V Regulator Disable

One feature of the flexPWR technology is the ability to configure the internal 1.8V regulator off. When the regulator is disabled, external 1.8V must be supplied to VDD_CORE. This makes it possible to reduce total system power, since an external switching regulator with greater efficiency than the internal linear regulator may be used to provide the +1.8V to the PHY circuitry.

4.9.1 DISABLE THE INTERNAL +1.8V REGULATOR

To disable the +1.8V internal regulator, a pullup strapping resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) is connected from RXCLK/REGOFF to VDDIO. At power-on, after both VDDIO and VDDA are within specification, the PHY will sample the RXCLK/REGOFF pin to determine if the internal regulator should turn on. If the pin is sampled at a voltage greater than V_{IH}, then the internal regulator is disabled, and the system must supply +1.8V to the VDD_CORE pin. The voltage at VDD33 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDD_CORE. As described in Section 4.9.2, when the RXCLK/REGOFF pin is left floating or connected to VSS, then the internal regulator is enabled and the system does not supply +1.8V to the VDD_CORE pin.

When the +1.8V internal regulator is disabled, a 0.1uF capacitor must be added at the VDD_CORE pin and placed close to the PHY to decouple the external power supply.

4.9.2 ENABLE THE INTERNAL +1.8V REGULATOR

The 1.8V for VDD_CORE is supplied by the on-chip regulator unless the PHY is configured for regulator off mode using the RX_CLK/REGOFF pin as described in Section 4.9.1. By default, the internal +1.8V regulator is enabled when the RXCLK/REGOFF pin is floating. As shown in Table 7-11, an internal pull-down resistor straps the regulator on if the RXCLK/REGOFF pin is floating.

During VDDIO and VDDA power-on, if the RXCLK/REGOFF pin is sampled below V_{IL}, then the internal +1.8V regulator will turn on and operate with power from the VDD33 pin.

When using the internal linear regulator, a 4.7uF bypass capacitor with ESR < 1ohm and a 0.1uF capacitor must always be added to VDD_CORE and placed close to the PHY to ensure stability of the internal regulator.

4.10 nINT/TX_ER/TXD4 Strapping

The nINT, TX_ER, and TXD4 functions share a common pin. There are two functional modes for this pin, the TX_ER/TXD4 mode and nINT (interrupt) mode. The RXD3/nINTSEL pin is used to select one of these two functional modes.

The RXD3/nINTSEL pin is latched on the rising edge of the nRST. The system designer must float the nINTSEL pin to put the nINT/TX_ER/TXD4 pin into nINT mode or pull-low to VSS with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to set the device in TX_ER/TXD4 mode. The default setting is to float the pin high for nINT mode.

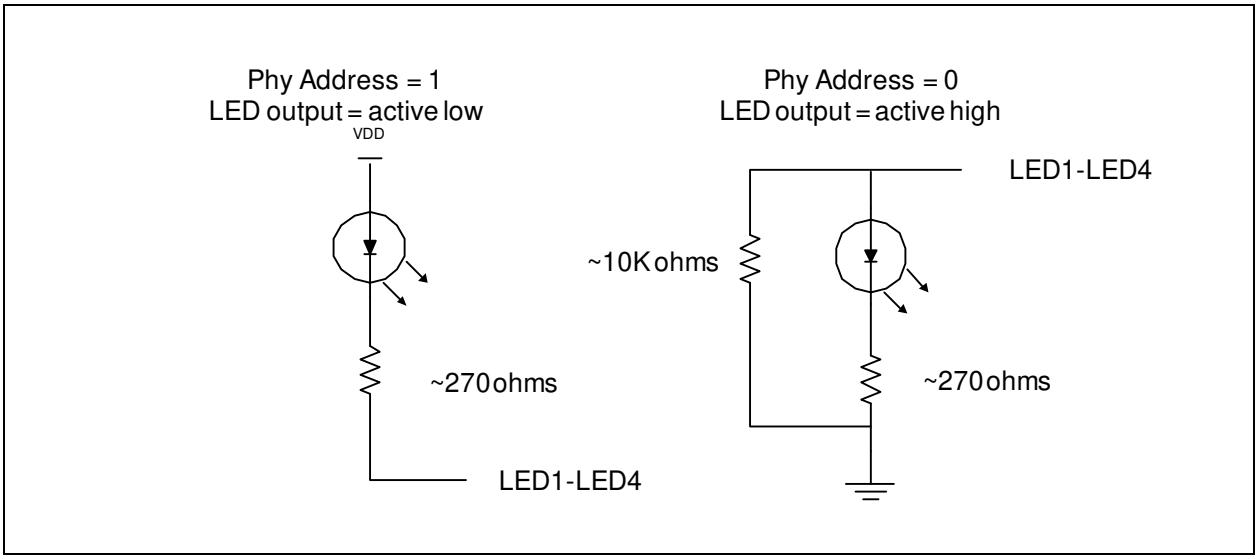
4.11 PHY Address Strapping and LED Output Polarity Selection

The PHY ADDRESS bits are latched on the rising edge of the internal reset (nRESET). The 5-bit address word[0:4] is input on the PHYAD[0:4] pins. The default setting is all high 5'b1_1111.

The address lines are strapped as defined in the diagram below. The LED outputs will automatically change polarity based on the presence of an external pull-down resistor. If the LED pin is pulled high (by an internal 100K pull-up resistor) to select a logical high PHY address, then the LED output will be active low. If the LED pin is pulled low (by an external pull-down resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to select a logical low PHY address, the LED output will then be an active high output.

To set the PHY address on the LED pins without LEDs or on the CRS pin, float the pin to set the address high or pull-down the pin with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to GND to set the address low. See Figure 4-5, "PHY Address Strapping on LEDs":

FIGURE 4-5: PHY ADDRESS STRAPPING ON LEDS



4.12 Variable Voltage I/O

The Digital I/O pins on the LAN8700/LAN8700i are variable voltage to take advantage of low power savings from shrinking technologies. These pins can operate from a low I/O voltage of +1.8V-10% up to +3.3V+10%. Due to this low voltage feature addition, the system designer needs to take consideration as for two aspects of their design. Boot strapping configuration and I/O voltage stability.

4.12.1 BOOT STRAPPING CONFIGURATION

Due to a lower I/O voltage, a lower strapping resistor needs to be used to ensure the strapped configuration is latched into the PHY device at power-on reset.

TABLE 4-3: BOOT STRAPPING CONFIGURATION RESISTORS

I/O Voltage	Pull-up/Pull-down Resistor
3.0 to 3.6	10k ohm resistor
2.0 to 3.0	7.5k ohm resistor
1.6 to 2.0	5k ohm resistor