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LAN8720A/LAN8720AI

Small Footprint RMII 10/100 Ethernet Transceiver with HP Auto-MDIX Support

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Comprehensive flexPWR® Technology
  - Flexible Power Management Architecture
  - LVCMOS Variable I/O voltage range: +1.6V to +3.6V
  - Integrated 1.2V regulator
- HP Auto-MDIX support
- Miniature 24-pin QFN/SQFN lead-free RoHS compliant packages (4 x 4mm).

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adapters/Servers
- Gaming Consoles
- POE Applications (Refer to Application Note 17.18)

Key Benefits

- High-Performance 10/100 Ethernet Transceiver
  - Compliant with IEEE802.3/802.3u (Fast Ethernet)
  - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
  - Loop-back modes
  - Auto-negotiation
  - Automatic polarity detection and correction
  - Link status change wake-up detection
  - Vendor specific register functions
  - Supports the reduced pin count RMII interface
- Power and I/Os
  - Various low power modes
  - Integrated power-on reset circuit
  - Two status LED outputs
  - Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
  - May be used with a single 3.3V supply
- Additional Features
  - Ability to use a low cost 25Mhz crystal for reduced BOM
- Packaging
  - 24-pin QFN/SQFN (4x4 mm) Lead-Free RoHS Compliant package with RMII
- Environmental
  - Extended commercial temperature range (0°C to +85°C)
  - Industrial temperature range version available (-40°C to +85°C)

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Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BYTE	8-bits
FIFO	First In First Out buffer; often used for elasticity buffer
MAC	Media Access Controller
RMII™	Reduced Media Independent Interface™
N/A	Not Applicable
X	Indicates that a logic state is “don’t care” or undefined.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SMI	Serial Management Interface

1.2 General Description

The LAN8720A/LAN8720Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8720A/LAN8720Ai supports communication with an Ethernet MAC via a standard RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps (10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8720A/LAN8720Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The LAN8720A/LAN8720Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in Section 3.7, "Configuration Straps," on page 29. Register-selectable configuration options may be used to further define the functionality of the transceiver.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. The device can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8720A/LAN8720Ai is available in both extended commercial and industrial temperature range versions. A typical system application is shown in Figure 1-1.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM

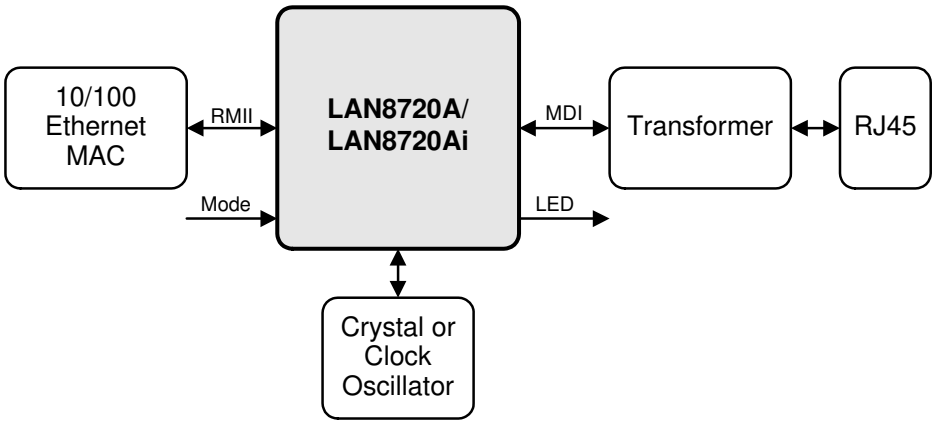
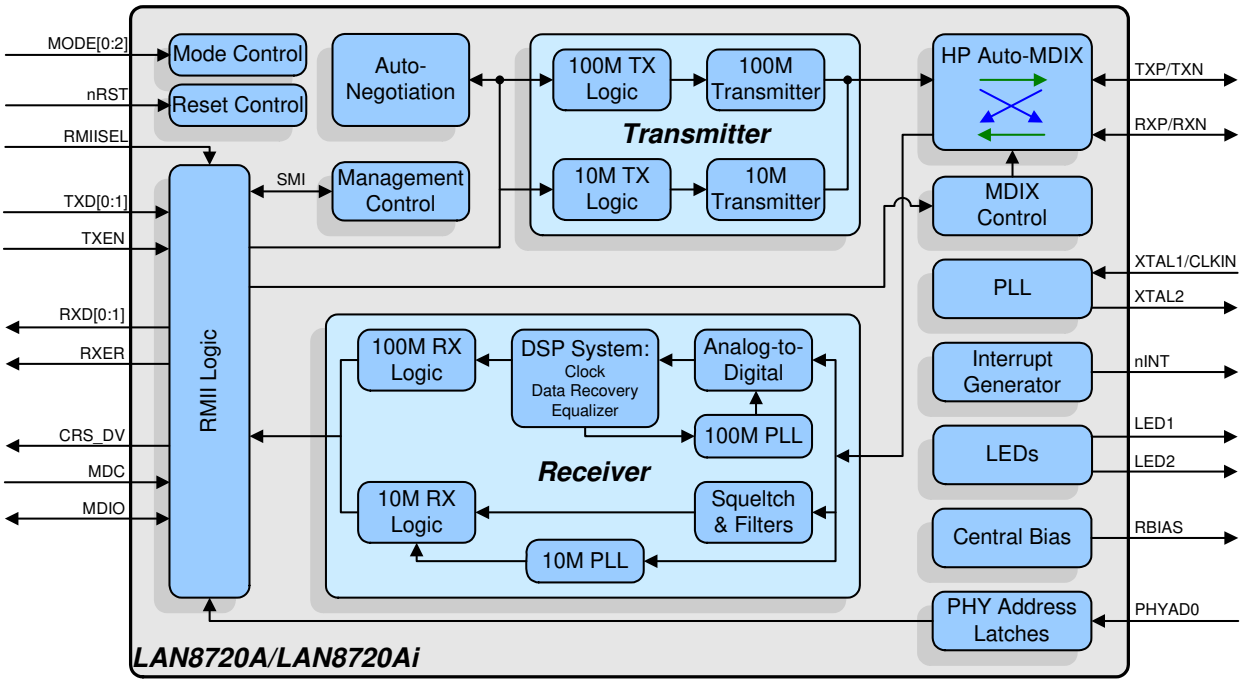
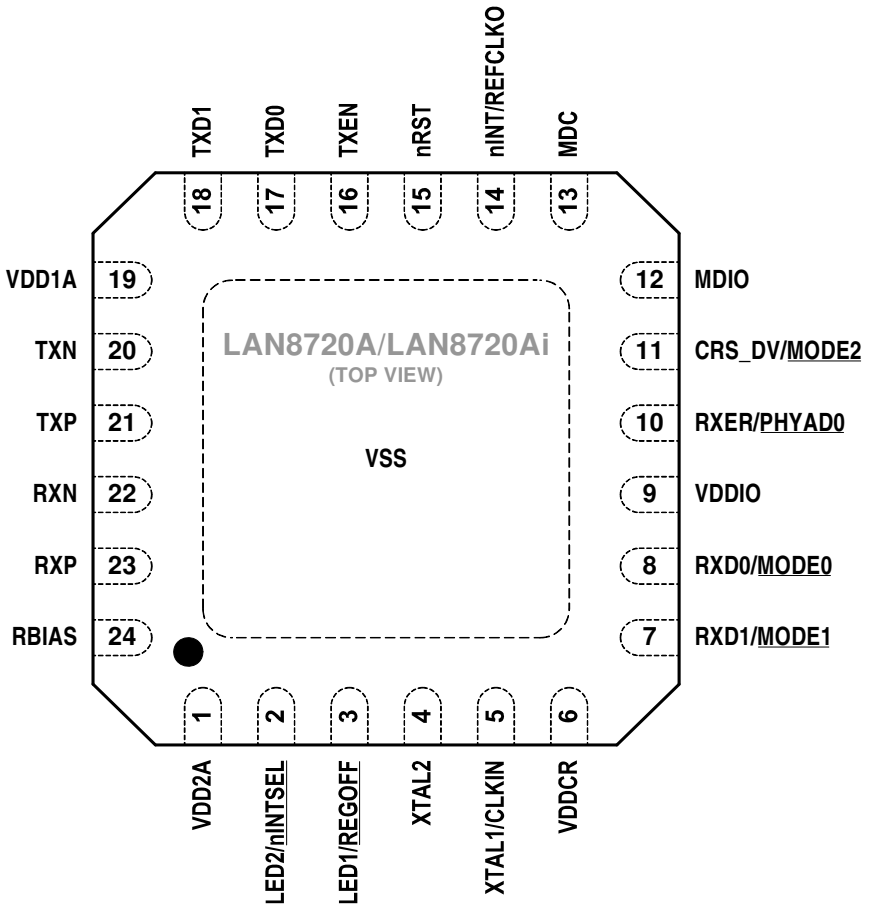


FIGURE 1-2: ARCHITECTURAL OVERVIEW



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 24-QFN/SQFN PIN ASSIGNMENTS (TOP VIEW)



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Note 2-1 When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

Note 2-2 The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in Section 2.2.

TABLE 2-1: RMII SIGNALS

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 0	TXD0	VIS	The MAC transmits data to the transceiver using this signal.
1	Transmit Data 1	TXD1	VIS	The MAC transmits data to the transceiver using this signal.
1	Transmit Enable	TXEN	VIS (PD)	Indicates that valid transmission data is present on TXD[1:0].
1	Receive Data 0	RXD0	VO8	Bit 0 of the 2 data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 0 Configuration Strap	MODE0	VIS (PU)	Combined with MODE1 and MODE2, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional details.
1	Receive Data 1	RXD1	VO8	Bit 1 of the 2 data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 1 Configuration Strap	MODE1	VIS (PU)	Combined with MODE0 and MODE2, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional details.
1	Receive Error	RXER	VO8	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver.
	PHY Address 0 Configuration Strap	PHYAD0	VIS (PD)	This configuration strap sets the transceiver's SMI address. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[0]: PHY Address Configuration," on page 26 for additional information.

TABLE 2-1: RMII SIGNALS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Carrier Sense / Receive Data Valid	CRS_DV	VO8	This signal is asserted to indicate the receive medium is non-idle. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. **Note:** Per the RMII standard, transmitted data is not looped back onto the receive data pins in 10BASE-T half-duplex mode.
	PHY Operating Mode 2 Configuration Strap	MODE2	VIS (PU)	Combined with MODE0 and MODE1, this configuration strap sets the default PHY mode. See Note 2-3 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 27 for additional details.

Note 2-3 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 29 for additional information.

TABLE 2-2: LED PINS

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	LED 1	LED1	O12	Link activity LED Indication. This pin is driven active when a valid link is detected and blinks when activity is detected. **Note:** Refer to Section 3.8.1, "LEDs," on page 32 for additional LED information.
1	Regulator Off Configuration Strap	REGOFF	IS (PD)	This configuration strap is used to disable the internal 1.2V regulator. When the regulator is disabled, external 1.2V must be supplied to VDDCR. • When REGOFF is pulled high to VDD2A with an external resistor, the internal regulator is disabled. • When REGOFF is floating or pulled low, the internal regulator is enabled (default). See Note 2-4 for more information on configuration straps. **Note:** Refer to Section 3.7.4, "REGOFF: Internal +1.2V Regulator Configuration," on page 32 for additional details.

TABLE 2-2: LED PINS (CONTINUED)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	LED 2	LED2	O12	Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation. **Note:** Refer to Section 3.8.1, "LEDs," on page 32 for additional LED information.
1	nINT/ REFCLKO Function Select Configuration Strap	nINTSEL	IS (PU)	This configuration strap selects the mode of the nINT/REFCLKO pin. • When nINTSEL is floated or pulled to VDD2A, nINT is selected for operation on the nINT/REFCLKO pin (default). • When nINTSEL is pulled low to VSS, REFCLKO is selected for operation on the nINT/REFCLKO pin. See Note 2-4 for more information on configuration straps. **Note:** Refer to See Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 33 for additional information.

Note 2-4 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 29 for additional information.

TABLE 2-3: SERIAL MANAGEMENT INTERFACE (SMI) PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	SMI Data Input/Output	MDIO	VIS/ VOD8	Serial Management Interface data input/output
1	SMI Clock	MDC	VIS	Serial Management Interface clock

TABLE 2-4: ETHERNET PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/ RX Positive Channel 1	TXP	AIO	Transmit/Receive Positive Channel 1
1	Ethernet TX/ RX Negative Channel 1	TXN	AIO	Transmit/Receive Negative Channel 1

TABLE 2-4: ETHERNET PINS (CONTINUED)

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/ RX Positive Channel 2	RXP	AIO	Transmit/Receive Positive Channel 2
1	Ethernet TX/ RX Negative Channel 2	RXN	AIO	Transmit/Receive Negative Channel 2

TABLE 2-5: MISCELLANEOUS PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External Crystal Input	XTAL1	ICLK	External crystal input
	External Clock Input	CLKIN	ICLK	Single-ended clock oscillator input. **Note:** When using a single ended clock oscillator, XTAL2 should be left unconnected.
1	External Crystal Output	XTAL2	OCLK	External crystal output
1	External Reset	nRST	VIS (PU)	System reset. This signal is active low.
1	Interrupt Output	nINT	VOD8 (PU)	Active low interrupt output. Place an external resistor pull-up to VDDIO. **Note:** Refer to Section 3.6, "Interrupt Management," on page 24 for additional details on device interrupts. **Note:** Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 32 for details on how the nINTSEL configuration strap is used to determine the function of this pin.
	Reference Clock Output	REFCLKO	VO8	This optional 50MHz clock output is derived from the 25MHz crystal oscillator. REFCLKO is selectable via the nINTSEL configuration strap. **Note:** Refer Section 3.7.4.2, "REF_CLK Out Mode," on page 29 for additional details. **Note:** Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 32 for details on how the nINTSEL configuration strap is used to determine the function of this pin.

TABLE 2-6: ANALOG REFERENCE PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External 1% Bias Resistor Input	RBIAS	AI	This pin requires connection of a 12.1k ohm (1%) resistor to ground. Refer to the LAN8720A/LAN8720Ai reference schematic for connection information. **Note:** The nominal voltage is 1.2V and the resistor will dissipate approximately 1mW of power.

TABLE 2-7: POWER PINS

Num PINs	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+1.6V to +3.6V Variable I/O Power	VDDIO	P	+1.6V to +3.6V variable I/O power Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.
1	+1.2V Digital Core Power Supply	VDDCR	P	Supplied by the on-chip regulator unless configured for regulator off mode via the REGOFF configuration strap. Refer to the LAN8720A/LAN8720Ai reference schematic for connection information. **Note:** 1 uF and 470 pF decoupling capacitors in parallel to ground should be used on this pin.
1	+3.3V Channel 1 Analog Port Power	VDD1A	P	+3.3V Analog Port Power to Channel 1 Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.
1	+3.3V Channel 2 Analog Port Power	VDD2A	P	+3.3V Analog Port Power to Channel 2 and the internal regulator. Refer to the LAN8720A/LAN8720Ai reference schematic for connection information.
1	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

2.1 Pin Assignments

TABLE 2-8: 24-QFN PACKAGE PIN ASSIGNMENTS

Pin NUM	Pin Name	Pin NUM	Pin Name
1	VDD2A	13	MDC
2	LED2/nINTSEL	14	nINT/REFCLKO
3	LED1/REGOFF	15	nRST
4	XTAL2	16	TXEN
5	XTAL1/CLKIN	17	TXD0
6	VDDCR	18	TXD1
7	RXD1/MODE1	19	VDD1A
8	RXD0/MODE0	20	TXN
9	VDDIO	21	TXP
10	RXER/PHYAD0	22	RXN
11	CRS_DV/MODE2	23	RXP
12	MDIO	24	RBIAS

2.2 Buffer Types

TABLE 2-9: BUFFER TYPES

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
O12	Output with 12mA sink and 12mA source
VIS	Variable voltage Schmitt-triggered input
VO8	Variable voltage output with 8mA sink and 8mA source
VOD8	Variable voltage open-drain output with 8mA sink
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin

TABLE 2-9: BUFFER TYPES (CONTINUED)

BUFFER TYPE	DESCRIPTION
OCLK	Crystal oscillator output pin
P	Power pin

Note 2-5 The digital signals are not 5V tolerant. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 54 for additional buffer information.

Note 2-6 Sink and source capabilities are dependent on the VDDIO voltage. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 54 for additional information.

3.0 FUNCTIONAL DESCRIPTION

This chapter provides functional descriptions of the various device features. These features have been categorized into the following sections:

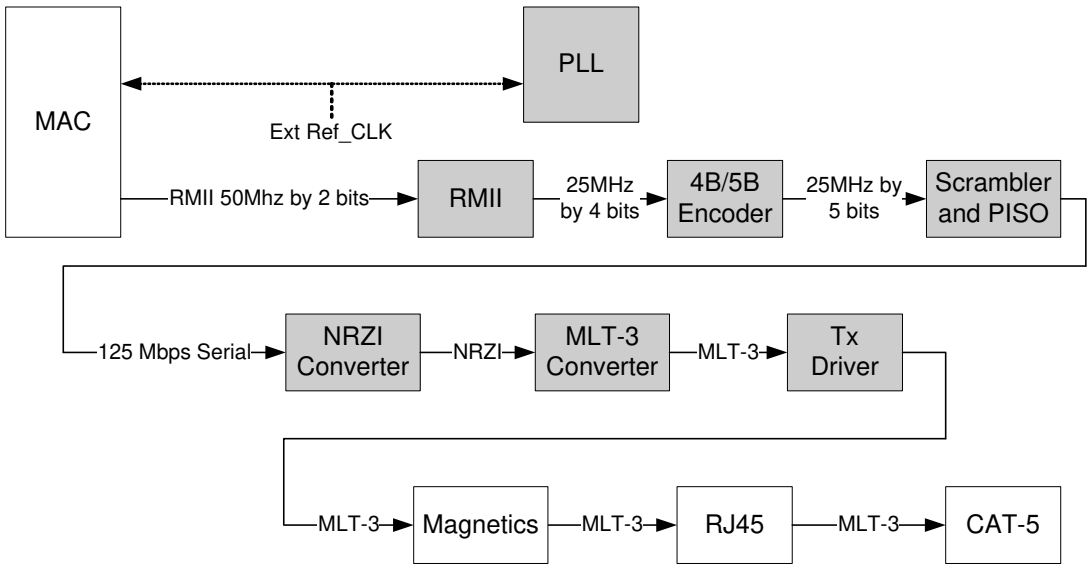
- Transceiver
- Auto-negotiation
- HP Auto-MDIX Support
- MAC Interface
- Serial Management Interface (SMI)
- Interrupt Management
- Configuration Straps
- Miscellaneous Functions
- Application Diagrams

3.1 Transceiver

3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit data path is shown in Figure 3-1. Each major block is explained in the following subsections.

FIGURE 3-1: 100BASE-TX TRANSMIT DATA PATH



3.1.1.1 100BASE-TX Transmit Data Across the RMII Interface

The MAC controller drives the transmit data onto the TXD bus and asserts TXEN to indicate valid data. The data is latched by the transceiver's RMII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50MHz data.

3.1.1.2 4B/5B Encoding

The transmit data passes from the RMII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to Table 3-1. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

TABLE 3-1: 4B/5B CODE TABLE

CODE GROUP	SYM	RECEIVER INTERPRETATION			TRANSMITTER INTERPRETATION		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001	—	1	0001	—
10100	2	2	0010	—	2	0010	—
10101	3	3	0011	—	3	0011	—
01010	4	4	0100	—	4	0100	—
01011	5	5	0101	—	5	0101	—
01110	6	6	0110	—	6	0110	—
01111	7	7	0111	—	7	0111	—
10010	8	8	1000	—	8	1000	—
10011	9	9	1001	—	9	1001	—
10110	A	A	1010	—	A	1010	—
10111	B	B	1011	—	B	1011	—
11010	C	C	1100	—	C	1100	—
11011	D	D	1101	—	D	1101	—
11100	E	E	1110	—	E	1110	—
11101	F	F	1111	—	F	1111	—
11111	I	IDLE			Sent after /T/R until TXEN		
11000	J	First nibble of SSD, translated to “0101” following IDLE, else RXER			Sent for rising TXEN		
10001	K	Second nibble of SSD, translated to “0101” following J, else RXER			Sent for rising TXEN		
01101	T	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RXER			Sent for falling TXEN		
00111	R	Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RXER			Sent for falling TXEN		
00100	H	Transmit Error Symbol			Sent for rising TXER		
00110	V	INVALID, RXER if during RXDV			INVALID		
11001	V	INVALID, RXER if during RXDV			INVALID		
00000	V	INVALID, RXER if during RXDV			INVALID		
00001	V	INVALID, RXER if during RXDV			INVALID		
00010	V	INVALID, RXER if during RXDV			INVALID		
00011	V	INVALID, RXER if during RXDV			INVALID		

TABLE 3-1: 4B/5B CODE TABLE (CONTINUED)

CODE GROUP	SYM	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
00101	V	INVALID, RXER if during RXDV	INVALID
01000	V	INVALID, RXER if during RXDV	INVALID
01100	V	INVALID, RXER if during RXDV	INVALID
10000	V	INVALID, RXER if during RXDV	INVALID

3.1.1.3 Scrambling

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the transceiver address, PHYAD, ensuring that in multiple-transceiver applications, such as repeaters or switches, each transceiver will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

3.1.1.4 NRZI and MLT-3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

3.1.1.5 100M Transmit Driver

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10BASE-T and 100BASE-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

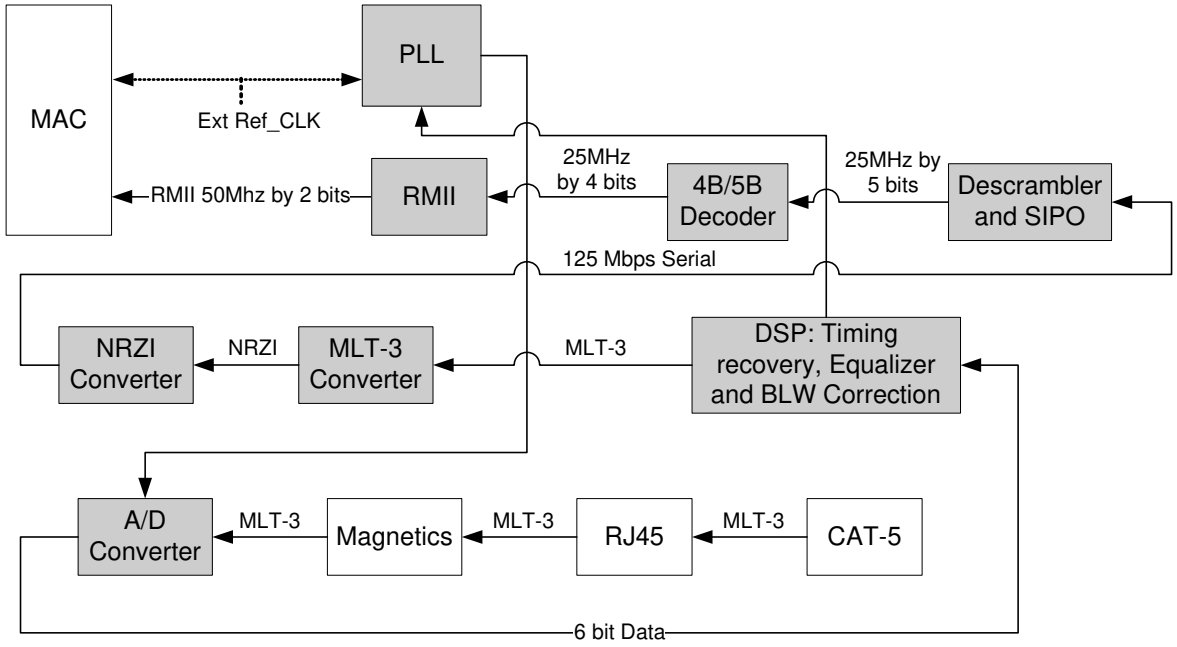
3.1.1.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100BASE-TX transmitter.

3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receive data path is shown in Figure 3-2. Each major block is explained in the following subsections.

FIGURE 3-2: 100BASE-TX RECEIVE DATA PATH



3.1.2.1 100M Receive Input

The MLT-3 from the cable is fed into the transceiver (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quanitizer, it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

3.1.2.2 Equalizer, Baseline Wander Correction and Clock and Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT- 5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the transceiver corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

3.1.2.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

3.1.2.4 Descrambling

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote transceiver by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

3.1.2.5 Alignment

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

3.1.2.6 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[1:0] signal lines. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the transceiver to assert the receive data valid signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the transceiver to de-assert the carrier sense and receive data valid signals.

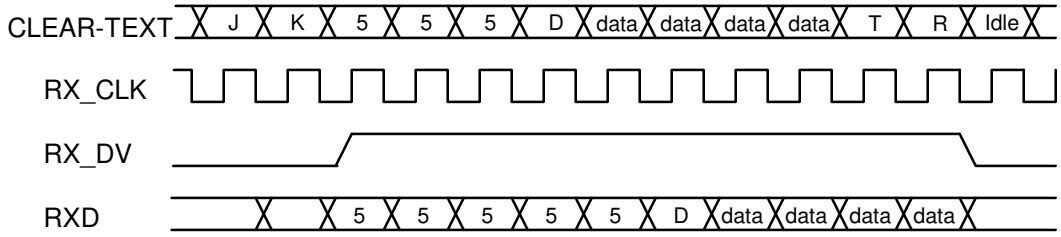
Note: These symbols are not translated into data.

3.1.2.7 Receive Data Valid Signal

The Receive Data Valid signal (RXDV) indicates that recovered and decoded nibbles are being presented on the RXD[1:0] outputs synchronous to RXCLK. RXDV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RXDV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII mode).

FIGURE 3-3: RELATIONSHIP BETWEEN RECEIVED DATA AND SPECIFIC MII SIGNALS



3.1.2.8 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RXER signal is asserted and arbitrary data is driven onto the RXD[1:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RXER is asserted true and the value ‘1110’ is driven onto the RXD[1:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

3.1.2.9 100M Receive Data Across the RMII Interface

The 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50MHz. The controller samples the data on the rising edge of XTAL1/CLKIN (REF_CLK). To ensure that the setup and hold requirements are met, the nibbles are clocked out of the transceiver on the falling edge of XTAL1/CLKIN (REF_CLK).

3.1.3 10BASE-T TRANSMIT

Data to be transmitted comes from the MAC layer controller. The 10BASE-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

3.1.3.1 10M Transmit Data Across the RMII Interface

The MAC controller drives the transmit data onto the TXD bus. TXD[1:0] shall transition synchronously with respect to REF_CLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the device. TXD[1:0] shall be “00” to indicate idle when TXEN is deasserted. Values of TXD[1:0] other than “00” when TXEN is deasserted are reserved for out-of-band signaling (to be defined). Values other than “00” on TXD[1:0] while TXEN is deasserted shall be ignored by the device.TXD[1:0] shall provide valid data for each REF_CLK period while TXEN is asserted.

In order to comply with legacy 10BASE-T MAC/Controllers, in half-duplex mode the transceiver loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The transceiver also supports the SQE (Heartbeat) signal.

3.1.3.2 Manchester Encoding

The 4-bit wide data is sent to the 10M TX block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TXEN is low), the 10M TX block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

3.1.3.3 10M Transmit Drivers

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

3.1.4 10BASE-T RECEIVE

The 10BASE-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller via MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

3.1.4.1 10M Receive Input and Squelch

The Manchester signal from the cable is fed into the transceiver (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

3.1.4.2 Manchester Decoding

The output of the SQUELCH goes to the 10M RX block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), the condition is identified and corrected. The reversed condition is indicated by the XPOL bit of the Special Control/Status Indications Register. The 10M PLL is locked onto the received Manchester signal, from which the 20MHz cock is generated. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The 10M RX block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

3.1.4.3 10M Receive Data Across the RMII Interface

The 2-bit data nibbles are sent to the RMII block. These data nibbles are valid on the rising edge of the RMII REF_CLK.

3.1.4.4 Jabber Detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, which results in holding the TXEN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line within 45ms. Once TXEN is deasserted, the logic resets the jabber condition.

As shown in Section 4.2.2, "Basic Status Register," on page 45, the Jabber Detect bit indicates that a jabber condition was detected.

3.2 Auto-negotiation

The purpose of the auto-negotiation function is to automatically configure the transceiver to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits of the PHY Special Control/Status Register, as well as in the Auto Negotiation Link Partner Ability Register. The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The advertised capabilities of the transceiver are stored in the Auto Negotiation Advertisement Register. The default advertised by the transceiver is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting the Restart Auto-Negotiate bit of the Basic Control Register

On detection of one of these events, the transceiver begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP), which are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the transceiver advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in the Auto Negotiation Advertisement Register.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest Priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex (Lowest Priority)

If the full capabilities of the transceiver are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of half and full duplex modes, then auto-negotiation selects full duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the transceiver are initially determined by the logic levels latched on the MODE[2:0] configuration straps after reset completes. These configuration straps can also be used to disable auto-negotiation on power-up. Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 30 for additional information.

Writing the bits 8 through 5 of the Auto Negotiation Advertisement Register allows software control of the capabilities advertised by the transceiver. Writing the Auto Negotiation Advertisement Register does not automatically re-start auto-negotiation. The Restart Auto-Negotiate bit of the Basic Control Register must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing the Auto-Negotiation Enable bit of the Basic Control Register.

Note: The device does not support “Next Page” capability.

3.2.1 PARALLEL DETECTION

If the LAN8720A/LAN8720Ai is connected to a device lacking the ability to auto-negotiate (for example, no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be half duplex per the IEEE standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then the Link Partner Auto-Negotiation Able bit of the Auto Negotiation Expansion Register is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, the Parallel Detection Fault bit of Link Partner Auto-Negotiation Able is set.

Auto Negotiation Link Partner Ability Register is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then the Auto Negotiation Link Partner Ability Register is updated after completion of parallel detection to reflect the speed capability of the link partner.

3.2.2 RESTARTING AUTO-NEGOTIATION

Auto-negotiation can be restarted at any time by setting the Restart Auto-Negotiate bit of the Basic Control Register. Auto-negotiation will also restart if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the link partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts auto-negotiation by setting the Restart Auto-Negotiate bit of the Basic Control Register, the LAN8720A/LAN8720Ai will respond by stopping all transmission/receiving operations. Once the break_link_timer is completed in the Auto-negotiation state-machine (approximately 1200ms), auto-negotiation will re-start. In this case, the link partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

3.2.3 DISABLING AUTO-NEGOTIATION

Auto-negotiation can be disabled by setting the Auto-Negotiation Enable bit of the Basic Control Register to zero. The device will then force its speed of operation to reflect the information in the Basic Control Register (Speed Select bit and Duplex Mode bit). These bits should be ignored when auto-negotiation is enabled.

3.2.4 HALF VS. FULL DUPLEX

Half duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. If data is received while the transceiver is transmitting, a collision results.

In full duplex mode, the transceiver is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

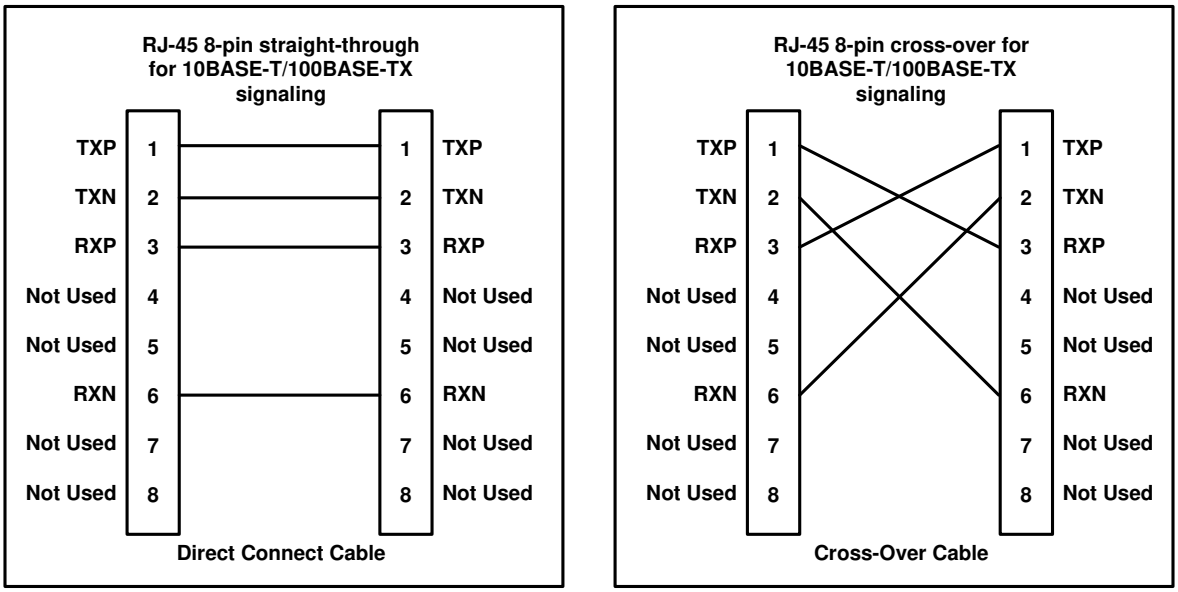
3.3 HP Auto-MDIX Support

HP Auto-MDIX facilitates the use of CAT-3 (10BASE-T) or CAT-5 (100BASE-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a cross-over patch cable, as shown in Figure 3-4, the device’s Auto-MDIX transceiver is capable of configuring the TXP/TXN and RXP/RXN pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled via the AMDIXCTRL bit in the Special Control/Status Indications Register.

FIGURE 3-4: DIRECT CABLE CONNECTION VS. CROSS-OVER CABLE CONNECTION



3.4 MAC Interface

3.4.1 RMII

The device supports the low pin count Reduced Media Independent Interface (RMII) intended for use between Ethernet transceivers and switch ASICs. Under IEEE 802.3, an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or transceiver interfaces such as switches, the number of pins can add significant cost as the port counts increase. RMII reduces this pin count while retaining a management interface (MDIO/MDC) that is identical to MII.

The RMII interface has the following characteristics:

- It is capable of supporting 10Mbps and 100Mbps data rates
- A single clock reference is used for both transmit and receive
- It provides independent 2-bit (di-bit) wide transmit and receive data paths
- It uses LVCMOS signal levels, compatible with common digital CMOS ASIC processes

The RMII includes the following interface signals (1 optional):

- transmit data - TXD[1:0]
- transmit strobe - TXEN
- receive data - RXD[1:0]
- receive error - RXER (Optional)
- carrier sense - CRS_DV
- Reference Clock - (RMII references usually define this signal as REF_CLK)

3.4.1.1 CRS_DV - Carrier Sense/Receive Data Valid

The CRS_DV is asserted by the device when the receive medium is non-idle. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. In 10BASE-T mode when squelch is passed, or in 100BASE-X mode when 2 non-contiguous zeros in 10 bits are detected, the carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (for example, CRS_DV is deasserted only on nibble boundaries). If the device has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the device shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and de-assert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is, starting on nibble boundaries, CRS_DV toggles at 25 MHz in 100Mbps mode and 2.5 MHz in 10Mbps mode when CRS ends before RXDV (for example, the FIFO still has bits to transfer when the carrier event ends). Therefore, the MAC can accurately recover RXDV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place.

3.4.1.2 Reference Clock (REF_CLK)

The RMII REF_CLK is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TXEN, TXD[1:0] and RXER. The device uses REF_CLK as the network clock such that no buffering is required on the transmit data path. However, on the receive data path, the receiver recovers the clock from the incoming data stream, and the device uses elasticity buffering to accommodate for differences between the recovered clock and the local REF_CLK.

3.5 Serial Management Interface (SMI)

The Serial Management Interface is used to control the device and obtain its status. This interface supports registers 0 through 6 as required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers 16 to 31 allowed by the specification. Non-supported registers (such as 7 to 15) will be read as hexadecimal “FFFF”. Device registers are detailed in Section 4.0, "Register Descriptions," on page 43.

At the system level, SMI provides 2 signals: MDIO and MDC. The MDC signal is an aperiodic clock provided by the station management controller (SMC). MDIO is a bi-directional data SMI input/output signal that receives serial data (commands) from the controller SMC and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges. The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is 400 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The frame structure and timing of the data is shown in Figure 3-5 and Figure 3-6. The timing relationships of the MDIO signals are further described in Section 5.5.6, "SMI Timing," on page 64.

FIGURE 3-5: MDIO TIMING AND FRAME STRUCTURE - READ CYCLE

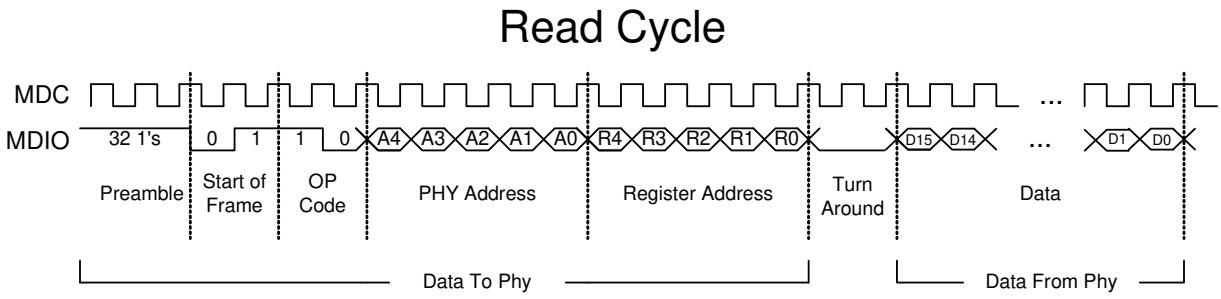
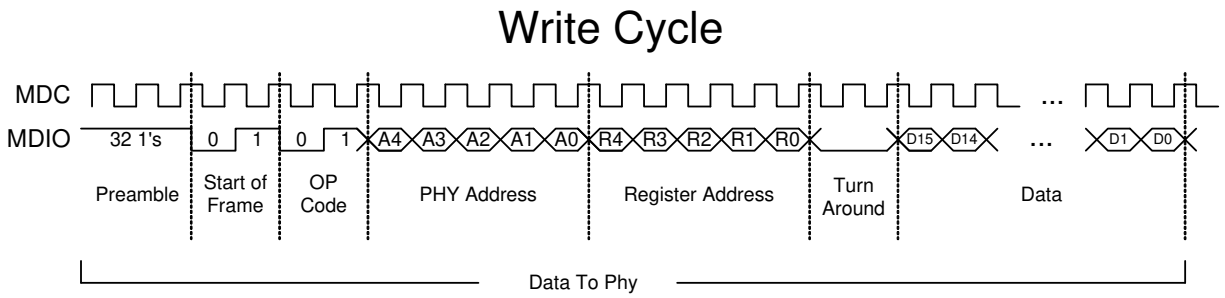


FIGURE 3-6: MDIO TIMING AND FRAME STRUCTURE - WRITE CYCLE



3.6 Interrupt Management

The device management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. This interrupt capability generates an active low asynchronous interrupt signal on the nINT output whenever certain events are detected as setup by the Interrupt Mask Register.

The device's interrupt system provides two modes, a Primary Interrupt mode and an Alternative interrupt mode. Both systems will assert the nINT pin low when the corresponding mask bit is set. These modes differ only in how they de-assert the nINT interrupt output. These modes are detailed in the following subsections.

Note: The Primary interrupt mode is the default interrupt mode after a power-up or hard reset. The Alternative interrupt mode requires setup after a power-up or hard reset.

3.6.1 PRIMARY INTERRUPT SYSTEM

The Primary interrupt system is the default interrupt mode (ALTINT bit of the Mode Control/Status Register is "0"). The Primary interrupt system is always selected after power-up or hard reset. In this mode, to set an interrupt, set the corresponding mask bit in the Interrupt Mask Register (see Table 3-3). Then when the event to assert nINT is true, the nINT output will be asserted. When the corresponding event to deassert nINT is true, then the nINT will be de-asserted.

TABLE 3-2: INTERRUPT MANAGEMENT TABLE

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert nINT	Event to De-Assert nINT
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1 (Note 3-3)	Falling 17.1 or Reading register 29
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	Falling 1.5 or Reading register 29

TABLE 3-2: INTERRUPT MANAGEMENT TABLE

30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	Falling 1.4, or Reading register 1 or Reading register 29
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	Reading register 1 or Reading register 29
30.3	29.3	Auto-Negotiation LP Acknowledge	5.14	Acknowledge	Rising 5.14	Falling 5.14 or Read register 29
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	Falling 6.4 or Reading register 6, or Reading register 29 or Re-Auto Negotiate or Link down
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	Falling of 6.1 or Reading register 6, or Reading register 29 Re-Auto Negotiate, or Link Down.

Note 3-1 If the mask bit is enabled and nINT has been de-asserted while ENERGYON is still high, nINT will assert for 256 ms, approximately one second after ENERGYON goes low when the Cable is unplugged. To prevent an unexpected assertion of nINT, the ENERGYON interrupt mask should always be cleared as part of the ENERGYON interrupt service routine.

Note: The ENERGYON bit in the Mode Control/Status Register is defaulted to a ‘1’ at the start of the signal acquisition process, therefore the INT7 bit in the Interrupt Mask Register will also read as a ‘1’ at power-up. If no signal is present, then both ENERGYON and INT7 will clear within a few milliseconds.

3.6.2 ALTERNATE INTERRUPT SYSTEM

The Alternate interrupt system is enabled by setting the ALTINT bit of the Mode Control/Status Register to “1”. In this mode, to set an interrupt, set the corresponding bit of the in the Mask Register 30, (see Table 3-4). To Clear an interrupt, either clear the corresponding bit in the Interrupt Mask Register to deassert the nINT output, or clear the interrupt source, and write a ‘1’ to the corresponding Interrupt Source Flag. Writing a ‘1’ to the Interrupt Source Flag will cause the state machine to check the Interrupt Source to determine if the Interrupt Source Flag should clear or stay as a ‘1’. If the Condition to deassert is true, then the Interrupt Source Flag is cleared and nINT is also deasserted. If the Condition to deassert is false, then the Interrupt Source Flag remains set, and the nINT remains asserted.