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# LAN8742A/LAN8742Ai

# Small Footprint RMII 10/100 Ethernet Transceiver with HP Auto-MDIX and flexPWR® Technology

## PRODUCT FEATURES

**Datasheet**

### Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Cable diagnostic support
- Wake on LAN (WoL) support
- Comprehensive flexPWR® technology
  - Flexible power management architecture
  - LVCMOS Variable I/O voltage range: +1.8 V to +3.3 V
  - Integrated 1.2 V regulator with disable feature
- HP Auto-MDIX support
- Miniature 24-pin SQFN, RoHS-compliant package (4 x 4 x 0.9 mm height)

### Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- Gaming Consoles
- POE Applications (Refer to SMSC Application Note 17.18)

### Key Benefits

- High-performance 10/100 Ethernet transceiver
  - Compliant with IEEE802.3/802.3u (Fast Ethernet)
  - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
  - Loop-back modes
  - Auto-negotiation
  - Automatic polarity detection and correction
  - Link status change wake-up detection
  - Vendor specific register functions
  - Supports the reduced pin count RMII interface
- Power and I/Os
  - Various low power modes
  - Integrated power-on reset circuit
  - Two status LED outputs
  - May be used with a single 3.3 V supply
- Additional Features
  - Ability to use a low cost 25 MHz crystal for reduced BOM
- Packaging
  - 24-pin SQFN (4 x 4 mm), RoHS-compliant package with RMII
- Environmental
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

## ORDER NUMBER(S):

**LAN8742A-CZ (Tray) for 24-pin, SQFN, RoHS-compliant package (0°C to +70°C temp)**

**LAN8742Ai-CZ (Tray) for 24-pin, SQFN, RoHS-compliant package (-40°C to +85°C temp)**

**LAN8742A-CZ-TR (Tape & Reel) for 24-pin, SQFN, RoHS-compliant package (0°C to +70°C temp)**

**LAN8742Ai-CZ-TR (Tape & Reel) for 24-pin, SQFN, RoHS-compliant package (-40 to +85°C temp)**

**This product meets the halogen maximum concentration values per IEC61249-2-21.**

**For RoHS compliance and environmental information, please visit www.smsc.com/rohs.**

*Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.*

# Table of Contents

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# Chapter 1 Introduction

## 1.1 General Terms and Conventions

The following is a list of the general terms used throughout this document:

| | |
|---|---|
| **BYTE** | 8 bits |
| **FIFO** | **F**irst **I**n **F**irst **O**ut buffer; often used for elasticity buffer |
| **MAC** | **M**edia **A**ccess **C**ontroller |
| **RMII™** | **R**educed **M**edia **I**ndependent **I**nterface |
| **N/A** | Not Applicable |
| **X** | Indicates that a logic state is “don’t care” or undefined. |
| **RESERVED** | Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses. |
| **SMI** | **S**erial **M**anagement **I**nterface |

## 1.2 General Description

The LAN8742A/LAN8742Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3 and 802.3u standards.

The LAN8742A/LAN8742Ai supports communication with an Ethernet MAC via a standard RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) operation. The LAN8742A/LAN8742Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables. Integrated Wake on LAN (WoL) support provides a mechanism to trigger an interrupt upon reception of a perfect DA, broadcast, magic packet, or wakeup frame.

The LAN8742A/LAN8742Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in Section 3.7, "Configuration Straps," on page 35. Register-selectable configuration options may be used to further define the functionality of the transceiver.

The LAN8742A/LAN8742Ai can be programmed to support wake-on-LAN at the physical layer, allowing detection of configurable Wake-up Frame and Magic packets. This feature allows filtering of packets at the PHY layer, without requiring MAC intervention. Additionally, the LAN8742A/LAN8742Ai supports cable diagnostics which allow the device to identify opens/shorts and their location on the cable via vendor-specific registers.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6 V. The device can be configured to operate on a single 3.3 V supply utilizing an integrated 3.3 V to 1.2 V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8742A/LAN8742Ai is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions. A typical system application is shown in Figure 1.1. Figure 1.2 provides an internal block diagram of the device.

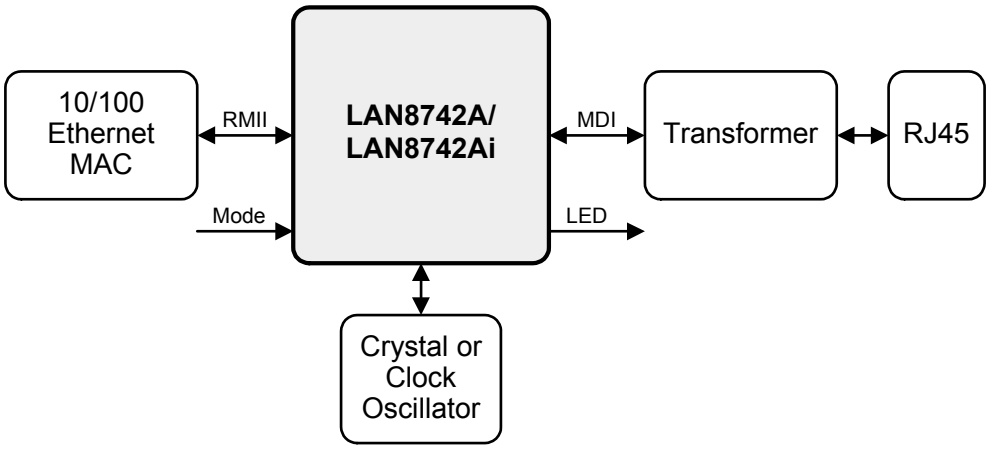



**Figure 1.1 System Block Diagram**

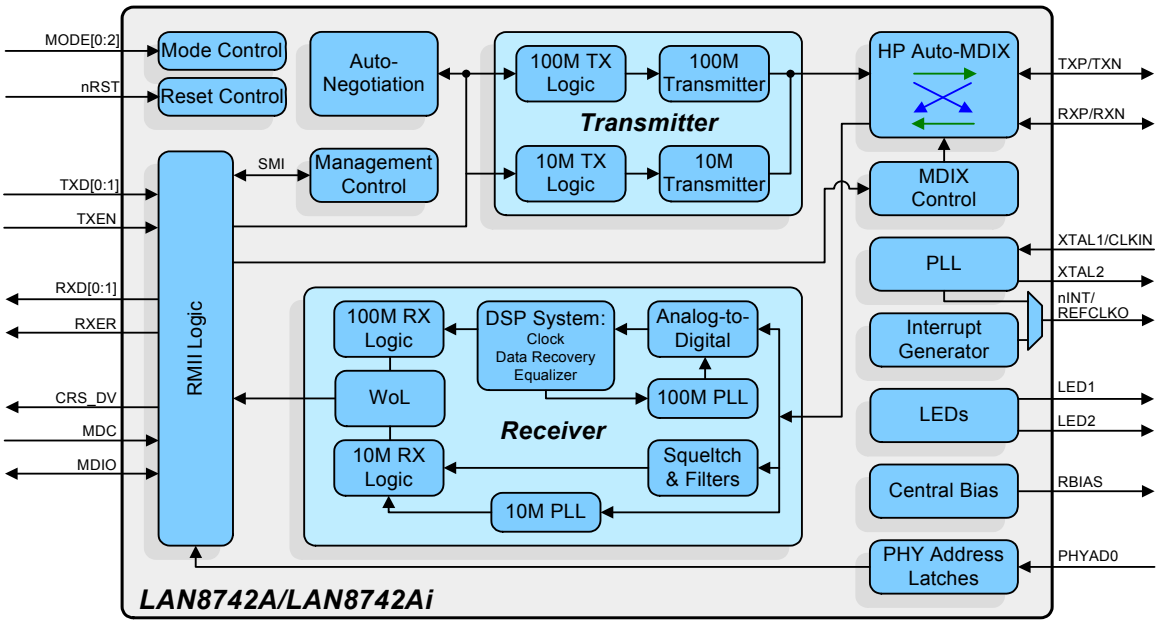
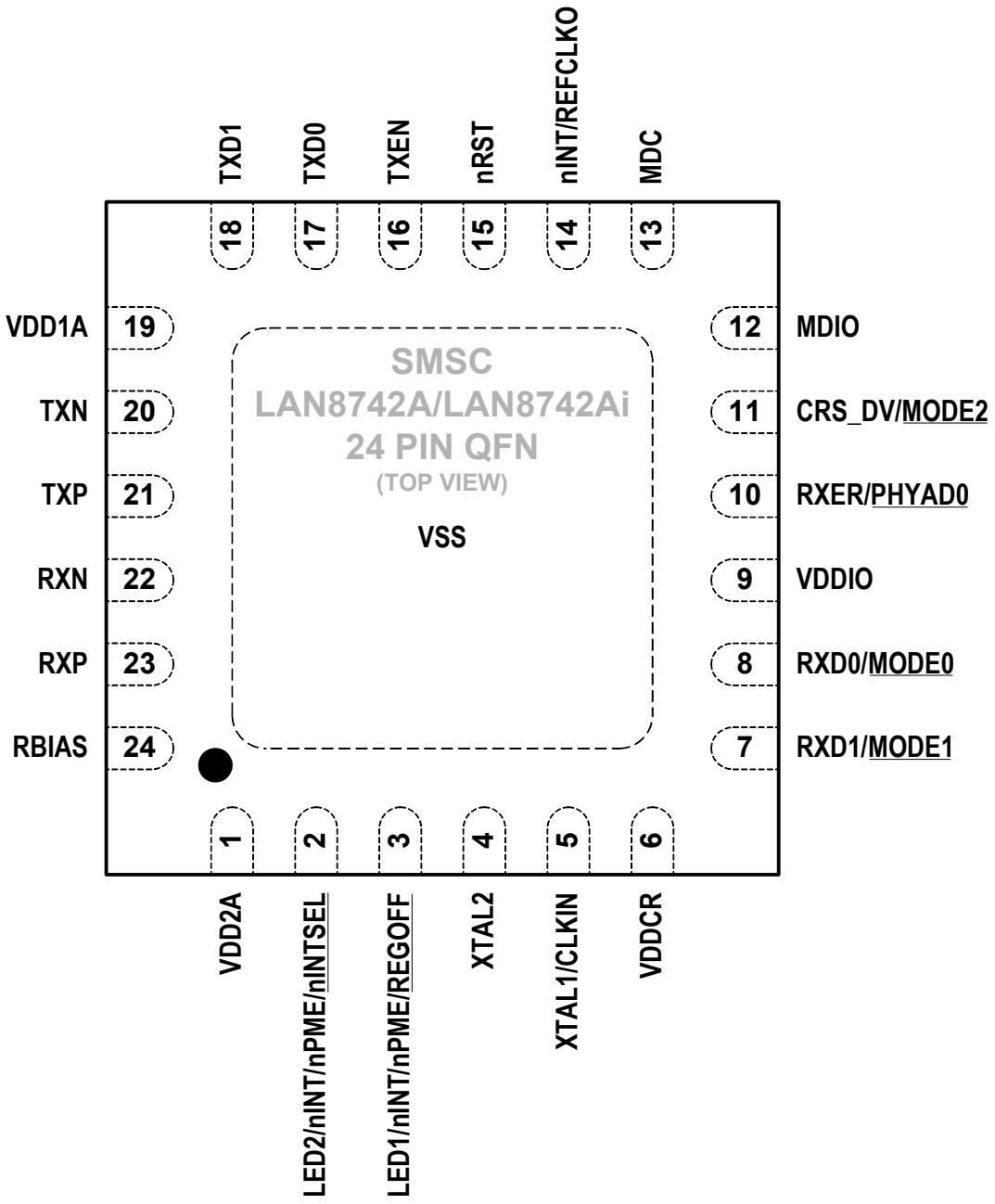



**Figure 1.2 Architectural Overview**

# Chapter 2 Pin Description and Configuration




**NOTE:** Exposed pad (VSS) on bottom of package must be connected to ground

**Figure 2.1 24-SQFN Pin Assignments (TOP VIEW)**

**Note:** When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

**Note:** The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in Section 2.2.

**Table 2.1 RMII Signals**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Transmit Data 0 | TXD0 | VIS | The MAC transmits data to the transceiver using this signal. |
| 1 | Transmit Data 1 | TXD1 | VIS | The MAC transmits data to the transceiver using this signal. |
| 1 | Transmit Enable | TXEN | VIS (PD) | Indicates that valid transmission data is present on TXD[1:0]. |
| 1 | Receive Data 0 | RXD0 | VO8 | Bit 0 of the 2 data bits that are sent by the transceiver on the receive path. |
| | PHY Operating Mode 0 Configuration Strap | MODE0 | VIS (PU) | Combined with MODE1 and MODE2, this configuration strap sets the default PHY mode.<br>See Note 2.1 for more information on configuration straps.<br>**Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details. |
| 1 | Receive Data 1 | RXD1 | VO8 | Bit 1 of the 2 data bits that are sent by the transceiver on the receive path. |
| | PHY Operating Mode 1 Configuration Strap | MODE1 | VIS (PU) | Combined with MODE0 and MODE2, this configuration strap sets the default PHY mode.<br>See Note 2.1 for more information on configuration straps.<br>**Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details. |
| 1 | Receive Error | RXER | VO8 | This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver. |
| | PHY Address 0 Configuration Strap | PHYAD0 | VIS (PD) | This configuration strap sets the transceiver's SMI address.<br>See Note 2.1 for more information on configuration straps.<br>**Note:** Refer to Section 3.7.1, "PHYAD[0]: PHY Address Configuration," on page 35 for additional information. |

**Table 2.1 RMII Signals (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Carrier Sense / Receive Data Valid | CRS_DV | VO8 | This signal is asserted to indicate the receive medium is non-idle. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received.<br>**Note:** Per the RMII standard, transmitted data is not looped back onto the receive data pins in 10BASE-T half-duplex mode. |
| | PHY Operating Mode 2 Configuration Strap | MODE2 | VIS (PU) | Combined with MODE0 and MODE1, this configuration strap sets the default PHY mode.<br>See Note 2.1 for more information on configuration straps.<br>**Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details. |

**Note 2.1** Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 35 for additional information.

**Table 2.2 LED Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | LED 1 | LED1 | O12 | This pin can be used to indicate link activity, link speed, nINT, or nPME as configured via the LED1 Function Select field of the Wakeup Control and Status Register (WUCSR).<br>**Note:** Refer to Section 3.8.1, "LEDs," on page 42 and Section 3.8.4, "Wake on LAN (WoL)," on page 47 for additional LED information. |
| | Interrupt Output | nINT | O12 | Active low interrupt output.<br>**Note:** By default, the nINT signal is output on the nINT/REFCLKO pin. The nINT signal can be optionally configured to output on the LED1 or LED2 pins. Refer to Section 3.6, "Interrupt Management," on page 32 for additional details on device interrupts. |
| | Power Management Event Output | nPME | O12 | Active low Power Management Event (PME) output.<br>**Note:** The nPME signal can be optionally configured to output on the LED1 or LED2 pins. Refer to Section 3.8.4, "Wake on LAN (WoL)," on page 47 for additional nPME and WoL information. |
| | Regulator Off Configuration Strap | REGOFF | IS (PD) | This configuration strap is used to disable the internal 1.2 V regulator. When the regulator is disabled, external 1.2 V must be supplied to VDDCR.<br>▪ When REGOFF is pulled high to VDD2A with an external resistor, the internal regulator is disabled.<br>▪ When REGOFF is floating or pulled low, the internal regulator is enabled (default).<br>See Note 2.2 for more information on configuration straps.<br>**Note:** Refer to Section 3.7.3, "REGOFF: Internal +1.2 V Regulator Configuration," on page 37 for additional details. |

**Table 2.2 LED Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | LED 2 | LED2 | O12 | This pin can be used to indicate link activity, link speed, nINT, or nPME as configured via the LED2 Function Select field of the Wakeup Control and Status Register (WUCSR).<br>**Note:** Refer to Section 3.8.1, "LEDs," on page 42 and Section 3.8.4, "Wake on LAN (WoL)," on page 47 for additional LED information. |
| | Interrupt Output | nINT | O12 | Active low interrupt output.<br>**Note:** By default, the nINT signal is output on the nINT/REFCLKO pin. The nINT signal can be optionally configured to output on the LED1 or LED2 pins. Refer to Section 3.6, "Interrupt Management," on page 32 for additional details on device interrupts. |
| | Power Management Event Output | nPME | O12 | Active low Power Management Event (PME) output.<br>**Note:** The nPME signal can be optionally configured to output on the LED1 or LED2 pins. Refer to Section 3.8.4, "Wake on LAN (WoL)," on page 47 for additional nPME and WoL information. |
| | nINT/ REFCLKO Function Select Configuration Strap | nINTSEL | IS (PU) | This configuration strap selects the mode of the nINT/REFCLKO pin.<br>▪ When nINTSEL is floated or pulled to VDD2A, nINT is selected for operation on the nINT/REFCLKO pin (default).<br>▪ When nINTSEL is pulled low to VSS, REFCLKO is selected for operation on the nINT/REFCLKO pin.<br>See Note 2.2 for more information on configuration straps.<br>**Note:** Refer to See Section 3.8.1.6, "nINTSEL and LED2 Polarity Selection," on page 46 for additional information. |

**Note 2.2** Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 35 for additional information.

**Table 2.3 Serial Management Interface (SMI) Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | SMI Data Input/Output | MDIO | VIS/ VO8 (PU) | Serial Management Interface data input/output |
| 1 | SMI Clock | MDC | VIS | Serial Management Interface clock |

**Table 2.4 Ethernet Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Ethernet TX/RX Positive Channel 1 | TXP | AIO | Transmit/Receive Positive Channel 1 |
| 1 | Ethernet TX/RX Negative Channel 1 | TXN | AIO | Transmit/Receive Negative Channel 1 |
| 1 | Ethernet TX/RX Positive Channel 2 | RXP | AIO | Transmit/Receive Positive Channel 2 |
| 1 | Ethernet TX/RX Negative Channel 2 | RXN | AIO | Transmit/Receive Negative Channel 2 |

**Table 2.5 Miscellaneous Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | External Crystal Input | XTAL1 | ICLK | External crystal input |
| | External Clock Input | CLKIN | ICLK | Single-ended clock oscillator input.<br>**Note:** When using a single ended clock oscillator, XTAL2 should be left unconnected. |
| 1 | External Crystal Output | XTAL2 | OCLK | External crystal output |
| 1 | External Reset | nRST | VIS (PU) | System reset. This signal is active low. |

**Table 2.5 Miscellaneous Pins (continued)**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Interrupt Output | nINT | VOD8 (PU) | Active low interrupt output. Place an external resistor pull-up to VDDIO.<br>**Note:** The nINT signal can be optionally configured to output on the LED1 or LED2 pins. Refer to Section 3.6, "Interrupt Management," on page 32 for additional details on device interrupts.<br>**Note:** Refer to Section 3.8.1.6, "nINTSEL and LED2 Polarity Selection," on page 46 for details on how the nINTSEL configuration strap is used to determine the function of this pin. |
| | Reference Clock Output | REFCLKO | VO8 | This optional 50 MHz clock output is derived from the 25 MHz crystal oscillator. REFCLKO is selectable via the nINTSEL configuration strap.<br>**Note:** Refer to Section 3.7.4.2, "REF_CLK Out Mode," on page 39 for additional details on device interrupts.<br>**Note:** Refer to Section 3.8.1.6, "nINTSEL and LED2 Polarity Selection," on page 46 for details on how the nINTSEL configuration strap is used to determine the function of this pin. |

**Table 2.6 Analog Reference Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | External 1% Bias Resistor Input | RBIAS | AI | This pin requires connection of a 12.1 kΩ (1%) resistor to ground.<br>Refer to the LAN8742A/LAN8742Ai reference schematic for connection information.<br>**Note:** The nominal voltage is 1.2 V and the resistor will dissipate approximately 1 mW of power. |

**Table 2.7 Power Pins**

| NUM PINS | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | +1.8 V to +3.3 V Variable I/O Power | VDDIO | P | +1.8 V to +3.3 V variable I/O power.<br>Refer to the LAN8742A/LAN8742Ai reference schematic for connection information. |
| 1 | +1.2 V Digital Core Power Supply | VDDCR | P | Supplied by the on-chip regulator unless configured for regulator off mode via the REGOFF configuration strap.<br>Refer to the LAN8742A/LAN8742Ai reference schematic for connection information.<br>**Note:** 1 µF and 470 pF decoupling capacitors in parallel to ground should be used on this pin. |
| 1 | +3.3 V Channel 1 Analog Port Power | VDD1A | P | +3.3 V Analog Port Power to Channel 1.<br>Refer to the LAN8742A/LAN8742Ai reference schematic for connection information. |
| 1 | +3.3 V Channel 2 Analog Port Power | VDD2A | P | +3.3 V Analog Port Power to Channel 2 and the internal regulator.<br>Refer to the LAN8742A/LAN8742Ai reference schematic for connection information. |
| 1 | Ground | VSS | P | Common ground. This exposed pad must be connected to the ground plane with a via array. |

## 2.1 Pin Assignments

**Table 2.8 24-SQFN Package Pin Assignments**

| PIN NUM | PIN NAME | PIN NUM | PIN NAME |
|---|---|---|---|
| 1 | VDD2A | 13 | MDC |
| 2 | LED2/nINT/nPME/nINTSEL | 14 | nINT/REFCLKO |
| 3 | LED1/nINT/nPME/REGOFF | 15 | nRST |
| 4 | XTAL2 | 16 | TXEN |
| 5 | XTAL1/CLKIN | 17 | TXD0 |
| 6 | VDDCR | 18 | TXD1 |
| 7 | RXD1/MODE1 | 19 | VDD1A |
| 8 | RXD0/MODE0 | 20 | TXN |
| 9 | VDDIO | 21 | TXP |
| 10 | RXER/PHYAD0 | 22 | RXN |
| 11 | CRS_DV/MODE2 | 23 | RXP |
| 12 | MDIO | 24 | RBIAS |

## 2.2 Buffer Types

**Table 2.9 Buffer Types**

| BUFFER TYPE | DESCRIPTION |
|---|---|
| IS | Schmitt-triggered input |
| O12 | Output with 12 mA sink and 12 mA source |
| VIS | Variable voltage Schmitt-triggered input |
| VO8 | Variable voltage output with 8 mA sink and 8 mA source |
| VOD8 | Variable voltage open-drain output with 8 mA sink |
| PU | 50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled.<br>**Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled.<br>**Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AI | Analog input |
| AIO | Analog bi-directional |
| ICLK | Crystal oscillator input pin |
| OCLK | Crystal oscillator output pin |
| P | Power pin |

**Note:** The digital signals are not 5 V tolerant. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 113 for additional buffer information.

**Note:** Sink and source capabilities are dependant on the VDDIO voltage. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 113 for additional information.

# Chapter 3 Functional Description

This chapter provides functional descriptions of the various device features. These features have been categorized into the following sections:

- Transceiver
- Auto-Negotiation
- HP Auto-MDIX Support
- MAC Interface
- Serial Management Interface (SMI)
- Interrupt Management
- Configuration Straps
- Miscellaneous Functions
- Application Diagrams

## 3.1 Transceiver

### 3.1.1 100BASE-TX Transmit

The 100BASE-TX transmit data path is shown in Figure 3.1. Each major block is explained in the following subsections.

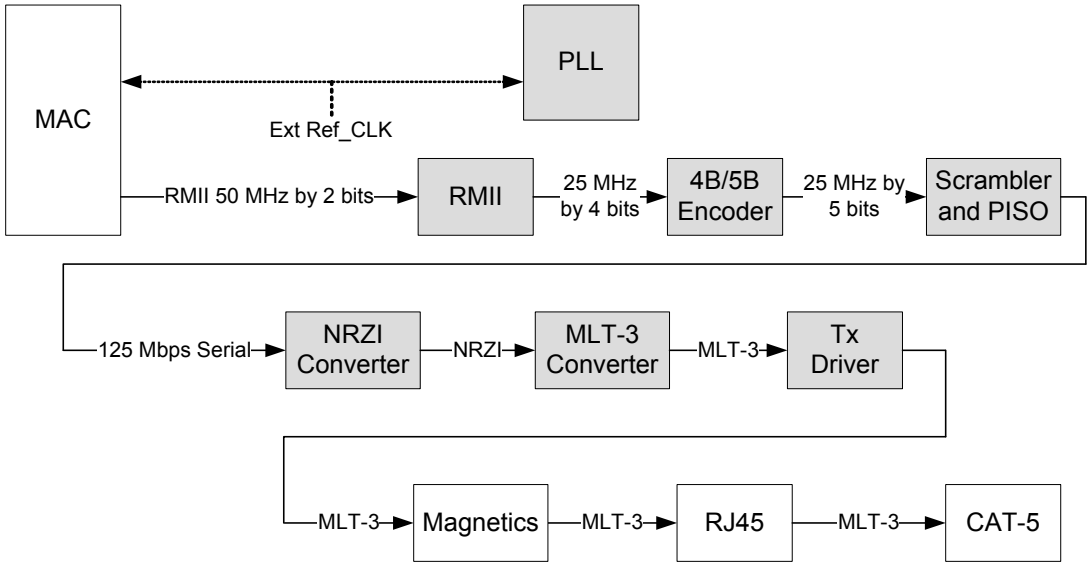



**Figure 3.1 100BASE-TX Transmit Data Path**

#### 3.1.1.1 100BASE-TX Transmit Data Across the RMII Interface

The MAC controller drives the transmit data onto the TXD bus and asserts TXEN to indicate valid data. The data is latched by the transceiver's RMII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50 MHz data.

#### 3.1.1.2 4B/5B Encoding

The transmit data passes from the RMII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to Table 3.1. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

**Table 3.1 4B/5B Code Table**

| CODE GROUP | SYM | RECEIVER INTERPRETATION | | | TRANSMITTER INTERPRETATION | | |
|---|---|---|---|---|---|---|---|
| 11110 | 0 | 0 | 0000 | DATA | 0 | 0000 | DATA |
| 01001 | 1 | 1 | 0001 | | 1 | 0001 | |
| 10100 | 2 | 2 | 0010 | | 2 | 0010 | |
| 10101 | 3 | 3 | 0011 | | 3 | 0011 | |
| 01010 | 4 | 4 | 0100 | | 4 | 0100 | |
| 01011 | 5 | 5 | 0101 | | 5 | 0101 | |
| 01110 | 6 | 6 | 0110 | | 6 | 0110 | |
| 01111 | 7 | 7 | 0111 | | 7 | 0111 | |
| 10010 | 8 | 8 | 1000 | | 8 | 1000 | |
| 10011 | 9 | 9 | 1001 | | 9 | 1001 | |
| 10110 | A | A | 1010 | | A | 1010 | |
| 10111 | B | B | 1011 | | B | 1011 | |
| 11010 | C | C | 1100 | | C | 1100 | |
| 11011 | D | D | 1101 | | D | 1101 | |
| 11100 | E | E | 1110 | | E | 1110 | |
| 11101 | F | F | 1111 | | F | 1111 | |
| 11111 | I | IDLE | | | Sent after /T/R until TXEN | | |
| 11000 | J | First nibble of SSD, translated to "0101" following IDLE, else RXER | | | Sent for rising TXEN | | |
| 10001 | K | Second nibble of SSD, translated to "0101" following J, else RXER | | | Sent for rising TXEN | | |

**Table 3.1 4B/5B Code Table (continued)**

| CODE GROUP | SYM | RECEIVER INTERPRETATION | TRANSMITTER INTERPRETATION |
|---|---|---|---|
| 01101 | T | First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RXER | Sent for falling TXEN |
| 00111 | R | Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RXER | Sent for falling TXEN |
| 00100 | H | Transmit Error Symbol | Sent for rising TXER |
| 00110 | V | INVALID, RXER if during RXDV | INVALID |
| 11001 | V | INVALID, RXER if during RXDV | INVALID |
| 00000 | V | INVALID, RXER if during RXDV | INVALID |
| 00001 | V | INVALID, RXER if during RXDV | INVALID |
| 00010 | V | INVALID, RXER if during RXDV | INVALID |
| 00011 | V | INVALID, RXER if during RXDV | INVALID |
| 00101 | V | INVALID, RXER if during RXDV | INVALID |
| 01000 | V | INVALID, RXER if during RXDV | INVALID |
| 01100 | V | INVALID, RXER if during RXDV | INVALID |
| 10000 | V | INVALID, RXER if during RXDV | INVALID |

#### 3.1.1.3 Scrambling

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the transceiver address, PHYAD, ensuring that in multiple-transceiver applications, such as repeaters or switches, each transceiver will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

#### 3.1.1.4 NRZI and MLT-3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125 MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

#### 3.1.1.5 100M Transmit Driver

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10BASE-T and 100BASE-TX signals pass through the same transformer so that common “magnetics” can be

used for both. The transmitter drives into the 100 Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

#### 3.1.1.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto reference clock and generates the 125 MHz clock used to drive the 125 MHz logic and the 100BASE-TX transmitter.

### 3.1.2 100BASE-TX Receive

The 100BASE-TX receive data path is shown in Figure 3.2. Each major block is explained in the following subsections.

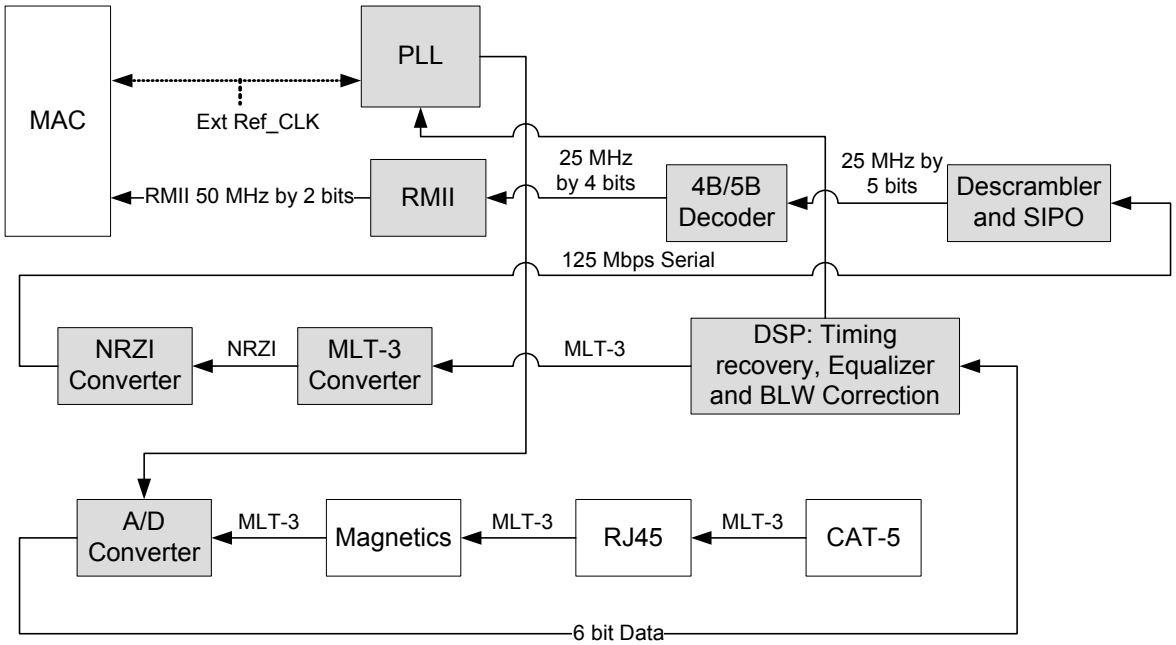



**Figure 3.2 100BASE-TX Receive Data Path**

#### 3.1.2.1 100M Receive Input

The MLT-3 from the cable is fed into the transceiver (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quanitizer, it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

#### 3.1.2.2 Equalizer, Baseline Wander Correction and Clock and Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT- 5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1 m and 100 m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become

significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the transceiver corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125 MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

#### 3.1.2.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

#### 3.1.2.4 Descrambling

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote transceiver by searching for IDLE symbols within a window of 4000 bytes (40 µs). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

#### 3.1.2.5 Alignment

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

#### 3.1.2.6 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[1:0] signal lines. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the transceiver to assert the receive data valid signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the transceiver to de-assert the carrier sense and receive data valid signals.

**Note:** These symbols are not translated into data.

#### 3.1.2.7 Receive Data Valid Signal

The Receive Data Valid signal (RXDV) indicates that recovered and decoded nibbles are being presented on the RXD[1:0] outputs synchronous to RXCLK. RXDV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RXDV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII mode).

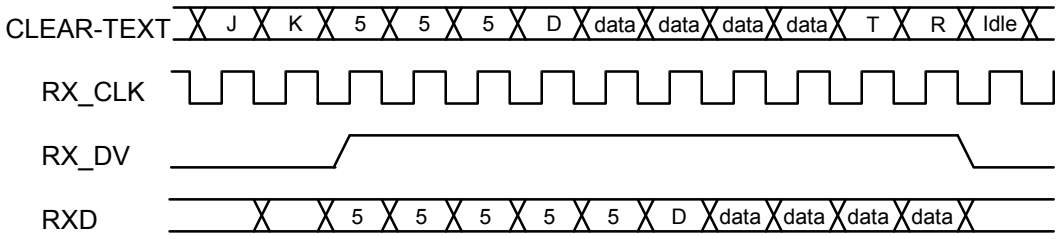



**Figure 3.3 Relationship Between Received Data and Specific MII Signals**

#### 3.1.2.8 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RXER signal is asserted and arbitrary data is driven onto the RXD[1:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RXER is asserted true and the value ‘1110’ is driven onto the RXD[1:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

#### 3.1.2.9 100M Receive Data Across the RMII Interface

The 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50 MHz. The controller samples the data on the rising edge of XTAL1/CLKIN (REF_CLK).

### 3.1.3 10BASE-T Transmit

Data to be transmitted comes from the MAC layer controller. The 10BASE-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5 MHz and converts them to a 10 Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

#### 3.1.3.1 10M Transmit Data Across the MII/RMII Interface

The MAC controller drives the transmit data onto the TXD bus. TXD[1:0] shall transition synchronously with respect to REF_CLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the device. TXD[1:0] shall be “00” to indicate idle when TXEN is deasserted. Values of TXD[1:0] other than “00” when TXEN is deasserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TXEN is deasserted shall be ignored by the device.TXD[1:0] shall provide valid data for each REF_CLK period while TXEN is asserted.

In order to comply with legacy 10BASE-T MAC/Controllers, in half-duplex mode the transceiver loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The transceiver also supports the SQE (Heartbeat) signal.