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LAN8810/LAN8810i

GMII 10/100/1000 Ethernet Transceiver with HP Auto-MDIX Support

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Compliant with IEEE 802.3ab (1000BASE-T), IEEE 802.3u (Fast Ethernet), and ISO 802-3/IEEE 802.3 (10BASE-T)
- HP Auto-MDIX support in accordance with IEEE 802.3ab specification at 10/100/1000 Mbps operation
- Small footprint 72-pin QFN lead-free RoHS compliant package with GMII (10 x 10 x 0.9mm height)
- Flexible configurations for LED status indicators
- Implements Reduced Power Operating Modes

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adapters/Servers
- Gaming Consoles
- POE Applications

Key Benefits

- High-Performance 10/100/1000 Ethernet Transceiver
  - Compliant with IEEE 802.3ab (1000BASE-T)
  - Compliant with IEEE 802.3/802.3u (Fast Ethernet)
  - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
  - 10BASE-T, 100BASE-TX and 1000BASE-T support
  - Loop-back modes
  - Auto-negotiation (NEXT page support)
  - Automatic polarity detection and correction
  - Link status change wake-up detection
  - Vendor specific register functions
  - Supports GMII interface
    - Controlled impedance outputs
  - Four status LED outputs and configurable LED modes with support for tricolor operation
  - Compliant with IEEE 802.3-2005 standards
    - GMII pins tolerant to 3.6V
  - Integrated DSP implements adaptive equalizer, echo cancelers, and crosstalk cancelers
  - Efficient digital baseline wander correction
- Power and I/Os
  - Configurable LED outputs
  - Various low power modes
  - Variable voltage I/O supply (2.5V/3.3V)
- Miscellaneous Features
  - IEEE 1149.1 (JTAG) boundary scan
  - Multiple clock options - 25MHz crystal or 25MHz single-ended clock
- Packaging
  - 72-pin QFN (10x10 mm) RoHS compliant package with GMII
- Environmental
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

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Table of Contents

1.0 INTRODUCTION

The LAN8810/LAN8810i is a low-power 10BASE-T/100BASE-TX/1000BASE-T Gigabit Ethernet physical layer (PHY) transceiver with variable I/O voltage that is fully compliant with the IEEE 802.3 and 802.3ab standards.

The LAN8810/LAN8810i can be configured to communicate with an Ethernet MAC via the standard MII(IEEE 802.3u)/GMII(IEEE 802.3z) interfaces. It contains a full-duplex transceiver for 1000 Mbps operation on four pairs of category 5 or better balanced twisted pair cable. Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V.

The LAN8810/LAN8810i is configurable via hardware and software, supporting both IEEE 802.3-2005 compliant and vendor-specific register functions via SMI. The LAN8810/LAN8810i implements Auto-Negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or crossover cables.

An internal block diagram of the LAN8810/LAN8810i is shown in Figure 1-1. A typical system-level diagram is shown in Figure 1-2.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM

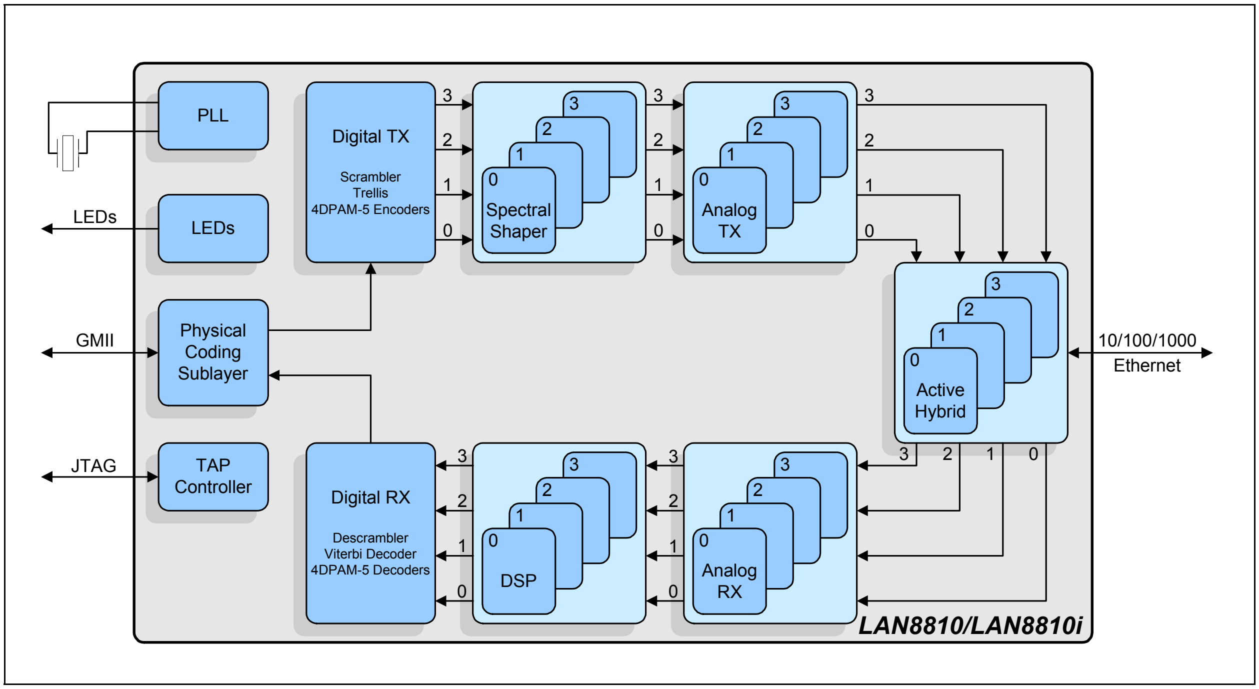
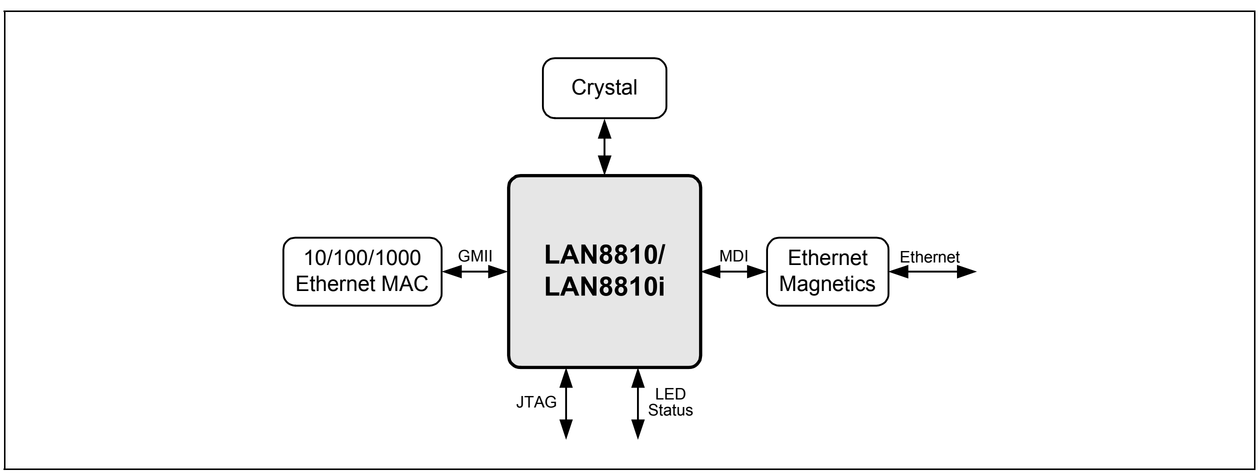
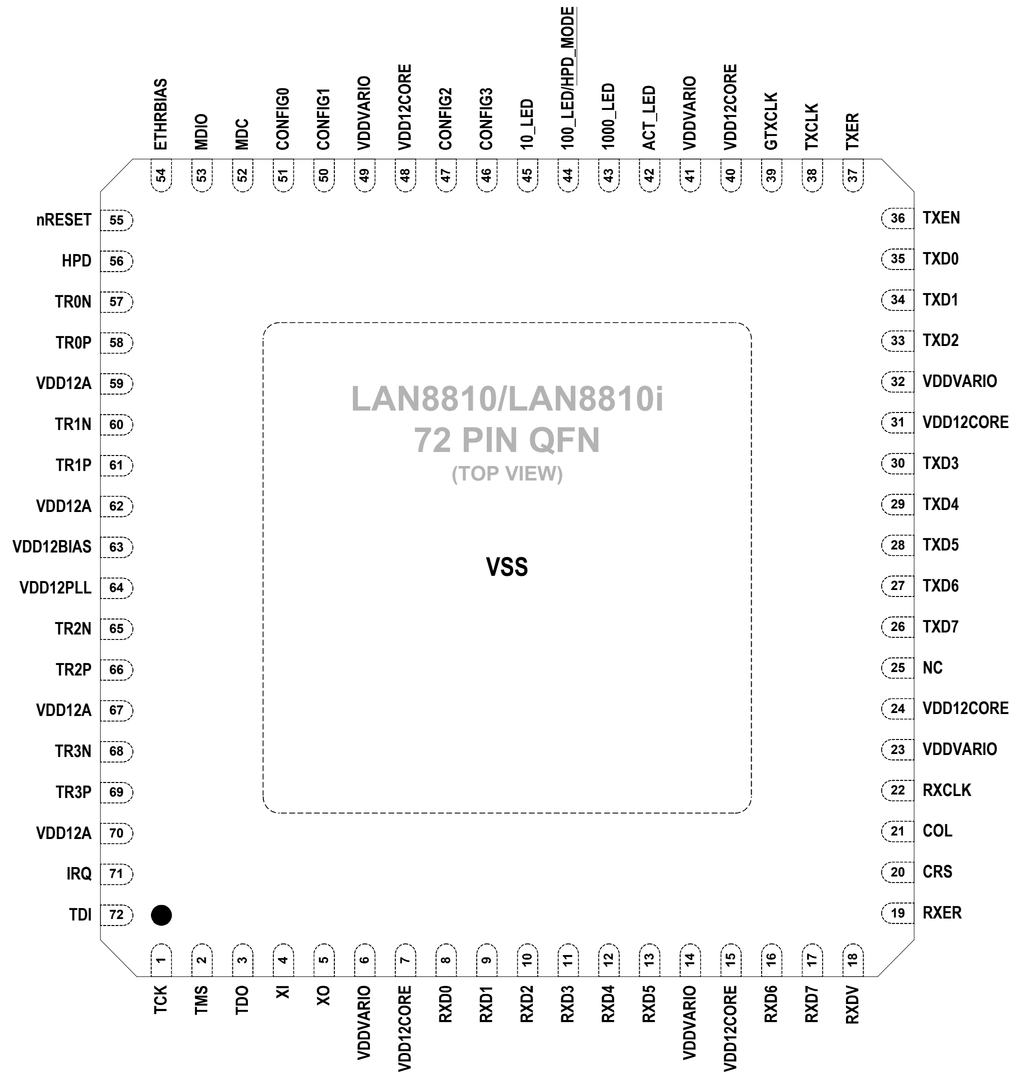


FIGURE 1-2: SYSTEM LEVEL BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 72-QFN PIN ASSIGNMENTS (TOP VIEW)



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

TABLE 2-1: GMII INTERFACE PINS

Num Pins	Name	Symbols	Buffer Type	Description
1	Transmit Data 0	TXD0	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 1	TXD1	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 2	TXD2	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 3	TXD3	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 4	TXD4	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 5	TXD5	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 6	TXD6	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Data 7	TXD7	VIS (PD)	The MAC transmits data to the PHY using this signal.
1	Transmit Error	TXER	VIS (PD)	Indicates a transmit error condition. **Note:** This input is ignored during 10BASE-T operation.
1	Transmit Enable	TXEN	VIS (PD)	Indicates the presence of valid data on TXD[7:0]
1	Transmit Clock	TXCLK	VO8	Used to latch data from the MAC into the PHY. MII (100BASE-TX): 25MHz MII (10BASE-T): 2.5MHz **Note:** For 1000BASE-T operation, GTXCLK is used as the transmit clock. TXCLK is not used in 1000BASE-T mode.
1	GMII Transmit Clock	GTXCLK	VIS (PD)	125MHz clock used to latch data from the MAC into the PHY in 1000BASE-T mode.
1	Receive Data 0	RXD0	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 1	RXD1	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 2	RXD2	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 3	RXD3	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 4	RXD4	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 5	RXD5	VO6	The PHY transfers data to the MAC using this signal.

TABLE 2-1: GMII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbols	Buffer Type	Description
1	Receive Data 6	RXD6	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data 7	RXD7	VO6	The PHY transfers data to the MAC using this signal.
1	Receive Data Valid	RXDV	VO6	Indicates that recovered and decoded data is being presented on the receive data pins.
1	Receive Error	RXER	VO6	Asserted to indicate an error has been detected in the frame presently being transferred from the PHY.
1	Receive Clock	RXCLK	VO6	Used to transfer data to the MAC. GMII (1000BASE-T): 125 MHz MII (100BASE-TX): 25 MHz MII (10BASE-T): 2.5 MHz
1	Collision Detect	COL	VO6	Asserted to indicate detection of a collision condition. (used in half-duplex mode only)
1	Carrier Sense	CRS	VO6	Indicates detection of carrier. (used in half-duplex mode only)

Note 2-1 Configuration strap values are latched on hardware reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.8, "Configuration," on page 22 for additional information.

TABLE 2-2: SERIAL MANAGEMENT INTERFACE (SMI) PINS

Num Pins	Name	Symbols	Buffer Type	Description
1	SMI Clock	MDC	VIS (PD)	Serial Management Interface clock.
1	SMI Data Input/ Output	MDIO	VIS/VO8 (PU)	Serial Management Interface data input/output.

TABLE 2-3: LED & CONFIGURATION PINS

Num Pins	Name	Symbols	Buffer Type	Description
1	10BASE-T Link LED Indicator	10_LED	VO8	10BASE-T LED link indication. Refer to Section 3.9.1, "LEDs," on page 26 for additional information.
1	100BASE-TX Link LED Indicator	100_LED	VO8	100BASE-TX LED link indication. Refer to Section 3.9.1, "LEDs," on page 26 for additional information.
	Hardware Power Down (HPD) Mode Configuration Strap	HPD_MODE	VIS (PD)	This configuration strap is used to select the Hardware Power Down (HPD) mode. When pulled-up, the PLL is not disabled when HPD is asserted. When pulled-down, the PLL is disabled when HPD is asserted. Refer to Section 3.7.3, "Hardware Power-Down," on page 22 for additional information. See Note 2-2 for more information on configuration straps.
1	1000BASE-T Link LED Indicator	1000_LED	VO8	1000BASE-T LED link indication. Refer to Section 3.9.1, "LEDs," on page 26 for additional information.
1	Link Activity LED Indicator	ACT_LED	VO8	Link activity LED indication. Refer to Section 3.9.1, "LEDs," on page 26 for additional information.
1	Configuration Input 0	CONFIG0	VIS (PD)	This pin sets the PHYADD[1:0] bits of the 10/100 Special Modes Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," on page 23 for additional information.
1	Configuration Input 1	CONFIG1	VIS (PD)	This pin sets the PAUSE bit of the Auto Negotiation Advertisement Register and PHYADD [2] bit of the 10/100 Special Modes Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," on page 23 for additional information.
1	Configuration Input 2	CONFIG2	VIS (PD)	This pin sets the MOD[1:0] bits of the Extended Mode Control/Status Register on reset or power-up. It must be connected to VSS, 100_LED, 1000_LED, or VDDVARIO. Refer to Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," on page 23 for additional information.
1	Configuration Input 3	CONFIG3	VIS (PD)	This pin sets the MOD[3] bit of the Extended Mode Control/Status Register on reset or power-up. It must be connected to 1000_LED or VDDVARIO. Refer to Section 3.8.1.2, "CONFIG[3:0] Configuration Pins," on page 23 for additional information.

Note 2-2 Configuration strap values are latched on hardware reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.8, "Configuration," on page 22 for additional information.

TABLE 2-4: ETHERNET PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Ethernet TX/ RX Positive Channel 0	TR0P	AIO	Transmit/Receive Positive Channel 0.
1	Ethernet TX/ RX Negative Channel 0	TR0N	AIO	Transmit/Receive Negative Channel 0.
1	Ethernet TX/ RX Positive Channel 1	TR1P	AIO	Transmit/Receive Positive Channel 1.
1	Ethernet TX/ RX Negative Channel 1	TR1N	AIO	Transmit/Receive Negative Channel 1.
1	Ethernet TX/ RX Positive Channel 2	TR2P	AIO	Transmit/Receive Positive Channel 2.
1	Ethernet TX/ RX Negative Channel 2	TR2N	AIO	Transmit/Receive Negative Channel 2.
1	Ethernet TX/ RX Positive Channel 3	TR3P	AIO	Transmit/Receive Positive Channel 3.
1	Ethernet TX/ RX Negative Channel 3	TR3N	AIO	Transmit/Receive Negative Channel 3.
1	External PHY Bias Resistor	ETHRBIAS	AI	Used for the internal bias circuits. Connect to an external 8.06K 1.0% resistor to ground.

TABLE 2-5: JTAG PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	JTAG Test Data Out	TDO	VO8	JTAG (IEEE 1149.1) data output.
1	JTAG Test Data Input	TDI	VIS (PU)	JTAG (IEEE 1149.1) data input. **Note:** When not used, tie this pin to VDDVARIO.
1	JTAG Test Clock	TCK	VIS (PD)	JTAG (IEEE 1149.1) test clock. **Note:** When not used, tie this pin to VSS.
1	JTAG Test Mode Select	TMS	VIS (PU)	JTAG (IEEE 1149.1) test mode select. **Note:** When not used, tie this pin to VDDVARIO.

TABLE 2-6: MISCELLANEOUS PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a 25 MHz single-ended clock oscillator. When this method is used, XO should be left unconnected. Refer to Section 5.6, "Clock Circuit," on page 75 for additional information.
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.
1	System Reset	nRESET	VIS (PU)	This active-low pin allows external hardware to reset the device.
1	Interrupt Request	IRQ	VO8	Programmable interrupt request. **Note:** When used, this pin requires an external 4.7K pull-up resistor.
1	Hardware Power Down	HPD	VIS (PD)	When asserted, this pin places the device into Hardware Power Down (HPD) mode. Refer to Section 3.7.3, "Hardware Power-Down," on page 22 for additional information.
1	No Connect	NC	-	This pin must be left floating for normal device operation.

TABLE 2-7: POWER PINS

Num Pins	Name	Symbol	Buffer Type	Description
6	+3.3V/+2.5V I/O Power Supply Input	VDDVARIO	P	+2.5V/+3.3V variable I/O power. Refer to Section 3.10, "Application Diagrams," on page 33 and the LAN8810/LAN8810i reference schematics for connection information.
6	Digital Core +1.2V Power Supply Input	VDD12CORE	P	Refer to Section 3.10, "Application Diagrams," on page 33 and the LAN8810/LAN8810i reference schematics for connection information.
4	Ethernet +1.2V Port Power Supply Input For Channels 0-3	VDD12A	P	Refer to Section 3.10, "Application Diagrams," on page 33 and the LAN8810/LAN8810i reference schematics for connection information.
1	Ethernet +1.2V Bias Power Supply Input	VDD12BIAS	P	Refer to Section 3.10, "Application Diagrams," on page 33 and the LAN8810/LAN8810i reference schematics for connection information.
1	Ethernet PLL +1.2V Power Supply Input	VDD12PLL	P	Refer to Section 3.10, "Application Diagrams," on page 33 and the LAN8810/LAN8810i reference schematics for connection information.
Note 2-3	Ground	VSS	P	Common Ground

Note 2-3 Exposed pad on package bottom (Figure 2-1).

TABLE 2-8: 72-QFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	TCK	19	RXER	37	TXER	55	nRESET
2	TMS	20	CRS	38	TXCLK	56	HPD
3	TDO	21	COL	39	GTXCLK	57	TR0N
4	XI	22	RXCLK	40	VDD12CORE	58	TR0P
5	XO	23	VDDVARIO	41	VDDVARIO	59	VDD12A
6	VDDVARIO	24	VDD12CORE	42	ACT_LED	60	TR1N
7	VDD12CORE	25	NC	43	1000_LED	61	TR1P
8	RXD0	26	TXD7	44	100_LED/ HPD_MODE	62	VDD12A
9	RXD1	27	TXD6	45	10_LED	63	VDD12BIAS
10	RXD2	28	TXD5	46	CONFIG3	64	VDD12PLL
11	RXD3	29	TXD4	47	CONFIG2	65	TR2N
12	RXD4	30	TXD3	48	VDD12CORE	66	TR2P
13	RXD5	31	VDD12CORE	49	VDDVARIO	67	VDD12A
14	VDDVARIO	32	VDDVARIO	50	CONFIG1	68	TR3N
15	VDD12CORE	33	TXD2	51	CONFIG0	69	TR3P
16	RXD6	34	TXD1	52	MDC	70	VDD12A
17	RXD7	35	TXD0	53	MDIO	71	IRQ
18	RXDV	36	TXEN	54	ETHRBIAS	72	TDI
EXPOSED PAD MUST BE CONNECTED TO VSS							

2.1 Buffer Types

TABLE 2-9: BUFFER TYPES

Buffer Type	Description
VIS	Variable voltage Schmitt-triggered input.
VO6	Variable voltage output with 6 mA sink and 6 mA source.
VO8	Variable voltage output with 8 mA sink and 8 mA source.
PU	50uA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50uA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input.
AIO	Analog bi-directional.
ICLK	Crystal oscillator input pin.
OCLK	Crystal oscillator output pin.
P	Power pin.

Note 1: The digital signals are not 5V tolerant. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 60 for additional buffer information.

2: Sink and source capabilities are dependent on the VDDVARIO voltage. Refer to Section 5.1, "Absolute Maximum Ratings*," on page 60 for additional information.

3.0 FUNCTIONAL DESCRIPTION

This chapter provides functional descriptions of the various device features. These features have been categorized into the following sections:

- Auto-negotiation
- HP Auto-MDIX
- GMII Interface
- Serial Management Interface (SMI)
- Interrupt Management
- Resets
- Power-Down modes
- Configuration
- Miscellaneous Functions
- Application Diagrams

3.1 Auto-negotiation

The purpose of the auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 and clause 40 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the integrated Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication field of the PHY Special Control / Status Register as well as the Auto Negotiation Link Partner Ability Register.

The advertised capabilities of the PHY are stored in Auto Negotiation Advertisement Register. The defaults advertised by the device are determined as described in Section 3.8.1.2.2, "Configuring the Mode of Operation (CONFIG[3:2])," on page 24.

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller. When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting the Restart Auto-Negotiate bit of the Basic Control Register

On detection of one of these events, the device begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). The data transmitted by an FLP burst is known as a “Link Code Word.” This exchange of information allows link partners to determine the Highest Common Ability (HCD).

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if all of the required FLP bursts are not received.

Writing the 100BASE-TX Full Duplex, 100BASE-TX, 10BASE-T Full Duplex, and 10BASE-T bits of the Auto Negotiation Advertisement Register allows software control of the advertised capabilities. However, writing the Auto Negotiation Advertisement Register does not automatically re-start auto-negotiation. The Restart Auto-Negotiate bit of the Basic Control Register must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing the Auto-Negotiation Enable bit of the Basic Control Register.

Auto-Negotiation also resolves the Master/Slave clocking relationship between two PHYs for a 1000BASE-T link. Refer to Section 3.1.4, "Master/Slave," on page 14 for additional information.

3.1.1 RESTARTING AUTO-NEGOTIATION

Auto-negotiation can be restarted at any time by using the Restart Auto-Negotiate bit of the Basic Control Register. Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity restarts Auto-negotiation by writing to the Restart Auto-Negotiate bit, the device will respond by stopping all transmission/receiving operations. Auto-negotiation will restart after approximately 1200 mS. The Link Partner will have also dropped the link and will resume auto-negotiation.

3.1.2 DISABLING AUTO-NEGOTIATION

Auto-negotiation can be disabled via software by clearing the Auto-Negotiation Enable bit of the Basic Control Register. The device will then force its speed of operation to reflect the information in the Speed Select[1], Speed Select[0], and Duplex Mode bits of the Basic Control Register. These bits are ignored when auto-negotiation is enabled.

3.1.3 PARALLEL DETECTION

If the LAN8810/LAN8810i is connected to a device lacking the ability to auto-negotiate (for example, no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case, the link is presumed to be half-duplex per the IEEE standard. This ability is known as “Parallel Detection”. This feature ensures inter operability with legacy link partners.

The Ethernet MAC has access to information regarding parallel detect via the Auto Negotiation Expansion Register. If a link is formed via parallel detection, the Link Partner Auto-Negotiation Able bit of the Auto Negotiation Expansion Register is cleared to indicate that the Link Partner is not capable of auto-negotiation. If a fault occurs during parallel detection, the Parallel Detection Fault bit of this register is set.

The Auto Negotiation Link Partner Ability Register is updated with information from the link partner which is coded in the received FLPs. If the Link Partner is not auto-negotiation capable, then the Auto Negotiation Link Partner Ability Register is updated after completion of parallel detection to reflect the speed capability of the Link Partner.

Parallel detect cannot be used to establish Gigabit Ethernet links because echo cancellation and signal recovery on a Gigabit Ethernet link requires resolution of the Master/Slave clock relationship, which requires the exchange of FLPs.

3.1.4 MASTER/SLAVE

In 1000BASE-T, one of the two link partner devices must be configured as Master and the other as Slave. The Master device transmits data using the local clock, while the Slave device uses the clock recovered from incoming data.

The Master and Slave assignments are set using the configuration pins as described in Section 3.8.1.2.2, "Configuring the Mode of Operation (CONFIG[3:2])," on page 24 or by using the Master/Slave Manual Config Enable and Master/Slave Manual Config Value bits of the Master/Slave Control Register. If both the link partner and the local device are manually given the same Master/Slave assignment, an error will be indicated in the Master/Slave Configuration Fault bit of the Master/Slave Status Register.

Depending on the link partner configuration, the manual Master/Slave mode can be resolved to sixteen possible outcomes, as shown in Table 3-1.

TABLE 3-1: MASTER/SLAVE RESOLUTION FOR 1000BASE-T

LAN8810/LAN8810i Advertisement	Link Partner Advertisement	LAN8810/LAN8810i Result	Link Partner Result
Single-Port	Single-Port	M/S resolved by random seed	M/S resolved by random seed
Single-Port	Multi-Port	Slave	Master
Single-Port	Manual Master	Slave	Master
Single-Port	Manual Slave	Master	Slave
Multi-Port	Single-Port	Master	Slave
Multi-Port	Multi-Port	M/S resolved by random seed	M/S resolved by random seed
Multi-Port	Manual Master	Slave	Master
Multi-Port	Manual Slave	Master	Slave
Manual Master	Single-Port	Master	Slave

TABLE 3-1: MASTER/SLAVE RESOLUTION FOR 1000BASE-T (CONTINUED)

LAN8810/LAN8810i Advertisement	Link Partner Advertisement	LAN8810/LAN8810i Result	Link Partner Result
Manual Master	Multi-Port	Master	Slave
Manual Master	Manual Master	No Link	No Link
Manual Master	Manual Slave	Master	Slave
Manual Slave	Single-Port	Slave	Master
Manual Slave	Multi-Port	Slave	Master
Manual Slave	Manual Master	Slave	Master
Manual Slave	Manual Slave	No Link	No Link

3.1.5 MANUAL OPERATION

The device supports a manual (forced) operation for test purposes. In manual operation, the user sets the link speed (10Mbps or 100Mbps) and the duplex state (full or half).

Auto-negotiation must be disabled in order to manually configure the speed and the duplex. This may be accomplished using the configuration pins, as described in Section 3.8.1.2.2, "Configuring the Mode of Operation (CONFIG[3:2])," on page 24, or by using the Basic Control Register as described in Section 3.1.2, "Disabling Auto-negotiation," on page 14. For 10BASE-T and 100BASE-TX, the link state of the device is determined by the Speed Select[1], Speed Select[0], and Duplex Mode bits of the Basic Control Register. Manual operation at a link speed of 1000Mbps is not supported.

3.1.6 HALF VS. FULL-DUPLEX

Half-duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the internal carrier sense signal, CRS, responds to both transmit and receive activity. If data is received while the PHY is transmitting, a collision results.

In full-duplex mode, the PHY is able to transmit and receive data simultaneously and collision detection is disabled. In this mode, the internal CRS responds only to receive activity. In 10BASE-T and 100BASE-T mode, CRS is redefined to respond only to received activity. In 1000BASE-T, CRS is disabled.

Table 3-2 describes the behavior of the internal CRS bit under all receive/transmit conditions.

TABLE 3-2: CRS BEHAVIOR

Mode	Speed	Duplex	Activity	CRS Behavior (Note 3-1)
Manual	10 Mbps	Half-Duplex	Transmitting	Active
Manual	10 Mbps	Half-Duplex	Receiving	Active
Manual	10 Mbps	Full-Duplex	Transmitting	Low
Manual	10 Mbps	Full-Duplex	Receiving	Active
Manual	100 Mbps	Half-Duplex	Transmitting	Active
Manual	100 Mbps	Half-Duplex	Receiving	Active
Manual	100 Mbps	Full-Duplex	Transmitting	Low
Manual	100 Mbps	Full-Duplex	Receiving	Active
Auto-Negotiation	10 Mbps	Half-Duplex	Transmitting	Active

TABLE 3-2: CRS BEHAVIOR (CONTINUED)

Mode	Speed	Duplex	Activity	CRS Behavior (Note 3-1)
Auto-Negotiation	10 Mbps	Half-Duplex	Receiving	Active
Auto-Negotiation	10 Mbps	Full-Duplex	Transmitting	Low
Auto-Negotiation	10 Mbps	Full-Duplex	Receiving	Active
Auto-Negotiation	100 Mbps	Half-Duplex	Transmitting	Active
Auto-Negotiation	100 Mbps	Half-Duplex	Receiving	Active
Auto-Negotiation	100 Mbps	Full-Duplex	Transmitting	Low
Auto-Negotiation	100 Mbps	Full-Duplex	Receiving	Active

Note 3-1 The internal CRS signal operates in two modes: Active and Low. When in Active mode, the internal CRS will transition high and low upon line activity, where a high value indicates a carrier has been detected. In Low mode, the internal CRS stays low and does not indicate carrier detection.

3.2 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-5 (100BASE-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a crossover patch cable, as shown in Figure 3-1, the Auto-MDIX PHY is capable of configuring the twisted pair pins for correct transceiver operation.

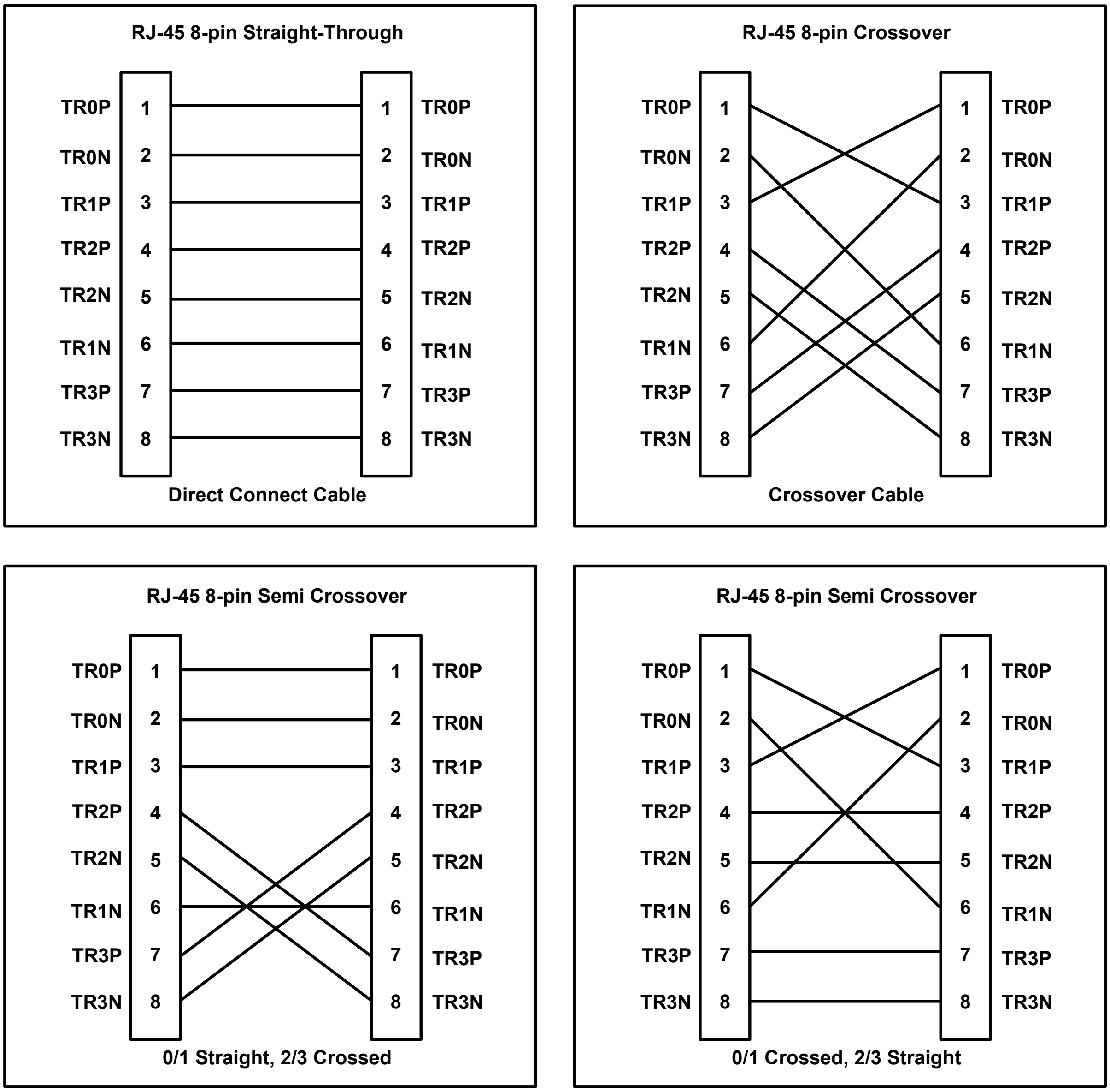
The internal logic of the device detects the TX and RX pins of the connecting device. It can automatically re-assign channel 0 and 1 if required to establish a link. In 1000BASE-T mode, it can re-assign channel 2 and 3. Crossover resolution precedes the actual auto-negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3ab Clause 40, section 40.8.2. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

Auto-MDIX is enabled by default, and can be disabled by the Auto MDIX Disable bit in the 10/100 Mode Control/Status Register. When Auto-MDIX is disabled, the TX and RX pins can be configured manually by the MDI/MDI-X 0:1 and MDI/MDI-X 2:3 bits in the Extended Mode Control/Status Register.

The device includes an advanced crossover resolution capability called Semi Crossover. This is an extension to HP Auto-MDIX that corrects for a cable with only two pairs crossed. If Semi Crossover is enabled, after the device has attempted to establish a link with all four signal pairs normal or crossed, it will attempt to establish a link with pairs 2/3 switched and 0/1 straight, and then with pairs 0/1 switched and pairs 2/3 straight. The Semi Crossover is enabled by default, and can be disabled by the Semi Crossover Enable bit in the 10/100 Mode Control/Status Register.

After resolution of crossed pairs is complete, using either HP Auto-MDIX or the Semi Crossover function, the MDI/MDI-X status is reported through the XOVER Resolution 0:1 and XOVER Resolution 2:3 bits of the User Status 2 Register.

FIGURE 3-1: CABLE CONNECTION TYPES: STRAIGHT-THROUGH, CROSSOVER, SEMI CROSSOVER



3.2.1 REQUIRED ETHERNET MAGNETICS

The magnetics selected for use with the device should be an Auto-MDIX style magnetic available from several vendors. Refer to Application Note 8.13 “Suggested Magnetics” for the latest qualified and suggested magnetics. Vendors and part numbers are provided in this application note.

3.3 GMII Interface

The device communicates with an external MAC using the Gigabit Media Independent Interface (GMII). The GMII is compliant with the IEEE 802.3 standard, and provides support for 1000BASE-T, 100BASE-TX, or 10BASE-T operation.

For 1000BASE-T, the MAC generated 125 MHz GTXCLK transmit clock is used to synchronize the TXD, TXEN and TXER signals. For 100BASE-TX and 10BASE-T operation, the device generated TXCLK transmit clock is used to synchronize the TXD, TXEN and TXER signals. TXCLK is 25 MHz or 2.5 MHz for 100BASE-TX and 10BASE-T operation, respectively. TXER and TXEN are both driven by the MAC and indicate a transmit error and valid transmit data, respectively. On the receiver side, the device generated RXCLK is used to synchronize the RXD, RXDV, RXER, COL and CRS signals for all modes of operation.

The GMII provides backwards compatibility with the legacy MII. Table 3-3, "GMII/MII Signal Mapping" describes which pins are used in each mode.

TABLE 3-3: GMII/MII SIGNAL MAPPING

GMII Mode (IEEE 802.3 Clause 35)	MII Mode (IEEE 802.3 Clause 22)
TXD[3:0]	TXD[3:0]
TXD[7:4]	
TXEN	TXEN
TXER	TXER
TXCLK (10/100Mbps operation)	TXCLK
GTXCLK (1000Mbps operation)	
COL	COL
CRS	CRS
RXD[3:0]	RXD[3:0]
RXD[7:4]	
RXDV	RXDV
RXER	RXER
RXCLK	RXCLK

Timing information for the GMII/MII interface is provided in Section 5.5, "AC Specifications," on page 65. For additional information on the GMII/MII interface, refer to the IEEE 802.3 specification.

3.3.1 MII ISOLATE MODE

The device may be configured to electrically isolate the GMII pins by setting the Isolate bit of the Basic Control Register. In this mode, all MAC data interface output pins are HIGH and all MAC data interface input pins are ignored. In this mode, the SMI interface is kept active, allowing the MAC to access the SMI registers and generate interrupts. All MDI operations are halted while in isolate mode.

3.4 Serial Management Interface (SMI)

The Serial Management Interface is used to control the device and obtain its status. This interface supports the standard PHY registers required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers allowed by the specification. Non-supported registers (such as 11 to 14) will be read as hexadecimal “FFFF”. Device registers are detailed in Section 4.0, "Register Descriptions," on page 35.

At the system level, SMI provides 2 signals: MDIO and MDC. The MDC signal is an aperiodic clock provided by the station management controller (SMC). MDIO is a bi-directional data SMI input/output signal that receives serial data (commands) from the controller SMC and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges. The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is 400 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The frame structure and timing of the data is shown in Figure 1-1 and Figure 1-2. The timing relationships of the MDIO signals are further described in Section 5.5.7, "SMI Timing," on page 73.

FIGURE 3-2: MDIO TIMING AND FRAME STRUCTURE - READ CYCLE

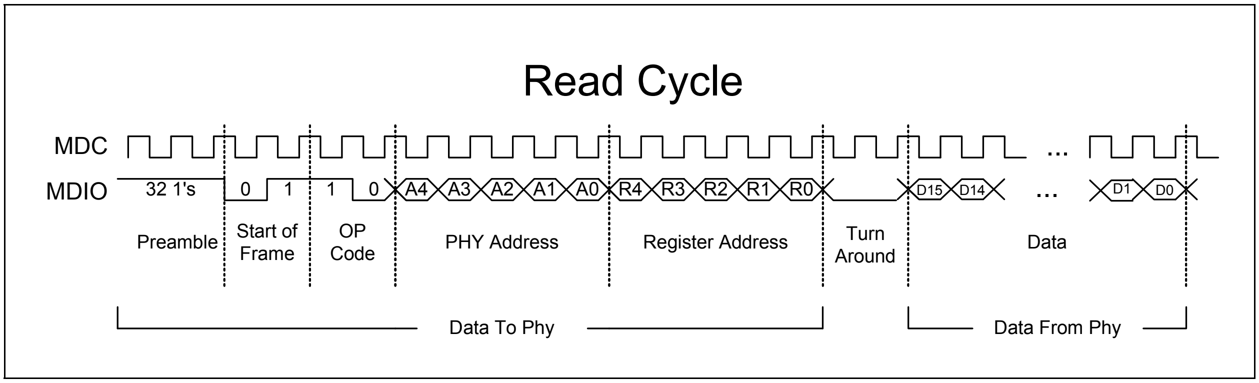
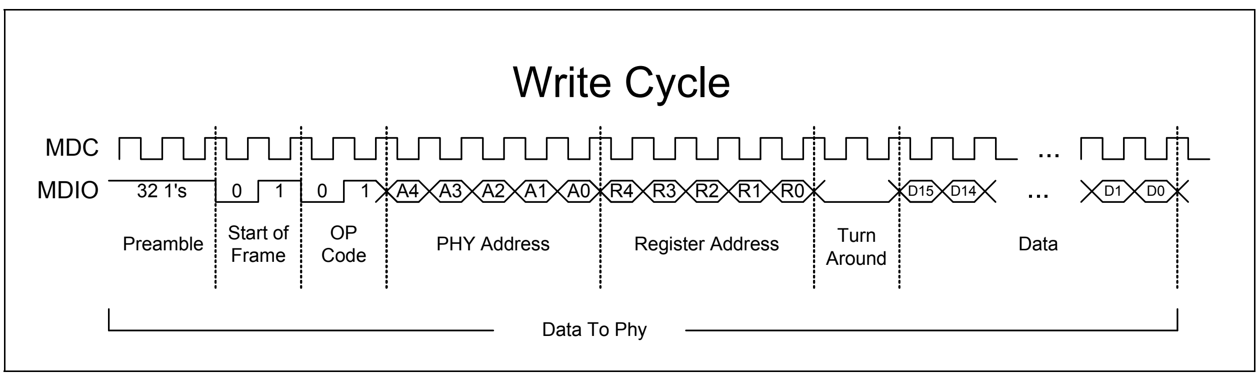


FIGURE 3-3: MDIO TIMING AND FRAME STRUCTURE - WRITE CYCLE



3.5 Interrupt Management

The device supports multiple interrupt capabilities which are not a part of the IEEE 802.3 specification. An active low asynchronous interrupt signal may be generated on the IRQ pin when selected events are detected, as configured by the Interrupt Mask Register.

To set an interrupt, the corresponding mask bit in the Interrupt Mask Register must be set (see Table 3-4). When the associated event occurs, the IRQ pin will be asserted. When the corresponding event to deassert IRQ is true, the IRQ pin will be deasserted. All interrupts are masked following a reset.

Note:	Table 3-4 utilizes register index and bit number referencing in lieu of individual names. For example, “30.10” is used to reference bit 10 (transmitter elastic buffer overflow interrupt enable) of the Interrupt Mask Register (register index 30).

TABLE 3-4: INTERRUPT MANAGEMENT TABLE

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert IRQ	Event to Deassert IRQ
30.15:11	29.15:11	RESERVED	-NA-	-NA-	-NA-	-NA-
30.10	29.10	Transmitter Elastic Buffer Overflow	-NA-	-NA- (Note 3-3)	Transmitter Elastic Buffer Overflow	Overflow condition resolved
30.9	29.9	Transmitter Elastic Buffer Underflow	-NA-	-NA- (Note 3-3)	Transmitter Elastic Buffer Underflow	Underflow condition resolved
30.8	29.8	Idle Error Count Overflow	10.7:0	Idle Error Count	Idle Error Count Overflow	Reading register 10
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1 (Note 3-2)	Falling 17.1 or Reading register 29
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	Falling 1.5 or Reading register 29
30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	Falling 1.4, or Reading register 1 or Reading register 29
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	Reading register 1 or Reading register 29
30.3	29.3	RESERVED	-NA-	-NA-	-NA-	-NA-
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	Falling 6.4 or Reading register 6, or Reading register 29 or Re-AutoNegotiate or Link down
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	Falling of 6.1 or Reading register 6, or Reading register 29 Re-auto-negotiate, or Link Down.

Note 3-2 The ENERGYON bit of the 10/100 Mode Control/Status Register (17.1) defaults to “1” after a hardware reset. If no energy is detected before 256mS, the ENERGYON bit will be cleared. When ENERGYON is “0” and energy is detected, due to the establishment of a valid link or the PHY auto-negotiation moving past the ability detect state, the ENERGYON bit will be set and the INT7 bit of the Interrupt Source Flags Register will assert. If ENERGYON is set and the energy is removed, the INT7 bit will assert. The ENERGYON bit will clear 256mS after the interrupt. If the PHY is in manual mode, INT7 will be asserted 256mS after the link is broken. If the PHY is auto-negotiating, INT7 will be asserted 256mS after the PHY returns to the ability detect state (maximum of 1.5S after the link

is broken). To prevent an unexpected assertion of IRQ, the ENERGYON interrupt mask (INT7_EN) should always be cleared as part of the ENERGYON interrupt service routine.

Note 3-3 The transmitter FIFO depth can be adjusted via the Transmitter FIFO Depth field of the Extended Mode Control/Status Register (19.10:9).

3.6 Resets

The device provides the following chip-level reset sources:

- Hardware Reset (nRESET)
- Software Reset
- Power-Down Reset

3.6.1 HARDWARE RESET (NRESET)

Note:	System implementers should connect the nRESET input pin to an output pin from the respective MAC or microcontroller, so that the required power-up sequence can be performed without causing a full system reset event.

A hardware reset will occur when the system reset nRESET input pin is driven low. Anytime nRESET is asserted, it must be held low for the minimum time specified in Section 5.5.4, "Reset Timing," on page 68 to ensure proper reset to the PHY. Following a hardware reset, the device resets the device registers and relatches the configuration straps and CONFIG[3:0] pins.

On first power-up of the device, the sequence below must be also be followed to ensure the device exits reset in the correct operational state:

1. Perform a hardware reset on power-up as per Section 5.5.3, "Power-On Hardware Reset Timing," on page 67.
2. Wait a minimum of 250mS
3. Write SMI Register 0 (Basic Control Register) = 0x4040
4. Wait a minimum of 1 second
5. Assert the nRESET input pin (nRESET = 0)
6. Wait a minimum of 50mS
7. Deassert the nRESET input pin (nRESET = 1)

After completing this sequence, the LAN8810/LAN8810i will be in the default states and ready for any initialization or configuration and allow operation.

Note:	A hardware reset (nRESET assertion) is required following power-up. Refer to Section 5.5.3, "Power-On Hardware Reset Timing," on page 67 for additional information.

3.6.2 SOFTWARE RESET

A software reset is initiated by writing a ‘1’ to the PHY Soft Reset (RESET) bit of the Basic Control Register. This self-clearing bit will return to ‘0’ after approximately 256µs, at which time the PHY reset is complete. This reset initializes the logic within the PHY, with the exception of register bits marked as “NASR” (Not Affected by Software Reset).

Following a software reset, the device configuration is reloaded from the register bit values, and not from the configuration straps and CONFIG[3:0] pins. The device does not relatch the hardware configuration settings. For example, if the device is powered up and a configuration strap is changed from its initial power up state, a software reset will not load the new strap setting.

3.6.3 POWER-DOWN RESET

A power-down reset is automatically activated when the device comes out of the power-down mode. During power-down, the registers are not reset. Configuration straps and CONFIG[3:0] pins are not latched as a result of a power-down reset. The power-down reset is internally extended by 256 µs after exiting the power-down mode to allow the PLLs to stabilize before the logic is released from reset. Refer to Section 3.7, "Power-Down modes," on page 22 for details on the various power-down modes.

3.7 Power-Down modes

The device supports 3 power-down modes:

- General Power-Down
- Energy Detect Power-Down
- Hardware Power-Down

3.7.1 GENERAL POWER-DOWN

This power-down mode is controlled by the Power Down bit of the Basic Control Register. In this mode, the entire device is powered-down except for the serial management interface. The device remains in the general power-down mode while Power Down is set. When Power Down is cleared, the device powers up and is automatically reset (via a Power-Down Reset). For maximum power savings, auto-negotiation should be disabled before enabling the general power-down mode.

3.7.2 ENERGY DETECT POWER-DOWN

This power-down mode is controlled by the EDPWRDOWN bit of the 10/100 Mode Control/Status Register. In this mode, when no energy is present on the line, nothing is transmitted and the device is powered-down except for the management interface, the SQUELCH circuit and the ENERGYON logic.

The ENERGYON bit in the 10/100 Mode Control/Status Register is asserted when there is valid energy from the line (100BASE-TX, 10BASE-T, or Auto-Negotiation signals) and the PHY powers-up. It automatically resets itself into the previous state prior to power-down, and stays in active mode as long as energy exists on the line. If the ENGERGYON interrupt is enabled (INT7_EN of the Interrupt Mask Register), IRQ is asserted.

Note:	The first and possibly second packet to activate ENERGYON may be lost.

3.7.3 HARDWARE POWER-DOWN

This power-down mode is controlled by the HPD pin. In this mode, the entire device is powered-down except for the serial management interface. The HPD_MODE configuration strap selects whether the PLL will be shut down when in hardware power-down mode. To exit the hardware power-down mode, the HPD pin must be deasserted, followed by the deassertion of the Power Down bit in the Basic Control Register. If the hardware power-down mode is set to shut down the PLL, a software reset must also be issued.

Note 1: The device will wake-up in the hardware power-down mode if the HPD pin is asserted during hardware reset.

2: For additional information on the HPD_MODE configuration strap, refer to Section 3.8.1.1, "Configuration Straps," on page 23.

3.8 Configuration

The device mode of operation may be controlled by hardware and software (register-selectable) configuration options. The initial configuration may be selected in hardware as described in Section 3.8.1. In addition, register-selectable software configuration options may be used to further define the functionality of the transceiver as described in Section 3.8.2. The device supports both IEEE 802.3-2005 compliant and vendor-specific register functions.

3.8.1 HARDWARE CONFIGURATION

Hardware configuration is controlled via multiple configuration straps and the CONFIG[3:0] configuration pins. These items are detailed in the following sub-sections.

3.8.1.1 Configuration Straps

Configuration straps are multi-function pins that are driven as outputs during normal operation. During a Hardware Reset (nRESET), these outputs are tri-stated. The high or low state of the signal is latched following de-assertion of the reset and is used to determine the default configuration of a particular feature. Table 3-5 details the configuration straps. Configuration straps are also listed as part of Section 2.0, "Pin Description and Configuration," on page 5 with underlined names.

Configuration straps include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note 1: The system designer must guarantee that configuration straps meet the timing requirements specified in Section 5.5.3, "Power-On Hardware Reset Timing," on page 67. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

2: Configuration straps must never be driven as inputs. If required, configuration straps can be augmented, or overridden with external resistors.

TABLE 3-5: CONFIGURATION STRAPS

Configuration Strap	Description	Logic 0 (PD)	Logic 1 (PU)
HPD_MODE	Selects the hardware power-down (HPD) mode	HPD with PLL disabled (Default)	HPD with PLL enabled

3.8.1.2 CONFIG[3:0] Configuration Pins

The device provides 4 dedicated configuration pins, CONFIG[3:0], which are used to select the default SMI address and mode of operation. The CONFIG[3:0] configuration pins differ from configuration straps in that they are single-purpose pins and have different latch timing requirements. The high or low states of the CONFIG[3:0] pins are latched following deassertion of a Hardware Reset (nRESET). Refer to Section 5.5.3, "Power-On Hardware Reset Timing," on page 67 for additional CONFIG[3:0] timing information.

Each CONFIG[3:0] configuration pin can be connected in one of four ways. The Configuration Pin Value (CPV) represented by each connection option is shown in Table 3-6.

TABLE 3-6: HARDWARE CONNECTION DETERMINES CONFIGURATION PIN VALUE (CPV)

CONFIG[X] Connects to:	Value
GND	CPV(0)
100_LED	CPV(1)
1000_LED	CPV(2)
VDD	CPV(3)

Using the CPV nomenclature for each CONFIG[3:0] pin, Section 3.8.1.2.1 describes how to configure the SMI address and Section 3.8.1.2.2 describes how to configure the initial mode of operation.

Note: The HPD pin is also a dedicated configuration pin. HPD forces the entire device to power down except for the management interface. The Hardware Power-Down mode is described in Section 3.7.3, "Hardware Power-Down," on page 22.

3.8.1.2.1 Configuring the SMI Address (CONFIG[1:0])

The SMI address may be configured via hardware to any value between 0 and 7. If an address greater than 7 is required, the user can configure the PHY address using Software Configuration via the PHYADD[4:0] field of the 10/100 Special Modes Register (after SMI communication at an address is established).

The CONFIG1 pin is used to configure both the SMI address and the value of the Pause Operation (PAUSE) bit in the Auto Negotiation Advertisement Register. The user must first determine the desired PAUSE value. The configuration pin values for CONFIG1 and CONFIG0 should then be selected using Table 3-7 (PAUSE=0) or Table 3-8 (PAUSE=1), respectively.

TABLE 3-7: SMI ADDRESS CONFIGURATION WITH PAUSE=0

PHYADD[2:0]	CONFIG1	CONFIG0
000	CPV(0)	CPV(0)
001	CPV(0)	CPV(1)
010	CPV(0)	CPV(2)
011	CPV(0)	CPV(3)
100	CPV(1)	CPV(0)
101	CPV(1)	CPV(1)
110	CPV(1)	CPV(2)
111	CPV(1)	CPV(3)

TABLE 3-8: SMI ADDRESS CONFIGURATION WITH PAUSE=1

PHYADD[2:0]	CONFIG1	CONFIG0
000	CPV(2)	CPV(0)
001	CPV(2)	CPV(1)
010	CPV(2)	CPV(2)
011	CPV(2)	CPV(3)
100	CPV(3)	CPV(0)
101	CPV(3)	CPV(1)
110	CPV(3)	CPV(2)
111	CPV(3)	CPV(3)

3.8.1.2.2 Configuring the Mode of Operation (CONFIG[3:2])

This section describes the initial modes of operation that are available using the CONFIG[3:2] configuration pins. The user may configure additional modes using Software Configuration when the CONFIG[3:2] options do not include the desired mode.

The CONFIG3 pin is used to configure the values of the MOD field (19.15:11) The configuration pin values for CONFIG3 and CONFIG2 should be selected using Table 3-9. These tables also detail how the MOD field of the Extended Mode Control/Status Register will be configured.

Section 3.8.1.2.3 describes how the MOD field controls other configuration bits in the device. When a soft reset is issued via the PHY Soft Reset (RESET) bit of the Basic Control Register, configuration is controlled by the register bit values and the CONFIG[3:0] pins have no affect. Likewise, changing the MOD field of the Extended Mode Control/Status Register bits does not change the configuration of the device in this case.

Note: Table 3-9 utilizes register index and bit number referencing in lieu of individual names.

TABLE 3-9: CONFIGURING THE MODE OF OPERATION

Mode Definitions	CONFIG3	CONFIG2	Reg 19 [15:11]
10BASE-T Half Duplex. Auto-negotiation disabled.	CPV(2)	CPV(0)	00000
10BASE-T Full Duplex. Auto-negotiation disabled.	CPV(2)	CPV(1)	00001
100BASE-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.	CPV(2)	CPV(2)	00010
100BASE-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.	CPV(2)	CPV(3)	00011
All mode capable (10/100/1000). Auto-negotiation enabled. Auto master/slave resolution single port.	CPV(3)	CPV(0)	00111
10BASE-T/100BASE-TX capable. Auto-negotiation enabled.	CPV(3)	CPV(1)	00100
All mode capable (10/100/1000). Auto-negotiation enabled. Manual master/slave resolution slave port.	CPV(3)	CPV(2)	01001
All mode capable (10/100/1000). Auto-negotiation enabled. Manual master/slave resolution master port.	CPV(3)	CPV(3)	01010

3.8.1.2.3 Configuration Bits Impacted by the Mode of Operation

Immediately after a reset, the MOD field of the Extended Mode Control/Status Register will be set dependent on the configuration pin values of the CONFIG3 and CONFIG2 pins, as described in Section 3.8.1.2.2. Table 3-10 details how the MOD field effects other device configuration register bits.

Note: Table 3-10 utilizes register index and bit number referencing in lieu of individual names

