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LAN89730

High-Speed Inter-Chip (HSIC) USB 2.0 to 10/100 Ethernet Controller for Automotive Applications

Highlights

- Single Chip HSIC USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX Support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated HSIC Interface[1]
- Implements Reduced Power Operating Modes

Target Applications

- Diagnostic Interface (for Dealership Service Bay)
- Fast Software Download Interface (e.g., OBD Connector)
- Gateway Service Interface (Dealership, Aftermarket Repair Shop)
- In-vehicle Engineering Development Interface
- Vehicle Manufacturing Test Interface (Production Plant Assembly Line)
- Legislated Inspections (Emissions Check, Safety Inspections)

Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification, revision 2.0
  - Supports HS (480 Mbps) mode
  - Four Endpoints supported
  - Supports vendor specific commands
  - Integrated HSIC Interface
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE 802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for three status LEDs
- Power and I/Os
  - Various low power modes
  - Supports PCI-like PME wake when USB host disabled
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3 V I/O supply
    - Optional internal core regulator
- Miscellaneous Features
  - EEPROM controller
  - Supports custom operation without EEPROM
  - IEEE 1149.1 (JTAG) boundary scan
  - Requires single 25 MHz crystal
- Software
  - Windows® 8/7/XP/Vista driver
  - Linux® driver
  - Win CE driver
  - MAC® OS driver
  - EEPROM utility
- Packaging
  - 56-pin VQFN (8 x 8 mm), RoHS-compliant
- Environmental
  - -40°C to +85°C temperature range

1. Compliant to HSIC ECN as of May 2010

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NOTES:

1.0 INTRODUCTION

1.1 General Terms

Byte	8 bits
CSR	Control and Status Registers
DWORD	32 bits
FCT	FIFO Controller
FIFO	First In First Out buffer
Frame	In the context of this document, a frame refers to transfers on the Ethernet interface.
FSM	Finite State Machine
GPIO	General Purpose I/O
HSIC	High-Speed Inter-Chip
Host	External system (includes processor, application software, etc.)
Level-Triggered Sticky Bit	This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero.
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MII	Media Independent Interface
N/A	Not Applicable
Packet	In the context of this document, a packet refers to transfers on the USB interface.
POR	Power on Reset
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not ensured when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SCSR	System Control and Status Register
SMI	Serial Management Interface
TLI	Transaction Layer Interface
URX	USB Bulk-Out Packet Receiver
UTX	USB Bulk-In Packet Transmitter
WORD	16 bits
ZLP	Zero Length USB Packet

1.2 Block Diagram

FIGURE 1-1: BLOCK DIAGRAM

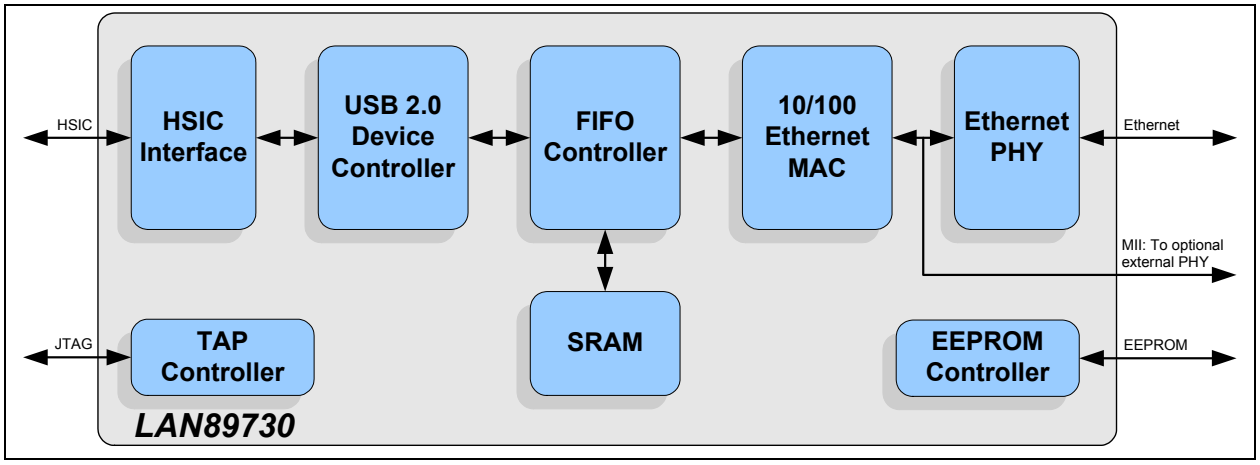
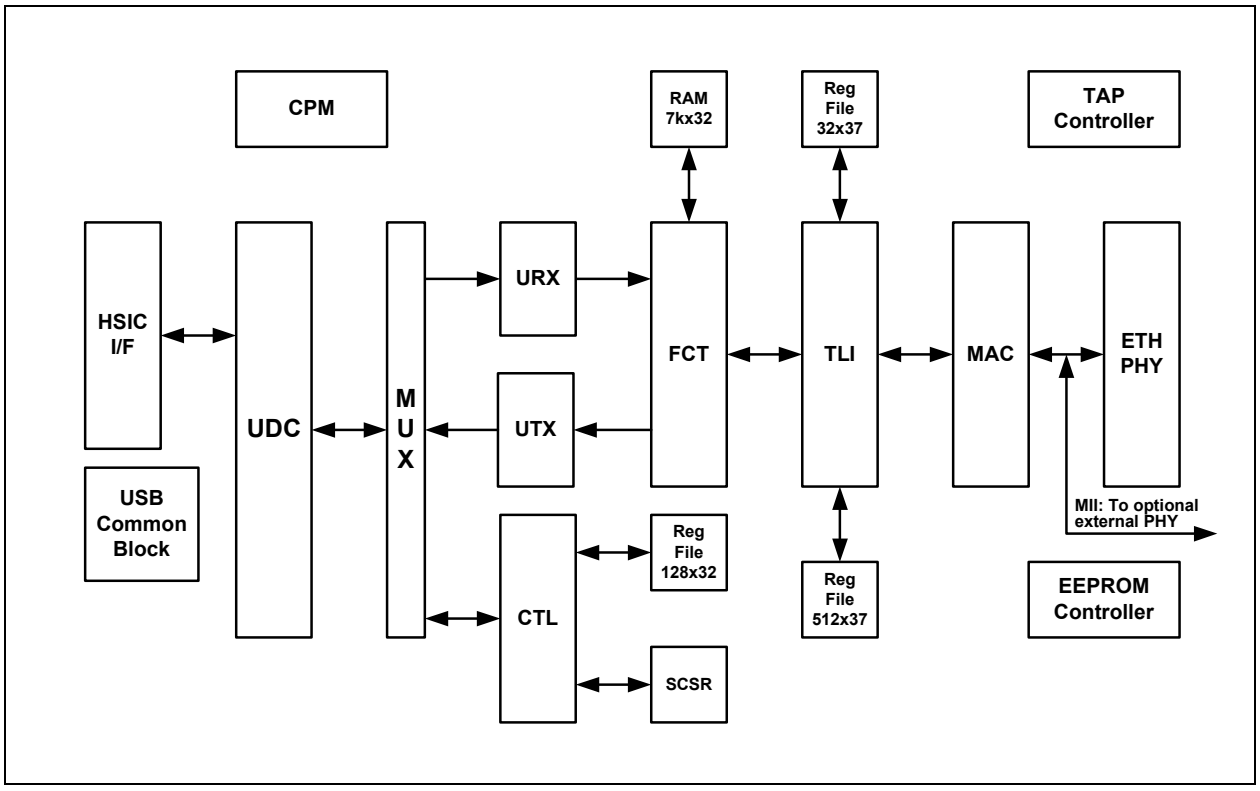


FIGURE 1-2: SYSTEM DIAGRAM



1.2.1 OVERVIEW

The LAN89730 is a high performance solution for USB to 10/100 Ethernet port bridging. With automotive applications ranging from diagnostics, fast software download, gateway services, in-vehicle engineering development, manufacturing test and legislated inspection interfaces, the device is targeted as a high-performance, low-cost USB/Ethernet connectivity solution.

The LAN89730 contains an integrated 10/100 Ethernet PHY, HSIC interface, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 kB of internal packet buffering. Two kB of buffer memory are allocated to the Transaction Layer Interface (TLI), while 28 kB are allocated to the FIFO Controller (FCT).

The internal USB 2.0 device controller is compliant with the USB 2.0 Hi-Speed standard. The HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0. High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The device implements Control, Interrupt, Bulk-In and Bulk-Out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY functionality.

Multiple power management features are provided, including various low-power modes, and Magic Packet, Wake On LAN and Link Status Change wake events. These wake events can be programmed to initiate a USB remote wakeup. A PCI-like PME wake is also supported when the host controller is disabled.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

1.2.2 USB

The USB portion of the LAN89730 consists of the USB Device Controller (UDC), USB Bulk-Out Packet Receiver (URX), USB Bulk-In Packet Transmitter (UTX), Control Block (CTL), System Control and Status Registers (SCSR), and HSIC interface.

The USB device controller (UDC) contains a USB low-level protocol interpreter which implements the USB bus protocol, packet generation/extraction, PID/Device ID parsing, and CRC coding/decoding with autonomous error handling. It has autonomous protocol handling functions such as stall condition clearing on setup packets, suspend/resume/reset conditions, and remote wakeup. It also autonomously handles contingency operations for error conditions such as retry for CRC errors, Data toggle errors, and generation of NYET, STALL, ACK, and NACK depending on the Endpoint buffer status. The UDC implements four USB Endpoints: Control, Interrupt, Bulk-In, and Bulk-Out.

The Control block (CTL) manages traffic to/from the control Endpoint that is not handled by the UDC and constructs the packets used by the interrupt Endpoint. The CTL is responsible for handling some USB standard commands and all vendor specific commands. The vendor specific commands allow for efficient statistics collection and access to the SCSR.

The URX and UTX implement the Bulk-Out and Bulk-In pipes, respectively, which connect the USB host and the UDC. They perform the following functions:

The URX passes USB Bulk-Out packets to the FIFO Controller (FCT). It tracks whether or not a USB packet is erroneous. It instructs the FCT to flush erroneous packets by rewinding its write pointer.

The UTX retrieves Ethernet frames from the FCT and constructs USB Bulk-In packets from them. If the handshake for a transmitted Bulk-In packet does not complete, the UTX is capable of retransmitting the packet. The UTX will not instruct the FCT to advance its read head pointer until the current USB packet has been successfully transmitted to the USB host.

Both the URX and UTX are responsible for handling Ethernet frames encapsulated over USB by one of the following methods:

- Multiple Ethernet frames per USB Bulk packet
- Single Ethernet frame per USB Bulk packet

The UDC also implements the System Control and Status Register (SCSR) space used by the host to obtain status and control overall system operation.

The integrated HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0 (09-23-07) and supports the Hi-Speed mode of operation.

1.2.3 FIFO CONTROLLER (FCT)

The FIFO controller uses a 28 kB internal SRAM to buffer RX and TX traffic. 20 kB are allocated for received Ethernet-USB traffic (RX buffer), while 8 kB are allocated for USB-Ethernet traffic (TX buffer). Bulk-Out packets from the USB controller are directly stored into the TX buffer. The FCT is responsible for extracting Ethernet frames from the USB packet data and passing the frames to the MAC. Ethernet frames are directly stored into the RX buffer and become the basis for Bulk-In packets. The FCT passes the stored data to the UTX in blocks typically 512 bytes in size.

1.2.4 ETHERNET

LAN89730 integrates an IEEE 802.3 PHY for twisted pair Ethernet applications and a 10/100 Ethernet Media Access Controller (MAC).

The PHY can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either full- or half-duplex configurations. The PHY block includes auto-negotiation, auto-polarity correction, and Auto-MDIX. Minimal external components are required for the utilization of the integrated PHY.

Optionally, an external PHY may be used via the MII (Media Independent Interface) port, effectively bypassing the internal PHY.

The transmit and receive data paths within the 10/100 Ethernet MAC are independent, allowing for the highest performance possible, particularly in full-duplex mode. The Ethernet MAC operates in store and forward mode, utilizing an independent 2 kB buffer for transmitted frames, and a smaller 128 byte buffer for received frames. The Ethernet MAC data paths connect to the FIFO controller. The MAC also implements a Control and Status Register (CSR) space used by the host to obtain status and control its operation.

The Ethernet MAC/PHY supports numerous power management wakeup features, including Magic Packet, Wake on LAN, and Link Status Change. Eight Wakeup Frame Filters are provided by the device.

1.2.5 POWER MANAGEMENT

The LAN89730 features four variations of USB suspend: SUSPEND0, SUSPEND1, SUSPEND2, and SUSPEND3. These modes allow the application to select the ideal balance of remote wakeup functionality and power consumption.

- **SUSPEND0:** Supports GPIO, Wake On LAN and Magic Packet events. This state reduces power by stopping the clocks of the MAC and other internal modules.
- **SUSPEND1:** Supports GPIO and Link Status Change for remote wakeup events. This suspend state consumes less power than SUSPEND0.
- **SUSPEND2:** Supports only GPIO assertion for a remote wakeup event. This is the default suspend mode for the device.
- **SUSPEND3:** Supports GPIO and Good Packet events. A Good Packet is a received frame passing certain filtering constraints independent of those imposed on Wake On LAN and Magic Packet frames. This SUSPEND state consumes power at a level similar to the full operational state, however, it allows for power savings in the host CPU.

Refer to Section 4.12, "Wake Events" for more information on the USB suspend states and the wake events supported in each state.

1.2.6 EEPROM CONTROLLER (EPC)

LAN89730 contains an EEPROM controller for connection to an external EEPROM. This allows for the automatic loading of static configuration data upon Power on Reset, pin reset or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and MAC address.

1.2.7 GENERAL PURPOSE I/O

When configured for Internal PHY mode, up to eleven GPIOs are supported. All GPIOs can serve as remote wakeup events when the LAN89730 is suspended.

1.2.8 TAP CONTROLLER

IEEE 1149.1 compliant TAP Controller supports boundary scan and various test modes.

The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of five pins (TDO, TDI, TCK, TMS, and nTRST) and includes a state machine, data register array and an instruction register. The JTAG pins are described in Table 2-3, “JTAG Pins”. The JTAG interface conforms to the IEEE Standard 1149.1 - *1990 Standard Test Access Port (TAP) and Boundary-Scan Architecture*.

All input and output data is synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.

The JTAG logic is reset via Power on Reset (POR) or when the nTRST pin is asserted active-low.

The implemented IEEE 1149.1 instructions and their op codes are shown in Table 1-1.

TABLE 1-1: IEEE 1149.1 OP CODES

Instruction	Op Code	Comment
Bypass	111111b	Mandatory Instruction
Sample/Preload	000100b	Mandatory Instruction
EXTEST	000001b	Mandatory Instruction
HIGHZ	000011b	Optional Instruction
IDCODE	001010b	Optional Instruction

Note: The JTAG device ID is 0001445h.

Note: All digital I/O pins support IEEE 1149.1 operation. Analog pins and the XI/XO pins do not support IEEE 1149.1 operation.

1.2.9 CONTROL AND STATUS REGISTERS (CSR)

LAN89730’s functions are controlled and monitored by the host via the Control and Status Registers (CSRs). This register space includes registers that control and monitor the USB controller, as well as elements of overall system operation (System Control and Status Registers - SCSRs), the MAC (MAC Control and Status Registers - MCSRs), and the PHY (accessed indirectly through the MAC via the MII_ACCESS and MII_DATA registers). The CSR may be accessed via the USB Vendor Commands (REGISTER READ/REGISTER WRITE). Refer to Section 4.3.3, "USB Vendor Commands" for more information.

1.2.10 RESETS

LAN89730 supports the following system reset events:

- Power on Reset (POR)
- Hardware Reset Input Pin Reset (nRESET)
- Lite Reset (LRST) (Does not affect the UDC)
- Software Reset (SRST)
- USB Reset

The device supports the following module level reset events:

- Ethernet PHY Software Reset (PHY_RST)
- nTRST Pin Reset for Tap Controller

1.2.11 TEST FEATURES

Read/write access to internal SRAMs is provided via the CSRs. JTAG-based USB BIST is available. Full internal scan and At Speed scan are supported.

1.2.12 SYSTEM SOFTWARE

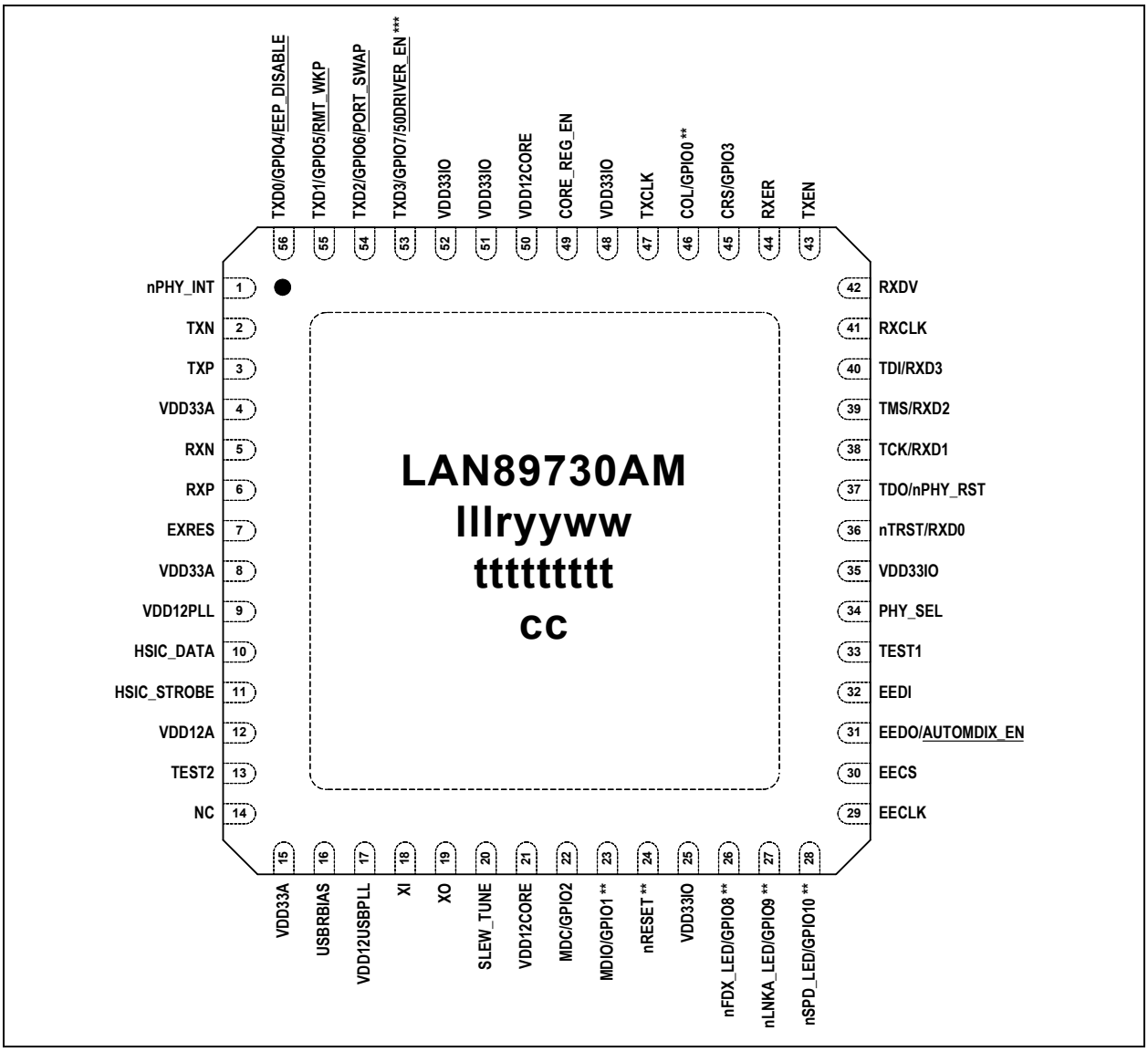
LAN89730 software drivers are available for the following operating systems:

- Windows 8
- Windows 7
- Windows Vista
- Windows XP
- Linux
- Win CE
- MAC OS

In addition, an EEPROM programming utility is available for configuring the external EEPROM.

2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: PIN ASSIGNMENTS (TOP VIEW)



The package designators are:

- lll - Lot sequence code (optional)
- r - Chip revision number
- yy - Last two digits of assembly year
- ww - Assembly work week
- ttttttttttt - Tracking number (up to 9 characters)
- cc - Country of original abbreviation (optional - up to 2 characters)

Note: ** This pin provides additional PME related functionality. Refer to the respective pin descriptions and Chapter 5.0, "PME Operation" for additional information.

Note: *** GPIO7 may provide additional PHY Link Up related functionality. Refer to Section 4.12.2.4, "Enabling External PHY Link Up Wake Events" for additional information.

Note: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa.

Note: Exposed pad (VSS) on bottom of package must be connected to ground.

TABLE 2-1: MII INTERFACE PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Receive Error (Internal PHY Mode)	RXER	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Receive Error (External PHY Mode)	RXER	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a receive error in the packet.
1	Transmit Enable (Internal PHY Mode)	TXEN	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Enable (External PHY Mode)	TXEN	O8 (PD)	In External PHY Mode, this pin functions as an output to the external PHY and indicates valid data on TXD[3:0].
1	Receive Data Valid (Internal PHY Mode)	RXDV	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Receive Data Valid (External PHY Mode)	RXDV	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates valid data on RXD[3:0].
1	Receive Clock (Internal PHY Mode)	RXCLK	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Receive Clock (External PHY Mode)	RXCLK	IS (PD)	In External PHY Mode, this pin is the receiver clock input from the external PHY.
1	Transmit Clock (Internal PHY Mode)	TXCLK	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Clock (External PHY Mode)	TXCLK	IS (PU)	In External PHY Mode, this pin is the transmitter clock input from the external PHY.

TABLE 2-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Carrier Sense (Internal PHY Mode)	CRS	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Carrier Sense (External PHY Mode)	CRS	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a network carrier.
	General Purpose I/O 3 (Internal PHY Mode Only)	GPIO3	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
1	MII Collision Detect (Internal PHY Mode)	COL	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	MII Collision Detect (External PHY Mode)	COL	IS (PD)	In External PHY Mode, the signal on this pin is input from the external PHY and indicates a collision event.
	General Purpose I/O 0 (Internal PHY Mode Only)	GPIO0	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may be used to signal PME when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5.0, "PME Operation" for additional information.
1	Management Data (Internal PHY Mode)	MDIO	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Management Data (External PHY Mode)	MDIO	IS/O8 (PD)	In External PHY Mode, this pin provides the management data to/from the external PHY.
	General Purpose I/O 1 (Internal PHY Mode Only)	GPIO1	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as the PME_MODE_SEL input when Internal PHY and PME Modes of operation are in effect. Refer to Chapter 5.0, "PME Operation" for additional information.

TABLE 2-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Management Clock (Internal PHY Mode)	MDC	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Management Clock (External PHY Mode)	MDC	O8 (PD)	In External PHY Mode, this pin outputs the management clock to the external PHY.
	General Purpose I/O 2 (Internal PHY Mode Only)	GPIO2	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
1	Transmit Data 3 (Internal PHY Mode)	TXD3	IS/O8 (PU)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Data 3 (External PHY Mode)	TXD3	O8 (PU)	In External PHY Mode, this pin functions as the transmit data 3 output to the external PHY.
	General Purpose I/O 7 (Internal PHY Mode Only)	GPIO7	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** GPIO7 may provide additional external PHY Link Up related functionality. Refer to Section 4.12.2.4, "Enabling External PHY Link Up Wake Events" for additional information.
	HSIC Output Impedance Configuration Strap	50DRIVER_EN	IS (PU)	The 50DRIVER_EN strap selects the driver output impedance for the HSIC_DATA and HSIC_STROBE pins. 0 = 40 Ω output impedance 1 = 50 Ω output impedance See Note 2-1 for more information on configuration straps.

TABLE 2-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 2 (Internal PHY Mode)	TXD2	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Data 2 (External PHY Mode)	TXD2	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 2 output to the external PHY.
	General Purpose I/O 6 (Internal PHY Mode Only)	GPIO6	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input.
	HSIC Port Swap Configuration Strap	PORT_SWAP	IS (PD)	Swaps the mapping of HSIC_DATA and HSIC_STROBE. 0 = The HSIC_DATA and HSIC_STROBE pin functionality is not swapped. 1 = The HSIC_DATA and HSIC_STROBE pin functionality is swapped. See Note 2-1 for more information on configuration straps.
1	Transmit Data 1 (Internal PHY Mode)	TXD1	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Data 1 (External PHY Mode)	TXD1	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 1 output to the external PHY.
	General Purpose I/O 5 (Internal PHY Mode Only)	GPIO5	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
	Remote Wakeup Configuration Strap	RMT_WKP	IS (PD)	This strap configures the default descriptor values to support remote wakeup. This strap is overridden by the EEPROM. 0 = Remote wakeup is not supported. 1 = Remote wakeup is supported. See Note 2-1 for more information on configuration straps.

TABLE 2-1: MII INTERFACE PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Transmit Data 0 (Internal PHY Mode)	TXD0	IS/O8 (PD)	In Internal PHY Mode, this pin can be configured to display the respective internal MII signal. Refer to the Internal MII Visibility Enable (IME) bit of the Hardware Configuration Register (HW_CFG) on page 123 for additional information.
	Transmit Data 0 (External PHY Mode)	TXD0	O8 (PD)	In External PHY Mode, this pin functions as the transmit data 0 output to the external PHY.
	General Purpose I/O 4 (Internal PHY Mode Only)	GPIO4	IS/O8/ OD8 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input.
	EEPROM Disable Configuration Strap	EEP_DISABLE	IS (PD)	This strap disables the autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM. 0 = EEPROM is recognized if present. 1 = EEPROM is not recognized even if it is present. See Note 2-1 for more information on configuration straps.

TABLE 2-2: EEPROM PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	EEPROM Data In	EEDI	IS (PD)	This pin is driven by the EEDO output of the external EEPROM.
1	EEPROM Data Out	EEDO	O8 (PU)	This pin drives the EEDI input of the external EEPROM.
	Auto-MDIX Enable Configuration Strap	AUTOMDIX_EN	IS (PU)	Determines the default Auto-MDIX setting. 0 = Auto-MDIX is disabled. 1 = Auto-MDIX is enabled. See Note 2-1 for more information on configuration straps.
1	EEPROM Chip Select	EECS	O8	This pin drives the chip select output of the external EEPROM. **Note:** The EECS output may tri-state briefly during power-up. Some EEPROM devices may be prone to false selection during this time. When an EEPROM is used, an external pull-down resistor is recommended on this signal to prevent false selection. Refer to your EEPROM manufacturer's datasheet for additional information.
1	EEPROM Clock	EECLK	O8 (PD)	This pin drives the EEPROM clock of the external EEPROM. **Note:** This pin must be pulled-up externally for proper operation.

Note 2-1 Configuration strap values are latched on Power on Reset (POR) or External Chip Reset (nRESET). Configuration straps are identified by an underlined symbol name. Pins that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 4.14, "Configuration Straps" for additional information.

TABLE 2-3: JTAG PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	JTAG Test Port Reset (Internal PHY Mode)	nTRST	IS (PU)	In Internal PHY Mode, this active-low pin functions as the JTAG test port reset input.
	Receive Data 0 (External PHY Mode)	RXD0	IS (PD)	In External PHY Mode, this pin functions as the receive data 0 input from the external PHY.
1	JTAG Test Data Out (Internal PHY Mode)	TDO	O8	In Internal PHY Mode, this pin functions as the JTAG data output.
	PHY Reset (External PHY Mode)	nPHY_RST	O8	In External PHY Mode, this active-low pin functions as the PHY reset output.
1	JTAG Test Clock (Internal PHY Mode)	TCK	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG test clock. The maximum operating frequency of this clock is 25 MHz.
	Receive Data 1 (External PHY Mode)	RXD1	IS (PD)	In External PHY Mode, this pin functions as the receive data 1 input from the external PHY.
1	JTAG Test Mode Select (Internal PHY Mode)	TMS	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG test mode select.
	Receive Data 2 (External PHY Mode)	RXD2	IS (PD)	In External PHY Mode, this pin functions as the receive data 2 input from the external PHY.
1	JTAG Test Data Input (Internal PHY Mode)	TDI	IS (PU)	In Internal PHY Mode, this pin functions as the JTAG data input.
	Receive Data 3 (External PHY Mode)	RXD3	IS (PD)	In External PHY Mode, this pin functions as the receive data 3 input from the external PHY.

TABLE 2-4: MISCELLANEOUS PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	PHY Select	PHY_SEL	IS (PD)	Selects whether to use the internal Ethernet PHY or the external PHY connected to the MII port. 0 = Internal PHY is used. 1 = External PHY is used. **Note:** When in External PHY Mode, the internal PHY is placed into general power down after a POR. Refer to Section 4.6, "10/100 Internal Ethernet PHY" for details.
1	System Reset	nRESET	IS (PU)	This active-low pin allows external hardware to reset the device. **Note:** This pin may be used to signal PME_CLEAR when PME Mode of operation is in effect. Refer to Chapter 5.0, "PME Operation" for additional information.
1	Ethernet Full-Duplex Indicator LED	nFDX_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet link is operating in Full-Duplex mode.
	General Purpose I/O 8	GPIO8	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may be used to signal PME when External PHY and PME Modes of operation are in effect. Refer to Chapter 5.0, "PME Operation" for additional information. **Note:** By default this pin is configured as a GPIO.

TABLE 2-4: MISCELLANEOUS PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Ethernet Link Activity Indicator LED	nLNKA_LED	OD12 (PU)	This pin is driven low (LED on) when a valid link is detected. This pin is pulsed high (LED off) for 80 ms whenever transmit or receive activity is detected. This pin is then driven low again for a minimum of 80 ms, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed, LED2 will function as an activity indicator.
	General Purpose I/O 9	GPIO9	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as the PME_MODE_SEL input when External PHY and PME Modes of operation are in effect. Refer to Chapter 5.0, "PME Operation" for additional information. **Note:** By default this pin is configured as a GPIO.
1	Ethernet Speed Indicator LED	nSPD_LED	OD12 (PU)	This pin is driven low (LED on) when the Ethernet operating speed is 100 Mbs, or during auto-negotiation. This pin is driven high during 10 Mbs operation or during line isolation.
	General Purpose I/O 10	GPIO10	IS/O12/ OD12 (PU)	This General Purpose I/O pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input. **Note:** This pin may serve as a wakeup pin whose detection mode is selectable when External PHY and PME Modes of operation are in effect. Refer to Chapter 5.0, "PME Operation" for additional information. **Note:** By default this pin is configured as a GPIO.
1	Core Regulator Enable	CORE_REG_EN	AI	This pin enables/disables the internal core logic voltage regulator. When tied low to VSS, the internal core regulator is disabled and +1.2 V must be supplied to the device by an external source. When tied high to +3.3 V, the internal core regulator is enabled. Refer to Chapter 3.0, "Power Connections" and the device reference schematics for connection information.
1	Test 1	TEST1	-	This pin must always be connected to VSS for proper operation.

TABLE 2-4: MISCELLANEOUS PINS (CONTINUED)

Num Pins	Name	Symbol	Buffer Type	Description
1	Test 2	TEST2	-	This pin must always be connected to +3.3 V for proper operation.
1	Crystal Input	XI	ICLK	External 25 MHz crystal input. **Note:** This pin can also be driven by a single-ended clock oscillator. When this method is used, XO should be left unconnected.
1	Crystal Output	XO	OCLK	External 25 MHz crystal output.

TABLE 2-5: USB PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	HSIC Data	HSIC_DATA	HSIC	Bi-directional Double Data Rate (DDR) data signal that is synchronous to the HSIC_STROBE signal as defined in the *High-Speed Inter-Chip USB Electrical Specification, Version 1.0*.
1	HSIC Strobe	HSIC_STROBE	HSIC	Bi-directional data strobe signal as defined in the *High-Speed Inter-Chip USB Electrical Specification, Version 1.0*.
1	HSIC Slew Tune	SLEW_TUNE	IS (PD)	Applies a 30% slew rate boost to the HSIC_DATA and HSIC_STROBE pins when driven high.
1	External USB Bias Resistor	USBRBIAS	AI	Used for setting HS transmit current level and on-chip termination impedance. Connect to an external 12.0 kΩ 1.0% resistor to ground.

TABLE 2-6: ETHERNET PHY PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	Ethernet TX Data Out Negative	TXN	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet TX Data Out Positive	TXP	AIO	The transmit data outputs may be swapped internally with receive data inputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Negative	RXN	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	Ethernet RX Data In Positive	RXP	AIO	The receive data inputs may be swapped internally with transmit data outputs when Auto-MDIX is enabled.
1	PHY Interrupt (Internal PHY Mode)	nPHY_INT	O8	In Internal PHY Mode, this pin can be configured to output the internal PHY interrupt signal. **Note:** The internal PHY interrupt signal is active-high.
	PHY Interrupt (External PHY Mode)	nPHY_INT	IS (PU)	In External PHY Mode, the active-low signal on this pin is input from the external PHY and indicates a PHY interrupt has occurred.
1	External PHY Bias Resistor	EXRES	AI	Used for the internal bias circuits. Connect to an external 12.0 kΩ 1.0% resistor to ground.

TABLE 2-7: POWER PINS AND GROUND PAD

Num Pins	Name	Symbol	Buffer Type	Description
5	+3.3 V I/O Power	VDD33IO	P	Refer to Chapter 3.0, "Power Connections" and the device reference schematics for connection information.
3	+3.3 V Analog Power	VDD33A	P	Refer to Chapter 3.0, "Power Connections" and the device reference schematics for connection information.
2	+1.2 V Digital Core Power	VDD12CORE	P	Refer to Chapter 3.0, "Power Connections" and the device reference schematics for connection information.
1	+1.2 V USB PLL Power	VDD12USBPLL	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3.0, "Power Connections" and the device reference schematics for additional connection information.
1	+1.2 V HSIC Power	VDD12A	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3.0, "Power Connections" and the device reference schematics for connection information.
1	+1.2 V Ethernet PLL Power	VDD12PLL	P	This pin must be connected to VDD12CORE for proper operation. Refer to Chapter 3.0, "Power Connections" and the device reference schematics for additional connection information.
Exposed pad on package bottom	Ground	VSS	P	Common Ground

TABLE 2-8: NO-CONNECT PINS

Num Pins	Name	Symbol	Buffer Type	Description
1	No Connect	NC	-	This pin must be left floating for normal device operation.

2.1 Pin Assignments

TABLE 2-9: 56-VQFN PACKAGE PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	nPHY_INT	15	VDD33A	29	EECLK	43	TXEN
2	TXN	16	USBRBIAS	30	EECS	44	RXER
3	TXP	17	VDD12USBPLL	31	EEDO/ AUTOMDIX_EN	45	CRS/GPIO3
4	VDD33A	18	XI	32	EEDI	46	COL/GPIO0 Note 2-2
5	RXN	19	XO	33	TEST1	47	TXCLK
6	RXP	20	SLEW_TUNE	34	PHY_SEL	48	VDD33IO
7	EXRES	21	VDD12CORE	35	VDD33IO	49	CORE_REG_EN
8	VDD33A	22	MDC/GPIO2	36	nTRST/RXD0	50	VDD12CORE
9	VDD12PLL	23	MDIO/GPIO1 Note 2-2	37	TDO/nPHY_RST	51	VDD33IO
10	HSIC_DATA	24	nRESET Note 2-2	38	TCK/RXD1	52	VDD33IO
11	HSIC_STROBE	25	VDD33IO	39	TMS/RXD2	53	TXD3/GPIO7/ 50DRIVER_EN
12	VDD12A	26	nFDX_LED/ GPIO8	40	TDI/RXD3	54	TXD2/GPIO6/ PORT_SWAP
13	TEST2	27	nLNKA_LED/ GPIO9 Note 2-2	41	RXCLK	55	TXD1/GPIO5/ RMT_WKP
14	NC	28	nSPD_LED/ GPIO10 Note 2-2	42	RXDV	56	TXD0/GPIO4/ EEP_DISABLE
EXPOSED PAD MUST BE CONNECTED TO VSS							

Note 2-2 This pin provides additional PME-related functionality. Refer to the respective pin descriptions and Chapter 5.0, "PME Operation" for additional information.

2.2 Buffer Types

TABLE 2-10: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
HSIC	*High-Speed Inter-Chip (HSIC) USB Electrical Specification, Version 1.0* compliant input/output
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AI	Analog input
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin