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LAN9118

High Performance Single-Chip 10/100 Non-PCI Ethernet Controller

Highlights

- Optimized for the highest data-rate applications such as high-definition video and multi-media applications
- Efficient architecture with low CPU overhead
- Easily interfaces to most 32-bit and 16-bit embedded CPU's
- Integrated PHY
- Supports audio & video streaming over Ethernet: multiple high-definition (HD) MPEG2 streams
- Pin compatible with other members of LAN9118 family (LAN9117, LAN9116 and LAN9115)

Target Applications

- Video distribution systems, multi-room PVR
- High-end Cable, satellite, and IP set-top boxes
- Digital video recorders
- High definition televisions
- Digital media clients/servers
- Home gateways

Key Benefits

- Supports highest performance applications
  - Highest performing non-PCI Ethernet controller in the market
  - 32-bit interface with fast bus cycle times
  - Burst-mode read support
- Eliminates dropped packets
  - Internal buffer memory can store over 200 packets
  - Supports automatic or host-triggered PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - Supports Slave-DMA
  - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
  - SRAM-like interface easily interfaces to most embedded CPU's or SoC's
  - Low-cost, low--pin count non-PCI interface for embedded designs
- Reduced Power Modes
  - Numerous power management modes
  - Wake on LAN*
  - Magic packet wakeup*
  - Wakeup indicator event signal
  - Link Status Change
- Single chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- Integrated Ethernet PHY
  - Auto-negotiation
  - Automatic polarity detection and correction
- High-Performance host bus interface
  - Simple, SRAM-like interface
  - 32/16-bit data bus
  - Large, 16Kbyte FIFO memory that can be allocated to RX or TX functions
  - One configurable host interrupt
- Miscellaneous features
  - Low profile 100-pin, TQFP RoHS Compliant package
  - Integral 1.8V regulator
  - General Purpose Timer
  - Support for optional EEPROM
  - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- 3.3V Power Supply with 5V tolerant I/O
- 0 to 70°C

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1.0 GENERAL DESCRIPTION

The LAN9118 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9118 has been specifically architected to provide the highest performance possible for any given architecture. The LAN9118 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant.

The LAN9118 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bit microprocessors and microcontrollers. The LAN9118 includes large transmit and receive data FIFOs with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9118 memory buffer architecture allows the most efficient use of memory resources by optimizing packet granularity.

Applications

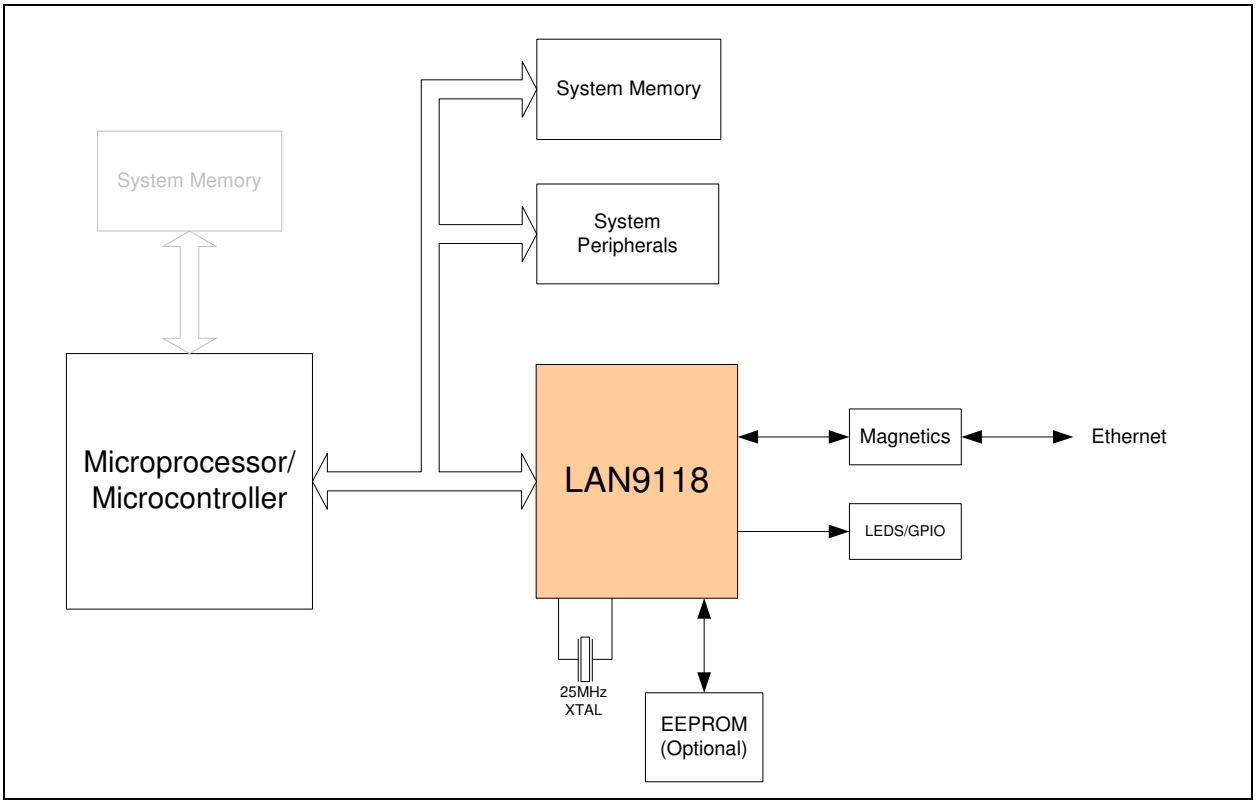
The LAN9118 is well suited for many high-performance embedded applications, including:

- High-end cable, satellite and IP set-top boxes
- Video distribution systems
- Multi-room PVR (Personal Video Recorder)
- Digital video recorders
- High-definition televisions
- Digital media clients/servers
- Home gateways

The LAN9118 also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9118 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9118 supports numerous power management and wakeup features. The LAN9118 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM UTILIZING THE MICROCHIP LAN9118



The Microchip LAN9118 integrated 10/100 MAC/PHY controller is a peripheral chip that performs the function of translating parallel data from a host controller into Ethernet packets. The LAN9118 Ethernet MAC/PHY controller is designed and optimized to function in an embedded environment. All communication is performed with programmed I/O transactions using the simple SRAM-like host interface bus.

The diagram shown above, describes a typical system configuration of the LAN9118 in a typical embedded environment.

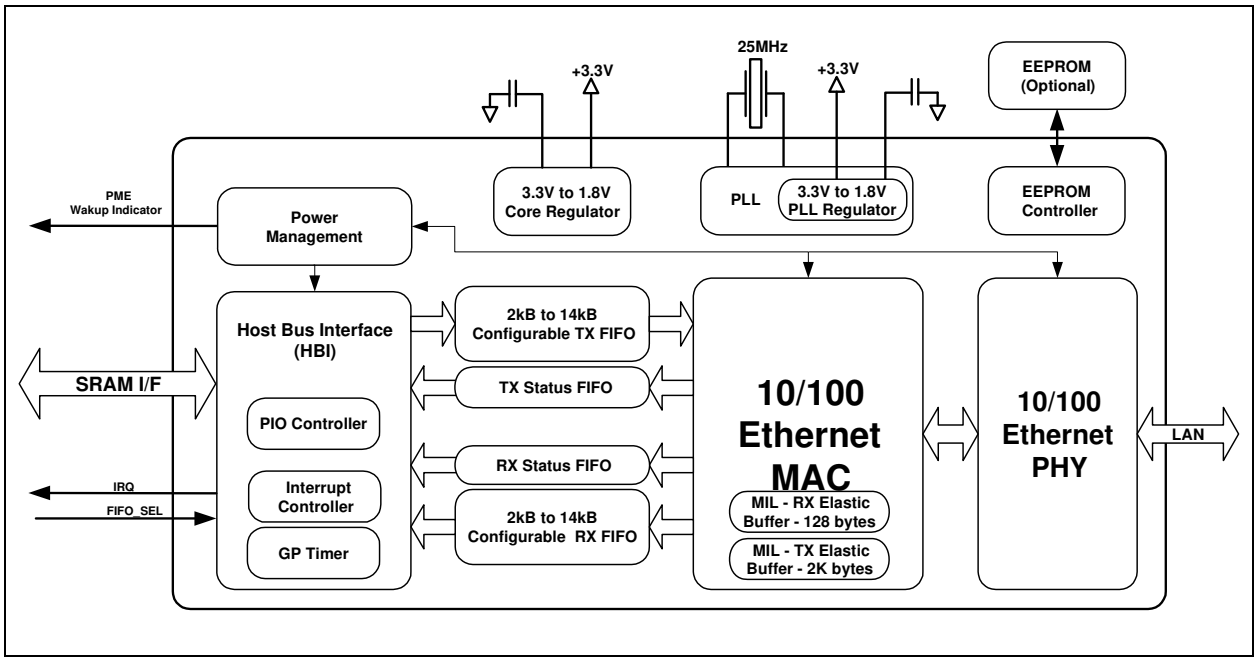
The LAN9118 is a general purpose, platform independent, Ethernet controller. The LAN9118 consists of four major functional blocks. The four blocks are:

- 10/100 Ethernet PHY
- 10/100 Ethernet MAC
- RX/TX FIFOs
- Host Bus Interface (HBI)

1.1 Internal Block Overview

This section provides an overview of each of these functional blocks as shown in Figure 1-2, "Internal Block Diagram".

FIGURE 1-2: INTERNAL BLOCK DIAGRAM



1.2 10/100 Ethernet PHY

The LAN9118 integrates an IEEE 802.3 physical layer for twisted pair Ethernet applications. The PHY can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation in either full or half duplex configurations. The PHY block includes auto-negotiation.

Minimal external components are required for the utilization of the Integrated PHY.

1.3 10/100 Ethernet MAC

The transmit and receive data paths are separate within the MAC allowing the highest performance especially in full duplex mode. The data paths connect to the PIO interface Function via separate busses to increase performance. Payload data as well as transmit and receive status is passed on these busses.

A third internal bus is used to access the MAC's Control and Status Registers (CSR's). This bus is accessible from the host through the PIO interface function.

On the backend, the MAC interfaces with the internal 10/100 PHY through a the MII (Media Independent Interface) port internal to the LAN9118. The MAC CSR's also provides a mechanism for accessing the PHY's internal registers through the internal SMI (Serial Management Interface) bus.

The MAC Interface Layer (MIL), within the MAC, contains a 2K Byte transmit and a 128 Byte receive FIFO which is separate from the TX and RX FIFOs. The FIFOs within the MAC are not directly accessible from the host interface. The differentiation between the TX/RX FIFO memory buffers and the MAC buffers is that when the transmit or receive packets are in the MAC buffers, the host no longer can control or access the TX or RX data. The MAC buffers (both TX and RX) are in effect the working buffers of the Ethernet MAC logic. In the case of reception, the data must be moved first to the RX FIFOs for the host to access the data. For TX operations, the MIL operates in store-and-forward mode and will queue an entire frame before beginning transmission.

1.4 Receive and Transmit FIFOs

The Receive and Transmit FIFOs allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the host interface and the MAC through which all transmitted and received data and status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks thus reducing or minimizing overrun conditions. Like the MAC, the FIFOs have separate receive and transmit data paths. In addition, the RX and TX FIFOs are configurable in size, allowing increased flexibility.

1.5 Interrupt Controller

The LAN9118 supports a single programmable interrupt. The programmable nature of this interrupt allows the user the ability to optimize performance dependent upon the application requirement. Both the polarity and buffer type of the interrupt pin are configurable for the external interrupt processing. The interrupt line can be configured as an open-drain output to facilitate the sharing of interrupts with other devices. In addition, a programmable interrupt de-assertion interval is provided.

1.6 GPIO Interface

A 3-bit GPIO and 2-bit GPO (Multiplexed on the EEPROM and LED Pins) interface is included in the LAN9118. It is accessible through the host bus interface via the CSRs. The GPIO signals can function as inputs, push-pull outputs and open drain outputs. The GPIO's (GPO's are not configurable) can also be configured to trigger interrupts with programmable polarity.

1.7 Serial EEPROM Interface

A serial EEPROM interface is included in the LAN9118. The serial EEPROM is optional and can be programmed with the LAN9118 MAC address. The LAN9118 can optionally load the MAC address automatically after power-on.

1.8 Power Management Controls

The LAN9118 supports comprehensive array of power management modes to allow use in power sensitive applications. Wake on LAN, Link Status Change and Magic Packet detection are supported by the LAN9118. An external PME (Power Management Event) interrupt is provided to indicate detection of a wakeup event.

1.9 General Purpose Timer

The general-purpose timer has no dedicated function within the LAN9118 and may be programmed to issue a timed interrupt.

1.10 Host Bus Interface (SRAM Interface)

The host bus interface provides a FIFO interface for the transmit and receive data paths, as well as an interface for the LAN9118 Control and Status Registers (CSR's).

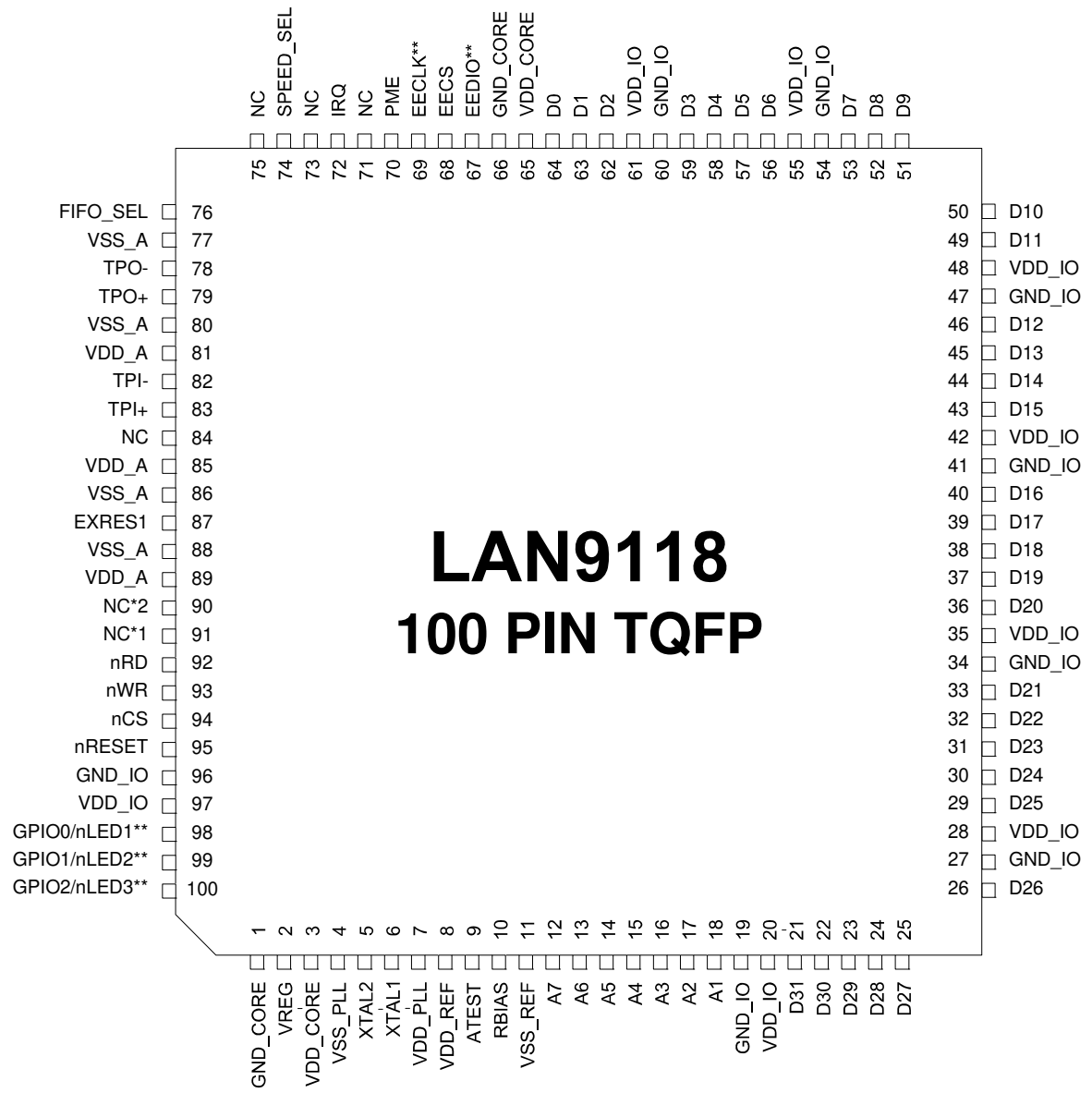
The host bus interface is the primary bus for connection to the embedded host system. This interface models an asynchronous SRAM. TX FIFO, RX FIFO, and CSR's are accessed through this interface. Programmed I/O transactions are supported.

The LAN9118 host bus interface supports 32-bit and 16-bit bus transfers; internally, all data paths are 32-bits wide. The LAN9118 can be interfaced to either Big-Endian or Little-Endian processors in either 32-bit or 16-bit external bus width modes of operation.

The host bus data Interface is responsible for host address decoding and data bus steering. The host bus interface handles the 16 to 32-bit conversion when the LAN9118 is configured with a 16-bit host interface. Additionally, when Big Endian mode is selected, the data path to the internal controller registers will be reorganized accordingly.

2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: PIN CONFIGURATION



**Denotes a multifunction pin

*1 This NC pin can also be tied to VDD_A for backward compatibility

*2 This NC pin can also be tied to VSS_A for backward compatibility

TABLE 2-1: HOST BUS INTERFACE SIGNALS

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
21-26,29-33,36-40	Host Data High	D[31:16]	I/O8 (PD)	16	Bi-directional data port. Note that Pull-down's are disabled in 32 bit mode.
43-46,49-53,56-59,62-64	Host Data Low	D[15:0]	I/O8	16	Bi-directional data port.
12-18	Host Address	A[7:1]	IS	7	7-bit Address Port. Used to select Internal CSR's and TX and RX FIFOs.
92	Read Strobe	nRD	IS	1	Active low strobe to indicate a read cycle.
93	Write Strobe	nWR	IS	1	Active low strobe to indicate a write cycle. This signal, qualified with nCS, is also used to wakeup the LAN9118 when it is in a reduced power state.
94	Chip Select	nCS	IS	1	Active low signal used to qualify read and write operations. This signal qualified with nWR is also used to wakeup the LAN9118 when it is in a reduced power state.
72	Interrupt Request	IRQ	O8/OD8	1	Programmable Interrupt request. Programmable polarity, source and buffer types.
76	FIFO Select	FIFO_SEL	IS	1	When driven high all accesses to the LAN9118 are to the RX or TX Data FIFOs. In this mode, the A[7:3] upper address inputs are ignored.

TABLE 2-2: DEFAULT ETHERNET SETTINGS

	Default Ethernet Settings		
SPEED_SEL	**Speed**	**Duplex**	**Auto Neg.**
0	**10MBPS**	**HALF-DUPLEX**	**DISABLED**
1	**100MBPS**	**HALF-DUPLEX**	**ENABLED**

TABLE 2-3: LAN INTERFACE SIGNALS

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
79	TXP	TPO+	AO	1	Twisted Pair Transmit Output, Positive
78	TXN	TPO-	AO	1	Twisted Pair Transmit Output, Negative
83	RXP	TPI+	AI	1	Twisted Pair Receive Input, Positive
82	RXN	TPI-	AI	1	Twisted Pair Receive Input, Negative
87	PHY External Bias Resistor	EXRES1	AI	1	Must be connected to ground through a 12.4K ohm 1% resistor.

TABLE 2-4: SERIAL EEPROM INTERFACE SIGNALS

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
67	EEPROM Data, GPO3, TX_EN, TX_CLK, D32/nD16	EEDIO/GPO3/ TX_EN/TX_CLK (D32/nD16)	I/O8	1	**EEPROM Data:** This bi-directional pin can be connected to a serial EEPROM DIO. This is optional. **General Purpose Output 3:** This pin can also function as a general purpose output, or it can be configured to monitor the TX_EN or TX_CLK signals on the internal MII port. When configured as a GPO signal, or as a TX_EN/TX_CLK monitor, the EECS pin is deasserted so as to never unintentionally access the serial EEPROM. This signal cannot function as a general-purpose input. **Data Bus Width Select:** This signal also functions as a configuration input on power-up and is used to select the host bus data width. Upon deassertion of reset, the value of the input is latched. When high, a 32-bit data bus is utilized. When low, a 16-bit interface is utilized.
68	EEPROM Chip Select	EECS	O8	1	Serial EEPROM chip select.
69	EEPROM Clock, GPO4 RX_DV, RX_CLK	EECLK/GPO4/ RX_DV/RX_CLK	O8	1	**EEPROM Clock:** Serial EEPROM Clock pin. **General Purpose Output 4:** This pin can also function as a general-purpose output, or it can be configured to monitor the RX_DV or RX_CLK signals on the internal MII port. When configured as a GPO signal, or as an RX_DV/RX_CLK monitor, the EECS pin is deasserted so as to never unintentionally access the serial EEPROM. This signal cannot function as a general-purpose input. **Note:** When the EEPROM interface is not used, the EECLK pin must be left unconnected.

TABLE 2-5: SYSTEM AND POWER SIGNALS

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
6	Crystal 1	XTAL1	Iclk	1	External 25MHz Crystal Input. Can also be connected to single-ended TTL oscillator. If this method is implemented, XTAL2 should be left unconnected.
5	Crystal 2	XTAL2	Oclk	1	External 25MHz Crystal output.

TABLE 2-5: SYSTEM AND POWER SIGNALS (CONTINUED)

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
95	Reset	nRESET	IS (PU)	1	Active-low reset input. Resets all logic and registers within the LAN9118 This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected, the LAN9118 will rely on its internal power-on reset circuitry **Note:** The LAN9118 must always be read at least once after power-up, reset, or upon return from a power-saving state or write operations will not function. See Section 3.11, "Detailed Reset Description," on page 31 for additional information
70	Wakeup Indicator	PME	O8/OD8	1	When programmed to do so, is asserted when the LAN9118 detects a wake event and is requesting the system to wake up from the associated sleep state. The polarity and buffer type of this signal is programmable. **Note:** Detection of a Power Management Event, and assertion of the PME signal will not wakeup the LAN9118. The LAN9118 will only wake up when it detects a host write cycle (assertion of nCS and nWR). Although any write to the LAN9118, regardless of the data written, will wake-up the device when it is in a power-saving mode, it is required that the BYTE_TEST register be used for this purpose.
71,73,75,84,90,91	Reserved	Reserved		5	No Connect
74	10/100 Selector	SPEED_SEL	I (PU)	1	This signal functions as a configuration input on power-up and is used to select the default Ethernet settings. Upon deassertion of reset, the value of the input is latched. This signal functions as shown in Table 2-2, "Default Ethernet Settings", below.

TABLE 2-5: SYSTEM AND POWER SIGNALS (CONTINUED)

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
100, 99, 98	General Purpose I/O data, nLED1 (Speed Indicator), nLED2 (Link & Activity Indicator), nLED3 (Full-Duplex Indicator).	GPIO[2:0]/ LED[3:1]	IS/O12/ OD12	3	**General Purpose I/O data:** These three general-purpose signals are fully programmable as either push-pull output, open-drain output or input by writing the GPIO_CFG configuration register in the CSR's. They are also multiplexed as GP LED connections. GPIO signals are Schmitt-triggered inputs. When configured as LED outputs these signals are open-drain. **nLED1 (Speed Indicator).** This signal is driven low when the operating speed is 100Mbs, during auto-negotiation and when the cable is disconnected. This signal is driven high only during 10Mbs operation. **nLED2 (Link & Activity Indicator).** This signal is driven low (LED on) when the LAN9118 detects a valid link. This signal is pulsed high (LED off) for 80mS whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed LED2 will flash as an activity indicator. **nLED3 (Full-Duplex Indicator).** This signal is driven low when the link is operating in full-duplex mode.
10	RBIAS	RBIAS	AI	1	**PLL Bias:** Connect to an external 12.0K ohm 1.0% resistor to ground. Used for the PLL Bias circuit.
9	Test Pin	ATEST	I	1	This pin must be connected to VDD for normal operation.
2	Internal Regulator Power	VREG	P	1	3.3V input for internal voltage regulator
20,28,35, 42,48,55,61,97	+3.3V I/O Power	VDD_IO	P	8	+3.3V I/O logic power supply pins
19,27,34,41,47, 54,60,96	I/O Ground	GND_IO	P	8	Ground for I/O pins
81,85,89	+3.3V Analog Power	VDD_A	P	3	+3.3V Analog power supply pins. See Note 2-1
77,80,86,88	Analog Ground	VSS_A	P	4	Ground for analog circuitry
3,65	Core Voltage Decoupling	VDD_CORE	P	2	1.8 V from internal core regulator. Both pins must be connected together externally and then tied to a 10uF 0.1-Ohm ESR capacitor, in parallel with a 0.01uF capacitor to Ground next to each pin. These pins must not be used to supply power to other external devices. See Note 2-1

TABLE 2-5: SYSTEM AND POWER SIGNALS (CONTINUED)

Pin No.	Name	Symbol	Buffer Type	# Pins	Description
1,66	Core Ground	GND_CORE	P	2	Ground for internal digital logic
7	PLL Power	VDD_PLL	P	1	1.8V Power from the internal PLL regulator. This external pin must be connected to a 10uF 0.1-Ohm ESR capacitor, in parallel with a 0.01uF capacitor to Ground. This pin must not be used to supply power to other external devices. See Note 2-1
4	PLL Ground	VSS_PLL	P	1	GND for the PLL
8	Reference Power	VDD_REF	P	1	Connected to 3.3v power and used as the reference voltage for the internal PLL
11	Reference Ground	VSS_REF	P	1	Ground for internal PLL reference voltage

Note 2-1 Please refer to the Microchip application note AN 12.5 titled “Designing with the LAN9118 - Getting Started”. It is also important to note that this application note applies to the whole Microchip LAN9118 family of Ethernet controllers. However, subtle differences may apply.

2.1 Buffer Types

TABLE 2-6: BUFFER TYPES

Type	Description
I	Input pin
IS	Schmitt triggered Input
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
IO8	I/O with 8mA symmetrical drive
OD8	Open-drain output with 8mA sink
O8	Output 8mA symmetrical drive
PU	50uA (typical) internal pull-up
PD	50uA (typical) internal pull-down
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin

3.0 FUNCTIONAL DESCRIPTION

3.1 10/100 Ethernet MAC

The Ethernet Media Access controller (MAC) incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the host subsystem and the internal Ethernet PHY. The MAC can operate in either 100-Mbps or 10-Mbps mode.

The MAC operates in both half-duplex and full-duplex modes. When operating in half-duplex mode, the MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the MAC complies with IEEE 802.3x full-duplex operation standard.

The MAC provides programmable enhanced features designed to minimize host supervision, bus utilization, and pre- or post-message processing. These features include the ability to disable retries after a collision, dynamic FCS (Frame Check Sequence) generation on a frame-by-frame basis, automatic pad field insertion and deletion to enforce minimum frame size attributes, and automatic retransmission and detection of collision frames.

The MAC can sustain transmission or reception of minimally-sized back-to-back packets at full line speed with an inter-packet gap (IPG) of 9.6 microseconds for 10 Mbps and 0.96 microseconds for 100 Mbps.

The primary attributes of the MAC Function are:

- Transmit and receive message data encapsulation
- Framing (frame boundary delimitation, frame synchronization)
- Error detection (physical medium transmission errors)
- Media access management
- Medium allocation (collision detection, except in full-duplex operation)
- Contention resolution (collision handling, except in full-duplex operation)
- Flow control during full-duplex mode
- Decoding of control frames (PAUSE command) and disabling the transmitter
- Generation of control frames
- Interface to the internal PHYI

The transmit and receive data paths are separate within the LAN9118 from the MAC to host interface allowing the highest performance, especially in full duplex mode. Payload data as well as transmit and receive status are passed on these busses.

A third internal bus is used to access the MAC's "Control and Status Registers" (CSR's). This bus is also accessible from the host.

On the backend, the MAC interfaces with the 10/100 PHY through an internal MII (Media Independent Interface) port, internal to the LAN9118. The MAC CSR's also provide a mechanism for accessing the PHY's internal registers through the internal SMI (Serial Management Interface) bus.

The receive and transmit FIFOs allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the host interface and the MAC through which all transmitted and received data and status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks reducing and minimizing overrun conditions. Like the MAC, the FIFOs have separate receive and transmit data paths.

The LAN9118 can store up to 250 Ethernet packets utilizing FIFOs, totaling 16K bytes, with a packet granularity of 4 bytes. This memory is shared by the RX and TX blocks and is configurable in terms of allocation. This depth of buffer storage minimizes or eliminates receive overruns.

3.2 Flow Control

The LAN9118 Ethernet MAC supports full-duplex flow control using the pause operation and control frame. It also supports half-duplex flow control using back pressure.

3.2.1 FULL-DUPLEX FLOW CONTROL

The pause operation inhibits data transmission of data frames for a specified period of time. A Pause operation consists of a frame containing the globally assigned multicast address (01-80-C2-00-00-01), the PAUSE opcode, and a parameter indicating the quantum of slot time (512 bit times) to inhibit data transmissions. The PAUSE parameter may range from 0 to 65,535 slot times. The Ethernet MAC logic, on receiving a frame with the reserved multicast address and PAUSE opcode, inhibits data frame transmissions for the length of time indicated. If a Pause request is received while a transmission is in progress, then the pause will take effect after the transmission is complete. Control frames are received and processed by the MAC and are passed on.

The MAC also transmits control frames (pause command) via both hardware and software control. The software driver requests the MAC to transmit a control frame and gives the value of the PAUSE time to be used in the control frame. The MAC Function constructs a control frame with the appropriate values set in all the different fields (as defined in the 802.3x specification) and transmits the frame to the MII interface. The transmission of the control frame is not affected by the current state of the Pause timer value that is set because of a recently received control frame.

3.2.2 HALF-DUPLEX FLOW CONTROL (BACKPRESSURE)

In half-duplex mode, back pressure is used for flow control. Whenever the receive buffer/FIFO becomes full or crosses a certain threshold level, the MAC starts sending a Jam signal. The MAC transmit logic enters a state at the end of current transmission (if any), where it waits for the beginning of a received frame. Once a new frame starts, the MAC starts sending the Jam signal, which will result in a collision. After sensing the collision, the remote station will back off its transmission. The MAC continues sending the jam to make other stations defer transmission. The MAC only generates this collision-based back pressure when it receives a new frame, in order to avoid any late collisions.

3.2.3 VIRTUAL LOCAL AREA NETWORK (VLAN)

VLAN is a means to form a “broadcast domain” without restriction on the physical or geographical location on the members of that domain. VLAN can be implemented in any number of different factors, such as:

- Physical port
- MAC address
- Layer-3 unicast address
- Multicast address
- Date/time in combination with MAC address, etc.

An example of a VLAN is depicted in Figure 3-1, "VLAN Topology". It demonstrates the freedom from physical constraint on the network, and the ability to divide a single switched network into a smaller broadcast domain.

Moreover, VLAN offers a number of other advantages, such as:

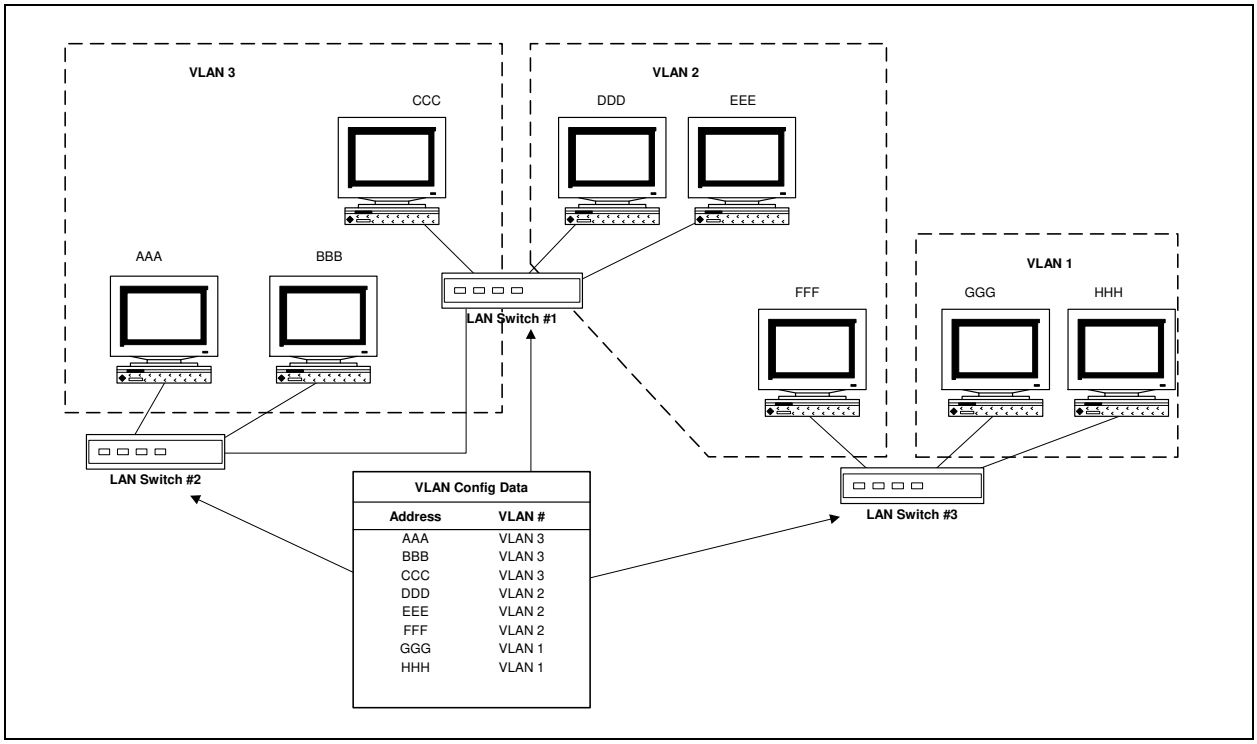
Configurability: Changes to an existing VLAN can be made on the network administrative level, rather than on the hardware level. A member of a VLAN can thus change its MAC address or its port and still be a member of the same VLAN. Extra routing is not necessary.

Security: VLAN can improve security by demanding a predefined authentication before admitting a new member to the domain.

Network efficiency: Allows shielding one system resource from traffic not meant for that resource. A workstation in one VLAN is shielded from traffic on another VLAN, increasing that workstation’s efficiency.

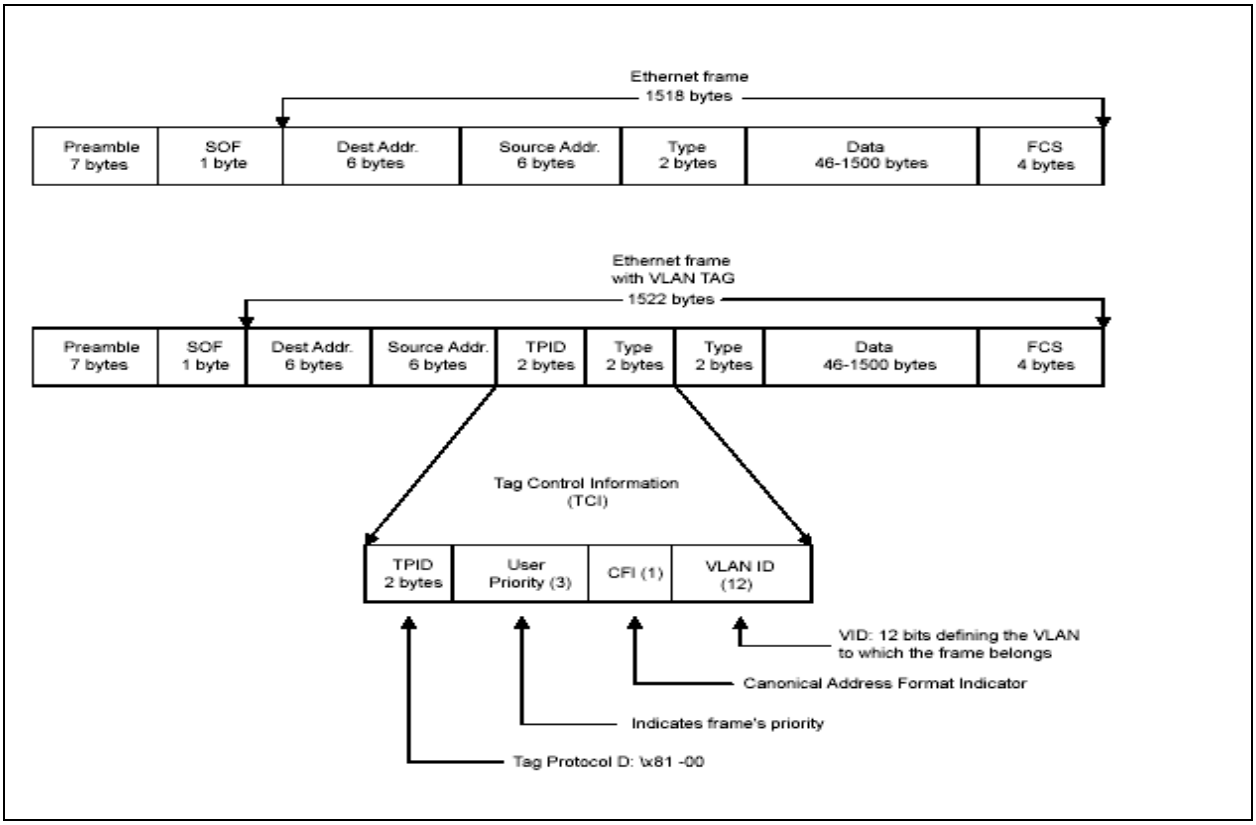
Broadcast containment: Leakage of broadcast frames from one VLAN to another is prevented.

FIGURE 3-1: VLAN TOPOLOGY



When the members of a VLAN are not located on the same physical medium, the VLAN uses a tag to help it determine how to forward the frame from one member to another. The tag structure was proprietary until the IEEE released a supplement to 802.3 defining the VLAN frame structure, including the tag. This new frame structure for VLAN is depicted in Figure 3-2, "VLAN Frame".

FIGURE 3-2: VLAN FRAME



The MAC Function recognizes transmitted and received frames tagged with either one-level or two-level VLAN IDs. The MAC compares the thirteenth and fourteenth bytes of transmit and receive frames to the contents of both the one-level VLAN tag register and the two-level VLAN tag register. If a match is found, the MAC Function identifies the frame as either a one- or two-level VLAN frame, depending on where the match was found. Upon recognizing that a frame has a VLAN tag, counter thresholds are adjusted to account for the extra bytes that the VLAN tag adds to the frame. The maximum length of the good packet is thus changed from 1518 bytes to 1522 bytes.

3.3 Address Filtering Functional Description

The Ethernet address fields of an Ethernet Packet, consists of two 6-byte fields: one for the destination address and one for the source address. The first bit of the destination address signifies whether it is a physical address or a multicast address.

The LAN9118 address check logic filters the frame based on the Ethernet receive filter mode that has been enabled. Filter modes are specified based on the state of the control bits in Table 3-1, "Address Filtering Modes", which shows the various filtering modes used by the Ethernet MAC Function. These bits are defined in more detail in the “MAC Control Register”. Please refer to Section 5.4.1, "MAC_CR—MAC Control Register," on page 75 for more information on this register.

If the frame fails the filter, the Ethernet MAC function does not receive the packet. The host has the option of accepting or ignoring the packet.

TABLE 3-1: ADDRESS FILTERING MODES

MCPAS	PRMS	INVFILT	HO	HPFILT	Description
0	0	0	0	0	MAC address perfect filtering only for all addresses.
0	0	0	0	1	MAC address perfect filtering for physical address and hash filtering for multicast addresses
0	0	0	1	1	Hash Filtering for physical and multicast addresses
0	0	1	0	0	Inverse Filtering
X	1	0	X	X	Promiscuous
1	0	0	0	X	Pass all multicast frames. Frames with physical addresses are perfect-filtered
1	0	0	1	1	Pass all multicast frames. Frames with physical addresses are hash-filtered

3.4 Filtering Modes

3.4.1 PERFECT FILTERING

This filtering mode passes only incoming frames whose destination address field exactly matches the value programmed into the MAC Address High register and the MAC address low register. The MAC address is formed by the concatenation of the above two registers in the MAC CSR Function.

3.4.2 HASH ONLY FILTERING

This type of filtering checks for incoming Receive packets with either multicast or physical destination addresses, and executes an imperfect address filtering against the hash table.

During imperfect hash filtering, the destination address in the incoming frame is passed through the CRC logic and the upper six bits of the CRC register are used to index the contents of the hash table. The hash table is formed by merging the register’s multicast hash table high and multicast hash table low in the MAC CSR Function to form a 64-bit hash table. The most significant bit determines the register to be used (High/Low), while the other five bits determine the bit within the register. A value of 00000 selects Bit 0 of the multicast hash table low register and a value of 11111 selects Bit 31 of the multicast hash table high register.

3.4.2.1 Hash Perfect Filtering

In hash perfect filtering, if the received frame is a physical address, the LAN9118 Packet Filter block perfect-filters the incoming frame’s destination field with the value programmed into the MAC Address High register and the MAC Address Low register. If the incoming frame is a multicast frame, however, the LAN9118 packet filter function performs an imperfect address filtering against the hash table.

The imperfect filtering against the hash table is the same imperfect filtering process described in the “Hash Only Filtering” section above.

3.4.2.2 Inverse Filtering

In inverse filtering, the LAN9118 Packet Filter Block accepts incoming frames with a destination address not matching the perfect address (i.e., the value programmed into the MAC Address High register and the MAC Address Low register in the CRC block and rejects frames with destination addresses matching the perfect address.

For all filtering modes, when MCPAS is set, all multicast frames are accepted. When the PRMS bit is set, all frames are accepted regardless of their destination address. This includes all broadcast frames as well.

3.5 Wake-up Frame Detection

Setting the Wake-Up Frame Enable bit (WUEN) in the “WUCSR—Wake-up Control and Status Register”, places the LAN9118 MAC in the wake-up frame detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for the pre-programmed wake-up frame patterns. The LAN9118 can be programmed to notify the host of the wake-up frame detection with the assertion of the host interrupt (IRQ) or assertion of the power management event signal (PME). Upon detection, the Wake-Up Frame Received bit (WUFR) in the WUCSR is set. When the host clears the WUEN bit the LAN9118 will resume normal receive operation.

Before putting the MAC into the wake-up frame detection state, the host must provide the detection logic with a list of sample frames and their corresponding byte masks. This information is written into the Wake-up Frame Filter register (WUFF). Please refer to Section 5.4.11, "WUFF—Wake-up Frame Filter," on page 82 for additional information on this register.

The MAC supports four programmable filters that support many different receive packet patterns. If remote wake-up mode is enabled, the remote wake-up function receives all frames addressed to the MAC. It then checks each frame against the enabled filter and recognizes the frame as a remote wake-up frame if it passes the wakeup frame filter register’s address filtering and CRC value match.

In order to determine which bytes of the frames should be checked by the CRC module, the MAC uses a programmable byte mask and a programmable pattern offset for each of the four supported filters.

The pattern’s offset defines the location of the first byte that should be checked in the frame. Since the destination address is checked by the address filtering Function, the pattern offset is always greater than 12.

The byte mask is a 31-bit field that specifies whether or not each of the 31 contiguous bytes within the frame, beginning in the pattern offset, should be checked. If bit j in the byte mask is set, the detection logic checks byte offset +j in the frame. In order to load the Wake-up Frame Filter register, the host LAN driver software must perform eight writes to the Wake-up Frame Filter register (WUFF). The Diagram shown in Table 3-2, "Wake-Up Frame Filter Register Structure" below, shows the wake-up frame filter register’s structure.

Note 3-1 Wake-up frame detection can be performed when LAN9118 is in the D0 or D1 power states. In the D0 state, wake-up frame detection is enabled when the WUEN bit is set.

Note 3-2 Wake-up frame detection, as well as Magic Packet detection, is always enabled and cannot be disabled when the device enters the D1 state.

Note 3-3 When wake-up frame detection is enabled via the WUEN bit of the WUCSR—Wake-up Control and Status Register, a broadcast wake-up frame will wake-up the device despite the state of the Disable Broadcast Frames (BCAST) bit in the MAC_CR—MAC Control Register.

TABLE 3-2: WAKE-UP FRAME FILTER REGISTER STRUCTURE

Filter 0 Byte Mask							
Filter 1 Byte Mask							
Filter 2 Byte Mask							
Filter 3 Byte Mask							
Reserved	Filter 3 Command	Reserved	Filter 2 Command	Reserved	Filter 1 Command	Reserved	Filter 0 Command
Filter 3 Offset		Filter 2 Offset		Filter 1Offset		Filter 0 Offset	
Filter 1 CRC-16				Filter 0 CRC-16			
Filter 3 CRC-16				Filter 2 CRC-16			

The Filter i Byte Mask defines which incoming frame bytes Filter i will examine to determine whether or not this is a wake-up frame. Table 3-3, describes the byte mask’s bit fields.

TABLE 3-3: FILTER I BYTE MASK BIT DEFINITIONS

Filter i Byte Mask Description	
Field	**Description**
31	Must be zero (0)
30:0	**Byte Mask:** If bit j of the byte mask is set, the CRC machine processes byte number pattern - (offset + j) of the incoming frame. Otherwise, byte pattern - (offset + j) is ignored.

The Filter i command register controls Filter i operation. Table 3-4 shows the Filter I command register.

TABLE 3-4: FILTER I COMMAND BIT DEFINITIONS

Filter i Commands	
Field	**Description**
3	**Address Type:** Defines the destination address type of the pattern. When bit is set, the pattern applies only to multicast frames. When bit is cleared, the pattern applies only to unicast frames.
2:1	**RESERVED**
0	**Enable Filter:** When bit is set, Filter i is enabled, otherwise, Filter i is disabled.

The Filter i Offset register defines the offset in the frame's destination address field from which the frames are examined by Filter i. Table 3-5 describes the Filter i Offset bit fields.

TABLE 3-5: FILTER I OFFSET BIT DEFINITIONS

Filter i Offset Description	
Field	**Description**
7:0	**Pattern Offset:** The offset of the first byte in the frame on which CRC is checked for wake-up frame recognition. The minimum value of this field must be 12 since there should be no CRC check for the destination address and the source address fields. The MAC checks the first offset byte of the frame for CRC and checks to determine whether the frame is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address.

The Filter i CRC-16 register contains the CRC-16 result of the frame that should pass Filter i.

Table 3-6 describes the Filter i CRC-16 bit fields.

TABLE 3-6: FILTER I CRC-16 BIT DEFINITIONS

Filter i CRC-16 Description	
Field	**Description**
15:0	**Pattern CRC-16:** This field contains the 16-bit CRC value from the pattern and the byte mask programmed to the wake-up filter register Function. This value is compared against the CRC calculated on the incoming frame, and a match indicates the reception of a wakeup frame.

3.5.1 MAGIC PACKET DETECTION

Setting the Magic Packet Enable bit (MPEN) in the "WUCSR—Wake-up Control and Status Register", places the LAN9118 MAC in the "Magic Packet" detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for a Magic Packet. The LAN9118 can be programmed to notify the host of the "Magic Packet" detection with the assertion of the host interrupt (IRQ) or assertion of the power management event signal (PME). Upon detection, the Magic Packet Received bit (MPR) in the WUCSR is set. When the host clears the MPEN bit the LAN9118 will resume normal receive operation. Please refer to Section 5.4.12, "WUCSR—Wake-up Control and Status Register," on page 82 for additional information on this register.

In Magic Packet mode, the Power Management Logic constantly monitors each frame addressed to the node for a specific Magic Packet pattern. It checks only packets with the MAC's address or a broadcast address to meet the Magic Packet requirement. The Power Management Logic checks each received frame for the pattern 48h FF_FF_FF_FF_FF_FF after the destination and source address field.

Then the Function looks in the frame for 16 repetitions of the MAC address without any breaks or interruptions. In case of a break in the 16 address repetitions, the PMT Function scans for the 48'hFF_FF_FF_FF_FF_FF pattern again in the incoming frame.

The 16 repetitions may be anywhere in the frame but must be preceded by the synchronization stream. The device will also accept a multicast frame, as long as it detects the 16 duplications of the MAC address. If the MAC address of a node is 00h 11h 22h 33h 44h 55h, then the MAC scans for the following data sequence in an Ethernet: Frame.

Destination Address Source Address ……FF FF FF FF FF FF

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55

…CRC

It should be noted that Magic Packet detection can be performed when LAN9118 is in the D0 or D1 power states. In the D0 state, “Magic Packet” detection is enabled when the MPEN bit is set. In the D1 state, Magic Packet detection, as well as wake-up frame detection, are automatically enabled when the device enters the D1 state.

3.6 32-bit vs. 16-bit Host Bus Width Operation

The LAN9118 can be configured to communicate with the host bus via either a 32-bit or a 16-bit bus. An external strap is used to select between the two modes. 32-bit mode is the native environment for the LAN9118 Ethernet controller and no special requirements exist for communication in this mode. However, when this part is used in the 16-bit mode, two writes or reads must be performed back to back to properly communicate.

The bus width is set by strapping the EEDIO pin; this setting can be read from bit 2 of the “Hardware Configuration Register”. Please refer to Section 5.3.9, "HW_CFG—Hardware Configuration Register," on page 61 for additional information on this register.

3.6.1 16-BIT BUS WRITES

The host processor is required to perform two contiguous 16-bit writes to complete a single DWORD transfer. This DWORD must begin and end on a DWORD address boundary (A[2] and higher, cannot change during a sixteen bit write). No ordering requirements exist. The processor can access either the low or high word first, as long as the next write is performed to the other word. If a write to the same word is performed, the LAN9118 disregards the transfer.

3.6.2 16-BIT BUS READS

The host processor is required to perform two consecutive 16-bit reads to complete a single DWORD transfer. This DWORD must begin and end on a DWORD address boundary (A[2] and higher, cannot change during a sixteen bit read). No ordering requirements exist. The processor can access either the low or high word first, as long as the next read is performed from the other word. If a read to the same word is performed, the data read is invalid and should be re-read. This is not a fatal error. The LAN9118 will reset its read counters and restart a new cycle on the next read. The Upper 16 data pins (D[31:16]) are not driven by the LAN9118 in 16-bit mode. These pins have internal pull-down’s and the signals are left in a high-impedance state.

3.7 Big and Little Endian Support

The Microchip LAN9118 supports “Big-” or “Little-Endian” processors in either 16 or 32-bit bus width modes. To support big-endian processors, the hardware designer must explicitly invert the layout of the byte lanes. In addition, for a 16-bit interface, the WORD_SWAP—Word Swap Control must be set correctly following Table 3-7, "Byte Lane Mapping".

The host bus interface can be selected via an external strap to translate the data bus into either mode. Please refer to Table 2-4, “Serial EEPROM Interface Signals,” on page 10, for information on multiplexed signal D32/nD16 for more information on data bus width selection.

Additionally, please refer to Section 5.3.17, "WORD_SWAP—Word Swap Control," on page 68 for additional information on status indication on Endian modes.

TABLE 3-7: BYTE LANE MAPPING

Mode of Operation	Data Pins				Description
	D[31:24]	D[23:16]	D[15:8]	D[7:0]	
32-bit	Byte 3 (MSB)	Byte 2	Byte 1	Byte 0 (LSB)	This is the native mode of the LAN9118. Endianess does not matter when both WORD lanes are in operation.
Mode 0 (WORD_SWAP—Word Swap Control equal to FFFFFFFFh)					
A1 = 0	--	--	Byte 3	Byte 2	**Note:** This mode can be used by 32-bit processors operating with an external 16-bit bus.
A1 = 1	--	--	Byte 1	Byte 0	
Mode 1 (WORD_SWAP—Word Swap Control not equal to FFFFFFFFh)					
A1 = 0	--	--	Byte 1	Byte 0	**Note:** This mode can also be used by native 16-bit processors.
A1 = 1	--	--	Byte 3	Byte 2	

Regarding the 32-bit mode description of operation comment described in the table above, mentioning “It should be noted that Endianess does not matter when both WORD lanes are in operation” is true for the LAN9118 device. However, as in all designs, it is important for the PCB layout designer to route the signal byte lanes appropriately relative to the processor type (Big vs. Little Endian).

3.8 General Purpose Timer (GP Timer)

The General Purpose Timer is a programmable block that can be used to generate periodic host interrupts. The resolution of this timer is 100uS.

The GP Timer loads the GPT_CNT Register with the value in the GPT_LOAD field and begins counting down when the TIMER_EN bit is set to a ‘1.’ On a reset, or when the TIMER_EN bit changes from set ‘1’ to cleared ‘0,’ the GPT_CNT field is initialized to FFFFh. The GPT_CNT register is also initialized to FFFFh on a reset. Software can write the pre-load value into the GPT_LOAD field at any time; e.g., before or after the TIMER_EN bit is asserted. The GPT Enable bit TIMER_EN is located in the GPT_CFG register.

Once enabled, the GPT counts down either until it reaches 0000h or until a new pre-load value is written to the GPT_-LOAD field. At 0000h, the counter wraps around to FFFFh, asserts the GPT interrupt status bit and the IRQ signal if the GPT_INT_EN bit is set, and continues counting. The GPT interrupt status bit is in the INT_STS Register. The GPT_INT hardware interrupt can only be set if the GPT_INT_EN bit is set. GPT_INT is a sticky bit (R/WC); i.e., once the GPT_INT bit is set, it can only be cleared by writing a ‘1’ to the bit.

3.9 EEPROM Interface

LAN9118 can optionally load its MAC address from an external serial EEPROM. If a properly configured EEPROM is detected by LAN9118 at power-up, hard reset or soft reset, the ADDRH and ADDRL registers will be loaded with the contents of the EEPROM. If a properly configured EEPROM is not detected, it is the responsibility of the host LAN Driver to set the IEEE addresses.

The LAN9118 EEPROM controller also allows the host system to read, write and erase the contents of the Serial EEPROM. The EEPROM controller supports most “93C46” type EEPROMs configured for 128 x 8-bit operation.

3.9.1 MAC ADDRESS AUTO-LOAD

On power-up, hard reset or soft reset, the EEPROM controller attempts to read the first byte of data from the EEPROM (address 00h). If the value A5h is read from the first address, then the EEPROM controller will assume that an external Serial EEPROM is present. The EEPROM controller will then access the next EEPROM byte and send it to the MAC Address register byte 0 (ADDRL[7:0]). This process will be repeated for the next five bytes of the MAC Address, thus fully programming the 48-bit MAC address. Once all six bytes have been programmed, the “MAC Address Loaded” bit is set in the E2P_CMD register. A detailed explanation of the EEPROM byte ordering with respect to the MAC address is given in Section 5.4.3, "ADDRL—MAC Address Low Register," on page 77.

If an 0xA5h is not read from the first address, the EEPROM controller will end initialization. It is then the responsibility of the host LAN driver software to set the IEEE address by writing to the MAC’s ADDRH and ADDRL registers.

The host can initiate a reload of the MAC address from the EEPROM by issuing the RELOAD command via the E2P command (E2P_CMD) register. If the first byte read from the EEPROM is not A5h, it is assumed that the EEPROM is not present, or not programmed, and the MAC address reload will fail. The “MAC Address Loaded” bit indicates a successful reload of the MAC address.

3.9.2 EEPROM HOST OPERATIONS

After the EEPROM controller has finished reading (or attempting to read) the MAC after power-on, hard reset or soft reset, the host is free to perform other EEPROM operations. EEPROM operations are performed using the E2P_CMD and E2P data (E2P_DATA) registers. Section 5.3.23, "E2P_CMD – EEPROM Command Register," on page 72 provides an explanation of the supported EEPROM operations.

If the EEPROM operation is the “write location” (WRITE) or “write all” (WRAL) commands, the host must first write the desired data into the E2P_DATA register. The host must then issue the WRITE or WRAL command using the E2P_CMD register by setting the EPC_CMD field appropriately. If the operation is a WRITE, the EPC_ADDR field in E2P_CMD must also be set to the desired location. The command is executed when the host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared.

If the EEPROM operation is the “read location” (READ) operation, the host must issue the READ command using the E2P_CMD with the EPC_ADDR set to the desired location. The command is executed when the host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared, at which time the data from the EEPROM may be read from the E2P_DATA register.

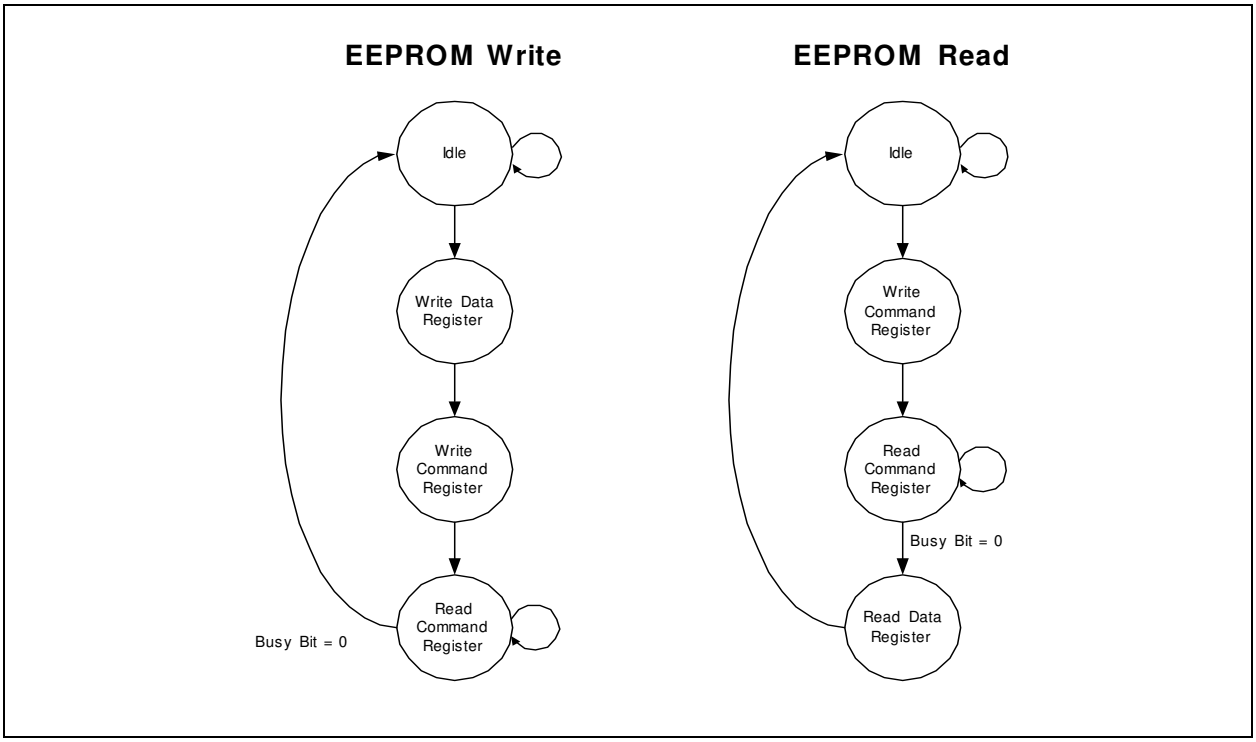
Other EEPROM operations are performed by writing the appropriate command to the EPC_CMD register. The command is executed when the host sets the EPC_BSY bit high. The completion of the operation is indicated when the EPC_BSY bit is cleared. In all cases the host must wait for EPC_BSY to clear before modifying the E2P_CMD register.

Note:	The EEPROM device powers-up in the erase/write disabled state. To modify the contents of the EEPROM the host must first issue the EWEN command.

If an operation is attempted, and an EEPROM device does not respond within 30mS, the LAN9118 will timeout, and the EPC timeout bit (EPC_TO) in the E2P_CMD register will be set.

Figure 3-3, "EEPROM Access Flow Diagram" illustrates the host accesses required to perform an EEPROM Read or Write operation.

FIGURE 3-3: EEPROM ACCESS FLOW DIAGRAM



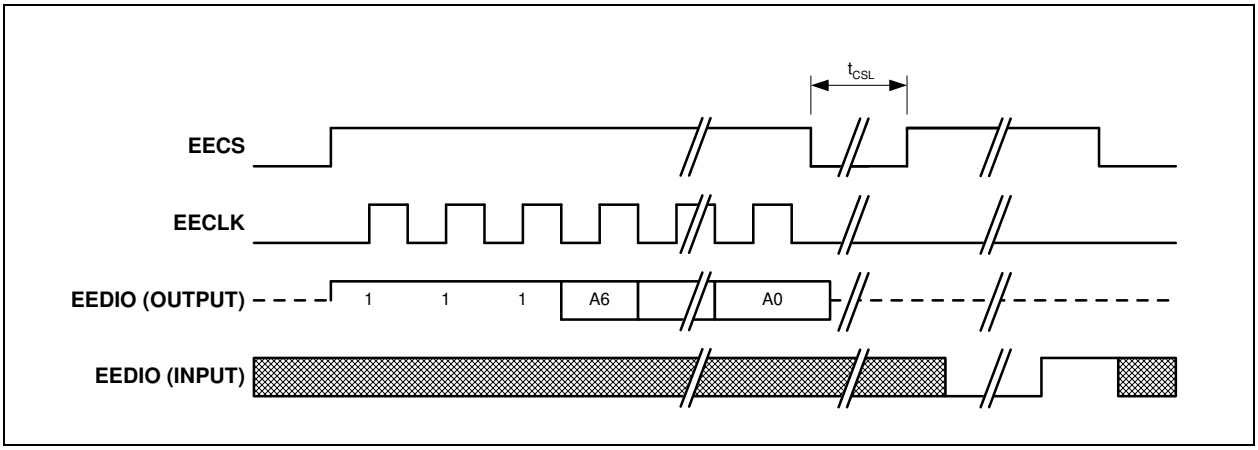
The host can disable the EEPROM interface through the GPIO_CFG register. When the interface is disabled, the EEDIO and ECLK signals can be used as general-purpose outputs, or they may be used to monitor internal MII signals.

3.9.2.1 Supported EEPROM Operations

The EEPROM controller supports the following EEPROM operations under host control via the E2P_CMD register. The operations are commonly supported by “93C46” EEPROM devices. A description and functional timing diagram is provided below for each operation. Please refer to the E2P_CMD register description in Section 5.3.23, "E2P_CMD – EEPROM Command Register," on page 72 for E2P_CMD field settings for each command.

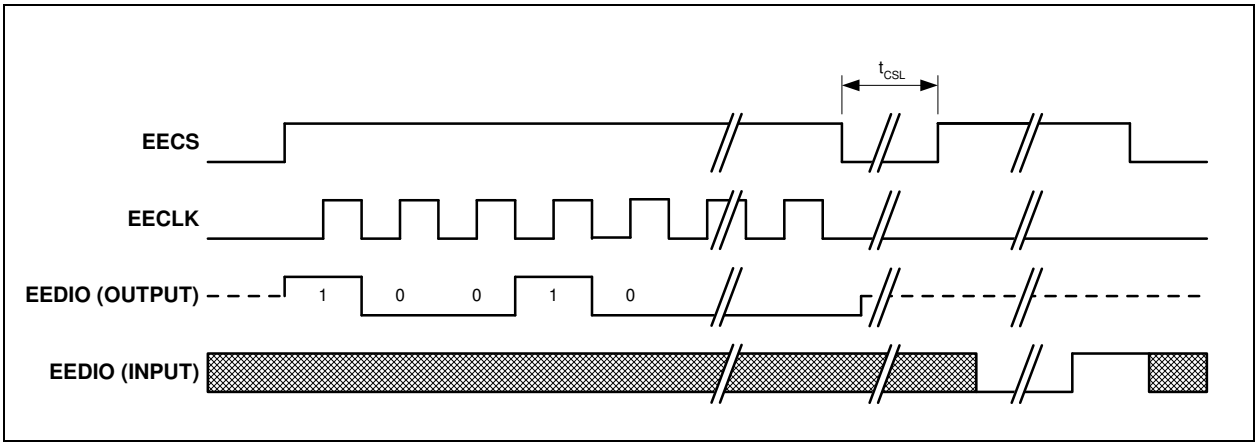
ERASE (Erase Location): If erase/write operations are enabled in the EEPROM, this command will erase the location selected by the EPC Address field (EPC_ADDR). The EPC_TO bit is set if the EEPROM does not respond within 30ms.

FIGURE 3-4: EEPROM ERASE CYCLE



ERAL (Erase All): If erase/write operations are enabled in the EEPROM, this command will initiate a bulk erase of the entire EEPROM.The EPC_TO bit is set if the EEPROM does not respond within 30ms.

FIGURE 3-5: EEPROM ERAL CYCLE



EWDS (Erase/Write Disable): After issued, the EEPROM will ignore erase and write commands. To re-enable erase/write operations issue the EWEN command.

FIGURE 3-6: EEPROM EWDS CYCLE