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## **FEAST Fast Ethernet Controller with Full Duplex Capability**

### **Datasheet**

### **Product Features**

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- Dual Speed CSMA/CD Engine (10 Mbps and 100 Mbps)
- Compliant with IEEE 802.3 100BASE-T Specification
- Supports 100BASE-TX, 100BASE-T4, and 10BASE-T Physical Interfaces
- 32 Bit Wide Data Path (into Packet Buffer Memory)
- Support for 32 and 16 Bit Buses
- Support for 32, 16 and 8 Bit CPU Accesses
- Synchronous, Asynchronous and Burst DMA Interface Mode Options
- 128 Kbyte External Memory
- Built-In Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- MII (Media Independent Interface) Compliant MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- Seven Wire Interface to 10 Mbps ENDEC
- EEPROM-Based Setup
- Full Duplex Capability

### **ORDER NUMBER(S):**

LAN91C100-FD for 208-pin QFP package

LAN91C100-FD-SS for 208-pin QFP lead-free RoHS compliant package

LAN91C100-FD for 208-pin TQFP package

LAN91C100-FD-ST for 208-pin TQFP lead-free RoHS compliant package



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## Chapter 1 General Description

The LAN91C100FD is designed to facilitate the implementation of first generation Fast Ethernet adapters and connectivity products. For this first generation of products, flexibility dominates over integration. The LAN91C100FD is a digital device that implements the MAC portion of the CSMA/CD protocol at 10 and 100 Mbps, and couples it with a lean and fast data and control path system architecture to ensure the CPU to packet RAM data movement does not cause a bottleneck at 100 Mbps.

Total memory size is 128 Kbytes, equivalent to a total chip storage (transmit plus receive) of 64 outstanding packets. The LAN91C100FD is software compatible with the LAN9000 family of products and can use existing LAN9000 drivers (ODI, IPX, and NDIS) in 16 and 32 bit Intel X86 based environments.

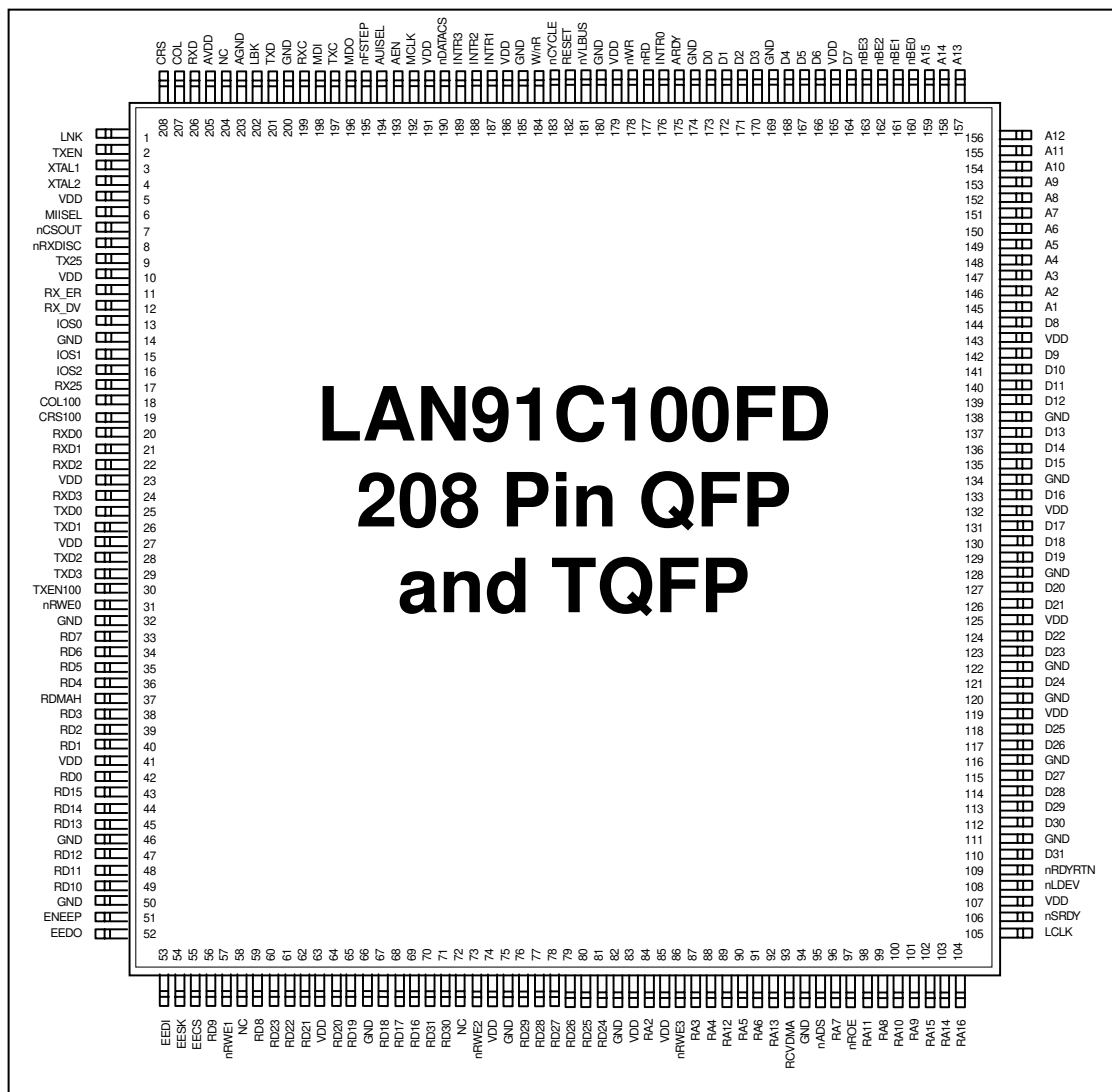
Memory management is handled using a unique MMU (Memory Management Unit) architecture and a 32-bit wide data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions. The total memory size is 128 Kbytes (external), equivalent to a total chip storage (transmit and receive) of 64 outstanding packets.

FEAST provides a flexible slave interface for easy connectivity with industry-standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous buses, with different signals being used for each one. FEAST's bus interface supports synchronous buses like the VESA local bus, as well as burst mode DMA for EISA environments. Asynchronous bus support for ISA is supported even though ISA cannot sustain 100 Mbps traffic. Fast Ethernet could be adopted for ISA-based nodes on the basis of the aggregate traffic benefits.

Two different interfaces are supported on the network side. The first is a conventional seven wire ENDEC interface that connects to the LAN83C694 for 10BASE-T and coax 10 Mbps Ethernet networks. The second interface follows the MII (Media Independent Interface) specification draft standard, consisting of 4 bit wide data transfers at the nibble rate. This interface is applicable to 10 Mbps or 100 Mbps networks. Three of the LAN91C100FD's pins are used to interface to the two-line MII serial management protocol. Four I/O ports (one input and three output pins) are provided for LAN83C694 configuration.

The LAN91C100FD is based on the LAN91C100 FEAST, functional revision G modified to add full duplex capability. Also added is a software-controlled option to allow collisions to discard receive packets. Previously, the LAN91C100 supported a "Diagnostic Full Duplex" mode. Under this mode the transmit packet is looped internally and received by the MAC. This mode was enabled using the FDUPLX bit in the TCR. In order to avoid confusion, the new, broader full duplex function of the LAN91C100FD is designated as Switched Full Duplex, and the TCR bit enabling it is designated as SWFDUP. When the LAN91C100FD is configured for SWFDUP, its transmit and receive paths will operate independently and some CSMA/CD functions will be disabled. When the controller is not configured for SWFDUP it will follow the CSMA/CD protocol.

## Chapter 2 Pin Configuration



## Chapter 3 Description of Pin Functions

PQFP/TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
148-159	Address	A4-A15	I	Input. Decoded by LAN91C100FD to determine access to its registers.
145-147	Address	A1-A3	I	Input. Used by LAN91C100FD for internal register selection.
193	Address Enable	AEN	I	Input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
160-163	nByte Enable	nBE0-nBE3	I	Input. Used during LAN91C100FD register accesses to determine the width of the access and the register(s) being accessed. nBE0-nBE3 are ignored when nDATACS is low (burst accesses) because 32 bit transfers are assumed.
173-170, 168-166, 164, 144, 142-139, 137-135, 133, 131-129, 127, 126, 124, 123, 121, 118, 117, 115-112, 110	Data Bus	D0-D31	I/O24	Bidirectional. 32 bit data bus used to access the LAN91C100FD's internal registers. Data bus has weak internal pullups. Supports direct connection to the system bus without external buffering. For 16 bit systems, only D0-D15 are used.
182	Reset	RESET	IS	Input. This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
95	nAddress Strobe	nADS	IS	Input. For systems that require address latching, the rising edge of nADS indicates the latching moment for A1-A15 and AEN. All LAN91C100FD internal functions of A1-A15, AEN are latched except for nLDEV decoding.
183	nCycle	nCYCLE	I	Input. This active low signal is used to control LAN91C100FD EISA burst mode synchronous bus cycles.
184	Write/ nRead	W/nR	IS	Input. Defines the direction of synchronous cycles. Write cycles when high, read cycles when low.
181	nVL Bus Access	nVLBUS	I with pullup	Input. When low, the LAN91C100FD synchronous bus interface is configured for VL Bus accesses. Otherwise, the LAN91C100FD is configured for EISA DMA burst accesses. Does not affect the asynchronous bus interface.
105	Local Bus Clock	LCLK	I	Input. Used to interface synchronous buses. Maximum frequency is 50 MHz. Limited to 8.33 MHz for EISA DMA burst mode.



PQFP/TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
175	Asynchronous Ready	ARDY	OD16	Open drain output. ARDY may be used when interfacing asynchronous buses to extend accesses. Its rising (access completion) edge is controlled by the XTAL1 clock and, therefore, asynchronous to the host CPU or bus clock.
106	nSynchronous Ready	nSRDY	O16	Output. This output is used when interfacing synchronous buses and nVLBUS=0 to extend accesses. This signal remains normally inactive, and its falling edge indicates completion. This signal is synchronous to the bus clock LCLK.
109	nReady Return	nRDYRTN	I	Input. This input is used to complete synchronous read cycles. In EISA burst mode it is sampled on falling LCLK edges, and synchronous cycles are delayed until it is sampled high.
176, 187-189	Interrupt	INTR0-INTR3	O24	Outputs. Only one of these interrupts is selected to be used; the other three are tri-stated. The selection is determined by the value of INT SEL 1-0 bits in the Configuration Register.
108	nLocal Device	nLDEV	O16	Output. This active low output is asserted when AEN is low and A4-A15 decode to the LAN91C100FD address programmed into the high byte of the Base Address Register. nLDEV is a combinatorial decode of unlatched address and AEN signals.
177	nRead Strobe	nRD	IS	Input. Used in asynchronous bus interfaces.
178	nWrite Strobe	nWR	IS	Input. Used in asynchronous bus interfaces.
190	nData Path Chip Select	nDATACS	I with pullup	Input. When nDATACS is low, the Data Path can be accessed regardless of the values of AEN, A1-A15 and the content of the BANK SELECT Register. nDATACS provides an interface for bursting to and from the LAN91C100FD 32 bits at a time.
54	EEPROM Clock	EESK	O4	Output. 4 $\mu$ sec clock used to shift data in and out of the serial EEPROM.
55	EEPROM Select	EECS	O4	Output. Serial EEPROM chip select. Used for selection and command framing of the serial EEPROM.
52	EEPROM Data Out	EEDO	O4	Output. Connected to the DI input of the serial EEPROM.
53	EEPROM Data In	EEDI	I with pulldown	Input. Connected to the DO output of the serial EEPROM.
13, 15, 16	I/O Base	IOS0- IOS2	I with pullup	Input. External switches can be connected to these lines to select between predefined EEPROM configurations.
51	Enable EEPROM	ENEPP	I with pullup	Input. Enables (when high or open) LAN91C100FD accesses to the serial EEPROM. Must be grounded if no EEPROM is connected to the LAN91C100FD.



PQFP/TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
42, 40-38, 36-33	RAM Data Bus	RD0-RD7	I/O4 with pullups	Bidirectional. Carries the local buffer memory read and write data. Reads are always 32 bits wide. Writes are controlled individually at the byte level. Floated if FLTST=1 during RECEIVE FRAME STATUS WORD writes for packet forwarding information (RA2-RA16=0, RCVDMA=1, nRWE0-nRWE3=0).
59, 56, 49-47, 45-43, 69-67, 65, 64, 62-60, 81-76, 71, 70	RAM Data Bus	RD8- RD31	I/O4 with pullups	Bidirectional. Carries the local buffer memory read and write data. Reads are always 32 bits wide. Writes are controlled individually at the byte level.
84, 87, 88, 90, 91, 96, 99, 101, 100, 98, 89, 92, 103, 102, 104	RAM Address Bus	RA2-RA16	O4	Outputs. This bus specifies the buffer RAM doubleword being accessed by the LAN91C100FD.
97		nROE	O4	Output. Active low signal used to read a doubleword from buffer RAM.
31, 57, 73, 86		nRWE0- RWE3	O4	Outputs. Active low signals used to write any byte, word or dword in RAM.
93	Receive DMA	RCVDMA	O4	Output. This pin is active during LAN91C100FD write memory cycles of receive packets.
3 4	Crystal 1 Crystal 2	XTAL1 XTAL2	Iclk	An external 25 MHz crystal is connected across these pins. If a TTL clock is supplied instead, it should be connected to XTAL1 and XTAL2 should be left open.
5, 10, 23, 27, 41, 63, 74, 83, 85, 107, 119, 125, 132, 143, 165, 179, 186, 191	Power	VDD		+5V power supply pins.
205	Analog Power	AVDD		+5V analog power supply pins.
14, 32, 46, 50, 66, 75, 82, 94, 111, 116, 120, 122, 128, 134, 138, 169, 174, 180, 185, 200	Ground	GND		Ground pins.
203	Analog Ground	AGND		Analog ground pin.
2	Transmit Enable	TXEN	O4	Output. Used for 10 Mbps ENDEC. This pin stays low when MIISEL is high.

PQFP/TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
201	Transmit Data	TXD	O4	Output. NRZ Transmit Data for 10 Mbps ENDEC interface.
208	Carrier Sense	CRS	I with pulldown	Input. Carrier sense from 10 Mbps ENDEC interface. This pin is ignored when MIISEL is high.
207	Collision Detect	COL	I with pulldown	Input. Collision detection indication from 10 Mbps ENDEC interface. This pin is ignored when MIISEL is high.
206	Receive Data	RXD	I with pullup	Input. NRZ Receive Data from 10 Mbps ENDEC interface. This pin is ignored when MIISEL is high.
197	Transmit Clock	TXC	I with pullup	Input. 10 MHz transmit clock used in 10 Mbps operation. This pin is ignored when MIISEL is high.
199	Receive Clock	RXC	I with pullup	Input. 10 MHz receive clock recovered by the 10 Mbps ENDEC. This pin is ignored when MIISEL is high.
202	Loopback	LBK	O4	Output. Active when LOOP bit is set (TCR bit 1). Independent of port selection (MIISEL=X).
1	nLink Status	nLNK	I with pullup	Input. General purpose input port used to convey LINK status (EPHSR bit 14). Independent of port selection (MIISEL=X).
195	nFullstep	nFSTEP	O4	Output. Non volatile output pin. Driven by inverse of FULLSTEP (CONFIG bit 10). Independent of port selection (MIISEL=X).
6	MII Select	MIISEL	O4	Output. Non volatile output pin. Driven by MII SELECT (CONFIG bit 15). High indicates the MII port is selected, low indicates the 10 Mbps ENDEC is selected.
194	AUI Select	AUISEL	O4	Output. Non volatile output pin. Driven by AUI SELECT (CONFIG bit 8). Independent of port selection (MIISEL= X).
30	Transmit Enable 100 Mbps	TXEN100	O12	Output to MII PHY. Envelope to 100 Mbps transmission. This pin stays low if MIISEL is low.
19	Carrier Sense 100 Mbps	CRS100	I with pulldown	Input from MII PHY. Envelope of packet reception used for deferral and backoff purposes. This pin is ignored when MIISEL is low.
12	Receive Data Valid	RX_DV	I with pulldown	Input from MII PHY. Envelope of data valid reception. Used for receive data framing. This pin is ignored when MIISEL is low.
18	Collision Detect 100 Mbps	COL100	I with pulldown	Input from MII PHY. Collision detection input. This pin is ignored when MIISEL is low.
25, 26, 28, 29	Transmit Data	TXD0-TXD3	O12	Outputs. Transmit Data nibble to MII PHY.
9	Transmit Clock	TX25	I with pullup	Input. Transmit clock input from MII. Nibble rate clock (25 MHz). This pin is ignored when MIISEL is low.
17	Receive Clock	RX25	I with pullup	Input. Receive clock input from MII PHY. Nibble rate clock. This pin is ignored when MIISEL is low.

PQFP/TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
20, 21, 22, 24	Receive Data	RXD0- RXD3	I	Inputs. Received Data nibble from MII PHY. These pins are ignored when MIISEL is low.
198	Manage- ment Data Input	MDI	I with pulldown	MI I management data input.
196	Manage- ment Data Output	MDO	O4	MI I management data output.
192	Manage- ment Clock	MCLK	O4	MI I management clock.
11	Receive Error	RX_ER	I with pulldown	Input. Indicates a code error detected by PHY. Used by the LAN91C100FD to discard the packet being received. The error indication reported for this event is the same as a bad CRC (Receive Status Word bit 13). This pin is ignored when MIISEL is low.
7	nChip Select Output	nCSOUT	O4	Output. Chip Select provided for mapping of PHY functions into LAN91C100FD decoded space. Active on accesses to LAN91C100FD's eight lower addresses when the BANK SELECTED is 7.
8	nReceive Packet Discard	nRXDISC	I with pullup	Input. Used to discard the receive packet being stored in memory. Assertion of the pin during a packet reception results in the interruption of packet reception into memory. The memory allocated to the packet and the packet number in use are freed. The input is driven asynchronously and is synchronized internally by the LAN91C100FD. Pin assertion may take place at any time during the receive DMA packet. The assertion has no effect if there is no packet being DMAed to memory or if asserted during the last DMA write to memory. Works for both MII and ENDEC. The typical use of nRXDISC is with the LAN91C100FD in PRMS mode with an external associative memory use for address filtering. *Note: The pin must be asserted for a minimum of 80ns.
37		RDMAH	O4	Output. Active when the first dword of the address is written (RCVDMA=1, RA10-RA4=0, RA3-RA2=X).

### Buffer Types

O4	Output buffer with 2mA source and 4mA sink
O12	Output buffer with 6mA source and 12mA sink
O16	Output buffer with 8mA source and 16mA sink
O24	Output buffer with 12mA source and 24mA sink
OD16	Open drain buffer with 16mA sink

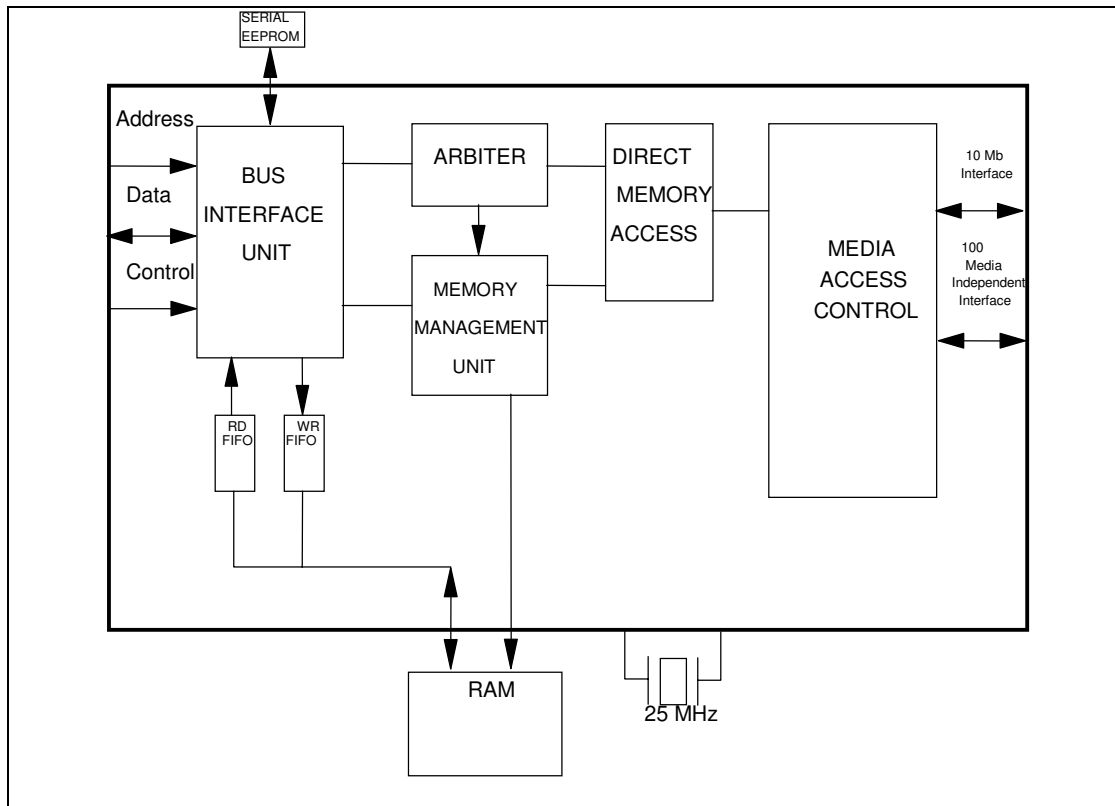
I/O4	Bidirectional buffer with 2mA source and 4mA sink
I/O24	Bidirectional buffer with 12mA source and 24mA sink
I	Input buffer with TTL levels
IS	Input buffer with Schmitt Trigger Hysteresis
Iclk	Clock input buffer

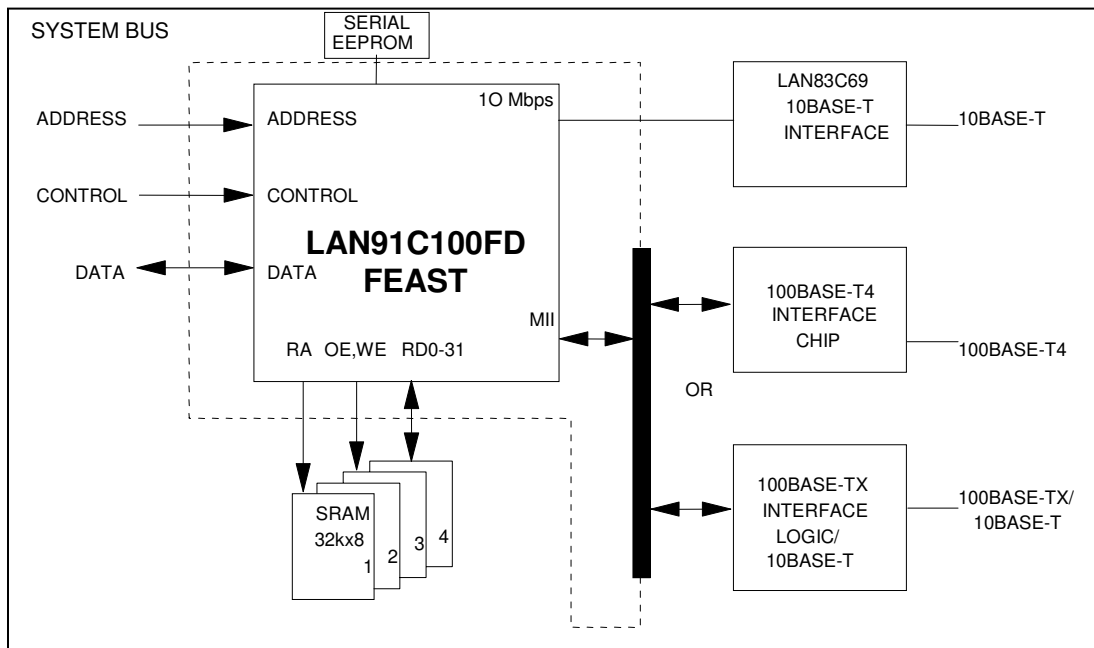
DC levels and conditions defined in the DC Electrical Characteristics section.

**Table 3.1 - LAN91C100FD Pin Requirements**

FUNCTION	PIN SYMBOLS	NUMBER OF PINS
System Address Bus	A1-A15, AEN, nBE0-nBE3	20
System Data Bus	D0-D31	32
System Control Bus	RESET, nADS, LCLK, ARDY, nRDYRTN, nSRDY, INTR0-INTR3, nLDEV, nRD, nWR, nDATAcs, nCYCLE, W/nR, nVLBUS	17
Serial EEPROM	EEDI, EEDO, EECS, EESK, ENEEP, IOS0-IOS2	8
RAM Data Bus	RD0-RD31	32
RAM Address Bus	RA2-RA16	15
RAM Control Bus	nROE, nRWE0-nRWE3, RCVDMA, RDMAH	7
Crystal Oscillator	XTAL1, XTAL2	2
Power	VDD, AVDD	19
Ground	GND, AGND	21
External ENDEC 10 Mbps	TXEN, TXD, CRS, COL, RXD, TXC, RXC, LBK, nLNK, nFSTEP, AUISEL, MIISEL	12
Physical Interface 100 Mbps	TXEN100, CRS100, COL100, RX_DV, RX_ER, TXD0-TXD3, RXD0-RXD3, MDI, MDO, MCLK	16
Clocks	TX25, RX25	2
Miscellaneous	nCSOUT, nRXDISC	2
<b>TOTAL</b>		<b>205</b>



**Figure 3.1 - LAN91C100FD Block Diagram**



**Figure 3.2 - LAN91C100FD System Diagram**

## Chapter 4 Functional Description

### 4.1 Description of Block

#### 4.1.1 Clock Generator Block

1. The XTAL1 and XTAL2 pins are to be connected to a 25 MHz crystal.
2. TXCLK and RXCLK are 10 MHz clock inputs. These clocks are generated by the external ENDEC in 10 Mbps mode and are only used by the CSMA/CD block.
3. TX25 is an input clock. It will be the nibble rate of the particular PHY connected to the MII (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).
4. RX25 - This is the MII nibble rate receive clock used for sampling received data nibbles and running the receive state machine. (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).
5. LCLK - Bus clock - Used by the BIU for synchronous accesses. Maximum frequency is 50 MHz for VL BUS mode, and 8.33 MHz for EISA slave DMA.

### 4.2 CSMA/CD Block

This is a 16 bit oriented block, with fully- independent Transmit and Receive logic. The data path in and out of the block consists of two 16-bit wide uni-directional FIFOs interfacing the DMA block. The DMA port of the FIFO stores 32 bits to exploit the 32 bit data path into memory, but the FIFOs themselves are 16 bit wide. The Control Path consists of a set of registers interfaced to the CPU via the BIU.

#### 4.2.1 DMA Block

This block accesses packet memory on the CSMA/CD's behalf, fetching transmit data and storing received data. It interfaces the CSMA/CD Transmit and Receive FIFOs on one side, and the Arbiter block on the other. To increase the bandwidth into memory, a 50 MHz clock is used by the DMA block, and the data path is 32 bits wide.

For example, during active reception at 100 Mbps, the CSMA/CD block will write a word into the Receive FIFO every 160ns. The DMA will read the FIFO and accumulate two words on the output port to request a memory cycle from the Arbiter every 320ns.

DMA will discard a packet if nRXDISC is asserted for a minimum of 80ns during a reception. If asserted late, the DMA will receive the packet normally. The nRXDISC is defined valid for the DMA interface for as long as the RCVDMA signal is active.

The DMA machine is able to support full duplex operation. Independent receive and transmit counters are used. Transmit and receive cycles are alternated when simultaneous receive and transmit accesses are needed.

#### 4.2.2 Arbiter Block

The Arbiter block sequences accesses to packet RAM requested by the BIU and by the DMA blocks. BIU requests represent pipelined CPU accesses to the Data Register, while DMA requests represent CSMA/CD data movement. The external memory used is a 25ns SRAM.

The Arbiter is also responsible for controlling the nRWE0-nRWE3 lines as a function of the bytes being written. Read accesses are always 32 bit wide, and the Arbiter steers the appropriate byte(s) to the appropriate lanes as a function of the address.

The CPU Data Path consists of two uni-directional FIFOs mapped at the Data Register location. These FIFOs can be accessed in any combination of bytes, word, or doublewords. The Arbiter will indicate 'Not Ready' whenever a cycle is initiated that cannot be satisfied by the present state of the FIFO.

### 4.2.3 MMU Block

The Hardware Memory Management Unit allocates memory and transmit and receive packet queues. It also determines the value of the transmit and receive interrupts as a function of the queues. The page size is 2k, with a maximum memory size of 128k. MIR and MCR values are interpreted in 512 byte units.

### 4.2.4 BIU Block

The Bus Interface Unit can handle synchronous as well as asynchronous buses; different signals are used for each one. Transparent latches are added on the address path using rising nADS for latching.

When working with an asynchronous bus like ISA, the read and write operations are controlled by the edges of nRD and nWR. ARDY is used for notifying the system that it should extend the access cycle. The leading edge of ARDY is generated by the leading edge of nRD or nWR while the trailing edge of ARDY is controlled by the internal LAN91C100FD clock and, therefore, asynchronous to the bus.

In the synchronous VL Bus type mode, nCYCLE and LCLK are used to for read and write operations. Completion of the cycle may be determined by using nSRDY. nSRDY is controlled by LCLK and synchronous to the bus.

Direct 32 bit access to the Data Path is supported by using the nDATACS input. By asserting nDATACS, external DMA type of devices will bypass the BIU address decoders and can sequentially access memory with no CPU intervention. nDATACS accesses can be used in the EISA DMA burst mode (nVLBUS=1) or in asynchronous cycles. These cycles MUST be 32 bit cycles. Please refer to the corresponding timing diagrams for details on these cycles.

The BIU is implemented using the following principles:

### 4.2.5 MAC-PHY Interface Block

Two separate interfaces are defined, one for the 10 Mbps bit rate interface and one for the MII 100 Mbps and 10 Mbps nibble rate interface. The 10 Mbps ENDEC interface comprises the signals used for interfacing Ethernet ENDECs. The 100 Mbps interface follows the MII for 100 Mbps 802.3 networks proposal, and it is based on transferring nibbles between the MAC and the PHY.

For the MII interface, transmit data is clocked out using the TX25 clock input, while receive data is clocked in using RX25.

In 100 Mbps mode, the LAN91C100FD provides the following interface signals to the PHY:

- For transmission: TXEN100 TXD0-3 TX25
- For reception: RX\_DV RX\_ER RXD0-3 RX25
- For CSMA/CD state machines: CRS100 COL100

A transmission begins by TXEN100 going active (high), and TXD0-TXD3 having the first valid preamble nibble. TXD0 carries the least significant bit of the nibble (that is the one that would go first out of the EPH



at 100 Mbps), while TXD3 carries the most significant bit of the nibble. TXEN100 and TXD0-TXD3 are clocked by the LAN91C100FD using TX25 rising edges. TXEN100 goes inactive at the end of the packet on the last nibble of the CRC.

During a transmission, COL100 might become active to indicate a collision. COL100 is asynchronous to the LAN91C100FD's clocks and will be synchronized internally to TX25.

Reception begins when RX\_DV (receive data valid) is asserted. A preamble pattern or flag octet will be present at RXD0-RXD3 when RX\_DV is activated. The LAN91C100FD requires no training sequence beyond a full flag octet for reception. RX\_DV as well as RXD0-RXD3 are sampled on RX25 rising edges. RXD0 carries the least significant bit and RXD3 the most significant bit of the nibble. RX\_DV goes inactive when the last valid nibble of the packet (CRC) is presented at RXD0-RXD3.

RX\_ER might be asserted during packet reception to signal the LAN91C100FD that the present receive packet is invalid. The LAN91C100FD will discard the packet by treating it as a CRC error.

When MIISEL=1, RXD0-RXD3 should always be aligned to packet nibbles, therefore, opening flag detection does not consider misaligned cases. Opening flag detection expects the 5Dh pattern and will not reject the packet on non-preamble patterns. When MIISEL=0 the opening flag detection expects a "10101011" pattern and will use it for determining nibble alignment.

CRS100 is used as a frame envelope signal for the CSMA/CD MAC state machines (deferral and backoff functions), but it is not used for receive framing functions. CRS100 is an asynchronous signal and it will be active whenever there is activity on the cable, including LAN91C100FD transmissions and collisions.

Switching between the ENDEC and MII interfaces is controlled by the MII SELECT bit in the CONFIG REGISTER. The MIISEL pin reflects the value of this bit and may be used to control external multiplexing logic.

Note that given the modular nature of the MII, TX25 and RX25 cannot be assumed to be free running clocks. The LAN91C100FD will not rely on the presence of TX25 and RX25 during reset and will use its own internal clock whenever a timeout on TX25 is detected.

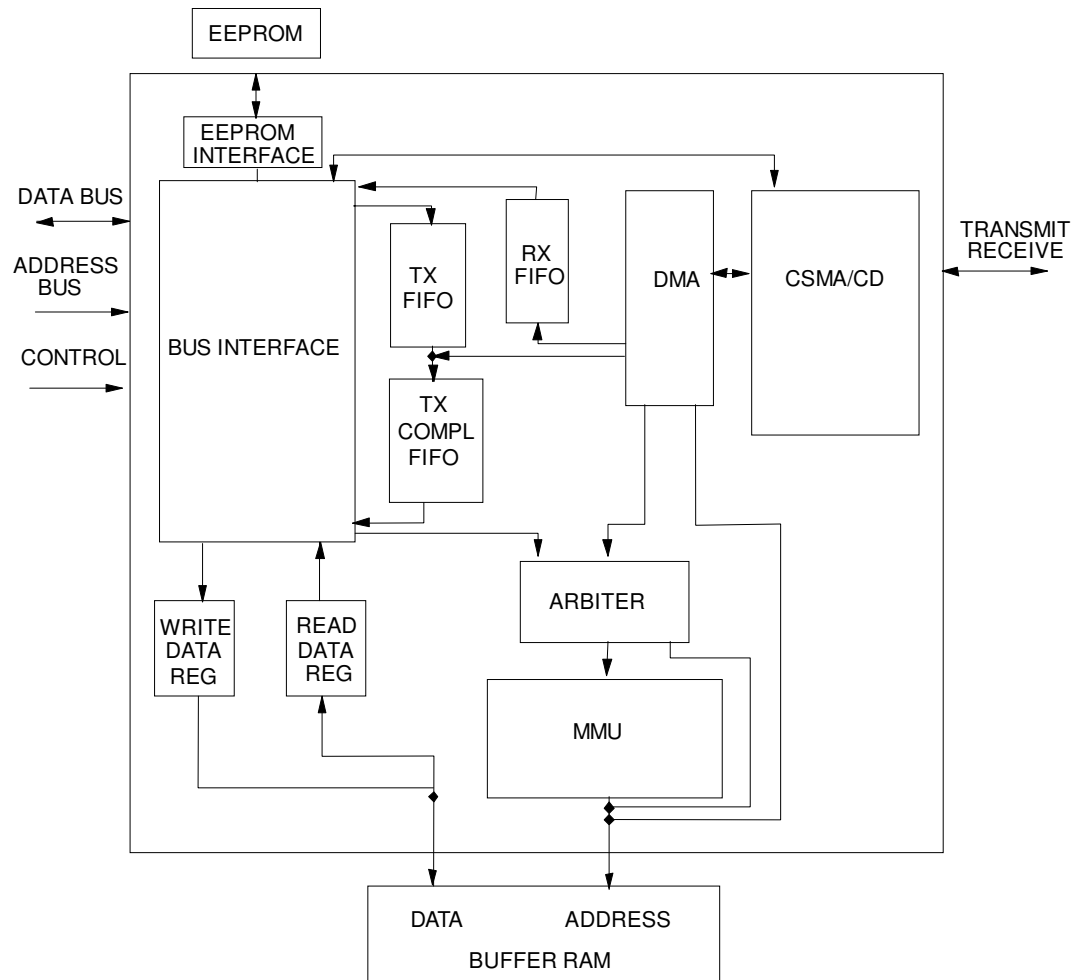
## 4.2.6 MII Management Interface Block

PHY management through the MII management interface is supported by the LAN91C100FD by providing the means to drive a tri-statable data output, a clock, and reading an input. Timing and framing for each management command is to be generated by the CPU.

## 4.2.7 Serial EEPROM Interface

This block is responsible for reading the serial EEPROM upon hardware reset (or equivalent command) and defining defaults for some key registers. A write operation is also implemented by this block, that under CPU command will program specific locations in the EEPROM. This block is an autonomous state machine and controls the internal Data Bus of the LAN91C100FD during active operation.



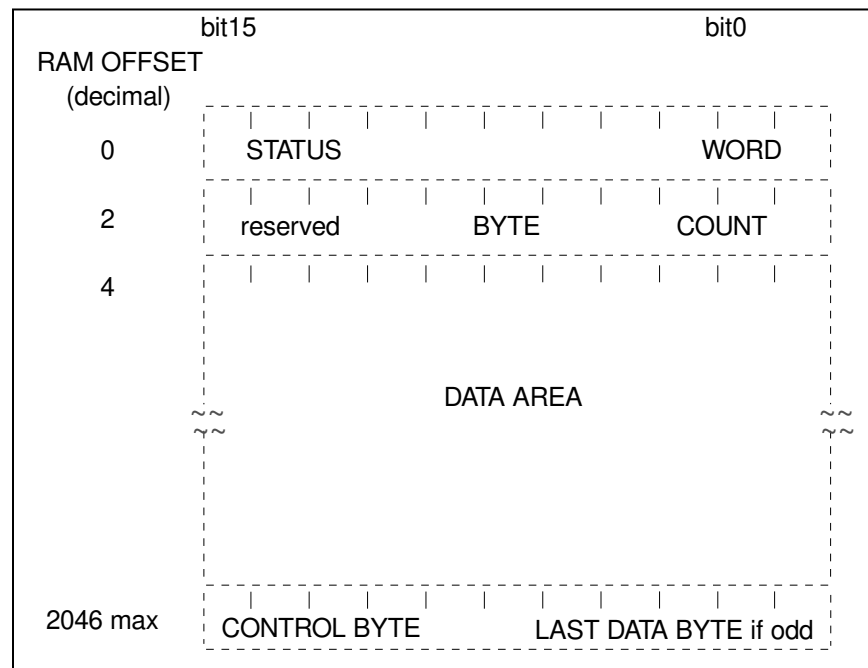


**Figure 4.1 - LAN91C100FD Internal Block Diagram with Data Path**

## Chapter 5 Data Structures and Registers

### 5.1 Packet Format in Buffer Memory

The packet format in memory is similar for the Transmit and Receive areas. The first word is reserved for the status word. The next word is used to specify the total number of bytes, and it is followed by the data area. The data area holds the packet itself.



**Figure 5.1 - Data Packet Format**

	TRANSMIT PACKET	RECEIVE PACKET
STATUS WORD	Written by CSMA upon transmit completion (see Status Register)	Written by CSMA upon receive completion (see RX Frame Status Word)
BYTE COUNT	Written by CPU	Written by CSMA
DATA AREA	Written/modified by CPU	Written by CSMA
CONTROL BYTE	Written by CPU to control odd/even data bytes	Written by CSMA; also has odd/even bit

BYTE COUNT - Divided by two, it defines the total number of words including the STATUS WORD, the BYTE COUNT WORD, the DATA AREA and the CONTROL BYTE.

The receive byte count always appears as even; the ODDFRM bit of the receive status word indicates if the low byte of the last word is relevant.

The transmit byte count least significant bit will be assumed 0 by the controller regardless of the value written in memory.

**DATA AREA** - The data area starts at offset 4 of the packet structure and can extend up to 2043 bytes.

The data area contains six bytes of **DESTINATION ADDRESS** followed by six bytes of **SOURCE ADDRESS**, followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The LAN91C100FD does not insert its own source address. On receive, all bytes are provided by the CSMA side.

The 802.3 Frame Length word (Frame Type in Ethernet) is not interpreted by the LAN91C100FD. It is treated transparently as data both for transmit and receive operations.

**CONTROL BYTE** - For transmit packets the CONTROL BYTE is written by the CPU as:

X	X	ODD	CRC	0	0	0	0
---	---	-----	-----	---	---	---	---

**ODD** - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE is not transmitted.

**CRC** - When set, CRC will be appended to the frame. This bit has only meaning if the NOCRC bit in the TCR is set.

For receive packets the CONTROL BYTE is written by the controller as:

0	1	ODD	0	0	0	0	0
---	---	-----	---	---	---	---	---

**ODD** - If set, indicates an odd number of bytes, with the last byte being right before the CONTROL BYTE. If clear, the number of data bytes is even and the byte before the CONTROL BYTE should be ignored.

## RECEIVE FRAME STATUS WORDRECEIVE FRAME STATUS WORD

This word is written at the beginning of each receive frame in memory. It is not available as a register.

HIGH BYTE	ALGN ERR	BROD CAST	BAD CRC	ODD FRM	TOOLNG	TOO SHORT		
	HASH VALUE							MULT CAST
LOW BYTE		5	4	3	2	1	0	



**ALGNERR** - Frame had alignment error. When MII SEL=1 alignment error is set when BADCRC=1 and an odd number of nibbles was received between SFD and RX\_DV going inactive. When MII SEL=0 alignment error is set when BADCRC=1 and the number of bits received between SFD and the CRS going inactive is not an octet multiple.

**BROADCAST** - Receive frame was broadcast.

**BADCRC** - Frame had CRC error, or RX\_ER was asserted during reception.

**ODDFRM** - This bit when set indicates that the received frame had an odd number of bytes.

**TOOLNG** - Frame length was longer than 802.3 maximum size (1518 bytes on the cable).

**TOOSHORT** - Frame length was shorter than 802.3 minimum size (64 bytes on the cable).

**HASH VALUE** - Provides the hash value used to index the Multicast Registers. Can be used by receive routines to speed up the group address search. The hash value consists of the six most significant bits of the CRC calculated on the Destination Address, and maps into the 64 bit multicast table. Bits 5,4,3 of the hash value select a byte of the multicast table, while bits 2,1,0 determine the bit within the byte selected. Examples of the address mapping:

ADDRESS	HASH VALUE 5-0	MULTICAST TABLE BIT
ED 00 00 00 00 00	000 000	MT-0 bit 0
0D 00 00 00 00 00	010 000	MT-2 bit 0
01 00 00 00 00 00	100 111	MT-4 bit 7
2F 00 00 00 00 00	111 111	MT-7 bit 7

**MULTICAST** - Receive frame was multicast. If hash value corresponds to a multicast table bit that is set, and the address was a multicast, the packet will pass address filtering regardless of other filtering criteria.

## I/O SPACE

The base I/O space is determined by the IOS0-IOS2 inputs and the EEPROM contents. To limit the I/O space requirements to 16 locations, the registers are assigned to different banks. The last word of the I/O area is shared by all banks and can be used to change the bank in use. Registers are described using the following convention:

	OFFSET		NAME		TYPE		SYMBOL	
HIGH BYTE	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
	X	X	X	X	X	X	X	X
LOW BYTE	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	X	X	X	X	X	X	X	X

**OFFSET** - Defines the address offset within the IOBASE where the register can be accessed at, provided the bank select has the appropriate value.

The offset specifies the address of the even byte (bits 0-7) or the address of the complete word.

The odd byte can be accessed using address (offset + 1).

Some registers (like the Interrupt Ack., or like Interrupt Mask) are functionally described as two eight bit registers, in that case the offset of each one is independently specified.

Regardless of the functional description, all registers can be accessed as doublewords, words or bytes.

The default bit values upon hard reset are highlighted below each register.

**Table 5.1 - Internal I/O Space Mapping**

	<b>BANK0</b>	<b>BANK1</b>	<b>BANK2</b>	<b>BANK3</b>
0	TCR	CONFIG	MMU COMMAND	MT0-1
2	EPH STATUS	BASE	PNR ARR	MT2-3
4	RCR	IA0-1	FIFO PORTS	MT4-5
6	COUNTER	IA2-3	POINTER	MT6-7
8	MIR	IA4-5	DATA	MGMT
A	MCR	GENERAL PURPOSE	DATA	REVISION
C	RESERVED (0)	CONTROL	INTERRUPT	RCV
E	BANK SELECT	BANK SELECT	BANK SELECT	BANK SELECT

A special BANK (BANK7) exists to support the addition of external registers.

#### **BANK SELECT REGISTER**

	<b>OFFSET E</b>	<b>NAME BANK SELECT REGISTER</b>	<b>TYPE READ/WRITE</b>	<b>SYMBOL BSR</b>
HIGH BYTE	0	0	1	1
	0	0	1	0
LOW BYTE				BS2
				BS1
				BS0
	X	X	X	0
				0
				0

BS2, BS1, BS0 Determine the bank presently in use. This register is always accessible and is used to select the register bank in use.

The upper byte always reads as 33h and can be used to help determine the I/O location of the LAN91C100FD.

The BANK SELECT REGISTER is always accessible regardless of the value of BS0-2.

**Note:** The bank select register can be accessed as a doubleword at offset Ch, as a word at offset Eh, or as at offset Fh, however a doubleword write to offset Ch will write the BANK SELECT REGISTER but will not write the registers Ch and Dh.

BANK 7 has no internal registers other than the BANK SELECT REGISTER itself. On valid cycles where BANK7 is selected (BS0=BS1=BS2=1), and A3=0, nCSOUT is activated to facilitate implementation of external registers.

**Note:** BANK7 does not exist in LAN91C9x devices. For backward S/W compatibility BANK7 accesses should be done if the Revision Control register indicates the device is the LAN91C100FD.



**BANK 0**

OFFSET	NAME	TYPE	SYMBOL
0	TRANSMIT CONTROL REGISTER	READ/WRITE	TCR

This register holds bits programmed by the CPU to control some of the protocol transmit options.

HIGH BYTE	SWFDUP	0	EPH LOOP	STP SQET	FDUPLX	MON_CSN	0	NOCRC
	0	0	0	0	0	0	0	0
LOW BYTE	PAD_EN	0	0	0	0	FORCOL	LOOP	TXENA
	0	0	0	0	0	0	0	0

**SWFDUP** - Enables Switched Full Duplex mode. In this mode, transmit state machine is inhibited from recognizing carrier sense, so deferrals will not occur. Also inhibits collision count, therefore, the collision related status bits in the EPHSR are not valid (CTR\_ROL, LATCOL, SQET, 16COL, MUL COL, and SNGL COL). Uses COL100 as flow control, limiting backoff and jam to 1 clock each before inter-frame gap, then retry will occur after IFG. If COL100 is active during preamble, full preamble will be output before jam. When SWFDUP is high, the values of FDUPLX and MON\_CSN have no effect. This bit should be low for non-MII operation.

**EPH\_LOOP** - Internal loopback at the EPH block. Serial data is internally looped back when set. Defaults low. When EPH\_LOOP is high the following transmit outputs are forced inactive: TXD0-TXD3 = 0h, TXEN100 = TXEN = 0, TXD = 1. The following and external inputs are blocked: CRS=CRS100=0, COL=COL100=0, RX\_DV= RX\_ER=0.

**STP\_SQET** - Stop transmission on SQET error. If set, stops and disables transmitter on SQE test error. Does not stop on SQET error and transmits next frame if clear. Defaults low.

**FDUPLX** - When set, the LAN91C100FD will cause frames to be received if they pass the address filter regardless of the source of the frame. When clear, the node will not receive a frame sourced by itself. This bit does not control the duplex mode operation, the duplex mode operation is controlled by the SWFDUP bit.

**MON\_CSN** - When set the LAN91C100FD monitors carrier while transmitting. It must see its own carrier by the end of the preamble. If it is not seen, or if carrier is lost during transmission, the transmitter aborts the frame without CRC and turns itself off and sets the LOST CARR bit in the EPHSR. When this bit is clear the transmitter ignores its own carrier. Defaults low. Should be 0 for MII operation.

**NOCRC** - Does not append CRC to transmitted frames when set. Allows software to insert the desired CRC. Defaults to zero, namely CRC inserted.

**PAD\_EN** - When set, the LAN91C100FD will pad transmit frames shorter than 64 bytes with 00. The CPU should write the actual byte count (1 – 1514/1518) into the BYTE COUNT area in the transmit buffer RAM. If the CPU provides the 4 byte CRC, the maximum byte count will be 1518. If the CPU elects to have the LAN91C100FD provide the CRC, the maximum byte count will be 1514. The CPU should then write the actual packet data in the DATA AREA of the transmit buffer RAM. The LAN91C100FD will then determine if padding is necessary, (BYTE COUNT AREA less than 64). If padding is required, the LAN91C100FD will append data bytes of 00 to meet the minimum requirement of 64 bytes. When this bit is cleared, the LAN91C100FD does not pad frames.

**FORCOL** - When set, the FORCOL bit will force a collision by not deferring deliberately. This bit is set and cleared only by the CPU. When TXENA is enabled with no packets in the queue and while the FORCOL bit is set, the LAN91C100FD will transmit a preamble pattern the next time a carrier is seen on the line. If a packet is queued, a preamble and SFD will be transmitted. This bit defaults low to normal operation. NOTE: The LATCOL bit in the EPHSR, setting up as a result of FORCOL, will reset TXENA to 0. In order to force another collision, TXENA must be set to 1 again.

LOOP - Loopback. General purpose output port used to control the LBK pin. Typically used to put the PHY chip in loopback mode.

TXENA - Transmit enabled when set. Transmit is disabled if clear. When the bit is cleared the LAN91C100FD will complete the current transmission before stopping. When stopping due to an error, this bit is automatically cleared.

## BANK 0

OFFSET	NAME	TYPE	SYMBOL
2	EPH STATUS REGISTER	READ ONLY	EPHSR

This register stores the status of the last transmitted frame. This register value, upon individual transmit packet completion, is stored as the first word in the memory area allocated to the packet. Packet interrupt processing should use the copy in memory as the register itself will be updated by subsequent packet transmissions. The register can be used for real time values (like TXENA and LINK OK). If TXENA is cleared the register holds the last packet completion status.

HIGH BYTE	Reserved	LINK_ OK	0	CTR _ROL	EXC _DEF	LOST CARR	LATCOL	0
	0	-nLNK pin	0	0	0	0	0	0
LOW BYTE	TX DEFR	LTX BRD	SQET	16COL	LTX MULT	MUL COL	SNGL COL	TX_SUC
	0	0	0	0	0	0	0	0

LINK\_OK - General purpose input port driven by nLNK pin inverted. Typically used for Link Test. A transition on the value of this bit generates an interrupt.

CTR\_ROL - Counter Roll Over. When set one or more 4 bit counters have reached maximum count (15). Cleared by reading the ECR register.

EXC\_DEF - Excessive Deferral. When set last/ current transmit was deferred for more than 1518 \* 2 byte times. Cleared at the end of every packet sent.

LOST\_CARR - Lost Carrier Sense. When set indicates that Carrier Sense was not present at end of preamble. Valid only if MON\_CSN is enabled. This condition causes TXENA bit in TCR to be reset. Cleared by setting TXENA bit in TCR.

LATCOL - Late collision detected on last transmit frame. If set a late collision was detected (later than 64 byte times into the frame). When detected the transmitter jams and turns itself off clearing the TXENA bit in TCR. Cleared by setting TXENA in TCR.

TX\_DEFR - Transmit Deferred. When set, carrier was detected during the first 6.4  $\mu$ s of the inter frame gap. Cleared at the end of every packet sent.

LTX\_BRD - Last transmit frame was a broadcast. Set if frame was broadcast. Cleared at the start of every transmit frame.

SQET - Signal Quality Error Test. In MII, SQET bit is always set after first transmit, except if SWFDUP=1. As a consequence, the STP\_SQET bit in the TCR register cannot be set as it will always result in transmit fatal error. In non-MII systems, the transmitter opens a 1.6  $\mu$ s window 0.8  $\mu$ s after transmission is completed and the receiver returns inactive. During this window, the transmitter expects to see the SQET signal from the transceiver. The absence of this signal is a 'Signal Quality Error' and is reported in this status bit. Transmission stops and EPH INT is set if STP\_SQET is in the TCR is also set when SQET is set. This bit is cleared by setting TXENA high.



**16COL** - 16 collisions reached. Set when 16 collisions are detected for a transmit frame. TXENA bit in TCR is reset. Cleared when TXENA is set high.

**LTX\_MULT** - Last transmit frame was a multicast. Set if frame was a multicast. Cleared at the start of every transmit frame.

**MULCOL** - Multiple collision detected for the last transmit frame. Set when more than one collision was experienced. Cleared when TX\_SUC is high at the end of the packet being sent.

**SNGLCOL** - Single collision detected for the last transmit frame. Set when a collision is detected. Cleared when TX\_SUC is high at the end of the packet being sent.

**TX\_SUC** - Last transmit was successful. Set if transmit completes without a fatal error. This bit is cleared by the start of a new frame transmission or when TXENA is set high. Fatal errors are:

- 16 collisions (1/2 duplex mode only)
- SQET fail and STP\_SQET = 1 (1/2 duplex mode only)
- Carrier lost and MON\_CSN = 1 (1/2 duplex mode only)
- Late collision (1/2 duplex mode only)

#### **BANK 0**

OFFSET		NAME		TYPE		SYMBOL	
4		RECEIVE CONTROL REGISTER		READ/WRITE		RCR	
HIGH BYTE	SOFT RST	FILT CAR	ABORT_E NB	0	Reserved	Reserved	STRIP CRC
	0	0	0	0	0	0	0
LOW BYTE	Reserved	Reserved	Reserved	Reserved	Reserved	ALMUL	PRMS
	0	0	0	0	0	0	0

**SOFT\_RST** - Software-Activated Reset. Active high. Initiated by writing this bit high and terminated by writing the bit low. The LAN91C100FD's configuration is not preserved except for Configuration, Base, and IA0-IA5 Registers. EEPROM is not reloaded after software reset.

**FILT\_CAR** - Filter Carrier. When set filters leading edge of carrier sense for 12 bit times (3 nibble times). Otherwise recognizes a receive frame as soon as carrier sense is active. (Does NOT filter RX DV on MII)

**ABORT\_ENB** - Enables abort of receive when collision occurs. Defaults low. When set, the LAN91C100FD will automatically abort a packet being received when the appropriate collision input is activated (COL100 for MII, COL for non-MII). This bit has no effect if the SWFDUP bit in the TCR is set.

**STRIP\_CRC** - When set it strips the CRC on received frames. When clear the CRC is stored in memory following the packet. Defaults low.

**RXEN** - Enables the receiver when set. If cleared, completes receiving current frame and then goes idle. Defaults low on reset.

**ALMUL** - When set accepts all multicast frames (frames in which the first bit of DA is '1'). When clear accepts only the multicast frames that match the multicast table setting. Defaults low.

**PRMS** - Promiscuous mode. When set receives all frames. Does not receive its own transmission unless it is in Full Duplex!

**RX\_ABORT** - This bit is set if a receive frame was aborted due to length longer than 2K bytes. The frame will not be received. The bit is cleared by RESET or by the CPU writing it low.