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LAN91C113

16-Bit 10/100 Non-PCI Ethernet Single Chip MAC + PHY

Datasheet

Product Features

- Single Chip Ethernet Controller
- Dual Speed - 10/100 Mbps
- Fully Supports Full Duplex Switched Ethernet
- 8 Kbytes Internal Memory for Receive and Transmit FIFO Buffers
- Enhanced Power Management Features
- Optional Configuration via Serial EEPROM Interface
- Supports 8, 16 Bit CPU Accesses
- Internal 16 Bit Wide Data Path (Into Packet Buffer Memory)
- Early TX, Early RX Functions
- Built-in Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- 3.3V Operation with 5V Tolerant IO Buffers (See Pin List Description for Additional Details)
- Single 25 MHz Reference Clock for Both PHY and MAC
- External 25Mhz-output pin for an external PHY supporting PHYs physical media.
- Low Power CMOS Design
- Supports Multiple Embedded Processor Host Interfaces
  - ARM
  - SH
  - Power PC
  - Coldfire
  - 680X0, 683XX
  - MIPS R3000
- 3.3V MII (Media Independent Interface) MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- 128 Pin QFP Package; Green, Lead-Free Package also available
- 128 Pin TQFP Package, 1.0 mm height; Green, Lead-Free Package also available
- Temperature Range from 0°C to 85°C

Network Interface

- Fully Integrated IEEE 802.3/802.3u-100Base-TX / 10Base-T Physical Layer
- Auto Negotiation: 10/100, Full / Half Duplex
- On Chip Wave Shaping - No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs (User selectable – Up to 2 LED functions at one time)
  - Link
  - Activity
  - Full Duplex
  - 10/100
  - Transmit
  - Receive

ORDERING INFORMATION

Order Number(s):

LAN91C113-NC for 128 Pin QFP Package
LAN91C113-NE for 128 Pin TQFP Package (1.0 mm height)
LAN91C113-NS for 128 Pin QFP Package (Green, Lead-Free)
LAN91C113-NU for 128 Pin TQFP Package (1.0 mm height) (Green, Lead-Free)

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Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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Chapter 1 General Description

The SMSC LAN91C113 is designed to facilitate the implementation of a third generation of Fast Ethernet connectivity solutions for embedded applications. For this third generation of products, flexibility and integration dominate the design requirements. The LAN91C113 is a mixed signal Analog/Digital device that implements the MAC and PHY portion of the CSMA/CD protocol at 10 and 100 Mbps. The design will also minimize data throughput constraints utilizing a 16-bit or 8-bit bus Host interface in embedded applications.

The total internal memory FIFO buffer size is 8 Kbytes, which is the total chip storage for transmit and receive operations.

The SMSC LAN91C113 is software compatible with the LAN9000 family of products.

Memory management is handled using a patented optimized MMU (Memory Management Unit) architecture and a 16-bit wide internal data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions.

The SMSC 91C113 provides a flexible slave interface for easy connectivity with industry-standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous transfers, with different signals being used for each one. Asynchronous bus support for ISA is supported even though ISA cannot sustain 100 Mbps traffic. Fast Ethernet data rates are attainable for ISA-based nodes on the basis of the aggregate traffic benefits.

Two different interfaces are supported on the network side. The first Interface is a standard Magnetics transmit/receive pair interfacing to 10/100Base-T utilizing the internal physical layer block. The second interface follows the MII (Media Independent Interface) specification standard, consisting of 4 bit wide data transfers at the nibble rate. This interface is applicable to 10 Mbps standard Ethernet or 100 Mbps Ethernet networks. Three of the LAN91C113's pins are used to interface to the two-line MII serial management protocol.

The SMSC LAN91C113 integrates IEEE 802.3 Physical Layer for twisted pair Ethernet applications. The PHY can be configured for either 100 Mbps (100Base-TX) or 10 Mbps (10Base-T) Ethernet operation. The Analog PHY block consists of a 4B5B/Manchester encoder/decoder, scrambler/de-scrambler, transmitter with wave shaping and output driver, twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, Auto-Negotiation, controller interface (MII), and serial port (MI). Internal output wave shaping circuitry and on-chip filters eliminate the need for external filters normally required in 100Base-TX and 10Base-T applications.

The LAN91C113 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip Auto-Negotiation algorithm. The LAN91C113 is ideal for media interfaces for embedded application desiring Ethernet connectivity as well as 100Base-TX/10Base-T adapter cards, motherboards, repeaters, switching hubs. The LAN91C113 operates from a single 3.3V supply. The inputs and outputs of the host Interface are 5V tolerant and will directly interface to other 5V devices.

Chapter 2 Pin Configurations

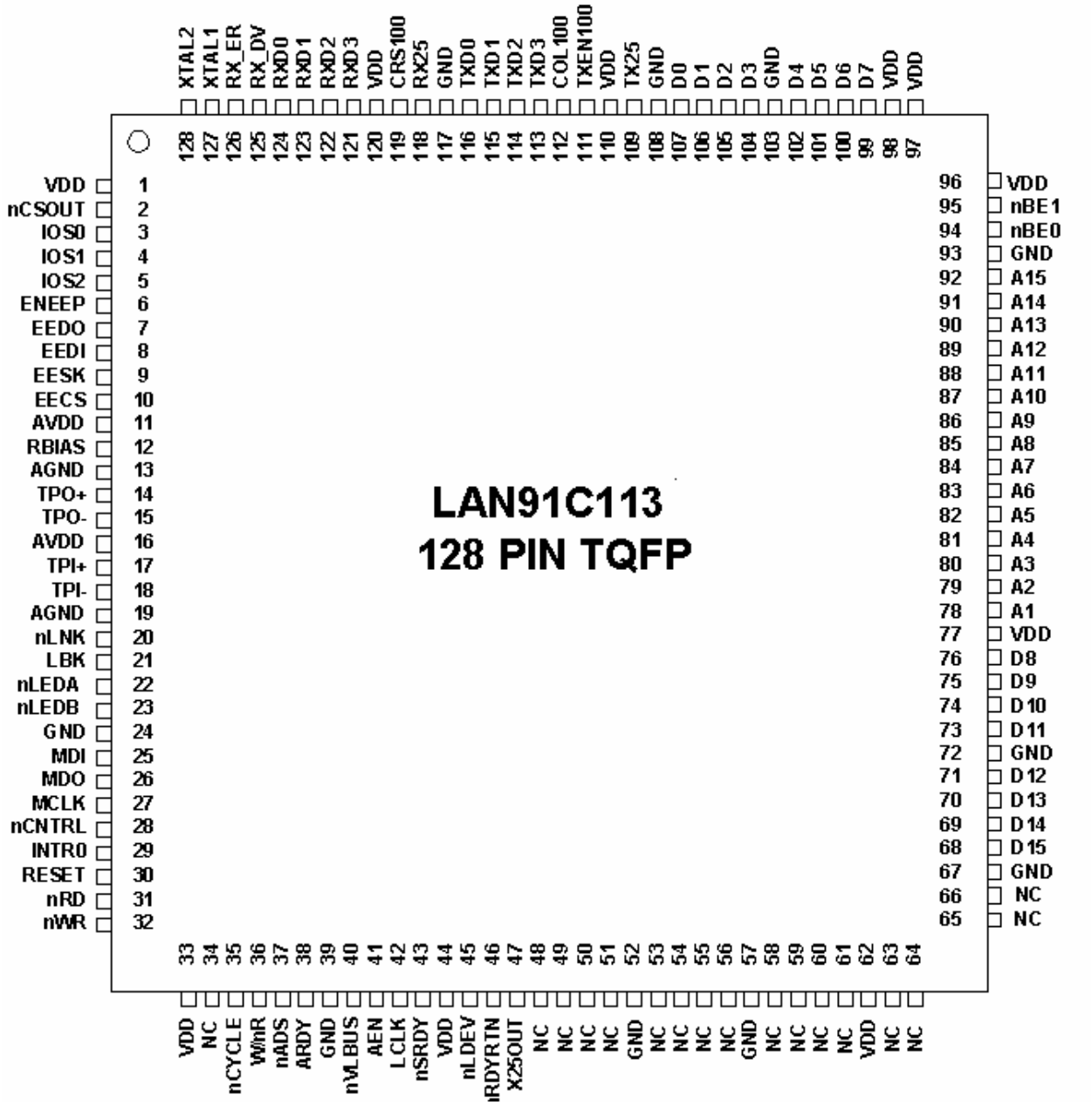

Figure 2.1 - Pin Configuration - LAN91C113 128 Pin TQFP

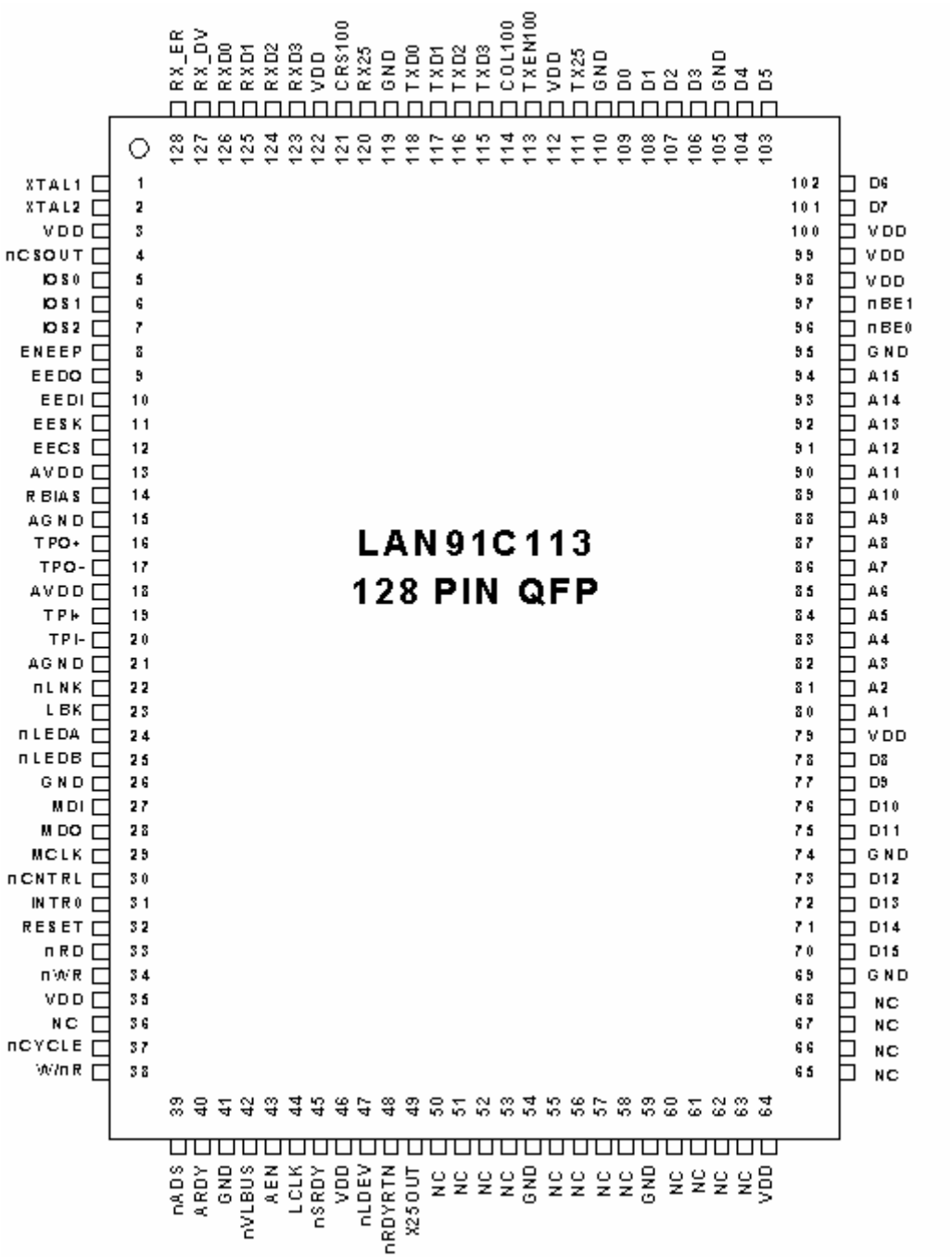

Figure 2.2 - Pin Configuration - LAN91C113 128 Pin QFP

Chapter 3 Block Diagrams

The diagram shown in Figure 3.1 - LAN91C113 - Basic Functional Block Diagram, describes the device basic functional blocks. The SMSC LAN91C113 is a single chip solution for embedded designs with minimal Host and external supporting devices required to implement 10/100 Ethernet connectivity solutions.

The optional Serial EEPROM is used to store information relating to default IO offset parameters as well as which of the Interrupt line are used by the host.

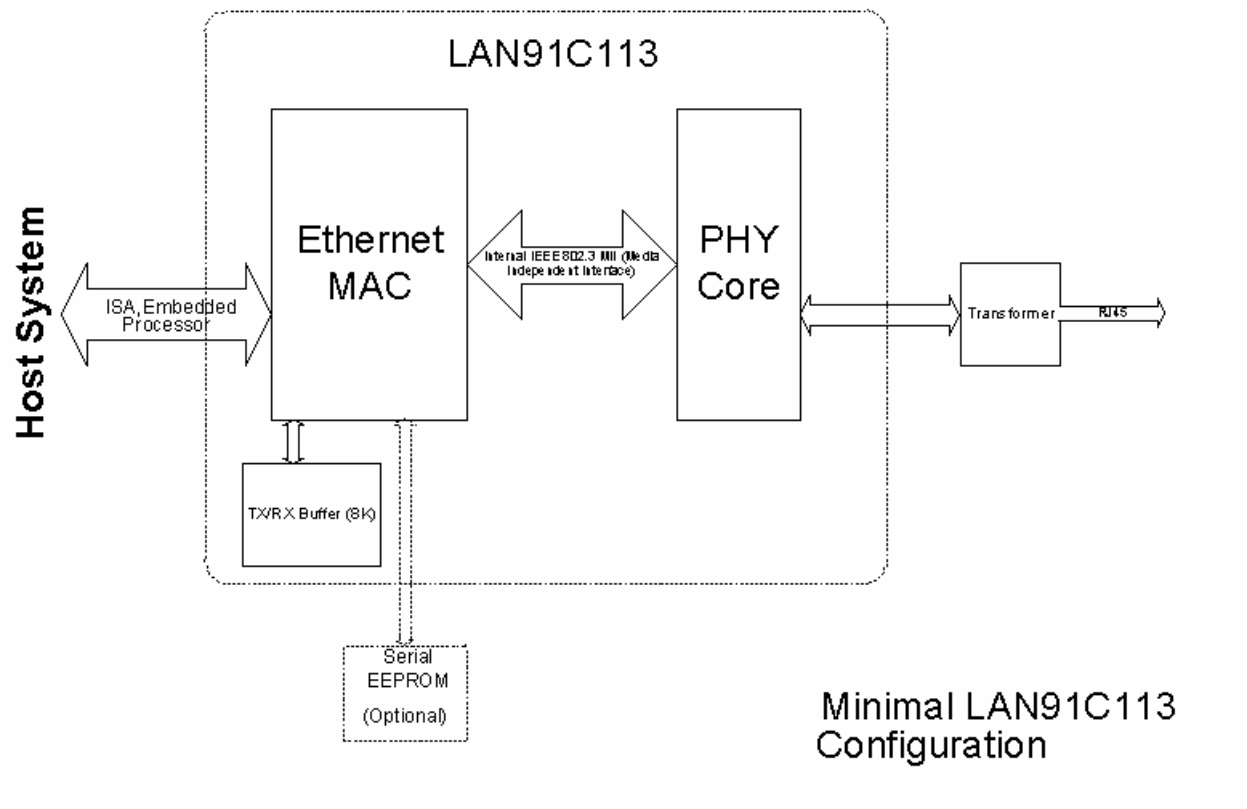

Figure 3.1 - LAN91C113 - Basic Functional Block Diagram

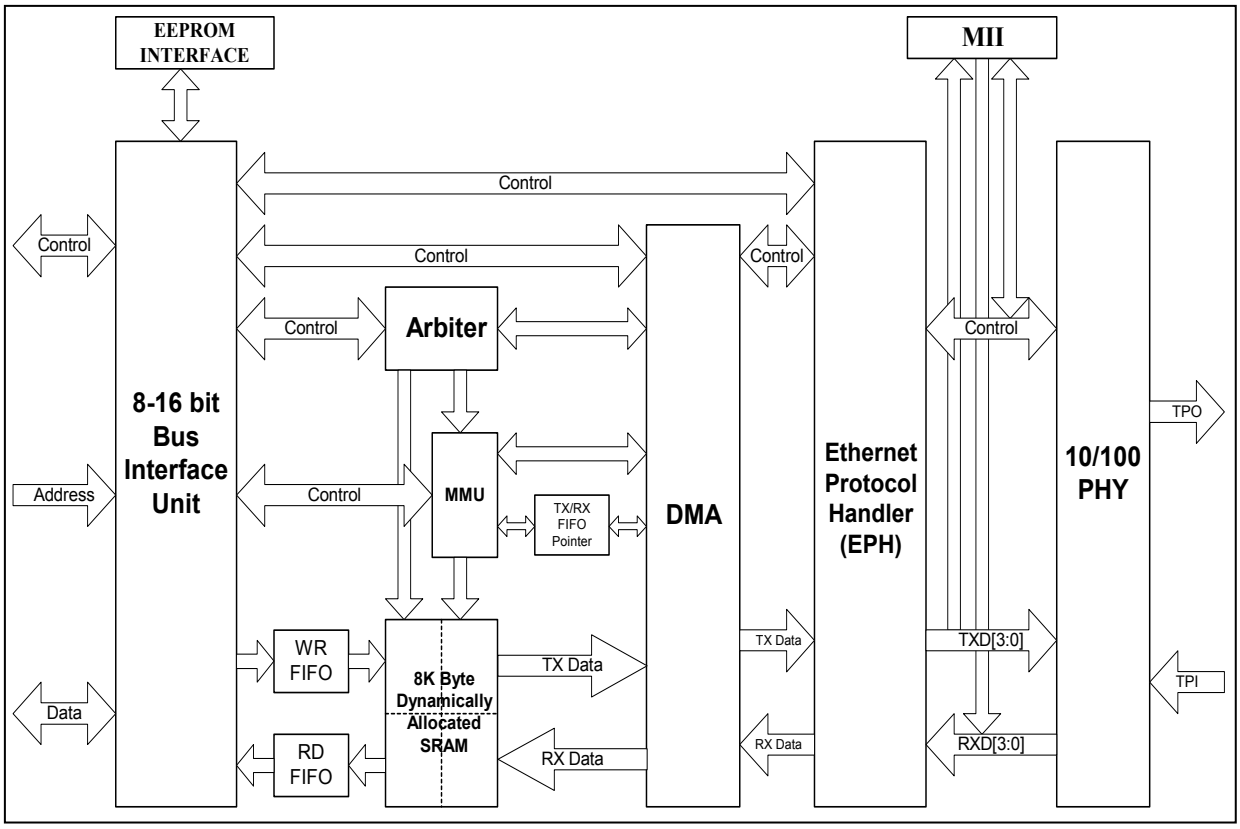

Figure 3.2 - Block Diagram

The diagram shown in Figure 3.2 describes the supported Host interfaces, which include ISA or Generic Embedded. The Host interface is an 8 or 16 bit wide address / data bus with extensions for embedded RISC and ARM processors.

The figure shown next page describes the SMSC LAN91C113 functional blocks required to integrate a 10/100 Ethernet Physical layer framer to the internal MAC.

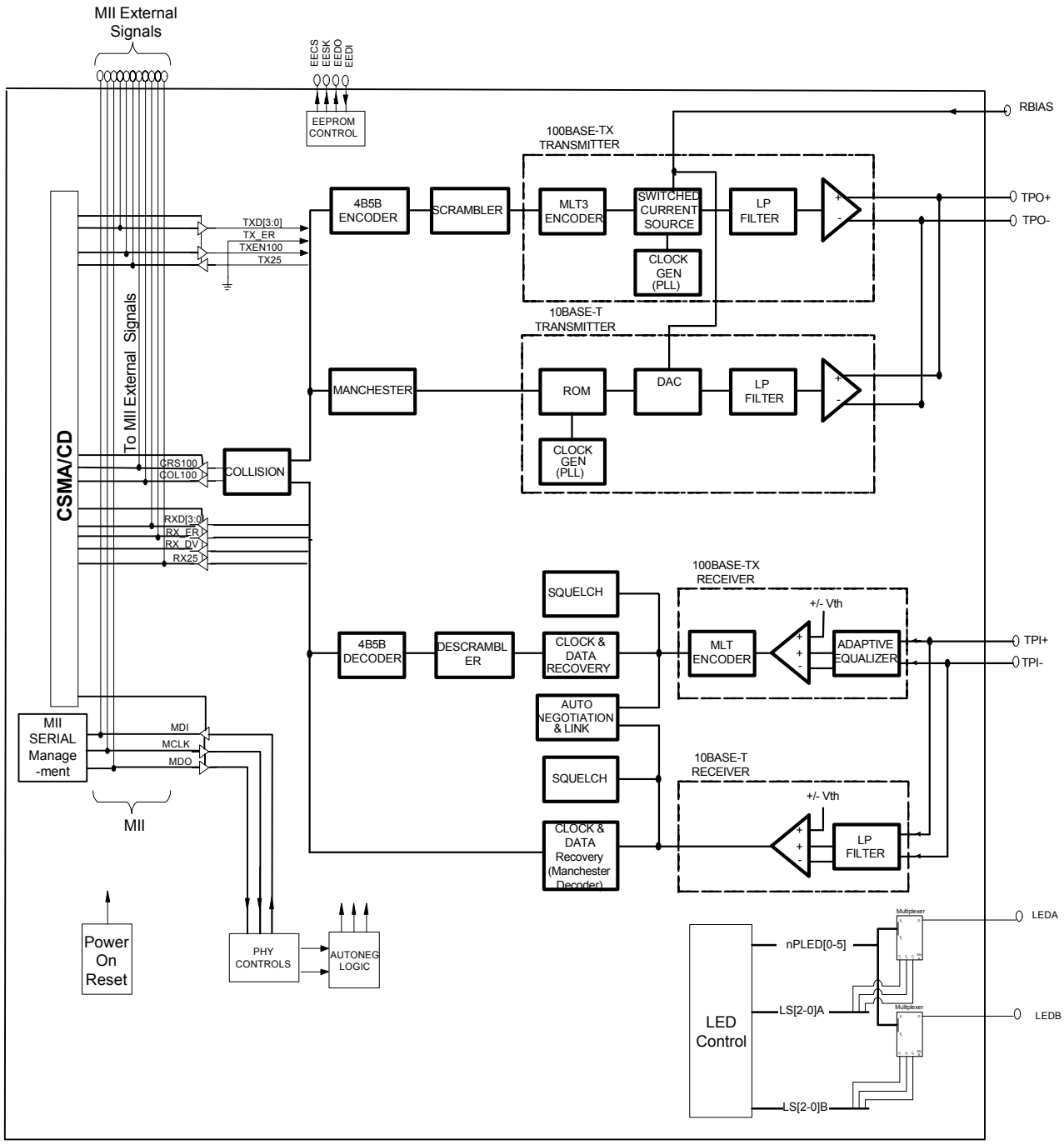

Figure 3.3 - LAN91C113 Physical Layer to Internal Mac Block Diagram

Chapter 4 Signal Descriptions

Table 4.1 - LAN91C113 Pin Requirements (128 Pin QFP and 1.0mm TQFP package)

FUNCTION	PIN SYMBOLS	NUMBER OF PINS
System Address Bus	A1-A15, AEN, nBE0, nBE1	18
System Data Bus	D0-D15	16
System Control Bus	RESET, nADS, LCLK, ARDY, nRDYRTN, nSRDY, INTR0, nLDEV, nRD, nWR, nCYCLE, W/nR, nVLBUS	13
Serial EEPROM	EEDI, EEDO, EECS, EESK, ENEEP, IOS0-IOS2	8
LEDs	nLEDA, nLEDB	2
PHY	TPO+, TPO-, TPI+, TPI-, nLNK, LBK, nCNTRL, RBIAS	8
Crystal Oscillator	XTAL1, XTAL2	2
Power	VDD, AVDD	29
Ground	GND, AGND	12
Physical Interface 100 Mbps	TXEN100, CRS100, COL100, RX_DV, RX_ER, TXD0-TXD3, RXD0-RXD3, MDI, MDO, MCLK, RX25, TX25	18
MISC	nCSOUT, X25OUT,	2
TOTAL		128

Chapter 5 Description of Pin Functions

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
81-92	83-94	Address	A4-A15	I**	Input. Decoded by LAN91C113 to determine access to its registers.
78-80	80-82	Address	A1-A3	I**	Input. Used by LAN91C113 for internal register selection.
41	43	Address Enable	AEN	I**	Input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
94-95	96-97	nByte Enable	nBE0-nBE1	I**	Input. Used during LAN91C113 register accesses to determine the width of the access and the register(s) being accessed.
107-104, 102-99, 76-73, 71-68	109-106, 104-101, 78-75, 73-70	Data Bus	D0-D15	I/O24**	Bidirectional. 16 bit data bus used to access the LAN91C113's internal registers. Data bus has weak internal pullups. Supports direct connection to the system bus without external buffering.
30	32	Reset	RESET	IS**	Input. When this pin is asserted high, the controller performs an internal system (MAC & PHY) reset. It programs all the registers to their default value, the controller will read the EEPROM device through the EEPROM interface. **(Note 5.1)** This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
37	39	nAddress Strobe	nADS	IS**	Input. For systems that require address latching, the rising edge of nADS indicates the latching moment for A1-A15 and AEN. All LAN91C113 internal functions of A1-A15, AEN are latched except for nLDEV decoding.
35	37	nCycle	nCYCLE	I**	Input. This active low signal is used to control LAN91C113 synchronous bus cycles. For write operation, this signal should be asserted one bus clock prior to data valid. For read operation, this signal should be asserted two bus clocks prior to data valid.
36	38	Write/ nRead	W/nR	IS**	Input. Defines the direction of synchronous cycles. Write cycles when high, read cycles when low.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
40	42	nVL Bus Access	nVLBUS	I with pullup**	Input. When low, the LAN91C113 synchronous bus interface is configured for Local Bus mode accesses. Otherwise, the LAN91C113 is configured for EISA accesses. Does not affect the asynchronous bus interface.
42	44	Local Bus Clock	LCLK	I**	Input. Used to interface synchronous buses. Maximum frequency is 50 MHz. This pin should be tied high if it is in asynchronous mode.
38	40	Asynchronous Ready	ARDY	OD16	Open drain output. ARDY may be used when interfacing asynchronous buses to extend accesses. Its rising (access completion) edge is controlled by the XTAL1 clock and, therefore, asynchronous to the host CPU or bus clock.
43	45	nSynchronous Ready	nSRDY	O16	Output. This output is used when interfacing synchronous buses and nVLBUS=0 to extend accesses. This signal remains normally inactive, and its falling edge indicates completion. This signal is synchronous to the bus clock LCLK.
46	48	nReady Return	nRDYRTN	I**	Input. This input is used to complete synchronous read cycles.
29	31	Interrupt	INTR0	O24	Interrupt Output – Active High, it's used to interrupt the Host on a status event. Note: The selection bits used to determined by the value of INT SEL 1-0 bits in the Configuration Register are no longer required and have been set to reserved in this revision of the FEAST family of devices.
45	47	nLocal Device	nLDEV	O16	Output. This active low output is asserted when AEN is low and A4-A15 decode to the LAN91C113 address programmed into the high byte of the Base Address Register. nLDEV is a combinatorial decode of unlatched address and AEN signals.
31	33	nRead Strobe	nRD	IS**	Input. Used in asynchronous bus interfaces.
32	34	nWrite Strobe	nWR	IS**	Input. Used in asynchronous bus interfaces.
9	11	EEPROM Clock	EESK	O4	Output. 4 μsec clock used to shift data in and out of the serial EEPROM.
10	12	EEPROM Select	EECS	O4	Output. Serial EEPROM chip select. Used for selection and command framing of the serial EEPROM.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
7	9	EEPROM Data Out	EEDO	O4	Output. Connected to the DI input of the serial EEPROM.
8	10	EEPROM Data In	EEDI	I with pulldown **	Input. Connected to the DO output of the serial EEPROM.
3-5	5-7	I/O Base	IOS0-IOS2	I with pullup**	Input. External switches can be connected to these lines to select between predefined EEPROM configurations.
6	8	Enable EEPROM	ENEEP	I with pullup**	Input. Enables (when high or open) LAN91C113 accesses to the serial EEPROM. Must be grounded if no EEPROM is connected to the LAN91C113.
127, 128	1, 2	Crystal 1 Crystal 2	XTAL1 XTAL2	Iclk	An external 25 MHz crystal is connected across these pins. If a TTL clock is supplied instead, it should be connected to XTAL1 and XTAL2 should be left open.
1, 33, 44, 62, 77, 98, 110, 120, 96, 97	3, 35, 46, 64, 79, 100, 112, 122, 98, 99	Power	VDD		+3.3V Power supply pins.
11, 16	13, 18	Analog Power	AVDD		+3.3V Analog power supply pins.
24, 39, 52, 57, 67, 72, 93, 103, 108, 117	26, 41, 54, 59, 69, 74, 95, 105, 110, 119	Ground	GND		Ground pins.
13, 19	15, 21	Analog Ground	AGND		Analog Ground pins
21	23	Loopback	LBK	O4	Output. Active when LOOP bit is set (TCR bit 1).
20	22	nLink Status	nLNK	I with pullup	Input. General-purpose input port used to convey LINK status (EPHSR bit 14).
28	30	nCNTRL	nCNTRL	O12	General Purpose Control Pin
47	49	X25out	X25out	O12	25Mhz Output to external PHY
111	113	Transmit Enable 100 Mbps	TXEN100	O12	Output to MII PHY. Envelope to 100 Mbps transmission.
119	121	Carrier Sense 100 Mbps	CRS100	I with pulldown	Input from MII PHY. Envelope of packet reception used for deferral and backoff purposes.
125	127	Receive Data Valid	RX_DV	I with pulldown	Input from MII PHY. Envelope of data valid reception. Used for receive data framing.
112	114	Collision Detect 100 Mbps	COL100	I with pulldown	Input from MII PHY. Collision detection input.

PIN NO.		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
113-116	115-118	Transmit Data	TXD3-TXD0	O12	Outputs. Transmit Data nibble to MII PHY.
109	111	Transmit Clock	TX25	I with pullup	Input. Transmit clock input from MII. Nibble rate clock (25MHz for 100Mbps & 2.5MHz for 10Mbps).
118	120	Receive Clock	RX25	I with pullup	Input. Receive clock input from MII PHY. Nibble rate clock. (25MHz for 100Mbps & 2.5MHz for 10Mbps).
121-124	123-126	Receive Data	RXD3-RXD0	I with pullup	Inputs. Received Data nibble from MII PHY.
25	27	Management Data Input	MDI	I with pulldown	MII management data input.
26	28	Management Data Output	MDO	O4	MII management data output.
27	29	Management Clock	MCLK	O4	MII management clock.
126	128	Receive Error	RX_ER	I with pulldown	Input. Indicates a code error detected by PHY. Used by the LAN91C113 to discard the packet being received. The error indication reported for this event is the same as a bad CRC (Receive Status Word bit 13).
2	4	nChip Select Output	nCSOUT	O4	Output. Chip Select provided for mapping of PHY functions into LAN91C113 decoded space. Active on accesses to LAN91C113's eight lower addresses when the BANK SELECTED is 7.
12	14	External Resistor	RBIAS	NA	Transmit Current Set. An external resistor connected between this pin and GND will set the output current for the TP transmit outputs
14	16		TPO+	O/I	Twisted Pair Transmit Output, Positive.
15	17		TPO-	O/I	Twisted Pair Transmit Output, Negative
17	19		TPI+	I/O	Twisted Pair Receive Input, Positive
18	20		TPI-	I/O	Twisted Pair Receive Input, Negative.
22	24		nLEDA	OD24	PHY LED Output
23	25		nLEDB	OD24	PHY LED Output
34, 48-51, 53-56, 58-61, 63-66	36, 50-53, 55-58, 60-63, 65-68		NC		No Connection

Note 5.1 If the EEPROM is enabled.

5.1 Signal Description Parameters

This section provides a detailed description of each SMSC LAN91C113 signal. The signals are arranged in functional groups according to their associated function.

The 'n' symbol at the beginning of a signal name indicates that it is an active low signal. When 'n' is not present before the signal name, it indicates an active high signal.

The term "assert" or "assertion" indicates that a signal is active; independent of whether that level is represented by a high or low voltage. The term negates or negation indicates that a signal is inactive.

The term High-Z means tri-stated.

The term Undefined means the signal could be high, low, tri-stated, or in some in-between level.

5.2 Buffer Types

O4	Output buffer with 2mA source and 4mA sink
O12	Output buffer with 6mA source and 12mA sink
O16	Output buffer with 8mA source and 16mA sink
O24	Output buffer with 12mA source and 24mA sink
OD16	Open drain buffer with 16mA sink
OD24	Open drain buffer with 24mA sink
I/O4	Bidirectional buffer with 2mA source and 4mA sink
I/O24	Bidirectional buffer with 12mA source and 24mA sink
I/OD	Bidirectional Open drain buffer with 4mA sink
I	Input buffer
IS	Input buffer with Schmitt Trigger Hysteresis
Iclk	Clock input buffer
I/O	Differential Input
O/I	Differential Output
**	5V tolerant. Input pins are able to accept 5V signals

DC levels and conditions defined in the DC Electrical Characteristics section.

Chapter 6 Functional Description

6.1 Clock Generator Block

1) The XTAL1 and XTAL2 pins are to be connected to a 25 MHz crystal.

2) TX25 is an input clock. It will be the nibble rate of the particular PHY connected to the MII (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

3) RX25 - This is the MII nibble rate receive clock used for sampling received data nibbles and running the receive state machine. (2.5 MHz for a 10 Mbps PHY, and 25 MHz for a 100 Mbps PHY).

4) LCLK - Bus clock - Used by the BIU for synchronous accesses. Maximum frequency is 50 MHz for VL BUS mode, and 8.33 MHz for EISA slave DMA.

6.2 CSMA/CD Block

This is a 16 bit oriented block, with fully- independent Transmit and Receive logic. The data path in and out of the block consists of two 16-bit wide uni-directional FIFOs interfacing the DMA block. The DMA port of the FIFO stores 32 bits to exploit the 32 bit data path into memory, but the FIFOs themselves are 16 bit wide. The Control Path consists of a set of registers interfaced to the CPU via the BIU.

6.2.1 DMA Block

This block accesses packet memory on the CSMA/CD's behalf, fetching transmit data and storing received data. It interfaces the CSMA/CD Transmit and Receive FIFOs on one side and the Arbiter block on the other. To increase the bandwidth into memory, a 50 MHz clock is used by the DMA block, and the data path is 32 bits wide.

For example, during active reception at 100 Mbps, the CSMA/CD block will write a word into the Receive FIFO every 160ns. The DMA will read the FIFO and accumulate two words on the output port to request a memory cycle from the Arbiter every 320ns.

The DMA machine is able to support full duplex operation. Independent receive and transmit counters are used. Transmit and receive cycles are alternated when simultaneous receive and transmit accesses are needed.

6.2.2 Arbiter Block

The Arbiter block sequences accesses to packet RAM requested by the BIU and by the DMA blocks. BIU requests represent pipelined CPU accesses to the Data Register, while DMA requests represent CSMA/CD data movement.

Internal SRAM read accesses are always 32 bit wide, and the Arbiter steers the appropriate byte(s) to the appropriate lanes as a function of the address.

The CPU Data Path consists of two uni-directional FIFOs mapped at the Data Register location. These FIFOs can be accessed in any combination of bytes or word. The Arbiter will indicate 'Not Ready' whenever a cycle is initiated that cannot be satisfied by the present state of the FIFO.

6.3 MMU Block

The Hardware Memory Management Unit allocates memory and transmit and receive packet queues. It also determines the value of the transmit and receive interrupts as a function of the queues. The page size is 2048 bytes, with a maximum memory size of 8kbytes. MIR values are interpreted in 2048 byte units.

6.4 BIU Block

The Bus Interface Unit can handle synchronous as well as asynchronous buses; different signals are used for each one. Transparent latches are added on the address path using rising nADS for latching.

When working with an asynchronous bus like ISA, the read and write operations are controlled by the edges of nRD and nWR. ARDY is used for notifying the system that it should extend the access cycle. The leading edge of ARDY is generated by the leading edge of nRD or nWR while the trailing edge of ARDY is controlled by the internal LAN91C113 clock and, therefore, asynchronous to the bus.

In the synchronous VL Bus type mode, nCYCLE and LCLK are used to for read and write operations. Completion of the cycle may be determined by using nSRDY. nSRDY is controlled by LCLK and synchronous to the bus.

The BIU is implemented using the following principles:

1) Address decoding is based on the values of A15-A4 and AEN.
2) Address latching is performed by using transparent latches that are transparent when nADS=0 and nRD=1, nWR=1 and latch on nADS rising edge.
3) Byte and word accesses to all registers and Data Path are supported.
4) No bus byte swapping is implemented (no eight bit mode).
5) Word swapping as a function of A1 is implemented for 16 bit bus support.
6) The asynchronous interface uses nRD and nWR strobes. If necessary, ARDY is negated on the leading edge of the strobe. The ARDY trailing edge is controlled by CLK.
7) The VLBUS synchronous interface uses LCLK, nADS, and W/nR as defined in the VESA specification as well as nCYCLE to control read and write operations and generate nSRDY.
8) Synchronous and asynchronous cycles can be mixed as long as they are not active simultaneously.

6.5 MAC-PHY Interface

The LAN91C113 integrates the IEEE 802.3 Physical Layer (PHY) and Media Access Control (MAC) into the same silicon. The data path connection between the MAC and the internal PHY is provided by the internal MII. The LAN91C113 also supports the EXT_PHY mode for the use of an external PHY, such as HPNA. This mode isolates the internal PHY to allow interface with an external PHY through the MII pins. To enter this mode, set EXT PHY bit to 1 in the Configuration Register.

6.5.1 Management Data Software Implementation

The MII interface contains of a pair of signals that physically transport the management information across the MII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. MII management refers to the ability of a management entity to communicate with PHY via the MII serial management interface (MI) for the purpose of displaying, selecting and/or controlling different PHY options. The host manipulates the MAC to drive the MII management serial interface. By manipulating the MAC's registers, MII management frames are

generated on the management interface for reading or writing information from the PHY registers. Timing and framing for each management command is to be generated by the CPU (host).

The MAC and external PHY communicate via MDIO and MDC of the MII Management serial interface.

MDIO: Management Data input/output. Bi-directional between MAC and PHY that carries management data. All control and status information sent over this pin is driven and sampled synchronously to the rising edge of MDC signal.

MDC: Management Data Clock. Sourced by the MAC as a timing reference for transfer of information on the MDIO signal. MDC is a periodic signal with no maximum high or low times. The minimum high and low times should be 160ns each and the minimum period of the signal should be 400ns. These values are regardless of the nominal period of the TX and RX clocks.

6.5.2 Management Data Timing

A timing diagram for a MI serial port frame is shown in Figure 6.1. The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

6.5.3 MI Serial Port Frame Structure

The structure of the PHY serial port frame is shown in Table 8.1 and timing diagram of a frame is shown in Figure 6.1. Each serial port access cycle consists of 32 bits (or 192 bits if multiple register access is enabled and REGAD[4:0]=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/176 bits are from one/all of the 11 data registers.

The first 2 bits in Table 8.1 and Figure 6.1 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are a read and write bit which determine if the accessed data register bits will be read or write. The next 5 bits are device addresses. The next 5 bits are register address select bits, which select one of the five data registers for access. The next 2 bits are the turnaround bits which are not actual register bits but extra time to switch MDIO from write to read if necessary, as shown in Figure 6.1. The final 16 bits of the PHY MI serial port cycle (or 176 bits if multiple register access is enabled and REGAD[4:0]=11111) come from the specific data register designated by the register address bits REGAD[4:0].

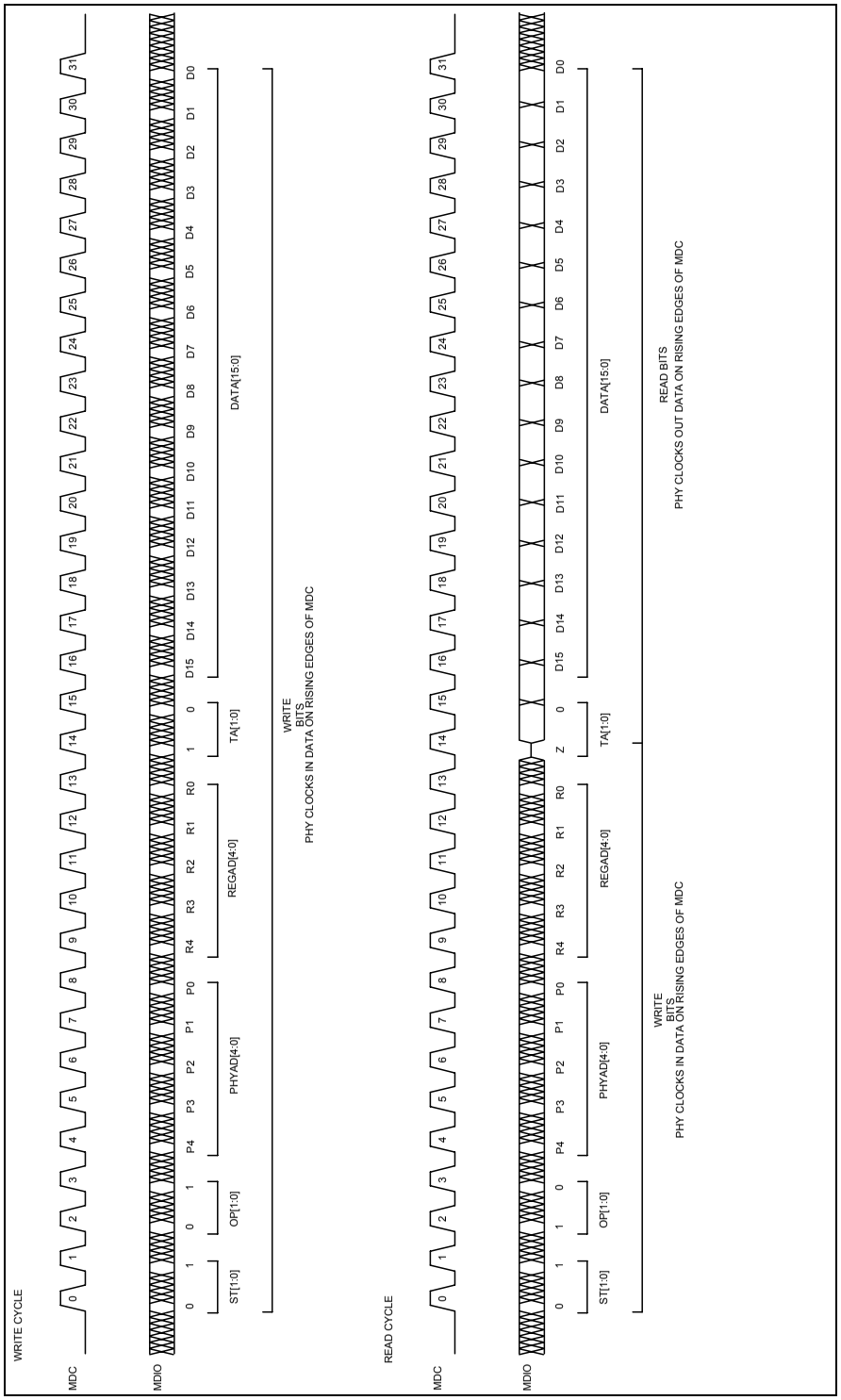

Figure 6.1 - MI Serial Port Frame Timing Diagram

6.5.4 MII Packet Data Communication with External PHY

The MII is a nibble wide packet data interface defined in IEEE 802.3. The LAN91C113 meets all the MII requirements outlined in IEEE 802.3 and shown in Figure 6.2.

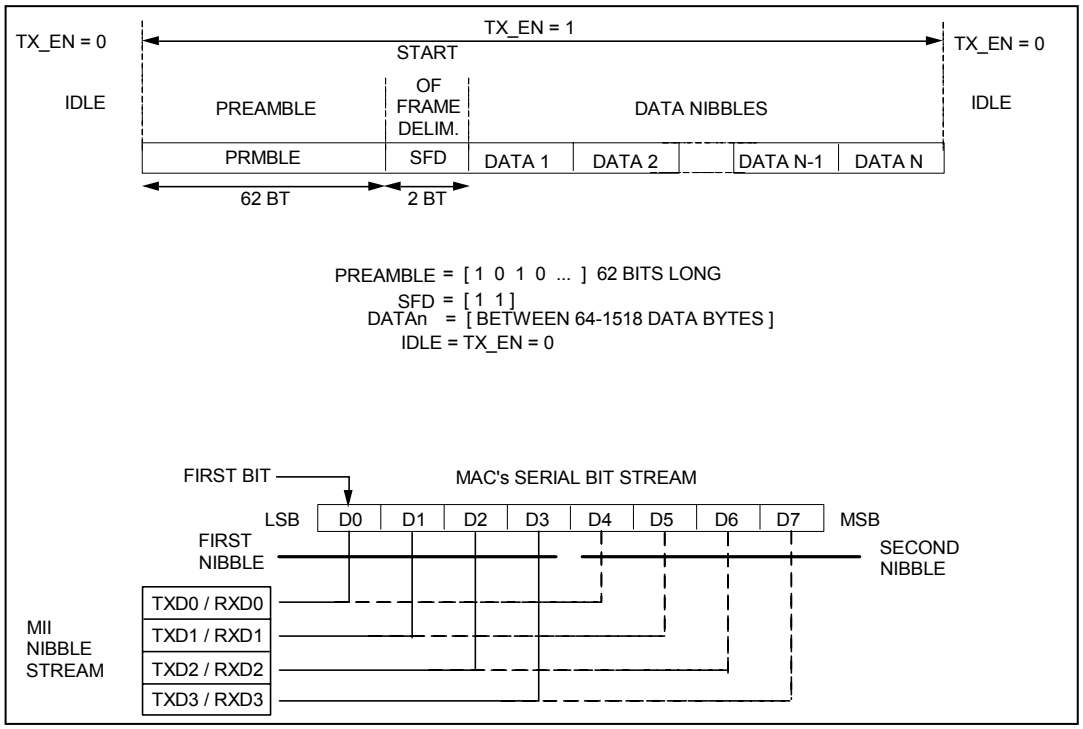

Figure 6.2 - MII Frame Format & MII Nibble Order

The MII consists of the following signals: four transmit data bits (TXD[3:0]), transmit clock (TX25),transmit enable (TXEN100), four receive data bits(RXD[3:0]), receive clock(RX25), carrier sense (CRS100), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL100). Transmit data is clocked out using the TX25 clock input, while receive data is clocked in using RX25. The transmit and receive clocks operate at 25 MHz in 100Mbps mode and 2.5 MHz in 10Mbps.

In 100 Mbps mode, the LAN91C113 provides the following interface signals to the PHY:

- For transmission: TXEN100, TXD0-3, TX25
- For reception: RX_DV, RX_ER RXD0-3, RX25
- For CSMA/CD state machines: CRS100, COL100

A transmission begins by TXEN100 going active (high), and TXD0-TXD3 having the first valid preamble nibble. TXD0 carries the least significant bit of the nibble (that is the one that would go first out of the EPH at 100 Mbps), while TXD3 carries the most significant bit of the nibble. TXEN100 and TXD0-TXD3 are clocked by the LAN91C113 using TX25 rising edges. TXEN100 goes inactive at the end of the packet on the last nibble of the CRC.

During a transmission, COL100 might become active to indicate a collision. COL100 is asynchronous to the LAN91C113's clocks and will be synchronized internally to TX25.

Reception begins when RX_DV (receive data valid) is asserted. A preamble pattern or flag octet will be present at RXD0-RXD3 when RX_DV is activated. The LAN91C113 requires no training sequence beyond a full flag octet for reception. RX_DV as well as RXD0-RXD3 are sampled on RX25 rising edges. RXD0

carries the least significant bit and RXD3 the most significant bit of the nibble. RX_DV goes inactive when the last valid nibble of the packet (CRC) is presented at RXD0-RXD3.

RX_ER might be asserted during packet reception to signal the LAN91C113 that the present receive packet is invalid. The LAN91C113 will discard the packet by treating it as a CRC error.

RXD0-RXD3 should always be aligned to packet nibbles, therefore, opening flag detection does not consider misaligned cases. Opening flag detection expects the 5Dh pattern and will not reject the packet on non-preamble patterns.

CRS100 is used as a frame envelope signal for the CSMA/CD MAC state machines (deferral and backoff functions), but it is not used for receive framing functions. CRS100 is an asynchronous signal and it will be active whenever there is activity on the cable, including LAN91C113 transmissions and collisions.

6.6 Serial EEPROM Interface

This block is responsible for reading the serial EEPROM upon hardware reset (or equivalent command) and defining defaults for some key registers. A write operation is also implemented by this block, that under CPU command will program specific locations in the EEPROM. This block is an autonomous state machine and controls the internal Data Bus of the LAN91C113 during active operation.

6.7 Internal Physical Layer

The LAN91C113 integrates the IEEE 802.3 physical layer (PHY) internally. The EXT PHY bit in the Configuration Register is 0 as the default configuration to set the internal PHY enabled. The internal PHY address is 00000, the driver must use this address to talk to the internal PHY. The internal PHY is placed in isolation mode at power up and reset. It can be removed from isolation mode by clearing the MII_DIS bit in the PHY Control Register. If necessary, the internal PHY can be enabled by clearing the EXT_PHY bit in the Configuration Register.

The internal PHY of LAN91C113 has nine main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, and MI serial port.

The LAN91C113 can operate as a 100BASE-TX device (hereafter referred to as 100Mbps mode) or as a 10BASE-T device (hereafter referred to as 10Mbps mode). The difference between the 100Mbps mode and the 10Mbps mode is data rate, signaling protocol, and allowed wiring. The 100Mbps TX mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a throughput of 100Mbps. The 10Mbps mode uses two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10MHz binary data to achieve a 10Mbps throughput. The data symbol format on the twisted pair cable for the 100 and 10Mbps modes are defined in IEEE 802.3 specifications and shown in Figure 6.3.

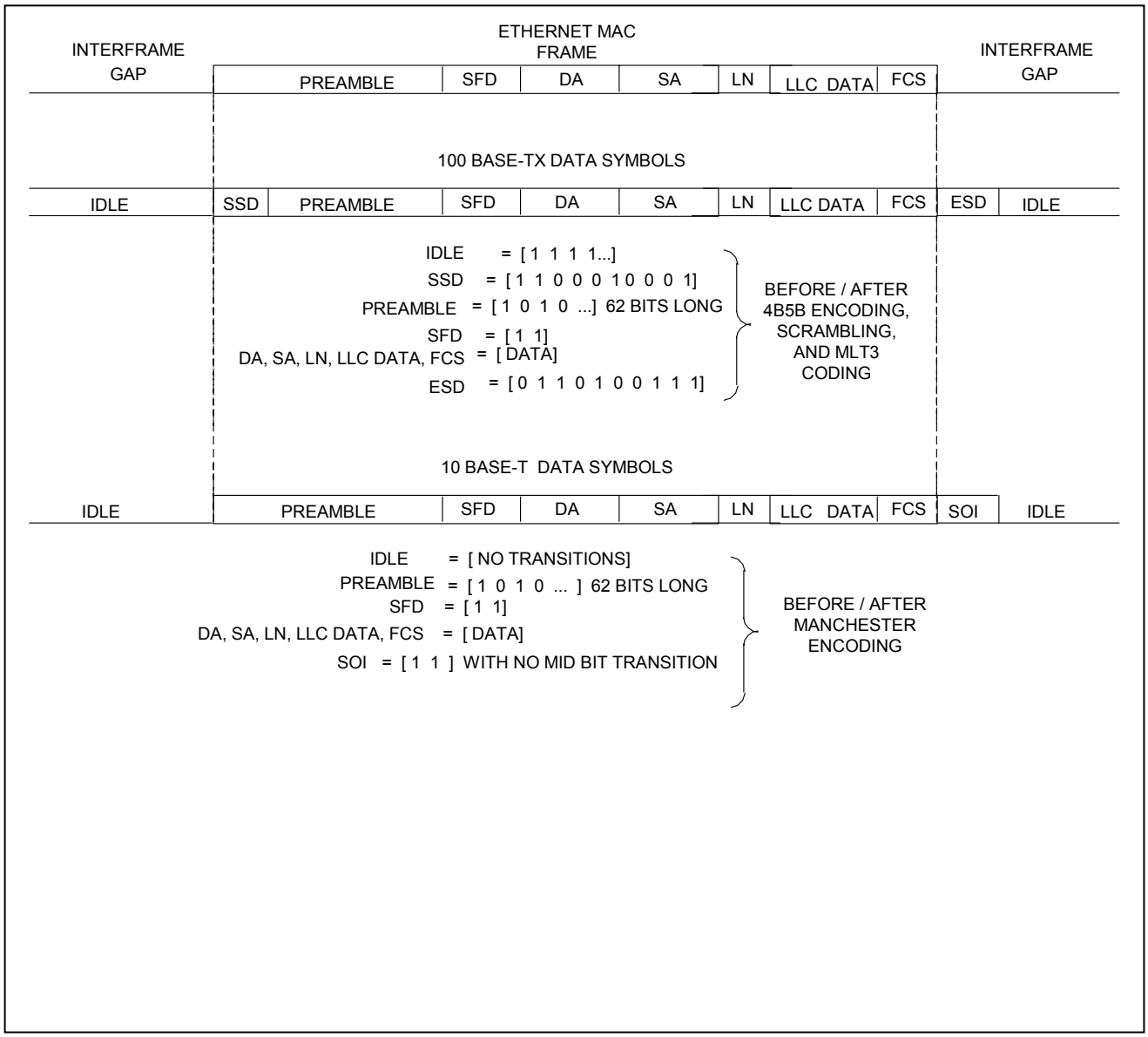

Figure 6.3 - TX/10BT Frame Format

On the transmit side for 100Mbps TX operation, data is received on the controller and then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, reshapes the output, and drives the twisted pair cable.

On the receive side for 100Mbps TX operation, the twisted pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, remove any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses