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LAN91C93I

Non-PCI Single-Chip Full Duplex Ethernet Controller

Datasheet

Product Features

- Non-PCI Single-Chip Ethernet Controller
- Fully Supports Full Duplex Switched Ethernet
- Supports Enhanced Transmit Queue Management
- 6K Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic Detection of TX/RX Polarity Reversal
- Simultasking Early Transmit and Early Receive Functions
- Enhanced Early Transmit Function
- Receive Counter for Enhanced Early Receive
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Supports single 5V or 3.3V VCC Design
- Supports Mixed Voltage External PHY Designs
- Supports Industrial Temp -40°C to 85°C
- Low Power CMOS Design
- 100 Pin QFP and TQFP (1.0mm body Thickness) packages; green, lead-free packages also available
- Direct Interface to local bus, with No Wait States
- 16 Bit Data and Control Paths
- Fast Access Time
- Pipelined Data Path
- Handles Block Word Transfers for any Alignment
- High Performance Chained ("Back-to-Back") Transmit and Receive
- Dynamic Memory Allocation Between Transmit and Receive
- Flat Memory Structure for Low CPU Overhead
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Supports Boot PROM for Diskless local bus Applications

Network Interface

- Integrated 10BASE-T Transceiver Functions:
  - Driver and Receiver
  - Link Integrity Test
  - Receive Polarity Detection and Correction
- Integrated AUI Interface
- 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

Software Drivers

- LAN9000 Drivers for Major Network Operating Systems Utilizing local bus Interface
- Software Drivers Utilize Full Capability of 32 Bit Microprocessor

ORDERING INFORMATION

Order Number(s):

LAN91C93I-MC for 100 pin QFP package

LAN91C93I-ME for 100 pin TQFP package

LAN91C93I-MS for 100 pin QFP package (green, lead-free)

LAN91C93I-MU for 100 pin TQFP package (green, lead-free)

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Chapter 1 General Description

The LAN91C93I is a VLSI, local bus interface Ethernet Controller. LAN91C93I integrates all MAC and physical layer functions, as well as the packet RAM, needed to implement a high performance 10BASE-T (twisted pair) node. For 10BASE5 (thick coax), 10BASE2 (thin coax), and 10BASE-F (fiber) implementations, the LAN91C93I interfaces to external transceivers via the provided AUI port. Only one additional IC is required for most applications. The LAN91C93I comes with Full Duplex Switched Ethernet (FDSWE) support allowing the controller to provide much higher throughput. 6K bytes of RAM is provided to support enhanced throughput and compensate for any increased system service latencies. The controller implements multiple advanced powerdown modes to conserve power and operate more efficiently. The LAN91C93I can directly interface with the local bus and deliver no-wait-state operation. For local bus interfaces, the LAN91C93I occupies 16 I/0 locations and no memory space.

The same I/O space is used for local bus operations. Its shared memory is sequentially accessed with 40ns access times to any of its registers, including its packet memory. DMA services are not used by the LAN91C93I, virtually decoupling network traffic from local or system bus utilization. For packet memory management, the LAN91C93I integrates a unique hardware Memory Management Unit (MMU) with enhanced performance and decreased software overhead when compared to ring buffer and linked list architectures. The LAN91C93I is portable to different CPU and bus platforms due to its flexible bus interface, flat memory structure (no pointers), and its loosely coupled buffered architecture (not sensitive to latency).

The LAN91C93I is available in 100-pin QFP and TQFP (1.0 mm body thickness) packages; green, lead-free packages are also available. The low profile TQFP is ideal for mobile applications such as PC Card LAN adapters. The LAN91C93I operates with a single power supply voltage of 5V or 3.3V.

Chapter 2 Overview

A unique architecture allows the LAN91C93I to combine high performance, flexibility, high integration and simple software interface.

The LAN91C93I incorporates the LAN91C92 functionality for local bus environments. The LAN91C93I consists of the same logical I/O register structure in local bus modes. The MMU (Memory Management Unit) architecture used by the LAN91C93I combines the simplicity and low overhead of fixed areas with the flexibility of linked lists providing improved performance over other methods.

Packet reception and transmission are determined by memory availability. All other resources are always available if memory is available. To complement this flexible architecture, bus interface functions are incorporated in the LAN91C93I, as well as a 6144 byte packet RAM - and serial EEPROM-based setup. The user can select or modify configuration choices. The LAN91C93I integrates most of the 802.3 functionality, incorporating the MAC layer protocol, the physical layer encoding and decoding functions with the ability to handle the AUI interface. For twisted pair networks, LAN91C93I integrates the twisted pair transceiver as well as the link integrity test functions.

The LAN91C93I is a true 10BASE-T single chip device able to interface to a system or a local bus.

Support for direct-driven LEDs for installation and run-time diagnostics is provided. 802.3 statistics are gathered to facilitate network management.

The LAN91C93I is a single chip Ethernet controller designed to be 100% software compatible with the LAN91C92, LAN91C94 and LAN91C96 in local bus mode.

The LAN91C93I has been designed to support full duplex switched Ethernet and provides Fully independent transmit and receive operations.

The LAN91C93I internal packet memory is extended to 6k bytes, and the MMU will continue to manage memory in 256 byte pages. The increase in memory size accommodates the potential for simultaneous transmit and receive traffic in some full duplex applications as well as support for enhanced performance on systems that introduce increased latency.

The LAN91C93I has the ability to retrieve configuration information from a serial EEPROM on reset or power-up. In local bus mode, the serial EEPROM acts as storage of configuration and IEEE Ethernet address information compatible with the existing LAN91C90, LAN91C92, LAN91C94, and LAN91C96 local bus Ethernet controllers. External Flash ROM is required for CIS storage.

The LAN91C93I offers:

High integration:

- Single chip controller including:
  - Packet RAM
  - local bus interface
  - EEPROM interface
  - Encoder/decoder with AUI interface
  - 10BASE-T transceiver

High performance:

- Chained ("Back-to-back") packet handling with no CPU intervention:
  - Queues transmit packets

- Queues receive packets
- Stores results in memory along with packet
- Queues interrupts
- Optional single interrupt upon completion of transmit chain

Fast block move operation for load/unload:

- CPU sees packet bytes as if stored continuously.
- Handles 16 bit transfers regardless of address alignment.
- Access to packet through fixed window.

Fast bus interface:

- Compatible with local bus type and faster buses.

Flexibility:

- Flexible packet and header processing:
  - Can be set to Simultasking - Early Receive and Transmit modes. With enhanced Early Receive functions.
  - Can access any byte in the packet.
  - Can immediately remove undesired packets from queue.
  - Can move packets from receive to transmit queue.
  - Can alter receive processing order without copying data.
  - Can discard or enqueue again a failed transmission.

Resource allocation:

- Memory dynamically allocated for transmit and receive.
- Can automatically release memory on successful transmission.

Configuration:

- local bus:
  - Uses non-volatile jumperless setup via serial EEPROM.
  - nROM on LAN91C93I, is left open with a pullup. This pin is sampled at the end of RESET.

Chapter 3 Pin Configurations

Pin Configuration

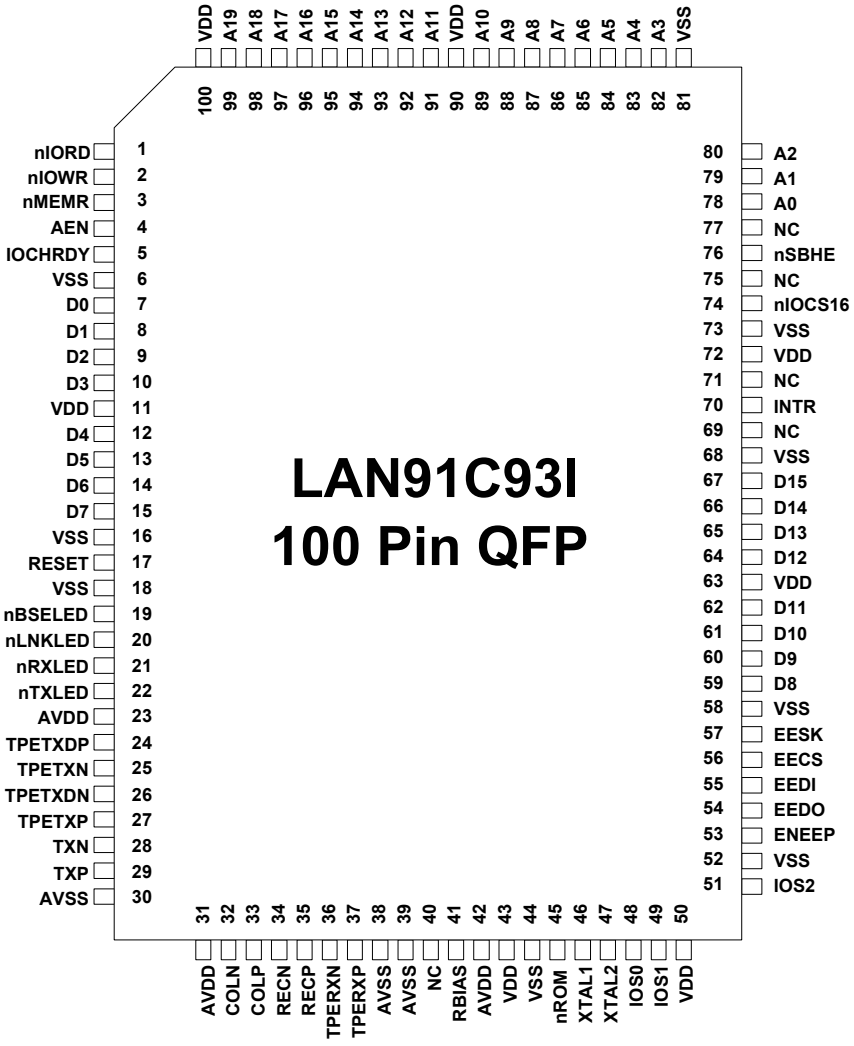

Figure 3.1 – Pin Configuration of LAN91C93I QFP

Pin Configuration

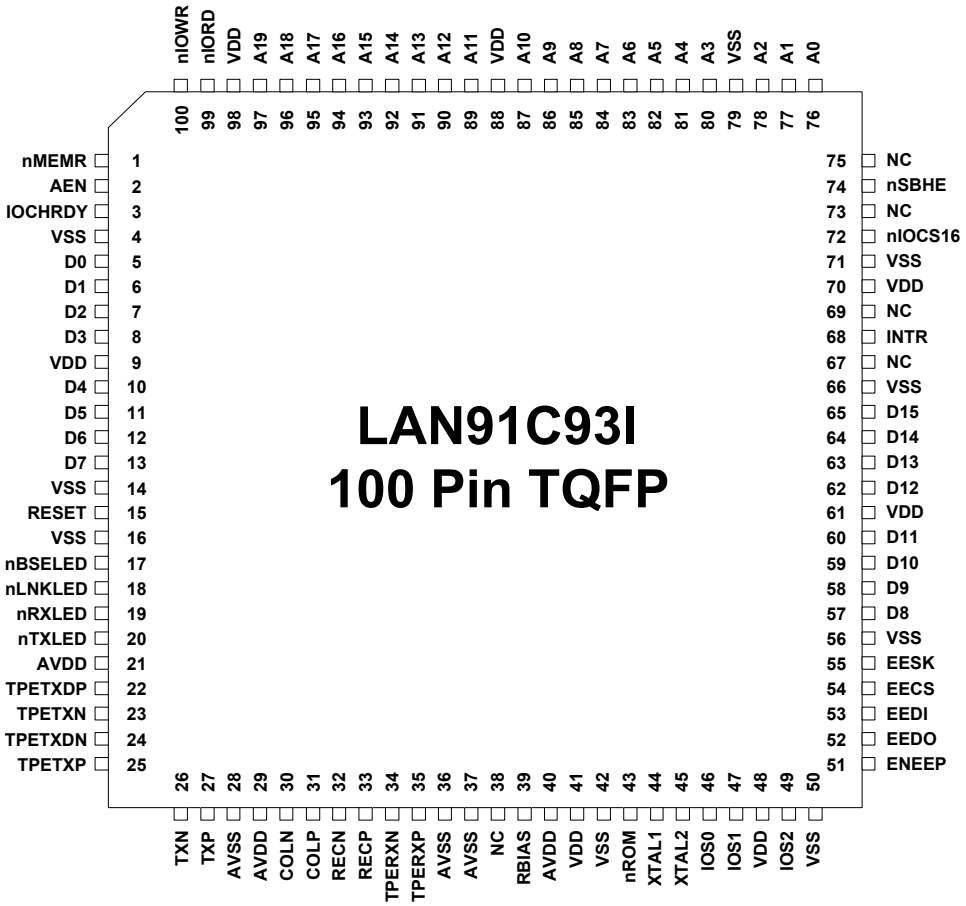

Figure 3.2 – Pin Configuration of LAN91C93I TQFP

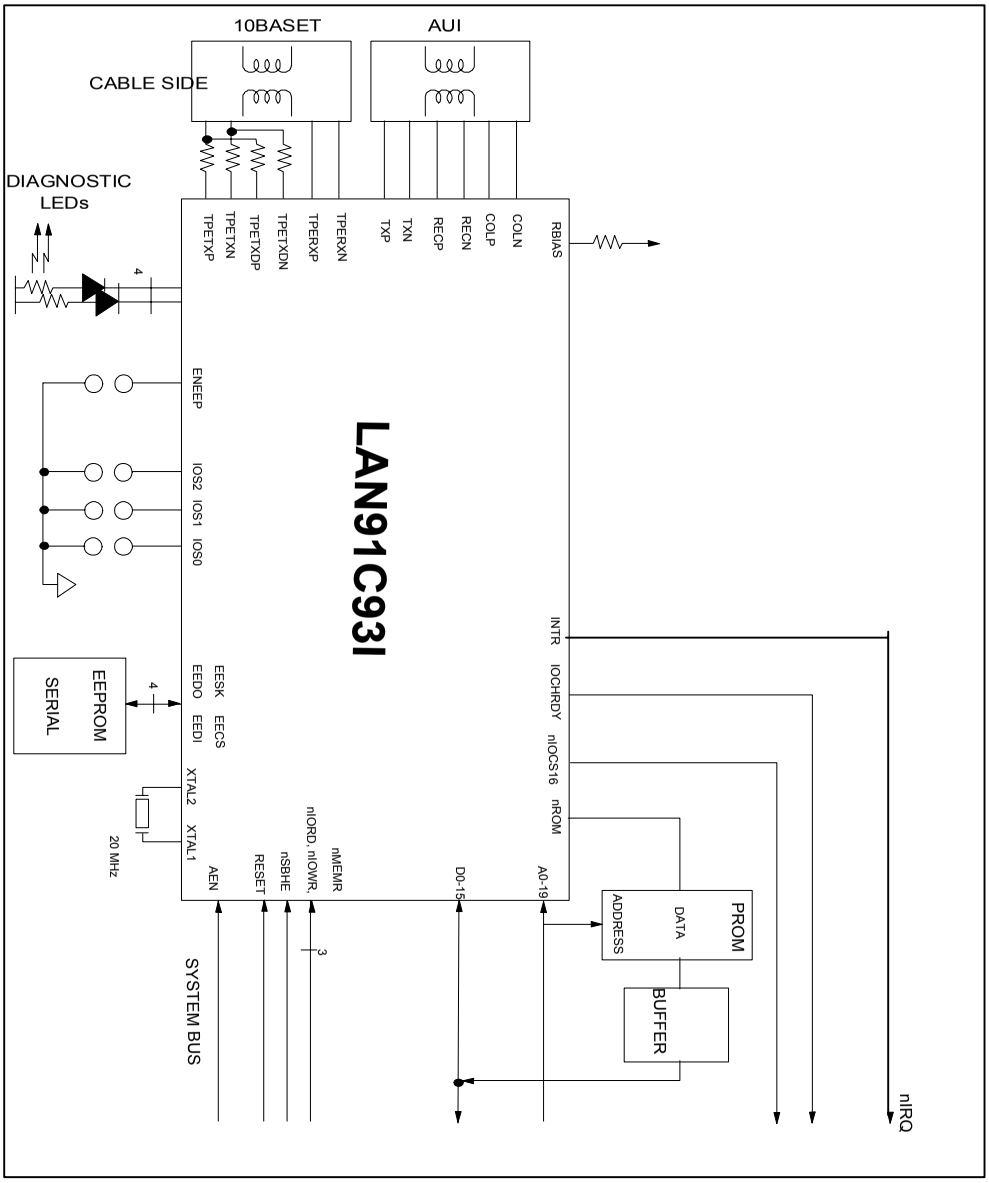

Figure 3.3 – System Diagram for Local Bus with Boot Prom

3.1 Local Bus Pin Requirements

FUNCTION	LOCAL BUS	MAX NUMBER OF PINS
SYSTEM ADDRESS BUS	A0 A1-9 A10 A11 A12-14 A15 A16-18 A19 AEN	21
SYSTEM DATA BUS	D0-15	16
SYSTEM CONTROL BUS	RESET nIORD nIOWR nMEMR IOCHRDY nIOCS16 nSBHE INTR	8
SERIAL EEPROM	EEDI EEDO EECS EESK ENEEP IOS0 IOS1 IOS2	8
CRYSTAL OSC.	XTAL1, XTAL2	2
POWER	VDD, AVDD	10
GROUND	VSS, AVSS	12
10BASE-T interface	TPERXP TPERXN TPETXP TPETXN TPETXDP TPETXDN	6
AUI interface	RECP RECN COLP COLN TXP TXN	6
LEDs	nLNKLED nRXLED nBSELED nTXLED	4
MISC.	RBIAS nROM	2
NC	NC	5

Chapter 4 Description of Pin Functions

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
43	45	nROM	I/O4 with pullup	This pin is sampled at the end of RESET. For local bus operation this pin is left open and it is used as a ROM chip select output that goes active when nMEMR is low and the address bus contains a valid ROM address.
76-78 80-87	78-80, 82-89	A0-10	I * *	Input address lines 0 through 10.
89-97	91-99	A11-19	I * *	Input address lines 11 through 19.
2	4	AEN	I with pullup **	Local bus - Address enable input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
74	76	nSBHE	I with pullup **	Local bus - Byte High Enable input. Asserted (low) by the system to indicate a data transfer on the upper data byte.
3	5	IOCHRDY	OD24 with pullup	Local bus - Output. Optionally used by the LAN91C93I to extend host cycles.
5-8 10-13 57-60 62-65	7-10, 12-15, 59-62, 64-67	D0-15	I/O24	Bi-directional. 16 bit data bus used to access the LAN91C93I internal registers. The data bus has weak internal pullups. Supports direct connection to the system bus without external buffering.
15	17	RESET	IS with pullup **	Input. Active high Reset. This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
68	70	INTR	O24	Local bus - Active high interrupt signal.
72	74	nIOCS16	OD24	Local bus - Active low output asserted in 16 bit mode when AEN is low and A4-A15 decode to the LAN91C93I address programmed into the high byte of the Base Address Register.
99	1	nIORD	IS with pullup **	Local bus, - Input. Active low read strobe used to access the LAN91C93I IO space.
100	2	nIOWR	IS with pullup **	Local bus - Input. Active low write strobe used to access the LAN91C93I IO space.
1	3	nMEMR	IS with pullup **	Local bus - Active low signal used by the host processor to read from the external ROM.
55	57	EESK	O4	Output. 4usec clock used to shift data in and out of a serial EEPROM.
54	56	EECS	O4	Output. Serial EEPROM chip select.
52	54	EEDO	O4	Output. Connected to the DI input of the serial EEPROM.
53	55	EEDI	I with pull-down **	Input. Connected to the DO output of the serial EEPROM.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
46,47	48,49	IOS0-1	I with pullup	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
49	51	IOS2	I with pullup **	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
20	22	nTXLED	OD16	Transmit LED output.
17	19	nBSELED	OD16	Board Select LED activated by accesses to I/O space (nIORD or nIOWR active with AEN low and valid address decode for local bus). The pulse is stretched beyond the access duration to make the LED visible.
19	21	nRXLED	OD16	Receive LED output.
18	20	nLNKLED	OD16	Link LED output.
51	53	ENEEP	I with pullup **	Input. This active high input enables the EEPROM to be read or written by the LAN91C93I. Internally pulled up. Must be connected to ground if no serial EEPROM is used.
44	46	XTAL1	Iclk **	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to this pin (XTAL1) and XTAL2 should be left open.
45	47	XTAL2	Iclk	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to XTAL1 and this pin (XTAL2) should be left open.
33 32	35 34	RECP/ RECN	Diff. Input **	AUI receive differential inputs.
27 26	29 28	TXP TXN	Diff. Output	TXP and TXN are the AUI transmit differential outputs. They must be externally pulled up using 150 ohm resistors.
31 30	33 32	COLP COLN	Diff. Input **	AUI collision differential inputs. A collision is indicated by a 10MHz signal at this input pair.
35 34	37 36	TPERXP TPERXN	Diff. Input * *	10BASE-T receive differential inputs.
25 23	27 25	TPETXP TPETXN	Diff. Output	INTERNAL ENDEC - 10BASE-T transmit differential outputs.
22 24	24 26	TPETXDP TPETXDN	Diff. Output	10BASE-T delayed transmit differential outputs. Used in combination with TPETXP and TPETXN to generate the 10BASE-T transmit pre-distortion.
39	41	RBIAS	Analog Input	A resistor should be connected between this pin and analog ground to determine the receive threshold voltage of TX Receive, AUI Receive, AUI Collision Receive, and AUI transmit voltage.
61,70, 98,9, 48,88,41	63, 72 ,90,100, 11,50,43	VDD		+5.0V power supply pins or 3.3V power supply pins
21,29, 40	23,31, 42	AVDD		+5.0V analog power supply pins or 3.3V power supply pins

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
50,56, 71,79 4,14,42, 66, 16	52,58,68, 73,81, 6,16, 44, 18,	VSS		Ground pins.
28,36, 37	30,38,39	AVSS		Analog ground pins.
75, 73, 69, 67, 38	40, 77, 75, 71, 69	NC	NC	No-Connected pins

4.1 Buffer Symbols

O4	Output buffer with 2mA source and 4mA sink *at 5V.* *Output buffer with 1mA source and 2mA sink at 3.3V*
I/O4	Output buffer with 2mA source and 4mA sink *at 5V.* *Output buffer with 1mA source and 2mA sink at 3.3V.*
O162	Output buffer with 2mA source and 16mA sink *at 5V.* *Output buffer with 1mA source and 8mA sink at 3.3V.*
O24	Output buffer with 12mA source and 24mA sink *at 5V.* *Output buffer with 6mA source and 12mA sink at 3.3V*.
OD16	Open drain buffer with 16mA sink *at 5V.* *Open drain buffer with 8mA sink at 3.3V.*
OD24	Open drain buffer with 24mA sink *at 5V.* *Open drain buffer with 12mA sink at 3.3V*.
I/O24	Bi-directional buffer with 12mA source and 24mA sink *at 5V.* *Bi-directional buffer with 6mA source and 16mA sink at 3.3V.*
I	Input buffer with TTL levels.
IS	Input buffer with Schmitt Trigger Hysteresis.
Iclk	Clock input buffer.
**	Signal is 5.0V input tolerant when V_{cc}=3.3V.

DC levels and conditions defined in the DC Electrical Characteristics section.

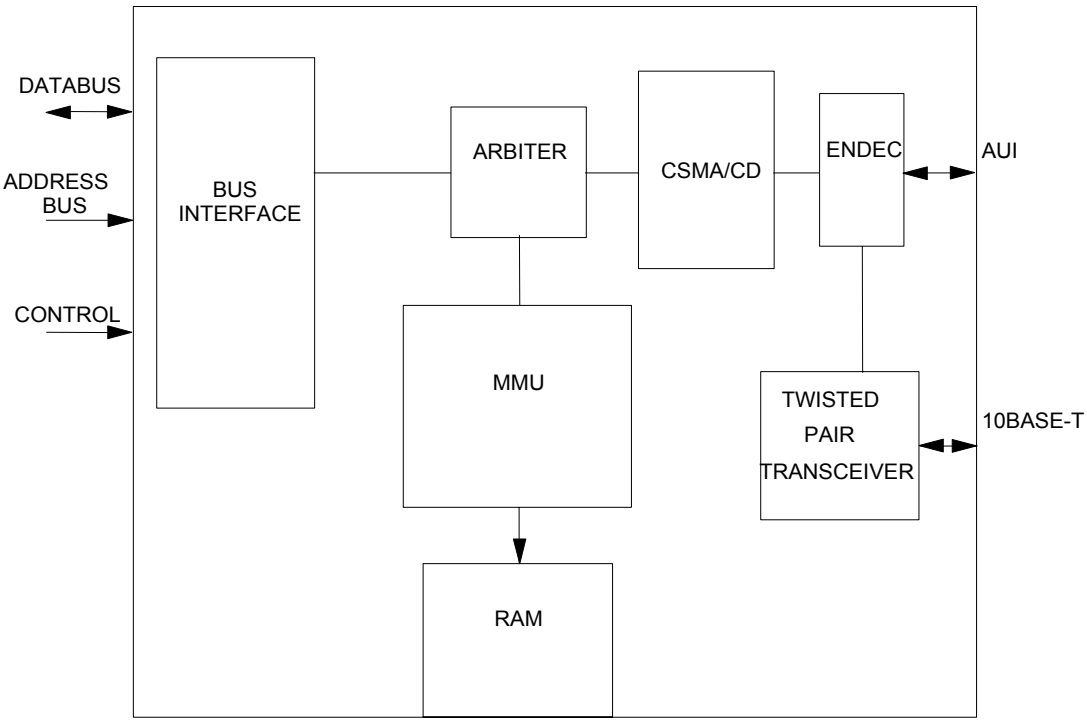

Figure 4.1 - LAN91C93I Internal Block Diagram

Chapter 5 Functional Description

The LAN91C93I includes an arbitrated-shared memory of 6144 bytes. Any portion of this memory can be used for receive or transmit packets.

The MMU unit allocates RAM memory to be used for transmit and receive packets, using 256 byte pages.

The arbitration is transparent to the CPU in every sense. There is no speed penalty for local bus type of machines due to arbitration. There are no restrictions on what locations can be accessed at any time. RAM accesses as well as MMU requests are arbitrated.

The RAM is accessed by mapping it into I/O space for sequential access. Except for the RAM accesses and the MMU request/release commands, I/O accesses are not arbitrated.

The I/O space is 16 bits wide. Provisions for 8 bit systems are handled by the bus interface.

In the system memory space, up to 64 kbytes are decoded by the LAN91C93I as expansion ROM. The ROM expansion area is 8 bits wide.

Device configuration is done using a serial EEPROM, with support for modifications to the EEPROM at installation time.

The CSMA/CD core implements the 802.3 MAC layer protocol. It has two independent interfaces, the data path and the control path.

In local bus mode, serial EEPROM is used for configuration and IEEE Node address making it software compatible to the LAN9xxx family of Ethernet LAN Controllers. The EEPROM is optional for local bus requiring a Minimum size of 64 X 16 bit word addresses. Both interfaces are 16 bits wide. The control path provides a set of registers used to configure and control the block. These registers are accessible by the CPU through the LAN91C93I I/O space. The data path is of sequential access nature and typically works in one direction at any given time. An internal DMA type of interface connects the data path to the device RAM through the arbiter and MMU.

The CSMA/CD data path interface is not accessible to the host CPU.

The internal DMA interface can arbitrate for RAM access and request memory from the MMU when necessary.

An encoder/decoder block interfaces the CSMA/CD block on the serial side. The encoder will do the Manchester encoding of the transmit data at 10 Mb/s, while the decoder will recover the receive clock, and decode received data.

Carrier and Collision detection signals are also handled by this block and relayed to the CSMA/CD block.

The encoder/decoder block can interface the network through the AUI interface pairs, or it can be programmed to use the internal 10BASE-T transceiver and connect to a twisted pair network.

The twisted pair interface takes care of the medium dependent signaling for 10BASE-T type of networks. It is responsible for line interface (with external pulse transformers and pre-distortion resistors), collision detection as well as the link integrity test function.

The LAN91C93I provides a 16-bit data path into RAM. The RAM is private and can only be accessed by the system via the arbiter. RAM memory is managed by the MMU. Byte and word accesses to the RAM are supported.

If the system to SRAM bandwidth is insufficient the LAN91C93I will automatically use its IOCHRDY line for flow control. However, for local bus, IOCHRDY will never be negated. The LAN91C93I consists of an integrated Ethernet controller mapped entirely in I/O space.

The Ethernet controller function includes a built-in 6kbyte RAM for packet storage. This RAM buffer is accessed by the CPU through sequential access regions of 256 bytes each. The RAM access is internally arbitrated by the LAN91C93I, and dynamically allocated between transmit and receive packets. Each packet may consist of one or more 256-byte page. The Ethernet controller functionality is identical to the LAN91C94 and LAN91C95 except where indicated otherwise.

The LAN91C93I Memory Management Unit parameters are:

RAM size	6kbytes
Max. number of pages	24
Max. number of packets	24 (FIFOs have 24 entries of 5 bits)
Max. pages per packet	6
Page Size	256 bytes

5.1 Buffer Memory

The logical addresses for RAM access are divided into TX area and RX area.

The TX area is seen by the CPU as a window through which packets can be loaded into memory before queuing them in the TX FIFO of packets. The TX area can also be used to examine the transmit completion status after packet transmission.

The RX area is associated to the output of the RX FIFO of packets, and is used to access receive packet data and status information.

The logical address is specified by loading the address pointer register. The pointer can automatically increment on accesses.

All accesses to the RAM are done via I/O space.

A bit in the address pointer also specifies if the address refers to the TX or RX area.

In the TX area, the host CPU has access to the next transmit packet being prepared for transmission. In the RX area, it has access to the first receive packet not processed by the CPU yet.

The FIFO of packets, existing beneath the TX and RX areas, is managed by the MMU. The MMU dynamically allocates and releases memory to be used by the transmit and receive functions.

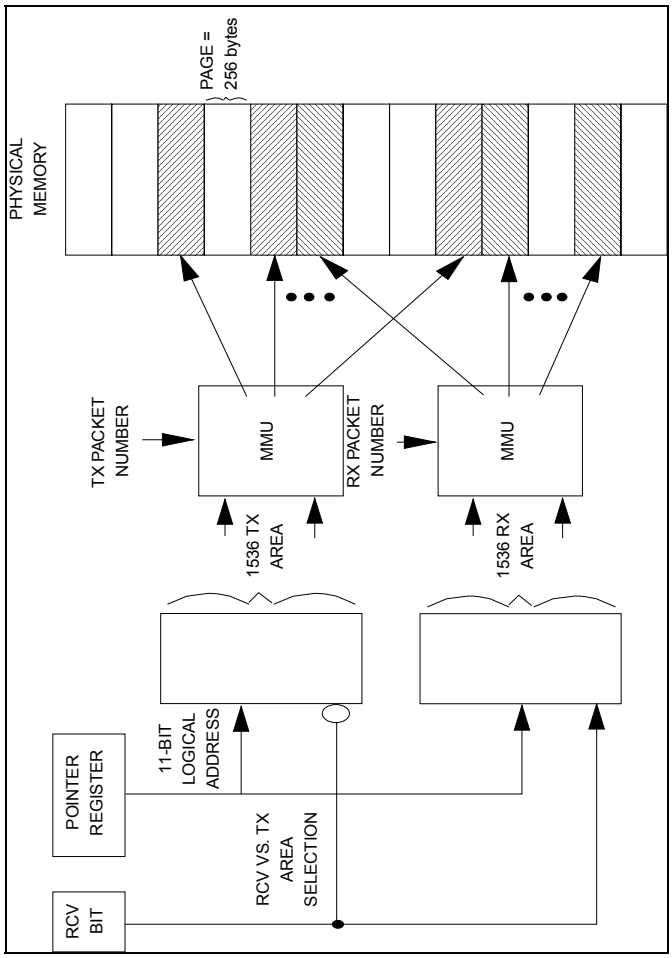

Figure 5.1 – Mapping and Paging vs. Receive and Transmit Area

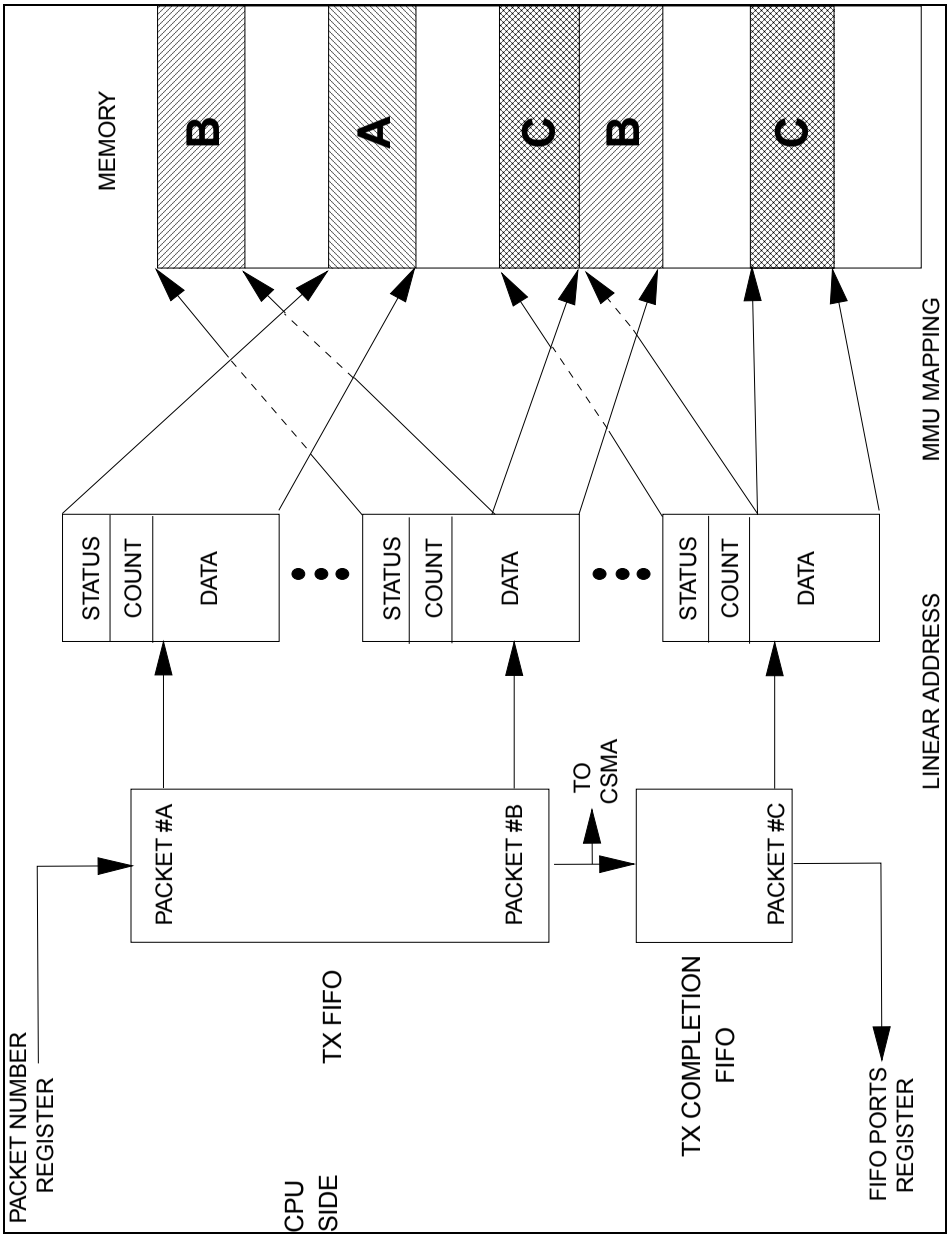

Figure 5.2 – Transmit Queues and Mapping

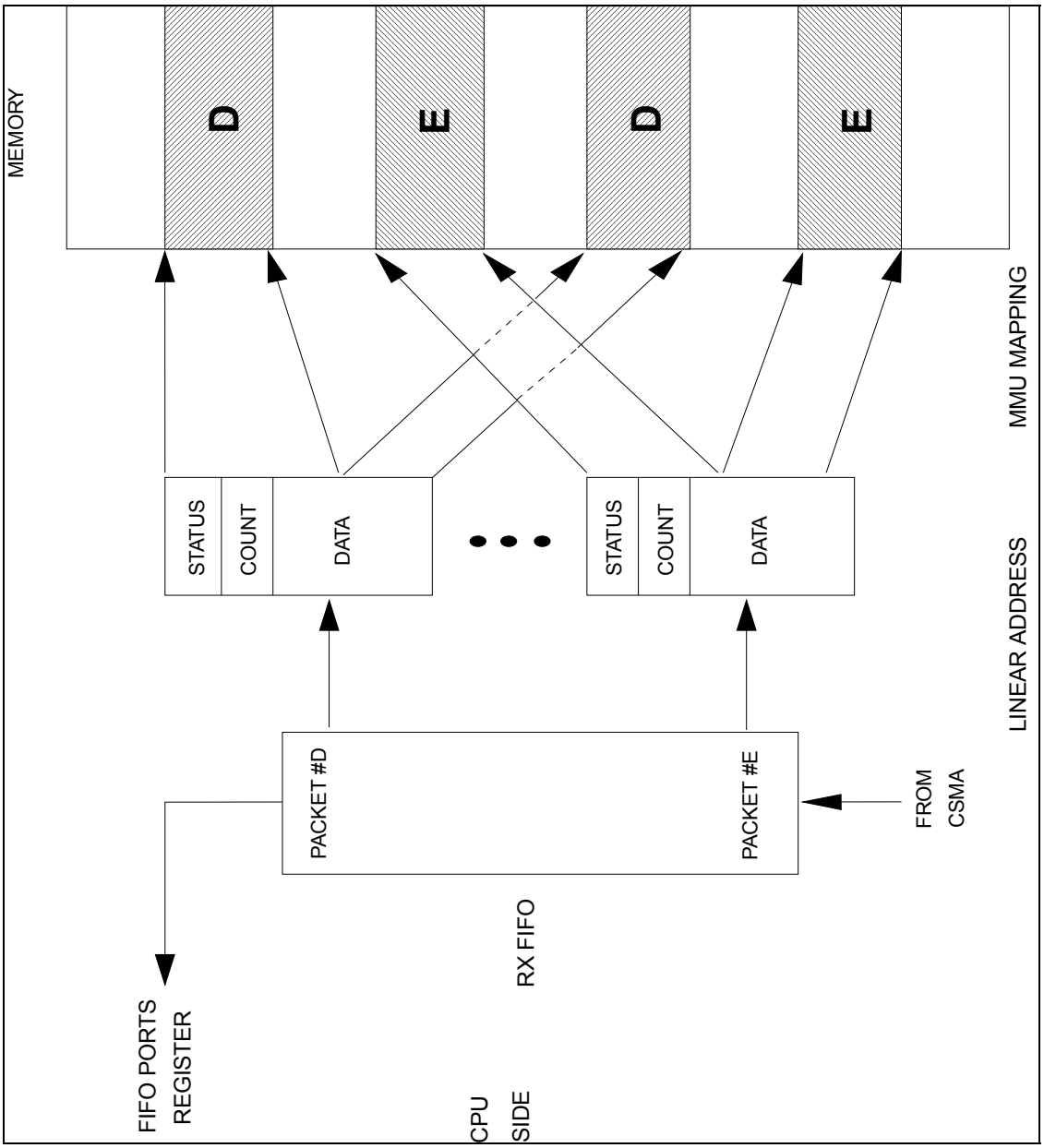

Figure 5.3 – Receive Queues and Mapping

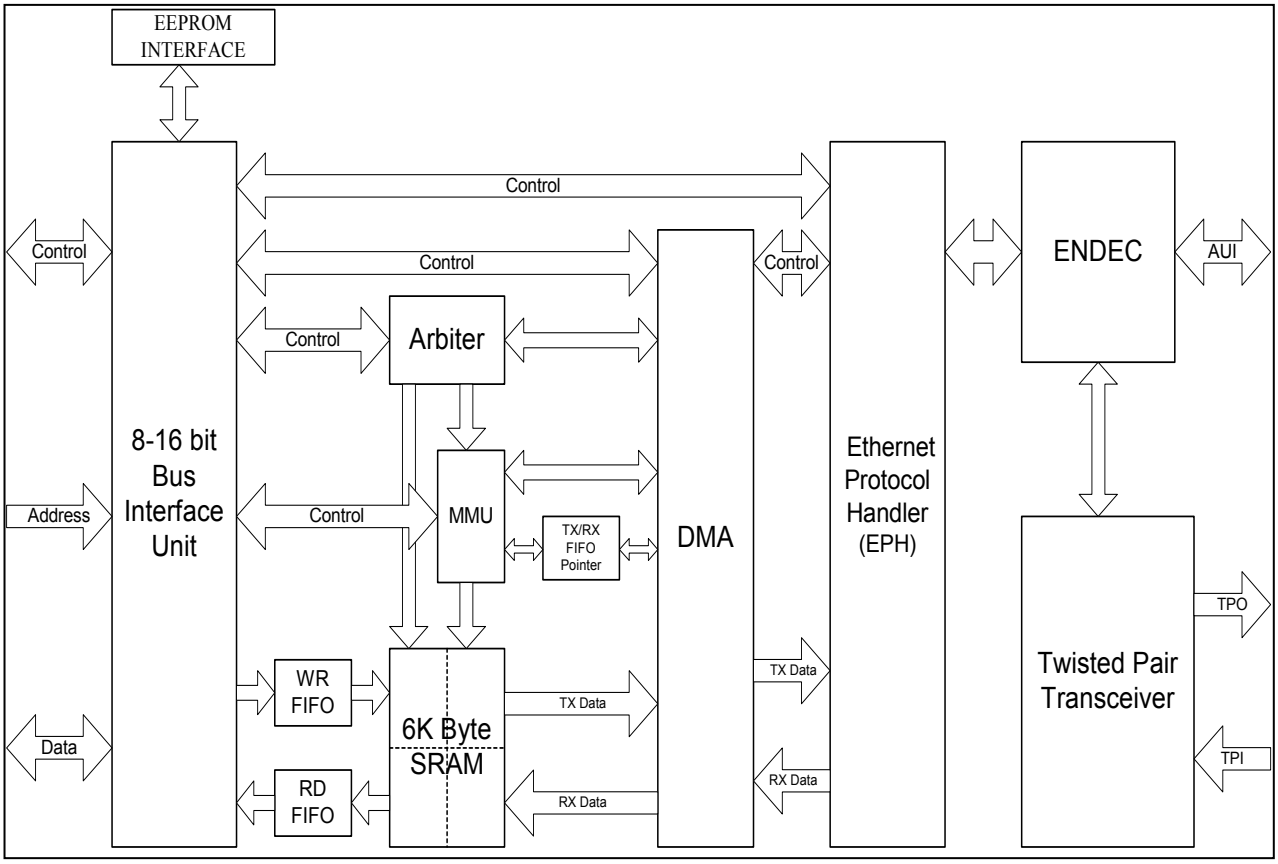

Figure 5.4 – LAN91C93I Internal Block Diagram with Data Path

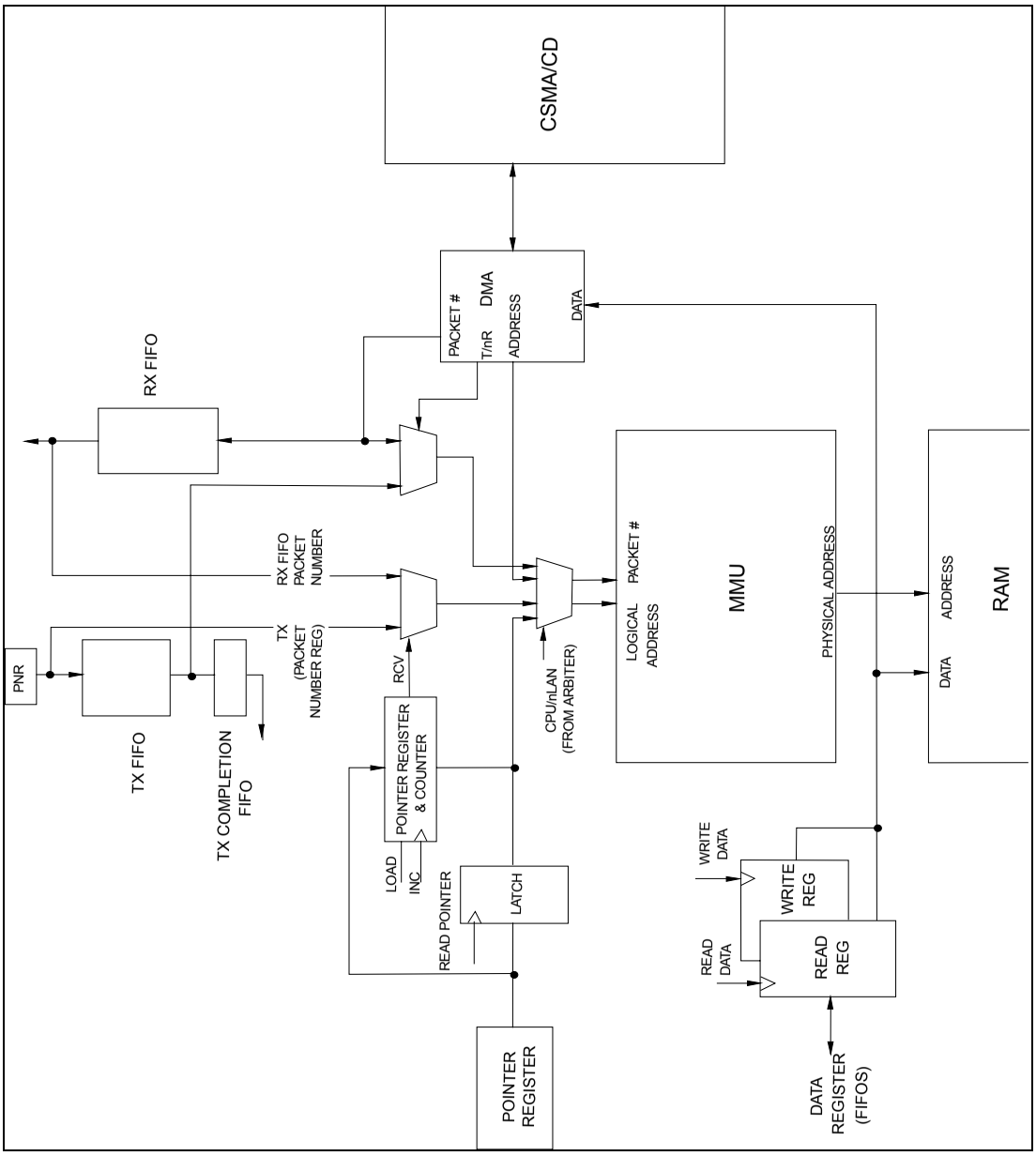

Figure 5.5 – Logical Address Generation and Relevant Registers

Table 5.1 - LAN91C93I Address Space

	SIGNALS USED	LOCAL BUS	ON-CHIP	DEPTH	WIDTH
Ethernet I/O space (1)	nIORD/ nIOWR	Y	Y	16 locations	8 or 16 bits

Table 5.2 - Bus Transactions in Local Bus Mode

	A0	NSBHE	D0-7	D8-15
8 BIT MODE (16BIT=0))	0	X	Even byte	-
	1	X	Odd byte	-
16 BIT MODE Otherwise	0	0	Even byte	Odd byte
	0	1	Even byte	-
	1	0	-	Odd byte
	1	1	Invalid cycle	

16 BIT: CONFIGURATION REGISTER bit 7

8 Bit mode: (nMIS16 = 1)

5.2 Interrupt Structure

The Ethernet interrupt is conceptually equivalent to the LAN91C94 interrupt line, it is the or function of all enabled interrupts within the Ethernet core.

Table 5.3 – Interrupt Merging

FUNCTION	LOCAL BUS MODE
Interrupt Output	INTR
Ethernet Interrupt Source	OR function of all interrupt bits specified in the Interrupt Status Register ANDed with their respective Enable bits
Ethernet Interrupt Enable	Not Applicable in local bus mode

5.3 Reset Logic

The pins and bits involved in the different reset mechanisms are:

RESET - Input Pin

SOFT RST - EPH Soft Reset bit in RCR

Table 5.4 – Reset Logic

	RESETS THE FOLLOWING FUNCTIONS	SAMPLES LOCAL BUS MODE	TRIGGERS EEPROM READ
RESET pin	All internal logic	Yes	Yes
SOFT RST	The Ethernet controller itself except for the IA, CONF and BASE registers.	No	No

5.4 Power Down Logic States

The following tables describe the power down states of the LAN91C93I. The bits involved in power down are:

- PWRDN - Legacy power down bit in Control Register
- LAN91C93I Power Down States

Table 5.5 - Local Bus Mode Defined States (Refer To Table 5.6 For Next States To Wake-Up Events)

CURRENT STATE			
NO.	CTR PWRDWN BIT	POWERS DOWN	DOES NOT POWER DOWN
1	X	Everything.	
2	0		Ethernet Tx, Rx, Link
3	0	Ethernet Tx	Ethernet Rx, Link
4	1	Ethernet Tx, Rx, Link	
5	1	Ethernet Tx, Rx, Link	

Table 5.6 – Local Bus Mode

		NEXT STATE		
NO.	WAKES UP BY	CTR PWR-DWN BIT	CTR WAKEUP_EN BIT	COMMENTS
1		0	0	Fully Awake
2	By writing a 0 to CTR PWRDWN bit = 0	0	0	The CTR PWRDWN bit has precedence unlike the LAN91C95
3	By writing 0 to CTR PWRDWN bit	0	0	