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LAN91C96

Non-PCI Single-Chip Full Duplex Ethernet Controller with Magic Packet

Datasheet

Product Features

- Non-PCI Single-Chip Ethernet Controller
- A Subset of Motorola 68000 Bus Interface Support
- Fully Supports Full Duplex Switched Ethernet
- Supports Enhanced Transmit Queue Management
- 6K Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic Detection of TX/RX Polarity Reversal
- Enhanced Power Management Features
- Supports “Magic Packet” Power Management Technology
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Supports single +5V or +3.3V (for Revisions E and Later) VCC Designs
- Supports Mixed Voltage External PHY Designs[1]
- Low Power CMOS Design
- 100 Pin QFP and TQFP (1.0 mm body Thickness) Lead-Free RoHS Compliant Packages
- Pin Compatible with the LAN91C92 and LAN91C94

Bus Interface

- Direct Interface to Local Bus, PCMCIA, and 68000 Buses with No Wait States
- Flexible Bus Interface
- 16 Bit Data and Control Paths
- Fast Access Time
- Pipelined Data Path
- Handles Block Word Transfers for any Alignment
- High Performance Chained ("Back-to-Back") Transmit and Receive
- Pin Compatible with the LAN91C92 (in Local Bus Mode) and the LAN91C94 in Both Local Bus and PCMCIA Modes
- Dynamic Memory Allocation Between Transmit and Receive
- Flat Memory Structure for Low CPU Overhead
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Supports Boot PROM for Diskless Local Bus Applications

Network Interface

- Integrated 10BASE-T Transceiver Functions:
  - Driver and Receiver
  - Link Integrity Test
  - Receive Polarity Detection and Correction
- Integrated AUI Interface
- 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

Software Drivers

- LAN9000 Drivers for Major Network Operating Systems Utilizing Local Bus or PCMCIA Interface
- Software Drivers Compatible with the LAN91C92, LAN91C94, LAN91C100FD (100 Mb/s), and LAN91C110 (100 Mb/s) Controllers in Local Bus Mode
- Software Drivers Utilize Full Capability of 32 Bit Microprocessor

[1] Refer to Description of Pin Functions on Page 17 for 5V tolerant pins

ORDER NUMBERS:

LAN91C96-MS for 100 pin, QFP Lead-Free RoHS Compliant package

LAN91C96-MU for 100 pin, TQFP Lead-Free RoHS Compliant package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 General Description

The LAN91C96 is a VLSI Ethernet Controller that combines Local Bus, PCMCIA, and Motorola 68000 bus interfaces in one chip. LAN91C96 integrates all MAC and physical layer functions, as well as the packet RAM, needed to implement a high performance 10BASE-T (twisted pair) node. For 10BASE5 (thick coax), 10BASE2 (thin coax), and 10BASE-F (fiber) implementations, the LAN91C96 interfaces to external transceivers via the provided AUI port. Only one additional IC is required for most applications. The LAN91C96 comes with Full Duplex Switched Ethernet (FDSWE) support allowing the controller to provide much higher throughput. 6K bytes of RAM is provided to support enhanced throughput and compensate for any increased system service latencies. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently. The LAN91C96 can directly interface with the Local Bus, PCMCIA, and 68000 buses and deliver no-wait-state operation. For Local Bus and PCMCIA interfaces, the LAN91C96 occupies 16 I/0 locations and no memory space except for PCMCIA attribute memory space. The same I/O space is used for both LOCAL BUS and PCMCIA operations. Its shared memory is sequentially accessed with 40ns access times to any of its registers, including its packet memory. DMA services are not used by the LAN91C96, virtually de-coupling network traffic from local or system bus utilization. For packet memory management, the LAN91C96 integrates a unique hardware Memory Management Unit (MMU) with enhanced performance and decreased software overhead when compared to ring buffer and linked list architectures. The LAN91C96 is portable to different CPU and bus platforms due to its flexible bus interface, flat memory structure (no pointers), and its loosely coupled buffered architecture (not sensitive to latency).

The LAN91C96 is available in 100-pin QFP and TQFP (1.0 mm body thickness) packages. The low profile TQFP is ideal for mobile applications such as PC Card LAN adapters. The LAN91C96 operates with a single power supply voltage of 5.0V. Revisions E and later will also operate using a single 3.3V power supply.

Chapter 2 Overview

A unique architecture allows the LAN91C96 to combine high performance, flexibility, high integration and simple software interface.

The LAN91C96 incorporates the LAN91C92 functionality for LOCAL BUS environments, as well as a PCMCIA interface and attribute registers like the LAN91C94 It also includes a subset of the Motorola 68000 interface. Mode selection between LOCAL BUS and PCMCIA is static and is done only at the end of a reset. Selection of 68000 operation mode is performed at power-up.

The LAN91C96 consists of the same logical I/O register structure in LOCAL BUS and PCMCIA modes. However, some of the signals used to access the PCMCIA differ from the LOCAL BUS mode. The MMU (Memory Management Unit) architecture used by the LAN91C96 combines the simplicity and low overhead of fixed areas with the flexibility of linked lists providing improved performance over other methods.

Packet reception and transmission are determined by memory availability. All other resources are always available if memory is available. To complement this flexible architecture, bus interface functions are incorporated in the LAN91C96, as well as a 6144 byte packet RAM - and serial EEPROM-based setup. The user can select or modify configuration choices. The LAN91C96 integrates most of the 802.3 functionality, incorporating the MAC layer protocol, the physical layer encoding and decoding functions with the ability to handle the AUI interface. For twisted pair networks, LAN91C96 integrates the twisted pair transceiver as well as the link integrity test functions.

The LAN91C96 is a true 10BASE-T single chip device able to interface to a system or a local bus.

Support for direct-driven LEDs for installation and run-time diagnostics is provided. 802.3 statistics are gathered to facilitate network management.

The LAN91C96 is a single chip Ethernet controller designed to be 100% pin and software compatible with the LAN91C92 and LAN91C94 in LOCAL BUS mode. Similar to the LAN91C94, the LAN91C96 has support necessary for providing a true single chip single function PCMCIA Ethernet socket adapter. The LAN91C96 incorporates all of the PCMCIA registers and signals that interface to the PCMCIA bus.

The LAN91C96 has been designed to support full duplex switched Ethernet and provides Fully independent transmit and receive operations.

The LAN91C96 internal packet memory is extended to 6k bytes, and the MMU will continue to manage memory in 256 byte pages. The increase in memory size accommodates the potential for simultaneous transmit and receive traffic in some full duplex applications as well as support for enhanced performance on systems that introduce increased latency.

The LAN91C96 has the ability to retrieve configuration information from a serial EEPROM on reset or power-up. In LOCAL BUS mode, the serial EPROM acts as storage of configuration and IEEE Ethernet address information compatible with the existing LAN91C90, LAN91C92, and LAN91C94 LOCAL BUS Ethernet controllers. In PCMCIA mode, the EEPROM function is the same as in LOCAL BUS mode. External Flash ROM is required for CIS storage.

THE LAN91C96 OFFERS:

High integration:

Single chip controller including:

- Packet RAM
- LOCAL BUS interface

- PCMCIA interface
- *68000 interface*
- EEPROM interface
- Encoder/decoder with AUI interface
- 10BASE-T transceiver

High performance:

Chained ("Back-to-back") packet handling with no CPU intervention:

- Queues transmit packets
- Queues receive packets
- Stores results in memory along with packet
- Queues interrupts
- Optional single interrupt upon completion of transmit chain

Fast block move operation for load/unload:

- CPU sees packet bytes as if stored continuously.
- Handles 16 bit transfers regardless of address alignment.
- Access to packet through fixed window.

Fast bus interface:

- Compatible with LOCAL BUS type and faster buses.

Flexibility:

Flexible packet and header processing:

- Can access any byte in the packet.
- Can immediately remove undesired packets from queue.
- Can move packets from receive to transmit queue.
- Can alter receive processing order without copying data.
- Can discard or enqueue again a failed transmission.

Resource allocation:

- Memory dynamically allocated for transmit and receive.
- Can automatically release memory on successful transmission.

Configuration:

LOCAL BUS:

- Uses non-volatile jumperless setup via serial EEPROM.

PCMCIA:

- Uses ROM or Flash ROM for attribute memory storage and optional serial EEPROM for IEEE address storage. PCMCIA I/O ignores address lines A4-A15 and relies on the PCMCIA host, decoding for the slot.
- nROM/nPCMCIA, on LAN91C96, is left open with a pullup for LOCAL BUS mode. This pin is sampled at the end of RESET. If found low, the LAN91C96 is configured for PCMCIA mode.

Motorola 68000:

- Uses non-volatile jumperless setup via serial EEPROM. The device must power up in LOCAL BUS mode with nIORD and nIOWR asserted simultaneously to make the controller enter the 68000 mode.

Note: The first write to the 68000 configured controller must be a write.

Chapter 3 Pin Configurations

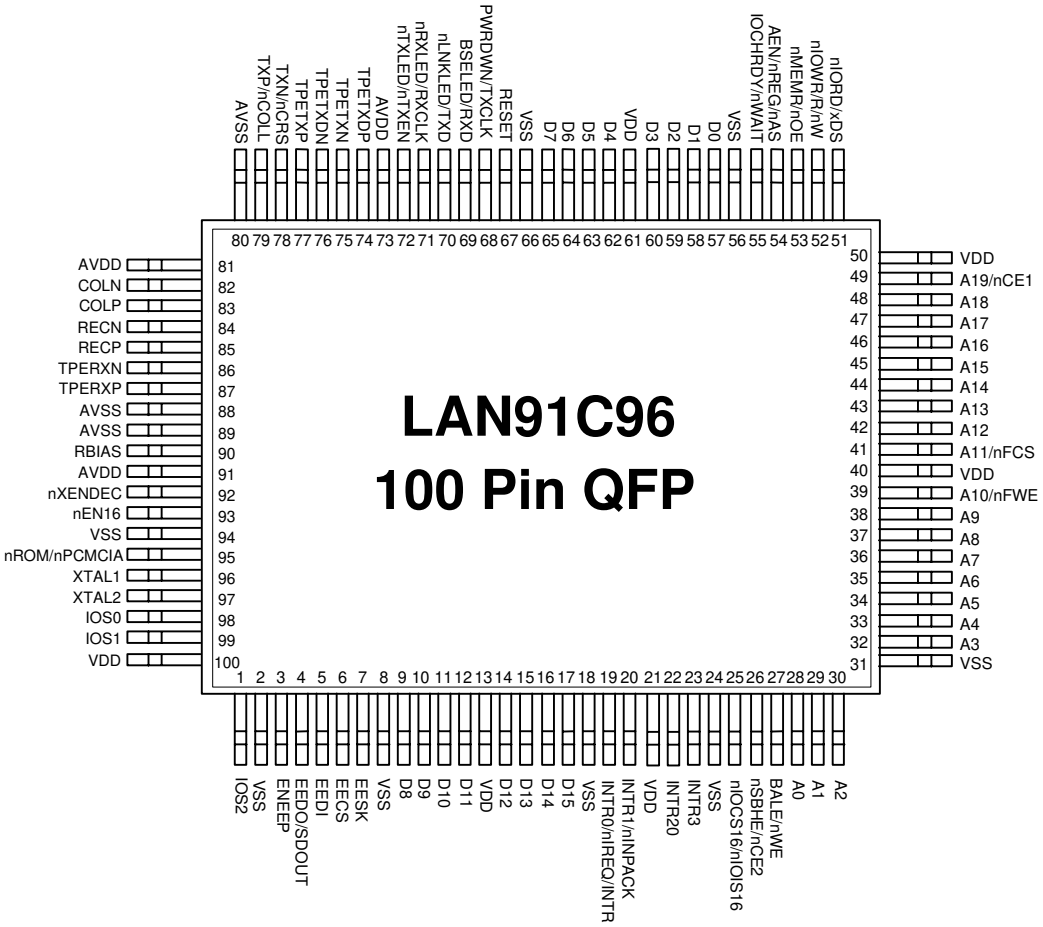

Figure 3.1 - LAN91C96 100 Pin QFP

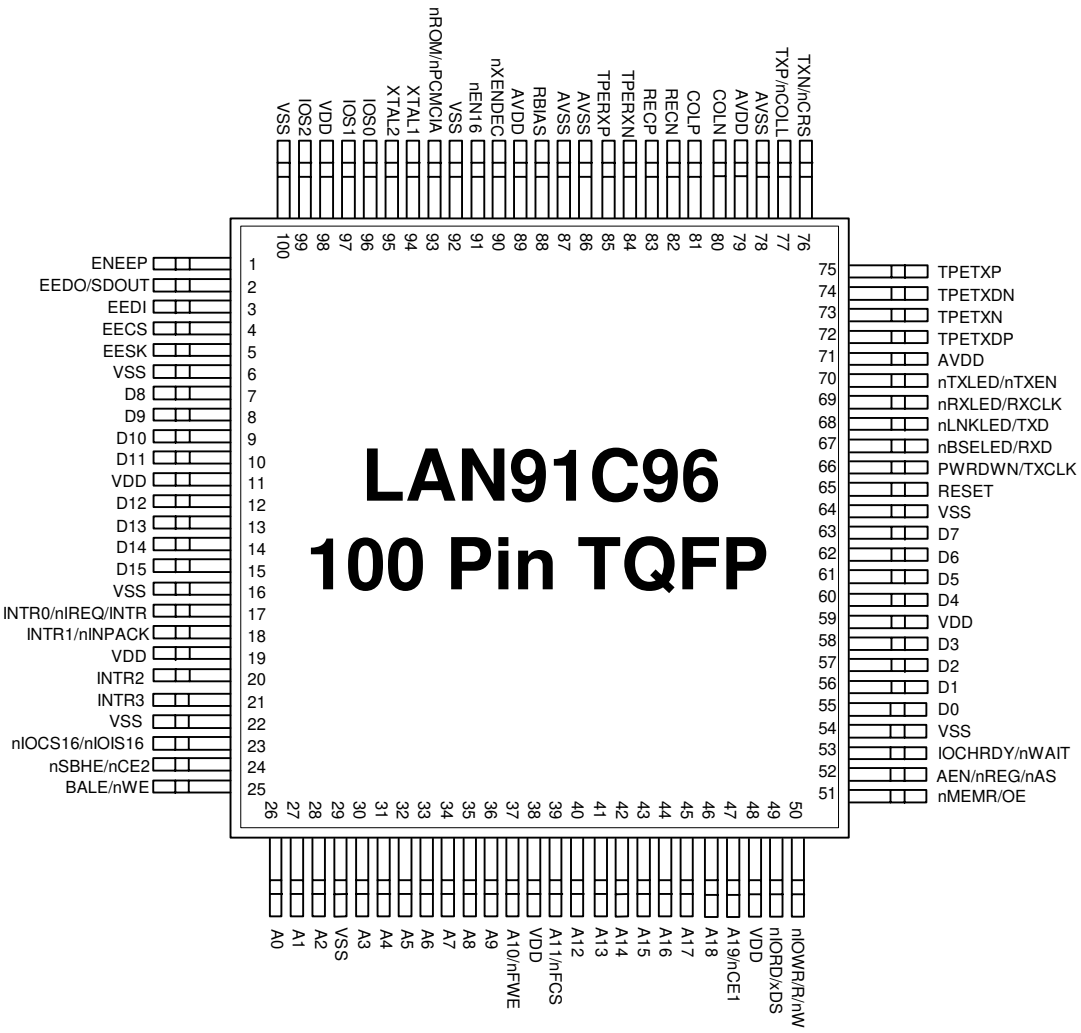

Figure 3.2 - LAN91C96 100 Pin TQFP

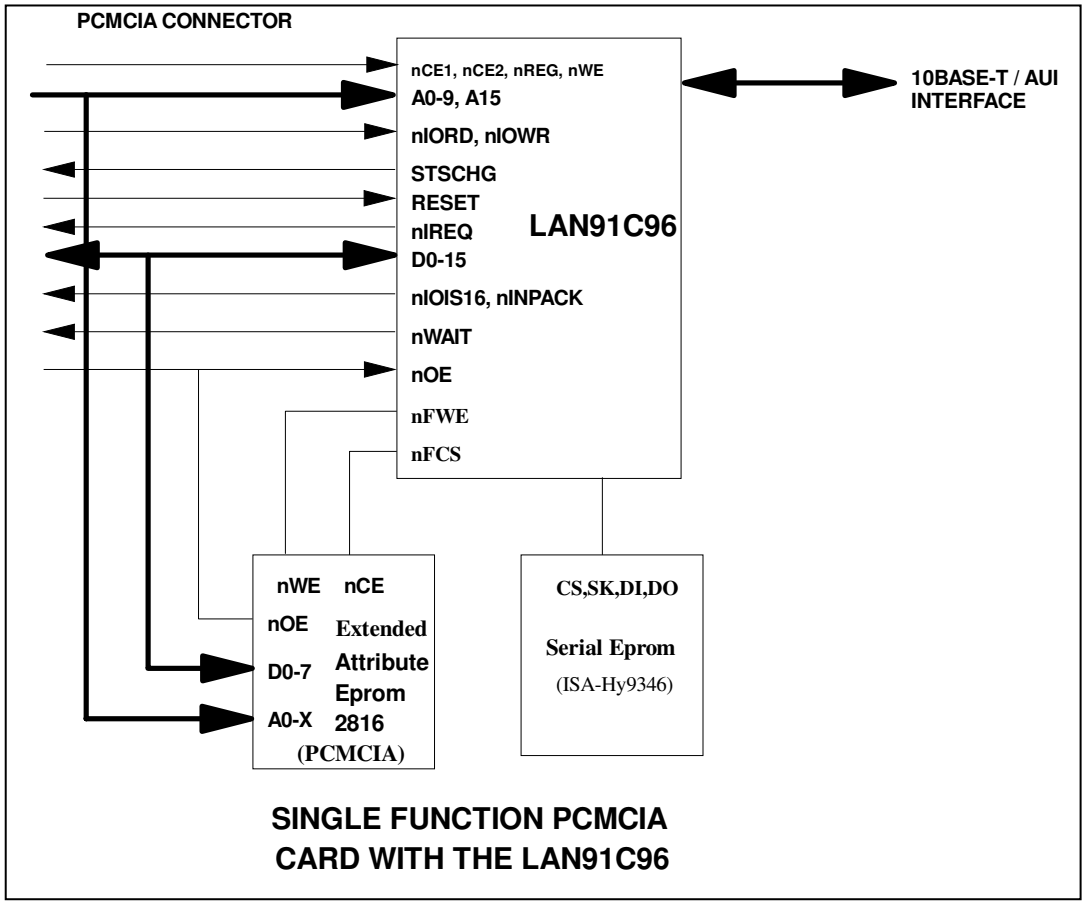

Figure 3.3 - LAN91C96 System Block Diagram

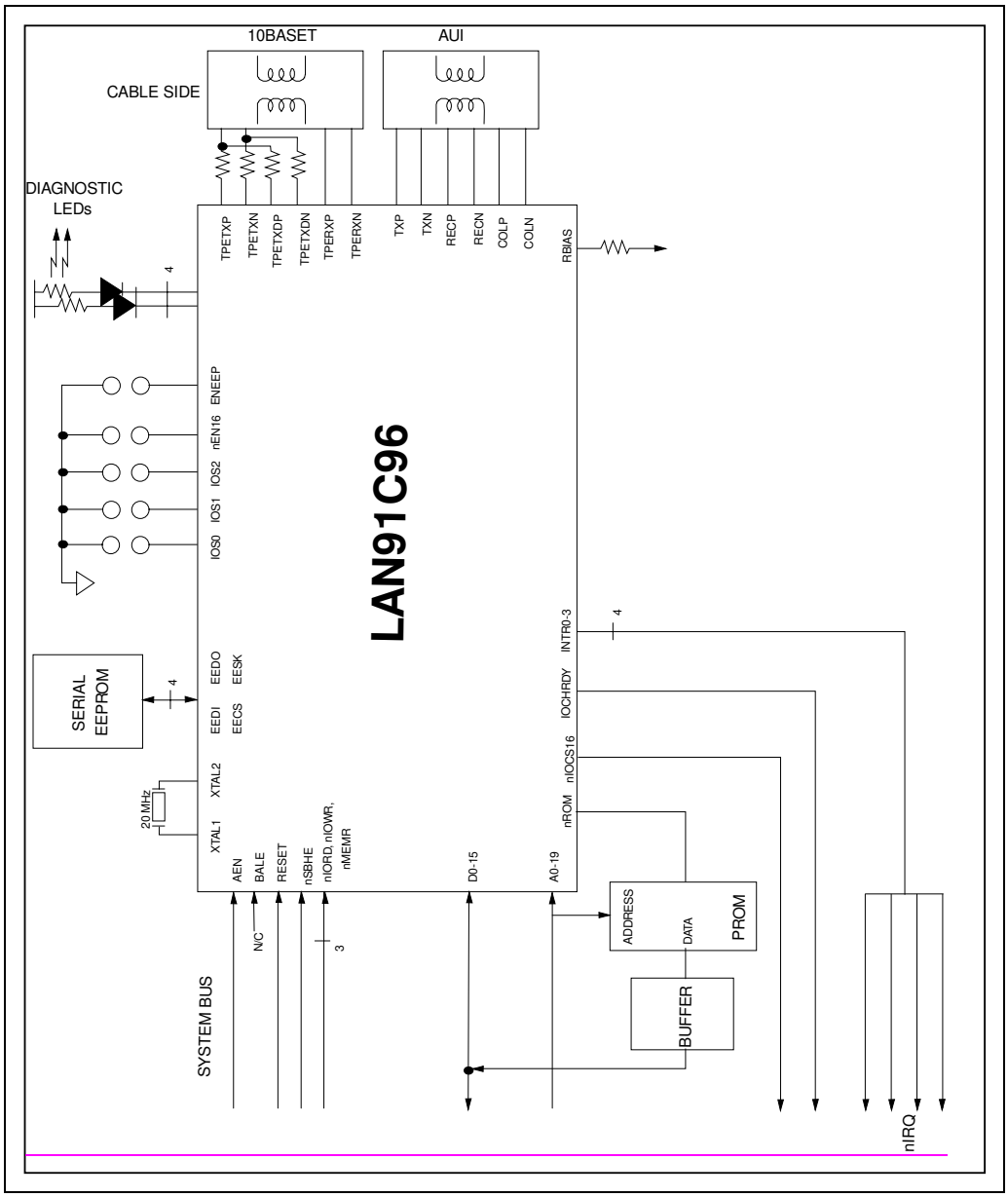

Figure 3.4 – System Diagram for Local Bus with Boot Prom

3.1 Local Bus vs. PCMCIA vs. 68000 Pin Requirements

FUNCTION	LOCAL BUS	PCMCIA	68000	MAX NUMBER OF PINS
SYSTEM ADDRESS BUS	A0 A1-9 A10 A11 A12-14 A15 A16-18 A19 AEN	A0 A1-9 nFWE nFCS A15 nCE1 nREG	 A1-9 A10 A11 A12-14 A15 A16-18 A19 nAS	21
SYSTEM DATA BUS	D0-15	D0-15	D0-15[2]	16
SYSTEM CONTROL BUS	RESET BALE nIORD nIOWR nMEMR IOCHRDY nIOCS16 nSBHE INTR0 INTR1 INTR2 INTR3	RESET nWE nIORD nIOWR nOE nWAIT nIOIS16 nCE2 nIREQ nINPACK	RESET xDS R/nW INTR	12
SERIAL EEPROM	EEDI EEDO EECS EESK ENEEP IOS0 IOS1 IOS2	EEDI EEDO EECS EESK ENEEP IOS0 IOS1 IOS2	EEDI EEDO EECS EESK ENEEP IOS0 IOS1 IOS2	8
CRYSTAL OSC.	XTAL1, XTAL2	XTAL1, XTAL2	XTAL1, XTAL2	2
POWER	VDD, AVDD	VDD, AVDD	VDD, AVDD	9
GROUND	GND, AGND	GND, AGND	GND, AGND	11
10BASE-T interface	TPERXP TPERXN TPETXP TPETXN TPETXDP TPETXDN	TPERXP TPERXN TPETXP TPETXN TPETXDP TPETXDN	TPERXP TPERXN TPETXP TPETXN TPETXDP TPETXDN	6
AUI interface	RECP RECN COLP COLN TXP/nCOLL TXN/nCRS	RECP RECN COLP COLN TXP/nCOLL TXN/nCRS	RECP RECN COLP COLN TXP/nCOLL TXN/nCRS	6

[2] The bytes connect to the 68000 host processor swapped

FUNCTION	LOCAL BUS	PCMCIA	68000	MAX NUMBER OF PINS
LEDs	nLNKLED/TXD nRXLED/RXCLK nBSELED/RXD nTXLED/nTXEN	nLNKLED/TXD nRXLED/RXCLK nBSELED/RXD nTXLED/nTXEN	nLNKLED/TXD nRXLED/RXCLK nBSELED/RXD nTXLED/nTXEN	4
MISC.	RBIAS PWRDWN/TX CLK nXENDEC nEN16 nROM	RBIAS PWRDWN/TX CLK nXENDEC nEN16 nPCMCIA	RBIAS PWRDWN/TXC LK nXENDEC nEN16 nROM	5

Chapter 4 Description of Pin Functions

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
93	95	nROM/ nPCMCIA	I/O4 with pullup	This pin is sampled at the end of RESET. When this pin is sampled low the LAN91C96 is configured for PCMCIA operation and all pin definitions correspond to the PCMCIA mode. For LOCAL BUS operation this pin is left open and it is used as a ROM chip select output that goes active when nMEMR is low and the address bus contains a valid ROM address. In LOCAL BUS mode the LAN91C96 is pin compatible with the LAN91C92 and LAN91C94. To enter the 68000 mode, this pin must be in the LOCAL BUS mode at power up.
26-28 30-36	28,29, 30, 32-38	A0-9	I **	Input address lines 0 through 9.
37	39	A10/nFWE	I	LOCAL BUS - Input address line 10.
			O4	PCMCIA - Output. Flash Memory Write Enable used for programming the attribute memory. Goes active (low) when WE*=0 and COR2=1.
39	41	A11/nFCS	I	LOCAL BUS - Input address line 11.
			O4	PCMCIA - Output. Flash Memory Chip Select used to access attribute memory. Goes active (low) when nREG=0 nCE1=0 and A15=0.
40-46	42-48	A12-18	I **	Input address lines 12 through 18.
47	49	A19/nCE1	I with pullup **	LOCAL BUS - Input address line 19.
				PCMCIA - Card Enable 1 input. Used to select card on even byte accesses.
52	54	AEN/ nREG/ nAS	I with pullup **	LOCAL BUS - Address enable input. Used as an address qualifier. Address decoding is only enabled when AEN is low.
				PCMCIA - Attribute memory and IO select input. Asserted when the card attribute space or IO space is being accessed.
				68000 – Active low input. Address strobe.
24	26	nSBHE/ nCE2	I with pullup **	LOCAL BUS - Byte High Enable input. Asserted (low) by the system to indicate a data transfer on the upper data byte.
				PCMCIA - Card Enable 2 input. Used to select card on odd byte accesses.
53	55	IOCHRDY/ nWAIT	OD24 with pullup	LOCAL BUS - Output. Optionally used by the LAN91C96 to extend host cycles.
				PCMCIA - Output. Optionally used by the LAN91C96 to extend host cycles.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
55-58 60-63 7-10 12-15	57-60, 62-65, 9-12, 14-17	D0-15	I/O24	Bidirectional. 16 bit data bus used to access the LAN91C96 internal registers. The data bus has weak internal pullups. Supports direct connection to the system bus without external buffering. In the case of a 68000 host processor, the upper byte of the data bus must be connected to the lower byte of the 68000 data bus and the lower byte of the data bus must be connected to the upper byte of the 68000 data bus.
65	67	RESET	IS with pullup **	Input. Active high Reset. This input is not considered active unless it is active for at least 100ns to filter narrow glitches.
25	27	BALE/nWE	IS with pullup **	LOCAL BUS - Input. Address strobe. For systems that require address latching, the falling edge of BALE latches address lines and nSBHE.
				PCMCIA - Write Enable input. Used for writing into COR and CSR registers as well as attribute memory space.
17	19	INTR0/ nIREQ/ INTR	O24	LOCAL BUS - Active high interrupt signal. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. This interrupt is tri-stated when not selected.
				PCMCIA - Active low interrupt request output.
				68000 – Active high interrupt signal. The INT SEL1-0 bits in the Configuration register must indicate INT0 selection.
18	20	INTR1/ nINPACK	O24	LOCAL BUS - Output. Active high interrupt signal. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. This interrupt is tri-stated when not selected.
				PCMCIA - Output asserted to acknowledge read cycles.
20	22	INTR2	O24	LOCAL BUS - Outputs. Active high interrupt signals. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. These interrupts are tri-stated when not selected.
21	23	INTR3	O24	LOCAL BUS - Outputs. Active high interrupt signals. The interrupt line selection is determined by the value of INT SEL1-0 bits in the Configuration Register. These interrupts are tri-stated when not selected.
23	25	nIOCS16/ nIOIS16	OD24	LOCAL BUS - Active low output asserted in 16 bit mode when AEN is low and A4-A15 decode to the LAN91C96 address programmed into the high byte of the Base Address Register.
				PCMCIA - Active low output asserted whenever the LAN91C96 is in 16 bit mode, COR0 bit is high and nREG is low.
49	51	nIORD/ xDS	IS with pullup **	LOCAL BUS, PCMCIA - Input. Active low read strobe used to access the LAN91C96 IO space.
				68000 – Data strobe input. UDS, LDS, or DS can be tied to this pin.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
50	52	nIOWR/ R/nW	IS with pullup **	LOCAL BUS, PCMCIA - Input. Active low write strobe used to access the LAN91C96 IO space.
				68000 – Read/nWrite strobe to read from or write to the chip.
51	53	nMEMR/ nOE	IS with pullup **	LOCAL BUS - Active low signal used by the host processor to read from the external ROM.
				PCMCIA - Output Enable input used to read from the COR, CSR and attribute memory.
5	7	EESK	O4	Output. 4usec clock used to shift data in and out of a serial EEPROM.
4	6	EECS	O4	Output. Serial EEPROM chip select.
2	4	EEDO/ SDOUT	O4	Output. Connected to the DI input of the serial EEPROM.
3	5	EEDI	I with pull-down **	Input. Connected to the DO output of the serial EEPROM.
96,97	98,99	IOS0-1	I with pullup	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
99	1	IOS2	I with pullup **	Input. External switches can be connected to these lines to select between predefined EEPROM configurations. The values of these pins are readable.
70	72	nTXLED/ nTXEN	OD16	INTERNAL ENDEC - Transmit LED output.
			O162	EXTERNAL ENDEC - Active low Transmit Enable output.
67	69	nBSELED/ RXD	OD16	INTERNAL ENDEC - Board Select LED activated by accesses to I/O space (nIORD or nIOWR active with AEN low and valid address decode for LOCAL BUS, and with nREG low and COR0 high for PCMCIA). The pulse is stretched beyond the access duration to make the LED visible.
			I with pullup	EXTERNAL ENDEC - NRZ receive data input.
69	71	nRXLED/ RXCLK	OD16	INTERNAL ENDEC - Receive LED output.
			I with pullup	EXTERNAL ENDEC - Receive clock input.
68	70	nLNKLED/ TXD	OD16	INTERNAL ENDEC - Link LED output.
			O162	EXTERNAL ENDEC - Transmit Data output.
1	3	ENEEP	I with pullup **	Input. This active high input enables the EEPROM to be read or written by the LAN91C96. Internally pulled up. Must be connected to ground if no serial EEPROM is used.

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
91	93	nEN16	I with pullup **	Input. When low the LAN91C96 is configured for 16 bit bus operation. If left open the LAN91C96 works in 8 bit bus mode. 16 bit configuration can also be programmed via serial EEPROM or software initialization of the CONFIGURATION REGISTER.
94	96	XTAL1	Iclk **	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to this pin (XTAL1) and XTAL2 should be left open.
95	97	XTAL2	Iclk	An external parallel resonance 20MHz crystal should be connected across these pins. If an external clock source is used, it should be connected to XTAL1 and this pin (XTAL2) should be left open.
83 82	85 84	RECP/ RECN	Diff. Input **	AUI receive differential inputs.
77 76	79 78	TXP/nCOLL TXN/nCRS	Diff. Output	INTERNAL ENDEC - (nXENDEC pin open). In this mode TXP and TXN are the AUI transmit differential outputs. They must be externally pulled up using 150 ohm resistors.
			I **	EXTERNAL ENDEC - (nXENDEC pin tied low). In this mode the pins are inputs used for collision and carrier sense functions.
81 80	83 82	COLP COLN	Diff. Input **	AUI collision differential inputs. A collision is indicated by a 10MHz signal at this input pair.
85 84	87 86	TPERXP TPERXN	Diff. Input **	10BASE-T receive differential inputs.
75 73	77 75	TPETXP TPETXN	Diff. Output	INTERNAL ENDEC - 10BASE-T transmit differential outputs.
72 74	74 76	TPETXDP TPETXDN	Diff. Output	10BASE-T delayed transmit differential outputs. Used in combination with TPETXP and TPETXN to generate the 10BASE-T transmit pre-distortion.
66	68	PWRDWN/ TXCLK	I with pullup **	INTERNAL ENDEC - Powerdown input. It keeps the LAN91C96 in powerdown mode when high (open). Must be low for normal operation.
				EXTERNAL ENDEC - Transmit clock input from external ENDEC.
88	90	RBIAS	Analog Input	A resistor should be connected between this pin and analog ground to determine the receive threshold voltage of TX Receive, AUI Receive, AUI Collision Receive, and AUI transmit voltage.
90	92	nXENDEC	I with pullup **	When tied low the LAN91C96 is configured for EXTERNAL ENDEC. When tied high or left open the LAN91C96 will use its internal encoder/decoder.
11,19, 48,59, 98,38	13,21,40, 50, 61,100	VDD		+5V power supply pins or 3.3V power supply pins (Revisions E and later)
71,79, 89	73,81, 91	AVDD		+5V analog power supply pins or 3.3V power supply pins (Revisions E and later)

PIN NO.		PIN NAME	TYPE	DESCRIPTION
TQFP	QFP			
100,6, 22,29 54,64,92, 16	2,8,18, 24,31, 56,66, 94	GND		Ground pins.
78,86 87	80,88,89	AGND		Analog ground pins.

4.1 Buffer Symbols

O4 Output buffer with 2mA source and 4mA sink *at 5V.*

Output buffer with 1mA source and 2mA sink at 3.3V

I/O4 Output buffer with 2mA source and 4mA sink *at 5V.*

Output buffer with 1mA source and 2mA sink at 3.3V.

O162 Output buffer with 2mA source and 16mA sink *at 5V.*

Output buffer with 1mA source and 8mA sink at 3.3V.

O24 Output buffer with 12mA source and 24mA sink *at 5V.*

Output buffer with 6mA source and 12mA sink at 3.3V.

OD16 Open drain buffer with 16mA sink *at 5V.*

Open drain buffer with 8mA sink at 3.3V.

OD24 Open drain buffer with 24mA sink *at 5V.*

Open drain buffer with 12mA sink at 3.3V.

I/O24 Bi-directional buffer with 12mA source and 24mA sink *at 5V.*

Bi-directional buffer with 6mA source and 16mA sink at 3.3V.

I Input buffer with TTL levels.

IS Input buffer with Schmitt Trigger Hysteresis.

Iclk Clock input buffer.

** Signal is 5.0V input tolerant when V_{cc}=3.3V. **For Revision E and later.**

DC levels and conditions defined in the DC Electrical Characteristics section.

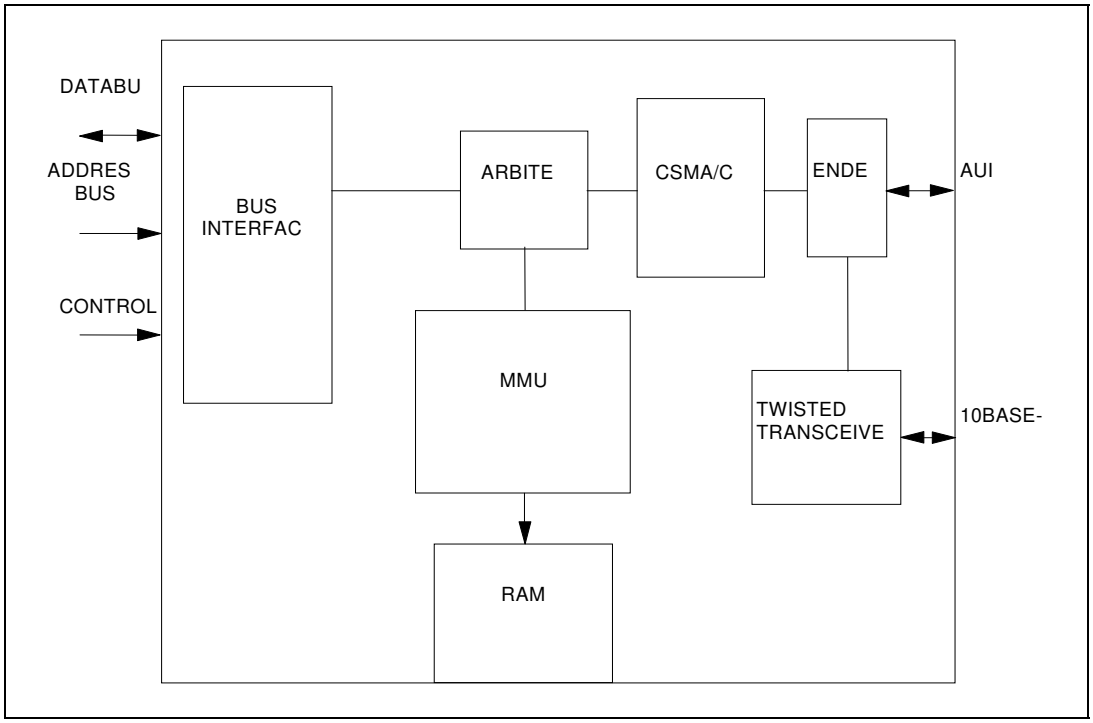

Figure 4.1 - LAN91C96 Internal Block Diagram

Chapter 5 Functional Description

Except for the bus interface, the functional behavior of the LAN91C96 after initial configuration is identical for LOCAL BUS and PCMCIA modes.

The LAN91C96 includes an arbitrated shared memory of 6144 bytes. Any portion of this memory can be used for receive or transmit packets.

The MMU unit allocates RAM memory to be used for transmit and receive packets, using 256 byte pages.

The arbitration is transparent to the CPU in every sense. There is no speed penalty for LOCAL BUS type of machines due to arbitration. There are no restrictions on what locations can be accessed at any time. RAM accesses as well as MMU requests are arbitrated.

The RAM is accessed by mapping it into I/O space for sequential access. Except for the RAM accesses and the MMU request/release commands, I/O accesses are not arbitrated.

The I/O space is 16 bits wide. Provisions for 8 bit systems are handled by the bus interface.

In the system memory space, up to 64 kbytes are decoded by the LAN91C96 as expansion ROM. The ROM expansion area is 8 bits wide.

Device configuration is done using a serial EEPROM, with support for modifications to the EEPROM at installation time. A Flash ROM is supported for PCMCIA attribute memory.

The CSMA/CD core implements the 802.3 MAC layer protocol. It has two independent interfaces, the data path and the control path.

Both interfaces are 16 bits wide. The control path provides a set of registers used to configure and control the block. These registers are accessible by the CPU through the LAN91C96 I/O space. The data path is of sequential access nature and typically works in one direction at any given time. An internal DMA type of interface connects the data path to the device RAM through the arbiter and MMU.

The CSMA/CD data path interface is not accessible to the host CPU.

The internal DMA interface can arbitrate for RAM access and request memory from the MMU when necessary.

An encoder/decoder block interfaces the CSMA/CD block on the serial side. The encoder will do the Manchester encoding of the transmit data at 10 Mb/s, while the decoder will recover the receive clock, and decode received data.

Carrier and Collision detection signals are also handled by this block and relayed to the CSMA/CD block.

The encoder/decoder block can interface the network through the AUI interface pairs, or it can be programmed to use the internal 10BASE-T transceiver and connect to a twisted pair network.

The twisted pair interface takes care of the medium dependent signaling for 10BASE-T type of networks. It is responsible for line interface (with external pulse transformers and pre-distortion resistors), collision detection as well as the link integrity test function. The LAN91C96 provides a 16-bit data path into RAM. The RAM is private and can only be accessed by the system via the arbiter. RAM memory is managed by the MMU. Byte and word accesses to the RAM are supported.

If the system to SRAM bandwidth is insufficient the LAN91C96 will automatically use its IOCHRDY line for flow control. However, for LOCAL BUS, IOCHRDY will never be negated.

The LAN91C96 consists of an integrated Ethernet controller mapped entirely in I/O space. In addition, PCMCIA attribute memory space is decoded to interface an external CIS ROM, with configuration registers as per PCMCIA 3.X extensions (except COR) implemented on-chip in attribute space above the ROM decode area. The PCMCIA Configuration Registers are accessible in I/O space and also to allow non-PCMCIA dual function designs.

The Ethernet controller function includes a built-in 6kbyte RAM for packet storage. This RAM buffer is accessed by the CPU through sequential access regions of 256 bytes each. The RAM access is internally arbitrated by the LAN91C96, and dynamically allocated between transmit and receive packets. Each packet may consist of one or more 256 byte page. The Ethernet controller functionality is identical to the LAN91C94 and LAN91C95 except where indicated otherwise.

The LAN91C96 Memory Management Unit parameters are:

RAM SIZE	6kbytes
MAX. NUMBER OF PAGES	24
MAX. NUMBER OF PACKETS	24 (FIFOs have 24 entries of 5 bits)
MAX. PAGES PER PACKET	6
PAGE SIZE	256 bytes

5.1 Buffer Memory

The logical addresses for RAM access are divided into TX area and RX area.

The TX area is seen by the CPU as a window through which packets can be loaded into memory before queuing them in the TX FIFO of packets. The TX area can also be used to examine the transmit completion status after packet transmission.

The RX area is associated to the output of the RX FIFO of packets, and is used to access receive packet data and status information.

The logical address is specified by loading the address pointer register. The pointer can automatically increment on accesses.

All accesses to the RAM are done via I/O space.

A bit in the address pointer also specifies if the address refers to the TX or RX area.

In the TX area, the host CPU has access to the next transmit packet being prepared for transmission. In the RX area, it has access to the first receive packet not processed by the CPU yet.

The FIFO of packets, existing beneath the TX and RX areas, is managed by the MMU. The MMU dynamically allocates and releases memory to be used by the transmit and receive functions.

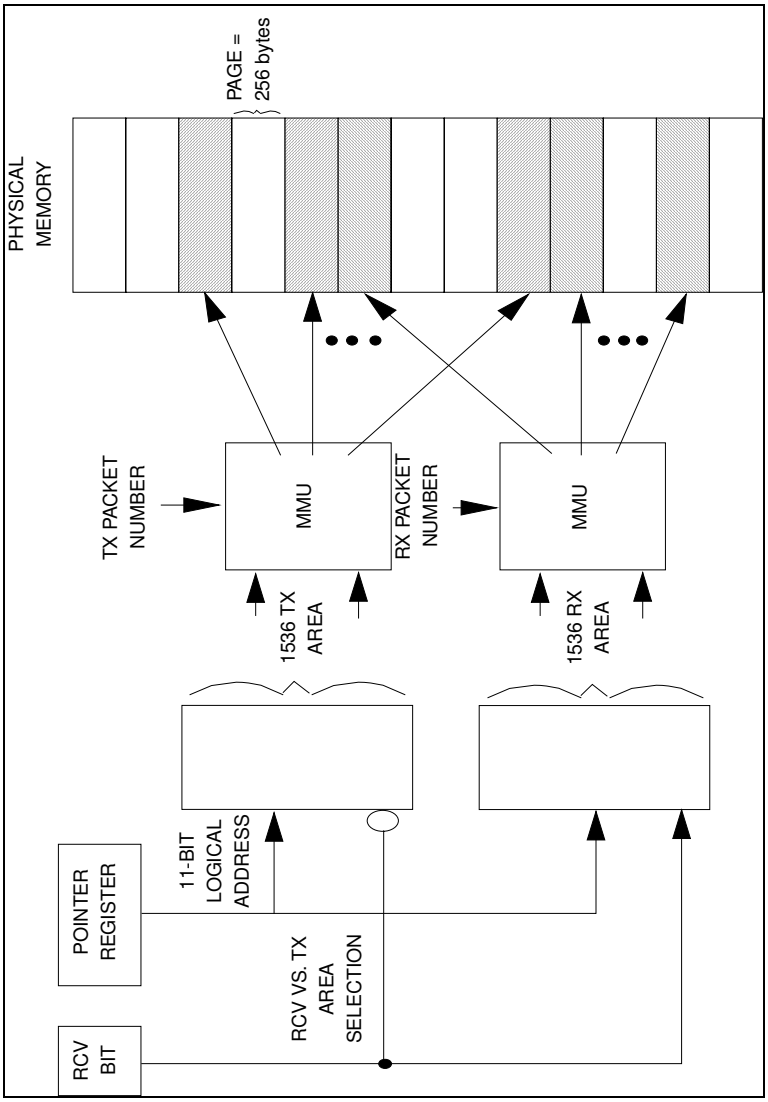

Figure 5.1 – Mapping and Paging vs. Receive and Transmit Area