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16-bit Non-PCI 10/100 Ethernet Controller with HP Auto-MDIX and Industrial Temperature Support

Highlights

- Optimized for medium performance applications
- Efficient architecture with low CPU overhead
- Easily interfaces to most 16-bit embedded CPU's
- Integrated PHY with HP Auto-MDIX support
- Supports audio & video streaming over Ethernet: multiple standard-definition (SD) MPEG2 streams

Target Applications

- Basic cable, satellite, and IP set-top boxes
- Digital video recorders
- Video-over IP solutions, IP PBX & video phones
- Wireless routers & access points
- Audio distribution systems
- Printers, kiosks, security systems
- General embedded applications

Key Benefits

- Non-PCI Ethernet controller for medium performance applications
 - 16-bit interface
 - Burst-mode read support
 - External MII Interface
- Eliminates dropped packets
 - Internal buffer memory can store over 200 packets
 - Automatic PAUSE and back-pressure flow control
- Minimizes CPU overhead
 - Supports Slave-DMA
 - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
- SRAM-like interface easily interfaces to most embedded CPU's or SoC's
- Reduced Power Modes
 - Numerous power management modes
 - Wake on LAN
 - Magic packet wakeup
 - Wakeup indicator event signal
 - Link Status Change

- Single chip Ethernet controller
 - Fully compliant with IEEE 802.3/802.3u standards
 - Integrated Ethernet MAC and PHY
 - 10BASE-T and 100BASE-TX support
 - Full- and Half-duplex support
 - Full-duplex flow control
 - Backpressure for half-duplex flow control
 - Preamble generation and removal
 - Automatic 32-bit CRC generation and checking
 - Automatic payload padding and pad removal
 - Loop-back modes
- Flexible address filtering modes
 - One 48-bit perfect address
 - 64 hash-filtered multicast addresses
 - Pass all multicast
 - Promiscuous mode
 - Inverse filtering
 - Pass all incoming with status report
 - Disable reception of broadcast packets
- Integrated 10/100 Ethernet PHY
 - Supports HP Auto-MDIX
 - Auto-negotiation
 - Supports energy-detect power down
- Host bus interface
 - Simple, SRAM-like interface
 - 16-bit data bus
 - 16Kbyte FIFO with flexible TX/RX allocation
 - One configurable host interrupt
- Miscellaneous features
 - Low-profile 100-pin TQFP, RoHS Compliant package
 - Integrated 1.8V regulator
 - General Purpose Timer
 - Optional EEPROM interface
 - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- Single 3.3V Power Supply with 5V tolerant I/O
- -40°C to +85°C Industrial Temperature Support

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Table of Contents

1.0 General Description	4
2.0 Pin Description and Configuration	9
3.0 Functional Description	18
4.0 Internal Ethernet PHY	53
5.0 Register Description	62
6.0 Timing Diagrams	108
7.0 Operational Characteristics	119
8.0 Package Information	126
Appendix A: Data Sheet Revision History	127

LAN9215i

1.0 GENERAL DESCRIPTION

The LAN9215i is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9215i has been architected to provide the best price-performance ratio for any 16-bit application with medium performance requirements. The LAN9215i is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

The LAN9215i includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with a 16-bit external bus. The LAN9215i includes large transmit and receive data FIFOs to accommodate high latency applications. In addition, the LAN9215i memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9215i is well suited for many medium-performance embedded applications, including:

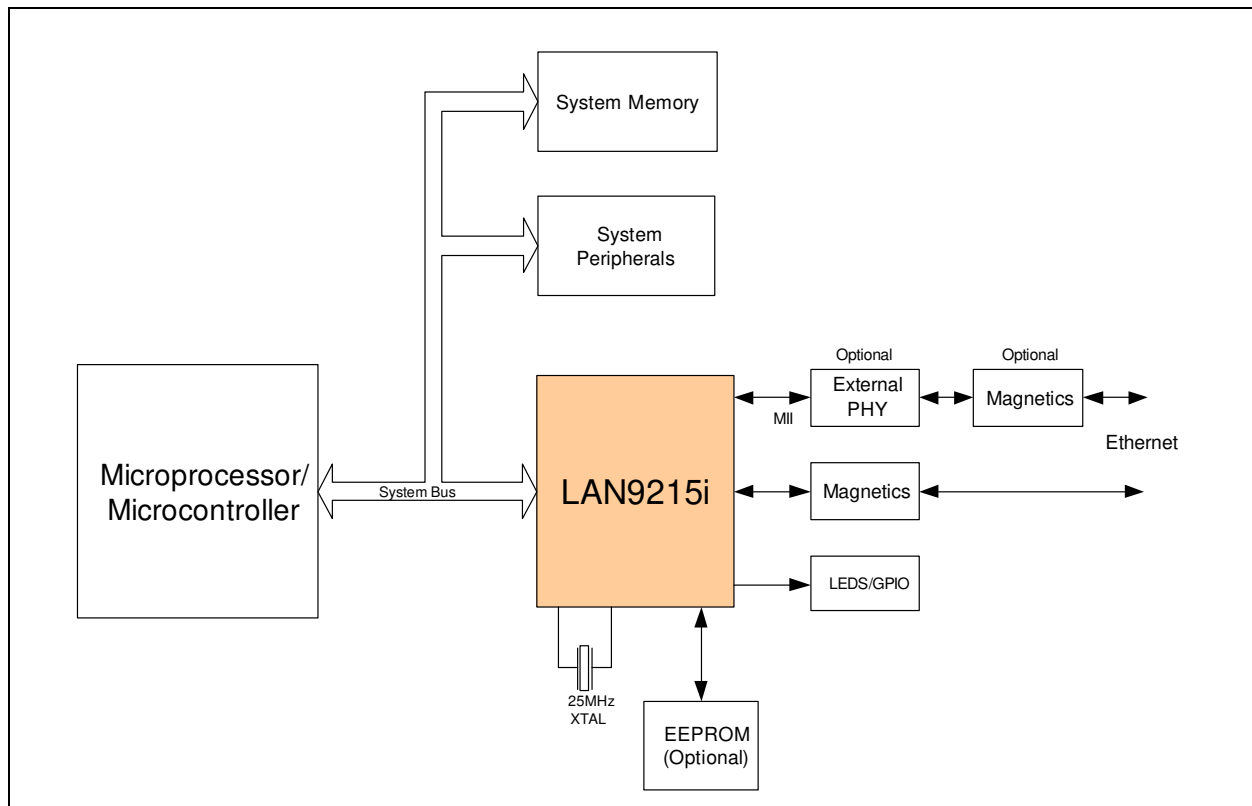
- Printers, kiosks, POS terminals and security systems
- Audio distribution systems
- General embedded systems
- Basic cable, satellite and IP set-top boxes
- Voice-over-IP solutions

The LAN9215i also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9215i can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9215i supports numerous power management and wakeup features. The LAN9215i can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including "Magic Packet", "Wake on LAN" and "Link Status Change". This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

1.1 Block Diagram

FIGURE 1-1: SYSTEM BLOCK DIAGRAM



The Microchip LAN9215i integrated 10/100 MAC/PHY controller is a peripheral chip that performs the function of translating parallel data from a host controller into Ethernet packets. The LAN9215i Ethernet MAC/PHY controller is designed and optimized to function in an embedded environment. All communication is performed with programmed I/O transactions using the simple SRAM-like host interface bus.

The diagram shown above, describes a typical system configuration of the LAN9215i in a typical embedded environment.

The LAN9215i is a general purpose, platform independent, Ethernet controller. The LAN9215i consists of four major functional blocks. The four blocks are:

- 10/100 Ethernet PHY
- 10/100 Ethernet MAC
- RX/TX FIFOs
- Host Bus Interface (HBI)

LAN9215i

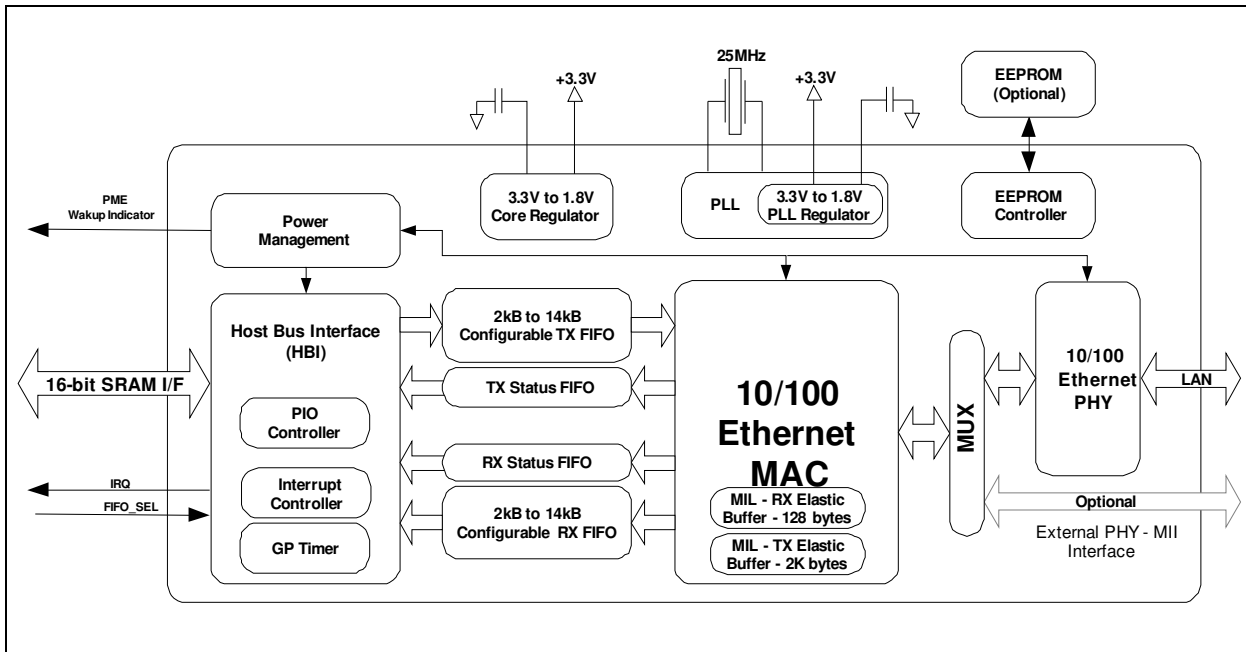
1.2 Compatibility with First-generation LAN9118 Family Devices

The LAN9215i is driver-, register-, and footprint-compatible with previous generation LAN9118 Family devices. Drivers written for these products will work with the LAN9215i. However, in order to support HP Auto-MDIX, other components such as the magnetics and the passive components around the magnetics need to change, and supporting these changes does require a minor PCB change. A reference design for the LAN9215i will be available on Microchip's web-site.

1.3 Internal Block Overview

This section provides an overview of each of these functional blocks as shown in Figure 1-2, "Internal Block Diagram".

FIGURE 1-2: INTERNAL BLOCK DIAGRAM



1.4 10/100 Ethernet PHY

The LAN9215i integrates an IEEE 802.3 physical layer for twisted pair Ethernet applications. The PHY can be configured for either 100 Mbps (100BASE-TX) or 10 Mbps (10BASE-T) Ethernet operation in either full or half duplex configurations. The PHY block supports HP Auto-MDIX and auto-negotiation.

Minimal external components are required for the utilization of the Integrated PHY.

1.5 10/100 Ethernet MAC

The transmit and receive data paths are separate within the MAC allowing the highest performance especially in full duplex mode. The data paths connect to the PIO interface Function via separate busses to increase performance. Payload data as well as transmit and receive status is passed on these busses.

A third internal bus is used to access the MAC's Control and Status Registers (CSR's). This bus is accessible from the host through the PIO interface function.

On the backend, the MAC interfaces with the internal 10/100 PHY through a MII (Media Independent Interface) port internal to the LAN9215i. The MAC CSR's also provide a mechanism for accessing the PHY's internal registers through the internal SMI (Serial Management Interface) bus. The Ethernet MAC can also communicate with an external PHY. This mode however, is optional.

The MAC Interface Layer (MIL), within the MAC, contains a 2K Byte transmit and a 128 Byte receive FIFO which is separate from the TX and RX FIFOs. The FIFOs within the MAC are not directly accessible from the host interface. The differentiation between the TX/RX FIFO memory buffers and the MAC buffers is that when the transmit or receive packets are in the MAC buffers, the host no longer can control or access the TX or RX data. The MAC buffers (both TX and RX) are in effect the working buffers of the Ethernet MAC logic. In the case of reception, the data must be moved first to the RX FIFOs for the host to access the data. For TX operations, the MIL operates in store-and-forward mode and will queue an entire frame before beginning transmission.

1.6 Receive and Transmit FIFOs

The Receive and Transmit FIFOs allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the host interface and the MAC through which all transmitted and received data and status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks thus reducing or minimizing overrun conditions. Like the MAC, the FIFOs have separate receive and transmit data paths. In addition, the RX and TX FIFOs are configurable in size, allowing increased flexibility.

1.7 Interrupt Controller

The LAN9215i supports a single programmable interrupt. The programmable nature of this interrupt allows the user the ability to optimize performance dependent upon the application requirement. Both the polarity and buffer type of the interrupt pin are configurable for the external interrupt processing. The interrupt line can be configured as an open-drain output to facilitate the sharing of interrupts with other devices. In addition, a programmable interrupt de-assertion interval is provided.

1.8 GPIO Interface

A 3-bit GPIO and 2-bit GPO (Multiplexed on the EEPROM and LED Pins) interface is included in the LAN9215i. It is accessible through the host bus interface via the CSRs. The GPIO signals can function as inputs, push-pull outputs and open drain outputs. The GPIO's (GPO's are not configurable) can also be configured to trigger interrupts with programmable polarity.

1.9 Serial EEPROM Interface

A serial EEPROM interface is included in the LAN9215i. The serial EEPROM is optional and can be programmed with the LAN9215i MAC address. The LAN9215i can optionally load the MAC address automatically after power-on reset, hardware reset, or soft reset.

1.10 Power Management Controls

The LAN9215i supports comprehensive array of power management modes to allow use in power sensitive applications. Wake on LAN, Link Status Change and Magic Packet detection are supported by the LAN9215i. An external PME (Power Management Event) interrupt is provided to indicate detection of a wakeup event.

1.11 General Purpose Timer

The general-purpose timer has no dedicated function within the LAN9215i and may be programmed to issue a timed interrupt.

1.12 Host Bus Interface (SRAM Interface)

The host bus interface provides a FIFO interface for the transmit and receive data paths, as well as an interface for the LAN9215i Control and Status Registers (CSR's).

The host bus interface is the primary bus for connection to the embedded host system. This interface models an asynchronous SRAM. TX FIFO, RX FIFO, and CSR's are accessed through this interface. Programmed I/O transactions are supported.

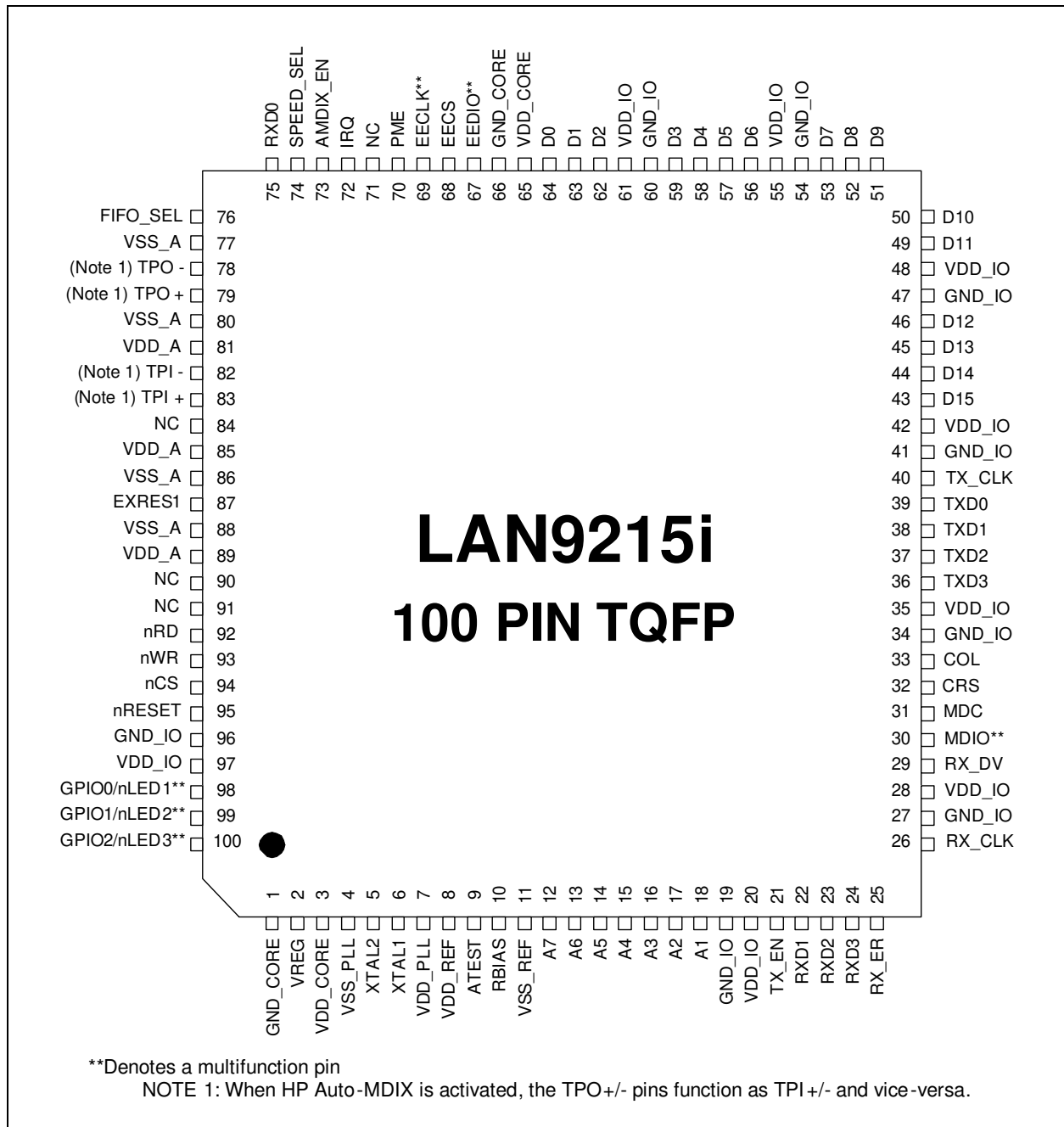
The LAN9215i host bus interface supports 16-bit bus transfers. Internally, all data paths are 32-bits wide. The LAN9215i can be interfaced to either Big-Endian or Little-Endian processors.

1.13 External MII Interface

The LAN9215i also supports the ability to interface to an external PHY device. This interface is compatible with all IEEE 802.3 MII compliant physical layer devices. For additional information on the MII interface and associated signals, please refer to [Section 3.11, "MII Interface - External MII Switching," on page 36](#) for more information.

2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: PIN CONFIGURATION (TOP VIEW)



LAN9215i

2.1 Pin List

TABLE 2-1: HOST BUS INTERFACE SIGNALS

Name	Symbol	Buffer Type	# Pins	Description
Host Data	D[15:0]	I/O8	16	Bi-directional data port.
Host Address	A[7:1]	IS	7	7-bit Address Port. Used to select Internal CSR's and TX and RX FIFOs.
Read Strobe	nRD	IS	1	Active low strobe to indicate a read cycle.
Write Strobe	nWR	IS	1	Active low strobe to indicate a write cycle. This signal, qualified with nCS, is also used to wakeup the LAN9215i when it is in a reduced power state.
Chip Select	nCS	IS	1	Active low signal used to qualify read and write operations. This signal qualified with nWR is also used to wakeup the LAN9215i when it is in a reduced power state.
Interrupt Request	IRQ	O8/OD8	1	Programmable Interrupt request. Programmable polarity, source and buffer types.
FIFO Select	FIFO_SEL	IS	1	When driven high all accesses to the LAN9215i are to the RX or TX Data FIFOs. In this mode, the A[7:3] upper address inputs are ignored.

TABLE 2-2: DEFAULT ETHERNET SETTINGS

Default Ethernet Settings			
SPEED_SEL	Speed	Duplex	Auto Neg.
0	10Mbps	Half-Duplex	Disabled
1	100Mbps	Half-Duplex	Enabled

TABLE 2-3: LAN INTERFACE SIGNALS

Name	Symbol	Buffer Type	# Pins	Description
TPO+	TPO+	AO	1	Transmit Positive Output (normal) Receive Positive Input (reversed)
TPO-	TPO-	AO	1	Transmit Negative Output (normal) Receive Negative Input (reversed)
TPI+	TPI+	AI	1	Receive Positive Input (normal) Transmit Positive Input (reversed)
TPI-	TPI-	AI	1	Receive Negative Input (normal) Transmit Negative Output (reversed)
PHY External Bias Resistor	EXRES1	AI	1	Must be connected to ground through a 12.4K ohm 1% resistor.

Note: The pin names for the twisted pair pins shown above apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected, or a reverse connection is manually selected, the input pins become outputs, and vice-versa, as indicated in the descriptions.

TABLE 2-4: SERIAL EEPROM INTERFACE SIGNALS

Name	Symbol	Buffer Type	# Pins	Description
EEPROM Data, GPO3, TX_EN, TX_CLK	EEDIO/GPO3/ TX_EN/TX_CLK	I/O8	1	<p>EEPROM Data: This bi-directional pin can be connected to a serial EEPROM DIO. This is optional.</p> <p>General Purpose Output 3: This pin can also function as a general purpose output, or it can be configured to monitor the TX_EN or TX_CLK signals on the internal MII port. When configured as a GPO signal, or as a TX_EN/TX_CLK monitor, the EECS pin is deasserted so as to never unintentionally access the serial EEPROM. This signal cannot function as a general-purpose input.</p>
EEPROM Chip Select	EECS	O8	1	Serial EEPROM chip select.
EEPROM Clock, GPO4 RX_DV, RX_CLK	EECLK/GPO4/ RX_DV/RX_CLK	O8	1	<p>EEPROM Clock: Serial EEPROM Clock pin.</p> <p>General Purpose Output 4: This pin can also function as a general-purpose output, or it can be configured to monitor the RX_DV or RX_CLK signals on the internal MII port. When configured as a GPO signal, or as an RX_DV/RX_CLK monitor, the EECS pin is deasserted so as to never unintentionally access the serial EEPROM. This signal cannot function as a general-purpose input.</p> <p>Note: When the EEPROM interface is not used, the EECLK pin must be left unconnected.</p>

LAN9215i

TABLE 2-5: SYSTEM AND POWER SIGNALS

Name	Symbol	Buffer Type	# Pins	Description
Crystal 1, Clock In	XTAL1/CLKIN	ICLK	1	External 25MHz Crystal Input. This pin can also be connected to single-ended TTL oscillator (CLKIN). If this method is implemented, XTAL2 should be left unconnected.
Crystal 2	XTAL2	OCLK	1	External 25MHz Crystal output.
Reset	nRESET	IS (PU)	1	Active-low reset input. Resets all logic and registers within the LAN9215i. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected, the LAN9215i will rely on its internal power-on reset circuitry. Note: The LAN9215i must always be read at least once after power-up, reset, or upon return from a power-saving state or write operations will not function. See Section 3.10, "Detailed Reset Description," on page 35 for additional information
Wakeup Indicator	PME	O8/OD8	1	When programmed to do so, is asserted when the LAN9215i detects a wake event and is requesting the system to wake up from the associated sleep state. The polarity and buffer type of this signal is programmable. Note: Detection of a Power Management Event, and assertion of the PME signal will not wakeup the LAN9215i. The LAN9215i will only wake up when it detects a host write cycle (assertion of nCS and nWR). Although any write to the LAN9215i, regardless of the data written, will wake-up the device when it is in a power-saving mode, it is required that the BYTE_TEST register be used for this purpose.
Auto-MDIX Enable	AMDIX_EN	I (PD)	1	Enables Auto-MDIX. Pull high enable Auto-MDIX, pull low or leave unconnected to disable Auto-MDIX.
10/100 Selector	SPEED_SEL	I (PU)	1	This signal functions as a configuration input on power-up and is used to select the default Ethernet settings. Upon deassertion of reset, the value of the input is latched. This signal functions as shown in Table 2-2, "Default Ethernet Settings," below.
No Connect	NC		4	No Connect. These pins must be left open.

TABLE 2-5: SYSTEM AND POWER SIGNALS (CONTINUED)

Name	Symbol	Buffer Type	# Pins	Description
General Purpose I/O data, nLED1 (Speed Indicator), nLED2 (Link & Activity Indicator), nLED3 (Full-Duplex Indicator).	GPIO[2:0]/nLED[3:1]	IS/O12/OD12	3	<p>General Purpose I/O data: These three general-purpose signals are fully programmable as either push-pull output, open-drain output or input by writing the GPIO_CFG configuration register in the CSR's. They are also multiplexed as GP LED connections. GPIO signals are Schmitt-triggered inputs. When configured as LED outputs these signals are open-drain.</p> <p>nLED1 (Speed Indicator). This signal is driven low when the operating speed is 100Mb. During auto-negotiation, when the cable is disconnected, and during 10Mbps operation, this signal is driven high.</p> <p>nLED2 (Link & Activity Indicator). This signal is driven low (LED on) when the LAN9215i detects a valid link. This signal is pulsed high (LED off) for 80mS whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed LED2 will flash as an activity indicator.</p> <p>nLED3 (Full-Duplex Indicator). This signal is driven low when the link is operating in full-duplex mode.</p>
RBIAS	RBIAS	AI	1	PLL Bias: Connect to an external 12.0K ohm 1.0% resistor to ground. Used for the PLL Bias circuit.
Test Pin	ATEST	I	1	This pin must be connected to VDD for normal operation.
Internal Regulator Power	VREG	P	1	3.3V input for internal voltage regulator
+3.3V I/O Power	VDD_IO	P	8	+3.3V I/O logic power supply pins
I/O Ground	GND_IO	P	8	Ground for I/O pins
+3.3V Analog Power	VDD_A	P	3	+3.3V analog power supply pins. See Note 2-1 .
Analog Ground	VSS_A	P	4	Ground for analog circuitry
Core Voltage Decoupling	VDD_CORE	P	2	+1.8 V from internal core regulator. Both pins must be connected together externally. Each pin requires a 0.01uF decoupling capacitor. In addition, pin 3 requires a bulk 10uF capacitor (<2 Ohm ESR) in parallel. These pins must not be used to supply power to other external devices. See Note 2-1 .
Core Ground	GND_CORE	P	2	Ground for internal digital logic

LAN9215i

TABLE 2-5: SYSTEM AND POWER SIGNALS (CONTINUED)

Name	Symbol	Buffer Type	# Pins	Description
PLL Power	VDD_PLL	P	1	+1.8V Power from the internal PLL regulator. This pin must be connected to a 10uF capacitor (<2 Ohm ESR), in parallel with a 0.01uF capacitor to ground. This pin must not be used to supply power to other external devices. See Note 2-1 .
PLL Ground	VSS_PLL	P	1	GND for the PLL
Reference Power	VDD_REF	P	1	Connected to 3.3v power and used as the reference voltage for the internal PLL
Reference Ground	VSS_REF	P	1	Ground for internal PLL reference voltage

Note 2-1 Please refer to Application Note "AN14.9 - "Migrating from LAN9115 to the LAN9215" for additional details.

TABLE 2-6: MII INTERFACE SIGNALS

Name	Symbol	Buffer Type	# Pins	Description
Transmit Clock:	TX_CLK	I (PD)	1	Transmit Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.
Transmit Data [3:0]	TXD[3:0]	O8 (PD)	4	Transmit Data 3-0: Data bits that are accepted by the PHY for transmission. When the internal PHY is selected, these signals are driven low (0).
Transmit Enable	TX_EN	O8 (PD)	1	Transmit Enable: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. When the internal PHY is selected, this signal is driven low (0).
Receive Clock	RX_CLK	I (PD)	1	Receive Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.
Receive Error	RX_ER	I (PD)	1	Receive Error: Asserted by the PHY to indicate that an error was detected somewhere in the frame presently being transferred from the PHY.
Collision Detect:	COL	I (PD)	1	MII Collision Detect: Asserted by the PHY to indicate detection of collision condition.
Receive Data[3:0]	RXD[3:0]	I Note 2-2	1	Receive Data 3-0: Data bits that are sent from the PHY to the Ethernet MAC. See Note 2-2 .
Carrier Sense	CRS	I (PD)	1	Carrier Sense: Indicates detection of carrier.
Receive Data Valid:	RX_DV	I (PD)	1	Receive Data Valid: Indicates that recovered and decoded data nibbles are being presented by the PHY on RXD[3:0].

TABLE 2-6: MII INTERFACE SIGNALS (CONTINUED)

Name	Symbol	Buffer Type	# Pins	Description
Management Data IO/External PHY Detect	MDIO (EXT_PHY_DET)	I/O8 (PD)	1	<p>Management Data IO: When SMI_SEL = 1, this pin is the MII SMI serial IO bus pin.</p> <p>External PHY Detect: This pin also functions as a strap input, which can be used to indicate the presence of an external PHY.</p> <p>See Note 2-3.</p> <p>Note: See Section 5.3.9, "HW_CFG—Hardware Configuration Register" for more information on SMI_SEL and EXT_PHY_DET</p>
Management Data Clock	MDC	O8 (PD)	1	<p>Management Data Clock: When SMI_SEL = 1, this pin is the MII management data clock. When SMI_SEL=0, this pin is driven low.</p> <p>See Note 2-3.</p> <p>Note: See Section 5.3.9, "HW_CFG—Hardware Configuration Register" for more information on SMI_SEL.</p>

Note 2-2 Pins RXD[3:1] provide internal pull-down resistors to prevent these pins from floating when unused. RXD0 (pin 75) does not provide an internal pull-down resistor. This pin must be pulled or driven to a valid state at all times.

Note 2-3 The external SMI port is selected when SMI_SEL = 1. When SMI_SEL = 0, MDIO is tri-stated and MDC is driven low.

TABLE 2-7: 100-TQFP PACKAGE PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
1	GND_CORE	26	RX_CLK	51	D9	76	FIFO_SEL
2	VREG	27	GND_IO	52	D8	77	VSS_A
3	VDD_CORE	28	VDD_IO	53	D7	78	TPO-
4	VSS_PLL	29	RX_DV	54	GND_IO	79	TPO+
5	XTAL2	30	MDIO	55	VDD_IO	80	VSS_A
6	XTAL1	31	MDC	56	D6	81	VDD_A
7	VDD_PLL	32	CRS	57	D5	82	TPI-
8	VDD_REF	33	COL	58	D4	83	TPI+
9	ATEST	34	GND_IO	59	D3	84	NC
10	RBIAS	35	VDD_IO	60	GND_IO	85	VDD_A
11	VSS_REF	36	TXD3	61	VDD_IO	86	VSS_A
12	A7	37	TXD2	62	D2	87	EXRES1
13	A6	38	TXD1	63	D1	88	VSS_A

LAN9215i

TABLE 2-7: 100-TQFP PACKAGE PIN ASSIGNMENTS (CONTINUED)

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
14	A5	39	TXD0	64	D0	89	VDD_A
15	A4	40	TX_CLK	65	VDD_CORE	90	NC
16	A3	41	GND_IO	66	GND_CORE	91	NC
17	A2	42	VDD_IO	67	EEDIO	92	nRD
18	A1	43	D15	68	EECS	93	nWR
19	GND_IO	44	D14	69	EECLK	94	nCS
20	VDD_IO	45	D13	70	PME	95	nRESET
21	TX_EN	46	D12	71	NC	96	GND_IO
22	RXD1	47	GND_IO	72	IRQ	97	VDD_IO
23	RXD2	48	VDD_IO	73	AMDIX_EN	98	GPIO0/nLED1
24	RXD3	49	D11	74	SPEED_SEL	99	GPIO1/nLED2
25	RX_ER	50	D10	75	RXD0	100	GPIO2/nLED3

2.2 Buffer Types

TABLE 2-8: BUFFER TYPES

Type	Description
I	Input pin
IS	Schmitt triggered Input
O12	Output with 12mA sink and 12mA source
OD12	Open-drain output with 12mA sink
OD8	Open-drain output with 8mA sink
O8	Output 8mA symmetrical drive
PU	50uA (typical) internal pull-up
PD	50uA (typical) internal pull-down
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin

3.0 FUNCTIONAL DESCRIPTION

3.1 10/100 Ethernet MAC

The Ethernet Media Access controller (MAC) incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the host subsystem and the internal Ethernet PHY. The MAC can operate in either 100-Mbps or 10-Mbps mode.

The MAC operates in both half-duplex and full-duplex modes. When operating in half-duplex mode, the MAC complies fully with Section 4 of ISO/IEC 8802-3 (ANSI/IEEE standard) and ANSI/IEEE 802.3 standards. When operating in full-duplex mode, the MAC complies with IEEE 802.3x full-duplex operation standard.

The MAC provides programmable enhanced features designed to minimize host supervision, bus utilization, and pre- or post-message processing. These features include the ability to disable retries after a collision, dynamic FCS (Frame Check Sequence) generation on a frame-by-frame basis, automatic pad field insertion and deletion to enforce minimum frame size attributes, and automatic retransmission and detection of collision frames.

The MAC can sustain transmission or reception of minimally-sized back-to-back packets at full line speed with an inter-packet gap (IPG) of 9.6 microseconds for 10 Mbps and 0.96 microseconds for 100 Mbps.

The primary attributes of the MAC Function are:

- Transmit and receive message data encapsulation
- Framing (frame boundary delimitation, frame synchronization)
- Error detection (physical medium transmission errors)
- Media access management
- Medium allocation (collision detection, except in full-duplex operation)
- Contention resolution (collision handling, except in full-duplex operation)
- Flow control during full-duplex mode
- Decoding of control frames (PAUSE command) and disabling the transmitter
- Generation of control frames
- Interface to the internal PHY and optional external PHY.

The transmit and receive data paths are separate within the LAN9215i from the MAC to host interface allowing the highest performance, especially in full duplex mode. Payload data as well as transmit and receive status are passed on these busses.

A third internal bus is used to access the MAC's "Control and Status Registers" (CSR's). This bus is also accessible from the host.

On the backend, the MAC interfaces with the 10/100 PHY through an MII (Media Independent Interface) port which is internal to the LAN9215i. In addition, there is an external MII interface supporting optional PHY devices. The MAC CSR's also provide a mechanism for accessing the PHY's internal registers through the internal SMI (Serial Management Interface) bus.

The receive and transmit FIFOs allow increased packet buffer storage to the MAC. The FIFOs are a conduit between the host interface and the MAC through which all transmitted and received data and status information is passed. Deep FIFOs allow a high degree of latency tolerance relative to the various transport and OS software stacks reducing and minimizing overrun conditions. Like the MAC, the FIFOs have separate receive and transmit data paths.

The LAN9215i can store up to 250 Ethernet packets utilizing FIFOs, totaling 16K bytes, with a packet granularity of 4 bytes. This memory is shared by the RX and TX blocks and is configurable in terms of allocation. This depth of buffer storage minimizes or eliminates receive overruns.

3.2 Flow Control

The LAN9215i Ethernet MAC supports full-duplex flow control using the pause operation and control frame. It also supports half-duplex flow control using back pressure.

3.2.1 FULL-DUPLEX FLOW CONTROL

The pause operation inhibits data transmission of data frames for a specified period of time. A Pause operation consists of a frame containing the globally assigned multicast address (01-80-C2-00-00-01), the PAUSE opcode, and a parameter indicating the quantum of slot time (512 bit times) to inhibit data transmissions. The PAUSE parameter may range from 0 to 65,535 slot times. The Ethernet MAC logic, on receiving a frame with the reserved multicast address and PAUSE opcode, inhibits data frame transmissions for the length of time indicated. If a Pause request is received while a transmission is in progress, then the pause will take effect after the transmission is complete. Control frames are received and processed by the MAC and are passed on.

The MAC also transmits control frames (pause command) via both hardware and software control. The software driver requests the MAC to transmit a control frame and gives the value of the PAUSE time to be used in the control frame. The MAC Function constructs a control frame with the appropriate values set in all the different fields (as defined in the 802.3x specification) and transmits the frame to the MII interface. The transmission of the control frame is not affected by the current state of the Pause timer value that is set because of a recently received control frame.

3.2.2 HALF-DUPLEX FLOW CONTROL (BACKPRESSURE)

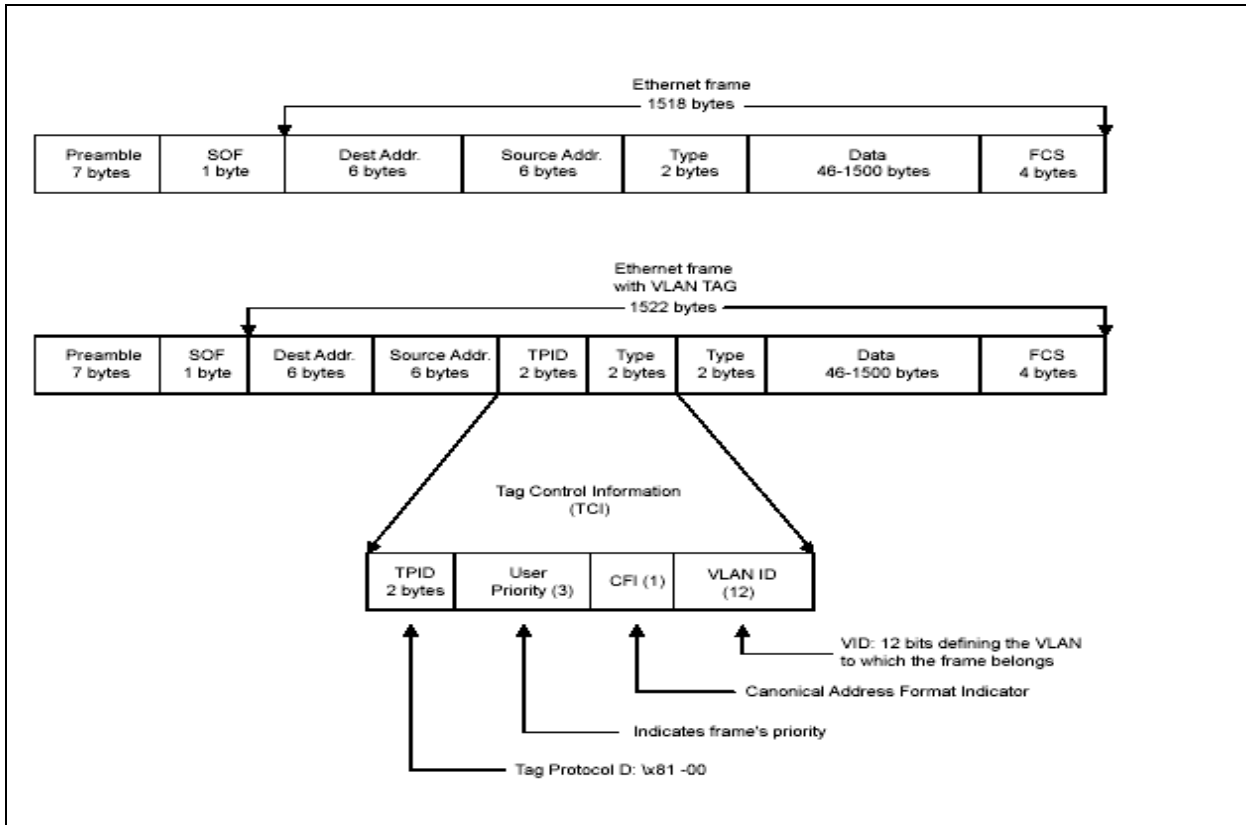
In half-duplex mode, back pressure is used for flow control. Whenever the receive buffer/FIFO becomes full or crosses a certain threshold level, the MAC starts sending a Jam signal. The MAC transmit logic enters a state at the end of current transmission (if any), where it waits for the beginning of a received frame. Once a new frame starts, the MAC starts sending the jam signal, which will result in a collision. After sensing the collision, the remote station will back off its transmission. The MAC continues sending the jam to make other stations defer transmission. The MAC only generates this collision-based back pressure when it receives a new frame, in order to avoid any late collisions.

3.2.3 VIRTUAL LOCAL AREA NETWORK (VLAN) SUPPORT

Virtual Local Area Networks or VLANs, as defined within the IEEE 802.3 standard, provide network administrators one means of grouping nodes within a larger network into broadcast domains. To implement a VLAN, four extra bytes are added to the basic Ethernet packet. As shown in Figure 3-1, "VLAN Frame", the four bytes are inserted after the Source Address Field and before the Type/Length field. The first two bytes of the VLAN tag identify the tag, and by convention are set to the value 0x8100. The last two bytes identify the specific VLAN associated with the packet; they also provide a priority field.

The LAN9215i supports VLAN-tagged packets. The LAN9215i provides two registers which are used to identify VLAN-tagged packets. One register should normally be set to the conventional VLAN ID of 0x8100. The other register provides a way of identifying VLAN frames tagged with a proprietary (not 0x8100) identifier. If a packet arrives bearing either of these tags in the two bytes succeeding the Source Address field, the controller will recognize the packet as a VLAN-tagged packet. In this case, the controller increases the maximum allowed packet size from 1518 to 1522 bytes (normally the controller filters packets larger than 1518 bytes). This allows the packet to be received, and then processed by host software, or to be transmitted on the network.

FIGURE 3-1: VLAN FRAME



3.3 Address Filtering Functional Description

The Ethernet address fields of an Ethernet Packet, consists of two 6-byte fields: one for the destination address and one for the source address. The first bit of the destination address signifies whether it is a physical address or a multicast address.

The LAN9215i address check logic filters the frame based on the Ethernet receive filter mode that has been enabled. Filter modes are specified based on the state of the control bits in [Table 3-1, "Address Filtering Modes"](#), which shows the various filtering modes used by the Ethernet MAC Function. These bits are defined in more detail in the "MAC Control Register". Please refer to [Section 5.4.1, "MAC_CR—MAC Control Register"](#) for more information on this register.

If the frame fails the filter, the Ethernet MAC function does not receive the packet. The host has the option of accepting or ignoring the packet.

TABLE 3-1: ADDRESS FILTERING MODES

MCPAS	PRMS	INVFILT	HO	HPFILT	Description
0	0	0	0	0	MAC address perfect filtering only for all addresses.
0	0	0	0	1	MAC address perfect filtering for physical address and hash filtering for multicast addresses
0	0	0	1	1	Hash Filtering for physical and multicast addresses
0	0	1	0	0	Inverse Filtering

TABLE 3-1: ADDRESS FILTERING MODES (CONTINUED)

MCPAS	PRMS	INVFILT	HO	HPFILT	Description
X	1	0	X	X	Promiscuous
1	0	0	0	X	Pass all multicast frames. Frames with physical addresses are perfect-filtered
1	0	0	1	1	Pass all multicast frames. Frames with physical addresses are hash-filtered

3.4 Filtering Modes

3.4.1 PERFECT FILTERING

This filtering mode passes only incoming frames whose destination address field exactly matches the value programmed into the MAC Address High register and the MAC address low register. The MAC address is formed by the concatenation of the above two registers in the MAC CSR Function.

3.4.2 HASH ONLY FILTERING

This type of filtering checks for incoming Receive packets with either multicast or physical destination addresses, and executes an imperfect address filtering against the hash table.

During imperfect hash filtering, the destination address in the incoming frame is passed through the CRC logic and the upper six bits of the CRC register are used to index the contents of the hash table. The hash table is formed by merging the register's multicast hash table high and multicast hash table low in the MAC CSR Function to form a 64-bit hash table. The most significant bit determines the register to be used (High/Low), while the other five bits determine the bit within the register. A value of 00000 selects Bit 0 of the multicast hash table low register and a value of 11111 selects Bit 31 of the multicast hash table high register.

3.4.2.1 Hash Perfect Filtering

In hash perfect filtering, if the received frame is a physical address, the LAN9215i Packet Filter block perfect-filters the incoming frame's destination field with the value programmed into the MAC Address High register and the MAC Address Low register. If the incoming frame is a multicast frame, however, the LAN9215i packet filter function performs an imperfect address filtering against the hash table.

The imperfect filtering against the hash table is the same imperfect filtering process described in the "Hash Only Filtering" section above.

3.4.2.2 Inverse Filtering

In inverse filtering, the Packet Filter Block accepts incoming frames with a destination address not matching the perfect address (i.e., the value programmed into the MAC Address High register and the MAC Address Low register in the CRC block and rejects frames with destination addresses matching the perfect address).

For all filtering modes, when the MCPAS bit is set, all multicast frames are accepted. When the PRMS bit is set, all frames are accepted regardless of their destination address. This includes all broadcast frames as well.

3.5 Wake-up Frame Detection

Setting the Wake-Up Frame Enable bit (WUEN) in the "WUCSR—Wake-up Control and Status Register", places the LAN9215i MAC in the wake-up frame detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for the pre-programmed wake-up frame patterns. The LAN9215i can be programmed to notify the host of the wake-up frame detection with the assertion of the host interrupt (IRQ) or assertion of the power management event signal (PME). Upon detection, the Wake-Up Frame Received bit (WUFR) in the WUCSR is set. When the host clears the WUEN bit the LAN9215i will resume normal receive operation.

Before putting the MAC into the wake-up frame detection state, the host must provide the detection logic with a list of sample frames and their corresponding byte masks. This information is written into the Wake-up Frame Filter register (WUFF). Please refer to [Section 5.4.11, "WUFF—Wake-up Frame Filter," on page 97](#) for additional information on this register.

LAN9215i

The MAC supports four programmable filters that support many different receive packet patterns. If remote wake-up mode is enabled, the remote wake-up function receives all frames addressed to the MAC. It then checks each frame against the enabled filter and recognizes the frame as a remote wake-up frame if it passes the wakeup frame filter register's address filtering and CRC value match.

In order to determine which bytes of the frames should be checked by the CRC module, the MAC uses a programmable byte mask and a programmable pattern offset for each of the four supported filters.

The pattern's offset defines the location of the first byte that should be checked in the frame. Since the destination address is checked by the address filtering Function, the pattern offset is always greater than 12.

The byte mask is a 31-bit field that specifies whether or not each of the 31 contiguous bytes within the frame, beginning in the pattern offset, should be checked. If bit *j* in the byte mask is set, the detection logic checks byte offset +*j* in the frame. In order to load the Wake-up Frame Filter register, the host LAN driver software must perform eight writes to the Wake-up Frame Filter register (WUFF). The Diagram shown in [Table 3-2, "Wake-Up Frame Filter Register Structure"](#) below, shows the wake-up frame filter register's structure.

- Note 3-1** Wake-up frame detection can be performed when the LAN9215i is in the D0 or D1 power states. In the D0 state, wake-up frame detection is enabled when the WUEN bit is set.
- Note 3-2** Wake-up frame detection, as well as Magic Packet detection, is always enabled and cannot be disabled when the device enters the D1 state.
- Note 3-3** When wake-up frame detection is enabled via the WUEN bit of the [WUCSR—Wake-up Control and Status Register](#), a broadcast wake-up frame will wake-up the device despite the state of the Disable Broadcast Frame (BCAST) bit in the [MAC_CR—MAC Control Register](#).

TABLE 3-2: WAKE-UP FRAME FILTER REGISTER STRUCTURE

Filter 0 Byte Mask							
Filter 1 Byte Mask							
Filter 2 Byte Mask							
Filter 3 Byte Mask							
Reserved	Filter 3 Command	Reserved	Filter 2 Command	Reserved	Filter 1 Command	Reserved	Filter 0 Command
Filter 3 Offset		Filter 2 Offset		Filter 1 Offset		Filter 0 Offset	
Filter 1 CRC-16				Filter 0 CRC-16			
Filter 3 CRC-16				Filter 2 CRC-16			

The Filter *i* Byte Mask defines which incoming frame bytes Filter *i* will examine to determine whether or not this is a wake-up frame. [Table 3-3](#), describes the byte mask's bit fields.

TABLE 3-3: FILTER I BYTE MASK BIT DEFINITIONS

Filter <i>i</i> Byte Mask Description	
Field	Description
31	Must be zero (0)
30:0	Byte Mask: If bit <i>j</i> of the byte mask is set, the CRC machine processes byte number pattern - (offset + <i>j</i>) of the incoming frame. Otherwise, byte pattern - (offset + <i>j</i>) is ignored.

The Filter *i* command register controls Filter *i* operation. [Table 3-4](#) shows the Filter *i* command register.

TABLE 3-4: FILTER I COMMAND BIT DEFINITIONS

Filter i Commands	
Field	Description
3	Address Type: Defines the destination address type of the pattern. When bit is set, the pattern applies only to multicast frames. When bit is cleared, the pattern applies only to unicast frames.
2:1	RESERVED
0	Enable Filter: When bit is set, Filter i is enabled, otherwise, Filter i is disabled.

The Filter i Offset register defines the offset in the frame's destination address field from which the frames are examined by Filter i. [Table 3-5](#) describes the Filter i Offset bit fields.

TABLE 3-5: FILTER I OFFSET BIT DEFINITIONS

Filter i Offset Description	
Field	Description
7:0	Pattern Offset: The offset of the first byte in the frame on which CRC is checked for wake-up frame recognition. The minimum value of this field must be 12 since there should be no CRC check for the destination address and the source address fields. The MAC checks the first offset byte of the frame for CRC and checks to determine whether the frame is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address.

The Filter i CRC-16 register contains the CRC-16 result of the frame that should pass Filter i.

[Table 3-6](#) describes the Filter i CRC-16 bit fields.

TABLE 3-6: FILTER I CRC-16 BIT DEFINITIONS

Filter i CRC-16 Description	
Field	Description
15:0	Pattern CRC-16: This field contains the 16-bit CRC value from the pattern and the byte mask programmed to the wake-up filter register Function. This value is compared against the CRC calculated on the incoming frame, and a match indicates the reception of a wakeup frame.

3.5.1 MAGIC PACKET DETECTION

Setting the Magic Packet Enable bit (MPEN) in the "WUCSR—Wake-up Control and Status Register", places the LAN9215i MAC in the "Magic Packet" detection mode. In this mode, normal data reception is disabled, and detection logic within the MAC examines receive data for a Magic Packet. The LAN9215i can be programmed to notify the host of the "Magic Packet" detection with the assertion of the host interrupt (IRQ) or assertion of the power management event signal (PME). Upon detection, the Magic Packet Received bit (MPR) in the WUCSR is set. When the host clears the MPEN bit the LAN9215i will resume normal receive operation. Please refer to [Section 5.4.12, "WUCSR—Wake-up Control and Status Register," on page 97](#) for additional information on this register.

LAN9215i

In Magic Packet mode, the Power Management Logic constantly monitors each frame addressed to the node for a specific Magic Packet pattern. It checks only packets with the MAC's address or a broadcast address to meet the Magic Packet requirement. The Power Management Logic checks each received frame for the pattern 48h FF_FF_FF_FF_FF_FF after the destination and source address field.

Then the Function looks in the frame for 16 repetitions of the MAC address without any breaks or interruptions. In case of a break in the 16 address repetitions, the PMT Function scans for the 48hFF_FF_FF_FF_FF_FF pattern again in the incoming frame.

The 16 repetitions may be anywhere in the frame but must be preceded by the synchronization stream. The device will also accept a multicast frame, as long as it detects the 16 duplications of the MAC address. If the MAC address of a node is 00h 11h 22h 33h 44h 55h, then the MAC scans for the following data sequence in an Ethernet: Frame.

```
Destination Address Source Address .....FF FF FF FF FF FF
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
...CRC
```

It should be noted that Magic Packet detection can be performed when LAN9215i is in the D0 or D1 power states. In the D0 state, "Magic Packet" detection is enabled when the MPEN bit is set. In the D1 state, Magic Packet detection, as well as wake-up frame detection, are automatically enabled when the device enters the D1 state.

3.6 Host Bus Operations

3.6.1 BUS WRITES

The host processor is required to perform two contiguous 16-bit writes to complete a single DWORD transfer. This DWORD must begin and end on a DWORD address boundary (A[2] and higher, cannot change during a sixteen bit write). No ordering requirements exist. The processor can access either the low or high word first, as long as the next write is performed to the other word. If a write to the same word is performed, the LAN9215i disregards the transfer.

3.6.2 BUS READS

The host processor is required to perform two consecutive 16-bit reads to complete a single DWORD transfer. This DWORD must begin and end on a DWORD address boundary (A[2] and higher, cannot change during a sixteen bit read). No ordering requirements exist. The processor can access either the low or high word first, as long as the next read is performed from the other word. If a read to the same word is performed, the data read is invalid and should be re-read. This is not a fatal error. The LAN9215i will reset its read counters and restart a new cycle on the next read.

3.6.3 BIG AND LITTLE ENDIAN SUPPORT

The LAN9215i supports "Big-" or "Little-Endian" processors with either 16 or 32-bit busses. To support big-endian processors, the hardware designer must explicitly invert the layout of the byte lanes.

3.6.4 WORD SWAP FUNCTION

Internally the LAN9215i is 32-bits wide. The LAN9215i supports a Word Swap Function. This feature is controlled by the Word Swap Register, which is described in [Section 5.3.17, "WORD_SWAP—Word Swap Control," on page 80](#). This register affects how words on the data bus are written to or read from the Control and Status Registers and the Transmit and Receive Data/Status FIFOs. Refer to [Table 3-7, "Word Swap Control"](#) below for more details. Whenever the LAN9215i transmits data from the Transmit Data FIFO to the network, the low order word is always transmitted first, and when the LAN9215i receives data from the network to the Receive Data FIFO, the low-order word is always received first.

TABLE 3-7: WORD SWAP CONTROL

Address A1 Pin	Byte Order		Description
	D[15:8]	D[7:0]	
Default Mode - Word Swap Register equal to 0x00000000 or any value other than 0xFFFFFFFF			
A1 = 0	Byte 1	Byte 0	When A1=0, the data bus is mapped to the low order words of CSRs and FIFOs. When A1=1, the data bus is mapped to the high-order words of CSRs and FIFOs. Since low-order words are always transmitted/received first, A1=0 data will always precede A1=1 data.
A1 = 1	Byte 3	Byte 2	
Word Swap Mode - Word Swap Register equal to 0xFFFFFFFF			
A1 = 0	Byte 3	Byte 2	When A1=0, the data bus is mapped to the high order words of CSRs and FIFOs. When A1=1, the data bus is mapped to the low order words of CSRs and FIFOs. In this case A1=1 data will always precede A1=0 data.
A1 = 1	Byte 1	Byte 0	

3.7 General Purpose Timer (GP Timer)

The General Purpose Timer is a programmable block that can be used to generate periodic host interrupts. The resolution of this timer is 100uS.

The GP Timer loads the GPT_CNT Register with the value in the GPT_LOAD field and begins counting down when the TIMER_EN bit is set to a '1.' On a reset, or when the TIMER_EN bit changes from set '1' to cleared '0,' the GPT_LOAD field is initialized to FFFFh. The GPT_CNT register is also initialized to FFFFh on a reset. Software can write the pre-load value into the GPT_LOAD field at any time; e.g., before or after the TIMER_EN bit is asserted. The GPT Enable bit TIMER_EN is located in the GPT_CFG register.

Once enabled, the GPT counts down either until it reaches 0000h or until a new pre-load value is written to the GPT_LOAD field. At 0000h, the counter wraps around to FFFFh, asserts the GPT interrupt status bit and the IRQ signal if the GPT_INT_EN bit is set, and continues counting. The GPT interrupt status bit is in the INT_STS Register. The GPT_INT hardware interrupt can only be set if the GPT_INT_EN bit is set. GPT_INT is a sticky bit (R/WC); i.e., once the GPT_INT bit is set, it can only be cleared by writing a '1' to the bit.

3.8 EEPROM Interface

The LAN9215i can optionally load its MAC address from an external serial EEPROM. If a properly configured EEPROM is detected by the LAN9215i at power-up, hard reset or soft reset, the ADDRH and ADDR_L registers will be loaded with the contents of the EEPROM. If a properly configured EEPROM is not detected, it is the responsibility of the host LAN Driver to set the IEEE addresses.

The LAN9215i EEPROM controller also allows the host system to read, write and erase the contents of the Serial EEPROM. The EEPROM controller supports most "93C46" type EEPROMs configured for 128 x 8-bit operation.

3.8.1 MAC ADDRESS AUTO-LOAD

On power-up, hard reset or soft reset, the EEPROM controller attempts to read the first byte of data from the EEPROM (address 00h). If the value A5h is read from the first address, then the EEPROM controller will assume that an external Serial EEPROM is present. The EEPROM controller will then access the next EEPROM byte and send it to the MAC Address register byte 0 (ADDR_L[7:0]). This process will be repeated for the next five bytes of the MAC Address, thus fully programming the 48-bit MAC address. Once all six bytes have been programmed, the "MAC Address Loaded" bit is set in the E2P_CMD register. A detailed explanation of the EEPROM byte ordering with respect to the MAC address is given in [Section 5.4.3, "ADDR_L—MAC Address Low Register," on page 92.](#)