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# LAN9250

## 10/100 Industrial Ethernet Controller & PHY

### Highlights

- 16-bit 10/100 industrial Ethernet controller & PHY
- Interfaces to most 8/16-bit embedded controllers and 32-bit embedded controllers with an 8/16-bit bus
- Integrated Ethernet PHY with HP Auto-MDIX
- Integrated Ethernet MAC
- Compliant with Energy Efficient Ethernet 802.3az
- Wake on LAN (WoL) support
- Integrated IEEE 1588v2 hardware time stamp unit
- Cable diagnostic support
- 1.8V to 3.3V variable voltage I/O
- Integrated 1.2V regulator for single 3.3V operation
- Low pin count and small body size package

### Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions & video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

### Key Benefits

- Single-chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - 100BASE-FX support for external fiber transceiver
  - Automatic polarity detection and correction (HP Auto-MDIX)
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Eliminates dropped packets
  - Internal buffer memory can store over 200 packets
  - Automatic PAUSE and back-pressure flow control
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- 8/16-Bit Host Bus Interface
  - Indexed register or multiplexed bus
  - 16Kbyte FIFO with flexible TX/RX allocation
  - SPI / Quad SPI support
- IEEE 1588v2 hardware time stamp unit
  - Global 64-bit tunable clock
  - Ordinary clock: master / slave, one-step / two-step, end-to-end / peer-to-peer delay
  - Fully programmable timestamp on TX or RX, timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive power management features
  - 3 power-down levels
  - Wake on link status change (energy detect)
  - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
  - Wakeup indicator event signal
  - Link status change
- Power and I/O
  - Integrated power-on reset circuit
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
  - Single 3.3V power supply (integrated 1.2V regulator)
- Additional Features
  - Multifunction GPIOs
  - General purpose timer
  - Optional EEPROM interface
  - Ability to use low cost 25MHz crystal for reduced BOM
- Packaging
  - Pb-free RoHS compliant 64-pin QFN or 64-pin TQFP-EP
- Available in commercial, industrial, and extended industrial* temp. ranges

*Extended temp. (105ºC) is supported only in the 64-QFN with an external voltage regulator (internal regulator must be disabled) and 2.5V (typ) Ethernet magnetics.

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# 1.0 PREFACE

## 1.1 General Terms

**TABLE 1-1: GENERAL TERMS**

| Term | Description |
|---|---|
| **10BASE-T** | 10 Mbps Ethernet, IEEE 802.3 compliant |
| **100BASE-TX** | 100 Mbps Fast Ethernet, IEEE802.3u compliant |
| **ADC** | Analog-to-Digital Converter |
| **ALR** | Address Logic Resolution |
| **AN** | Auto-Negotiation |
| **BLW** | Baseline Wander |
| **BM** | Buffer Manager - Part of the switch fabric |
| **BPDU** | Bridge Protocol Data Unit - Messages which carry the Spanning Tree Protocol information |
| **Byte** | 8 bits |
| **CSMA/CD** | Carrier Sense Multiple Access/Collision Detect |
| **CSR** | Control and Status Registers |
| **CTR** | Counter |
| **DA** | Destination Address |
| **DWORD** | 32 bits |
| **EPC** | EEPROM Controller |
| **FCS** | Frame Check Sequence - The extra checksum characters added to the end of an Ethernet frame, used for error detection and correction. |
| **FIFO** | First In First Out buffer |
| **FSM** | Finite State Machine |
| **GPIO** | General Purpose I/O |
| **Host** | External system (Includes processor, application software, etc.) |
| **IGMP** | Internet Group Management Protocol |
| **Inbound** | Refers to data input to the device from the host |
| **Level-Triggered Sticky Bit** | This type of status bit is set whenever the condition that it represents is asserted. The bit remains set until the condition is no longer true and the status bit is cleared by writing a zero. |
| **lsb** | Least Significant Bit |
| **LSB** | Least Significant Byte |
| **LVDS** | Low Voltage Differential Signaling |
| **MDI** | Medium Dependent Interface |
| **MDIX** | Media Independent Interface with Crossover |
| **MII** | Media Independent Interface |
| **MIIM** | Media Independent Interface Management |
| **MIL** | MAC Interface Layer |
| **MLD** | Multicast Listening Discovery |
| **MLT-3** | Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”. |
| **msb** | Most Significant Bit |
| **MSB** | Most Significant Byte |

**TABLE 1-1: GENERAL TERMS (CONTINUED)**

| Term | Description |
|---|---|
| **NRZI** | Non Return to Zero Inverted. This encoding method inverts the signal for a “1” and leaves the signal unchanged for a “0” |
| **N/A** | Not Applicable |
| **NC** | No Connect |
| **OUI** | Organizationally Unique Identifier |
| **Outbound** | Refers to data output from the device to the host |
| **PISO** | Parallel In Serial Out |
| **PLL** | Phase Locked Loop |
| **PTP** | Precision Time Protocol |
| **RESERVED** | Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses. |
| **RTC** | Real-Time Clock |
| **SA** | Source Address |
| **SFD** | Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame. |
| **SIPO** | Serial In Parallel Out |
| **SMI** | Serial Management Interface |
| **SQE** | Signal Quality Error (also known as “heartbeat”) |
| **SSD** | Start of Stream Delimiter |
| **UDP** | User Datagram Protocol - A connectionless protocol run on top of IP networks |
| **UUID** | Universally Unique IDentifier |
| **WORD** | 16 bits |

## 1.2 Buffer Types

**TABLE 1-2: BUFFER TYPES**

| Buffer Type | Description |
|---|---|
| IS | Schmitt-triggered input |
| VIS | Variable voltage Schmitt-triggered input |
| VO8 | Variable voltage output with 8 mA sink and 8 mA source |
| VOD8 | Variable voltage open-drain output with 8 mA sink |
| VO12 | Variable voltage output with 12 mA sink and 12 mA source |
| VOD12 | Variable voltage open-drain output with 12 mA sink |
| VOS12 | Variable voltage open-source output with 12 mA source |
| VO16 | Variable voltage output with 16 mA sink and 16 mA source |
| PU | 50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled.<br>Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added. |
| PD | 50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled.<br>Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added. |
| AI | Analog input |
| AIO | Analog bidirectional |
| ICLK | Crystal oscillator input pin |
| OCLK | Crystal oscillator output pin |
| ILVPECL | Low voltage PECL input pin |
| OLVPECL | Low voltage PECL output pin |
| P | Power pin |

## 1.3 Register Nomenclature

**TABLE 1-3: REGISTER NOMENCLATURE**

| Register Bit Type Notation | Register Bit Description |
|---|---|
| R | **Read:** A register or bit with this attribute can be read. |
| W | **Read:** A register or bit with this attribute can be written. |
| RO | **Read only:** Read only. Writes have no effect. |
| WO | **Write only:** If a register or bit is write-only, reads will return unspecified data. |
| WC | **Write One to Clear:** Writing a one clears the value. Writing a zero has no effect |
| WAC | **Write Anything to Clear:** Writing anything clears the value. |
| RC | **Read to Clear:** Contents is cleared after the read. Writes have no effect. |
| LL | **Latch Low:** Clear on read of register. |
| LH | **Latch High:** Clear on read of register. |
| SC | **Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read. |
| SS | **Self-Setting:** Contents are self-setting after being cleared. Writes of one have no effect. Contents can be read. |
| RO/LH | **Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will either remain high if the high condition remains, or will go low if the high condition has been removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition. This mode is used in some Ethernet PHY registers. |
| NASR | **Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset. |
| RESERVED | **Reserved Field:** Reserved fields must be written with zeros to ensure future compatibility. The value of reserved bits is not guaranteed on a read. |

## 2.0 GENERAL DESCRIPTION

The LAN9250 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9250 has been specifically designed to provide high performance and throughput for 16-bit applications. The LAN9250 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and the IEEE 1588v2 precision time protocol. 100BASE-FX is supported via an external fiber transceiver.

The LAN9250 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The integrated checksum offload engines enable the automatic generation of the 16-bit checksum for received and transmitted Ethernet frames, offloading the task from the CPU. The LAN9250 also includes large transmit and receive data FIFOs to accommodate high latency applications. In addition, the LAN9250 memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

The LAN9250 also supports features which reduce or eliminate packet loss. The internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9250 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

Two user selectable host bus interface options are available:

- ***Indexed register access***
  This implementation provides three index/data register banks, each with independent Byte/WORD to DWORD conversion. Internal registers are accessed by first writing one of the three index registers, followed by reading or writing the corresponding data register. Three index/data register banks support up to 3 independent driver threads without access conflicts. Each thread can write its assigned index register without the issue of another thread overwriting it. Two 16-bit cycles or four 8-bit cycles are required within the same 32-bit index/data register - however, these access can be interleaved. Direct (non-indexed) read and write accesses are supported to the packet data FIFOs. The direct FIFO access provides independent Byte/WORD to DWORD conversion, supporting interleaved accesses with the index/data registers. Direct FIFO access also supports burst reading of the data FIFO.
- ***Multiplexed address/data bus***
  This implementation provides a multiplexed address and data bus with both single phase and dual phase address support. The address is loaded with an address strobe followed by data access using a read or write strobe. Two back to back 16-bit data cycles or 4 back to back 8-bit data cycles are required within the same 32-bit DWORD. These accesses must be sequential without any interleaved accesses to other registers. Burst read and write accesses are supported to the packet data and status FIFOs by performing one address cycle followed by multiple read or write data cycles.

The HBI supports 8/16-bit operation with big, little, and mixed endian operations. Four separate FIFO mechanisms (TX/RX Data FIFO's, TX/RX Status FIFO's) interface the HBI to the Host MAC and facilitate the transferring of packet data and status information between the host CPU and the device. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

An SPI / Quad SPI slave controller provides a low pin count synchronous slave interface that facilitates communication between the device and a host system. The SPI / Quad SPI slave allows access to the System CSRs, internal FIFOs and memories. It supports single and multiple register read and write commands with incrementing, decrementing and static addressing. Single, Dual and Quad bit lanes are supported with a clock rate of up to 80 MHz.

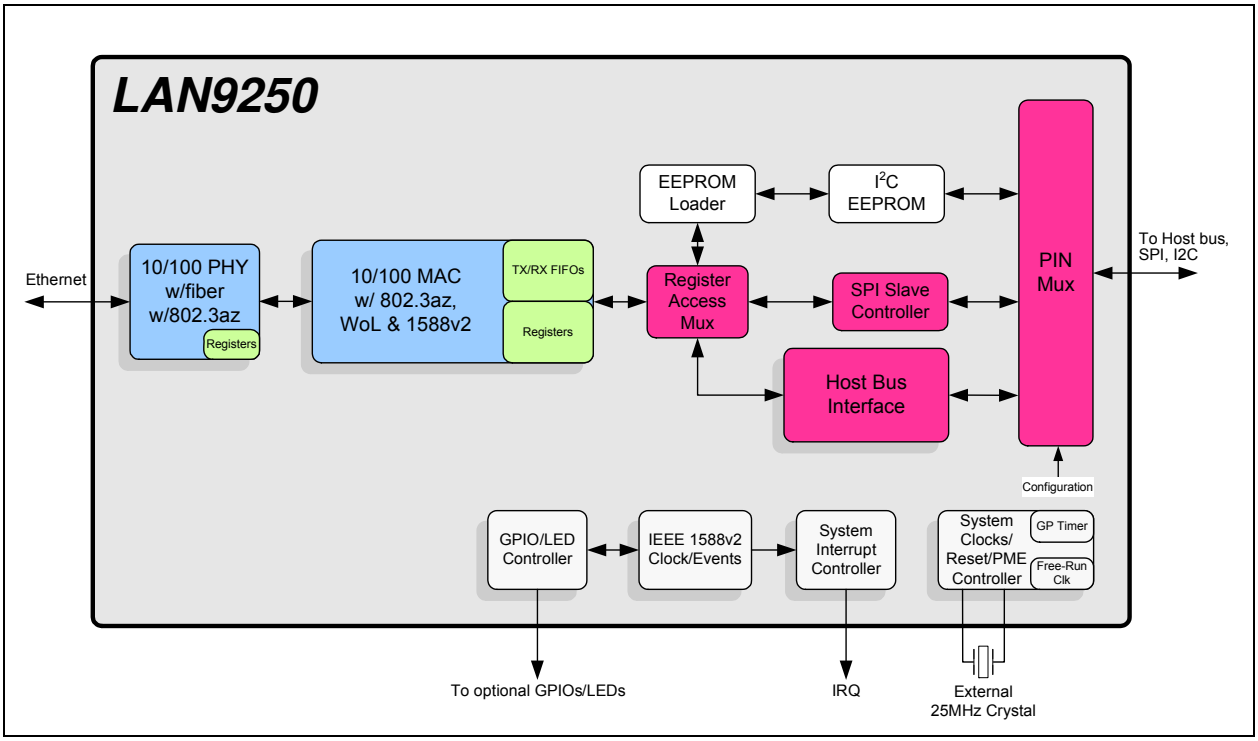
The LAN9250 contains an $I^2C$ master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset.

The LAN9250 supports numerous power management and wakeup features. The LAN9250 can be placed in a reduced power mode and can be programmed to issue an external wake signal (PME) via several methods, including "Magic Packet", "Wake on LAN", wake on broadcast, wake on perfect DA, and "Link Status Change". This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events.

The LAN9250 can be configured to operate via a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN9250 is available in commercial, industrial, and extended industrial temperature ranges. Figure 2-1 provides an internal block diagram of the LAN9250.

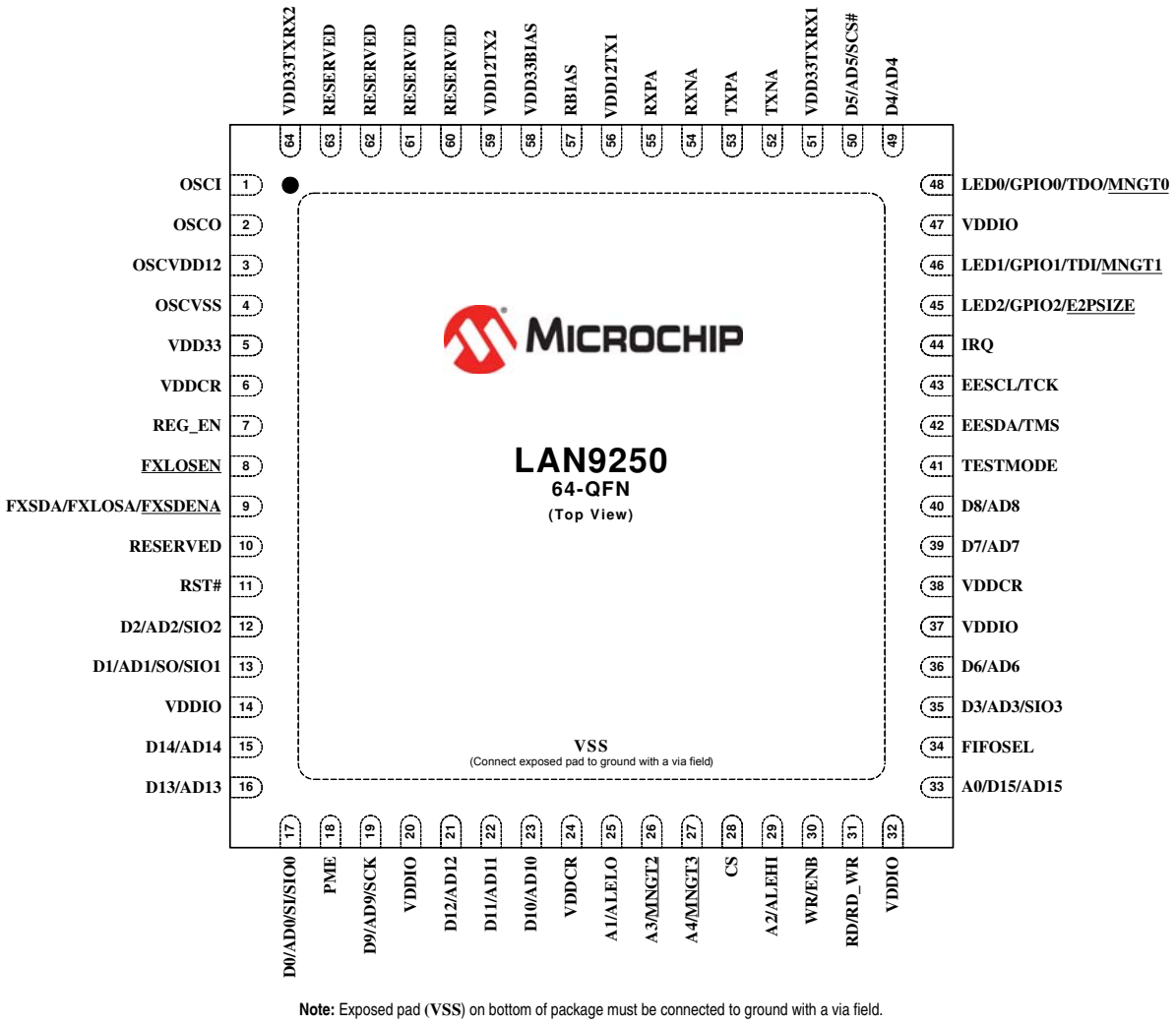
**FIGURE 2-1: INTERNAL BLOCK DIAGRAM**



## 3.0 PIN DESCRIPTIONS AND CONFIGURATION

### 3.1 64-QFN Pin Assignments

**FIGURE 3-1: 64-QFN PIN ASSIGNMENTS (TOP VIEW)**




**Note:** Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

**Note:** When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-1 details the 64-QFN package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

**TABLE 3-1: 64-QFN PACKAGE PIN ASSIGNMENTS**

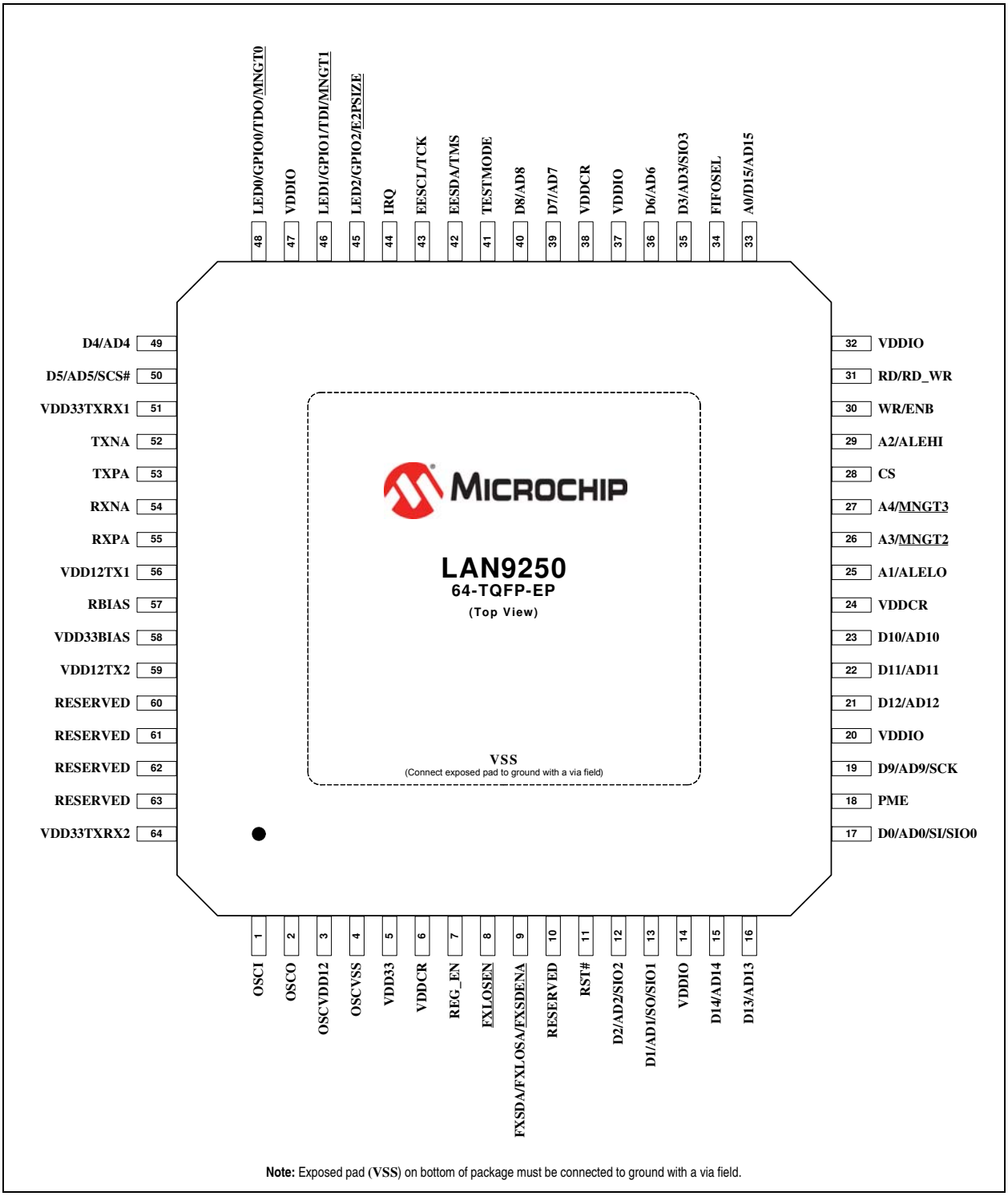
| Pin Number | HBI Indexed Mode Pin Name | HBI Multiplexed Mode Pin Name | SPI Mode Pin Name |
|---|---|---|---|
| 1 | OSCI | | |
| 2 | OSCO | | |
| 3 | OSCVDD12 | | |
| 4 | OSCVSS | | |
| 5 | VDD33 | | |
| 6 | VDDCR | | |
| 7 | REG_EN | | |
| 8 | FXLOSEN | | |
| 9 | FXSDA/FXLOSA/FXSDENA | | |
| 10 | RESERVED | | |
| 11 | RST# | | |
| 12 | D2 | AD2 | SIO2 |
| 13 | D1 | AD1 | SO/SIO1 |
| 14 | VDDIO | | |
| 15 | D14 | AD14 | - |
| 16 | D13 | AD13 | - |
| 17 | D0 | AD0 | SI/SIO0 |
| 18 | PME | | |
| 19 | D9 | AD9 | SCK |
| 20 | VDDIO | | |
| 21 | D12 | AD12 | - |
| 22 | D11 | AD11 | - |
| 23 | D10 | AD10 | - |
| 24 | VDDCR | | |
| 25 | A1 | ALELO | - |
| 26 | A3 | MNGT2 | - |
| 27 | A4 | MNGT3 | - |
| 28 | CS | | - |
| 29 | A2 | ALEHI | - |
| 30 | WR/ENB | | - |
| 31 | RD/RD_WR | | - |
| 32 | VDDIO | | |

**TABLE 3-1: 64-QFN PACKAGE PIN ASSIGNMENTS (CONTINUED)**

| Pin Number | HBI Indexed Mode Pin Name | HBI Multiplexed Mode Pin Name | SPI Mode Pin Name |
|---|---|---|---|
| 33 | A0/D15 | AD15 | - |
| 34 | FIFOSEL | - | |
| 35 | D3 | AD3 | SIO3 |
| 36 | D6 | AD6 | - |
| 37 | VDDIO | | |
| 38 | VDDCR | | |
| 39 | D7 | AD7 | - |
| 40 | D8 | AD8 | - |
| 41 | TESTMODE | | |
| 42 | EESDA/TMS | | |
| 43 | EESCL/TCK | | |
| 44 | IRQ | | |
| 45 | LED2/GPIO2/E2PSIZE | | |
| 46 | LED1/GPIO1/TDI/MNGT1 | | |
| 47 | VDDIO | | |
| 48 | LED0/GPIO0/TDO/MNGT0 | | |
| 49 | D4 | AD4 | - |
| 50 | D5 | AD5 | SCS# |
| 51 | VDD33TXRX1 | | |
| 52 | TXNA | | |
| 53 | TXPA | | |
| 54 | RXNA | | |
| 55 | RXPA | | |
| 56 | VDD12TX1 | | |
| 57 | RBIAS | | |
| 58 | VDD33BIAS | | |
| 59 | VDD12TX2 | | |
| 60 | RESERVED | | |
| 61 | RESERVED | | |
| 62 | RESERVED | | |
| 63 | RESERVED | | |
| 64 | VDD33TXRX2 | | |
| Exposed Pad | VSS | | |

## 3.2 64-TQFP-EP Pin Assignments

**FIGURE 3-2: 64-TQFP-EP PIN ASSIGNMENTS (TOP VIEW)**




**Note:** Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

**Note:** When a "#" is used at the end of the signal name, it indicates that the signal is active low. For example, **RST#** indicates that the reset signal is active low.

The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables in Section 3.3, "Pin Descriptions". A description of the buffer types is provided in Section 1.2, "Buffer Types".

Table 3-2 details the 64-TQFP-EP package pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-".

**TABLE 3-2: 64-TQFP-EP PACKAGE PIN ASSIGNMENTS**

| Pin Number | HBI Indexed Mode Pin Name | HBI Multiplexed Mode Pin Name | SPI Mode Pin Name |
|---|---|---|---|
| 1 | OSCI | | |
| 2 | OSCO | | |
| 3 | OSCVDD12 | | |
| 4 | OSCVSS | | |
| 5 | VDD33 | | |
| 6 | VDDCR | | |
| 7 | REG_EN | | |
| 8 | FXLOSEN | | |
| 9 | FXSDA/FXLOSA/FXSDENA | | |
| 10 | RESERVED | | |
| 11 | RST# | | |
| 12 | D2 | AD2 | SIO2 |
| 13 | D1 | AD1 | SO/SIO1 |
| 14 | VDDIO | | |
| 15 | D14 | AD14 | - |
| 16 | D13 | AD13 | - |
| 17 | D0 | AD0 | SI/SIO0 |
| 18 | PME | | |
| 19 | D9 | AD9 | SCK |
| 20 | VDDIO | | |
| 21 | D12 | AD12 | - |
| 22 | D11 | AD11 | - |
| 23 | D10 | AD10 | - |
| 24 | VDDCR | | |
| 25 | A1 | ALELO | - |
| 26 | A3 | MNGT2 | - |
| 27 | A4 | MNGT3 | - |
| 28 | CS | | - |

**TABLE 3-2: 64-TQFP-EP PACKAGE PIN ASSIGNMENTS (CONTINUED)**

| Pin Number | HBI Indexed Mode Pin Name | HBI Multiplexed Mode Pin Name | SPI Mode Pin Name |
|---|---|---|---|
| 29 | A2 | ALEHI | - |
| 30 | WR/ENB | | - |
| 31 | RD/RD_WR | | - |
| 32 | VDDIO | | |
| 33 | A0/D15 | AD15 | - |
| 34 | FIFOSEL | - | |
| 35 | D3 | AD3 | SIO3 |
| 36 | D6 | AD6 | - |
| 37 | VDDIO | | |
| 38 | VDDCR | | |
| 39 | D7 | AD7 | - |
| 40 | D8 | AD8 | - |
| 41 | TESTMODE | | |
| 42 | EESDA/TMS | | |
| 43 | EESCL/TCK | | |
| 44 | IRQ | | |
| 45 | LED2/GPIO2/E2PSIZE | | |
| 46 | LED1/GPIO1/TDI/MNGT1 | | |
| 47 | VDDIO | | |
| 48 | LED0/GPIO0/TDO/MNGT0 | | |
| 49 | D4 | AD4 | - |
| 50 | D5 | AD5 | SCS# |
| 51 | VDD33TXRX1 | | |
| 52 | TXNA | | |
| 53 | TXPA | | |
| 54 | RXNA | | |
| 55 | RXPA | | |
| 56 | VDD12TX1 | | |
| 57 | RBIAS | | |
| 58 | VDD33BIAS | | |
| 59 | VDD12TX2 | | |
| 60 | RESERVED | | |
| 61 | RESERVED | | |
| 62 | RESERVED | | |
| 63 | RESERVED | | |

**TABLE 3-2: 64-TQFP-EP PACKAGE PIN ASSIGNMENTS (CONTINUED)**

| Pin Number | HBI Indexed Mode Pin Name | HBI Multiplexed Mode Pin Name | SPI Mode Pin Name |
|---|---|---|---|
| 64 | VDD33TXRX2 | | |
| Exposed Pad | VSS | | |

## 3.3 Pin Descriptions

This section contains descriptions of the various LAN9250 pins. The pin descriptions have been broken into functional groups as follows:

- LAN Pin Descriptions
- Host Bus Pin Descriptions
- SPI/SQI Pin Descriptions
- EEPROM Pin Descriptions
- GPIO, LED & Configuration Strap Pin Descriptions
- Miscellaneous Pin Descriptions
- JTAG Pin Descriptions
- Core and I/O Power Pin Descriptions

**TABLE 3-3: LAN PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | TP TX/RX Positive Channel 1 | **TXPA** | AIO | Twisted Pair Transmit/Receive Positive Channel 1. See Note 1 |
| | FX TX Positive | | OLVPECL | Fiber Transmit Positive. |
| 1 | TP TX/RX Negative Channel 1 | **TXNA** | AIO | Twisted Pair Transmit/Receive Negative Channel 1. See Note 1. |
| | FX TX Negative | | OLVPECL | Fiber Transmit Negative. |
| 1 | TP TX/RX Positive Channel 2 | **RXPA** | AIO | Twisted Pair Transmit/Receive Positive Channel 2. See Note 1. |
| | FX RX Positive | | AI | Fiber Receive Positive. |
| 1 | TP TX/RX Negative Channel 2 | **RXNA** | AIO | Twisted Pair Transmit/Receive Negative Channel 2. See Note 1. |
| | FX RX Negative | | AI | Fiber Receive Negative. |

**TABLE 3-3: LAN PIN DESCRIPTIONS (CONTINUED)**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | FX Signal Detect (SD) | **FXSDA** | ILVPECL | Fiber Signal Detect. When FX-LOS mode is not selected, this pin functions as the Signal Detect input from the external transceiver. A level above 2 V (typ.) indicates valid signal.<br><br>When FX-LOS mode is selected, the input buffer is disabled. |
| | FX Loss Of Signal (LOS) | **FXLOSA** | IS (PU) | Fiber Loss of Signal. When FX-LOS mode is selected (via fx_los_strap_1), this pin functions as the Loss of Signal input from the external transceiver. A high indicates LOS while a low indicates valid signal.<br><br>When FX-LOS mode is not selected, the input buffer and pull-up are disabled. |
| | FX-SD Enable Strap | **FXSDENA** | AI | FX-SD Enable. When FX-LOS mode is not selected, this strap input selects between FX-SD and copper twisted pair mode. A level above 1 V (typ.) selects FX-SD.<br><br>When FX-LOS mode is selected, the input buffer is disabled.<br><br>See Note 2. |
| 1 | Bias Reference | **RBIAS** | AI | Used for internal bias circuits. Connect to an external 12.1 kΩ, 1% resistor to ground.<br><br>Refer to the device reference schematic for connection information.<br><br>**Note:** The nominal voltage is 1.2 V and the resistor will dissipate approximately 1 mW of power. |
| 1 | FX-LOS Enable Strap | **FXLOSEN** | AI | FX-LOS Enable. This strap input selects between FX-LOS and FX-SD / copper twisted pair mode.<br><br>A level below 1 V (typ.) selects FX-SD / copper twisted pair for the port, further determined by FXSDENA.<br><br>A level of 1.5 V (typ.) or above selects FX-LOS for the port.<br><br>See Note 2. |
| 1 | +3.3 V Analog Power Supply | **VDD33TXRX1** | P | See Note 3. |
| 1 | +3.3 V Analog Power Supply | **VDD33TXRX2** | P | See Note 3. |
| 1 | +3.3 V Master Bias Power Supply | **VDD33BIAS** | P | See Note 3. |

**TABLE 3-3: LAN PIN DESCRIPTIONS (CONTINUED)**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | Transmitter +1.2 V Power Supply | **VDD12TX1** | P | This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX2** pin for proper operation.<br><br>See Note 3. |
| 1 | Transmitter +1.2 V Power Supply | **VDD12TX2** | P | This pin is supplied from either an external 1.2 V supply or from the device's internal regulator via the PCB. This pin must be tied to the **VDD12TX1** pin for proper operation.<br><br>See Note 3. |

**Note 1:** In copper mode, either channel 1 or 2 may function as the transmit pair while the other channel functions as the receive pair. The pin name symbols for the twisted pair pins apply to a normal connection. If HP Auto-MDIX is enabled and a reverse connection is detected or manually selected, the RX and TX pins will be swapped internally.

**Note 2:** Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

**Note 3:** Refer to Section 4.0, "Power Connections," on page 26, the device reference schematics, and the device LANCheck schematic checklist for additional connection information.

**TABLE 3-4: HOST BUS PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | Read | **RD** | VIS | This pin is the host bus read strobe.<br><br>Normally active low, the polarity can be changed via the HBI_rd_rdwr_polarity_strap. |
| | Read or Write | **RD_WR** | VIS | This pin is the host bus direction control. Used in conjunction with the ENB pin, it indicates a read or write operation.<br><br>The normal polarity is read when 1, write when 0 (R/nW) but can be changed via the HBI_rd_rdwr_polarity_strap. |
| 1 | Write | **WR** | VIS | This pin is the host bus write strobe.<br><br>Normally active low, the polarity can be changed via the HBI_wr_en_polarity_strap. |
| | Enable | **ENB** | VIS | This pin is the host bus data enable strobe. Used in conjunction with the RD_WR pin it indicates the data phase of the operation.<br><br>Normally active low, the polarity can be changed via the HBI_wr_en_polarity_strap. |

**TABLE 3-4: HOST BUS PIN DESCRIPTIONS (CONTINUED)**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | Chip Select | **CS** | VIS | This pin is the host bus chip select and indicates that the device is selected for the current transfer.<br><br>Normally active low, the polarity can be changed via the HBI_cs_polarity_strap. |
| 1 | FIFO Select | **FIFOSEL** | VIS | This input directly selects the Host MAC TX and RX Data FIFOs for non-multiplexed address mode. |
| 5 | Address | **A[4:0]** | VIS | These pins provide the address for non-multiplexed address mode.<br><br>In 16-bit data mode, bit 0 is not used. |
| 16 | Data | **D[15:0]** | VIS/VO8 | These pins are the host bus data bus for non-multiplexed address mode.<br><br>In 8-bit data mode, bits 15-8 are not used and their input and output drivers are disabled. |
| | Address & Data | **AD[15:0]** | VIS/VO8 | These pins are the host bus address / data bus for multiplexed address mode.<br><br>Bits 15-8 provide the upper byte of address for single phase multiplexed address mode.<br><br>Bits 7-0 provide the lower byte of address for single phase multiplexed address mode and both bytes of address for dual phase multiplexed address mode.<br><br>In 8-bit data dual phase multiplexed address mode, bits 15-8 are not used and their input and output drivers are disabled. |
| 1 | Address Latch Enable High | **ALEHI** | VIS | This pin indicates the address phase for multiplexed address modes. It is used to load the higher address byte in dual phase multiplexed address mode.<br><br>Normally active low (address saved on rising edge), the polarity can be changed via the HBI_ale_polarity_strap. |
| 1 | Address Latch Enable Low | **ALELO** | VIS | This pin indicates the address phase for multiplexed address modes. It is used to load both address bytes in single phase multiplexed address mode and the lower address byte in dual phase multiplexed address mode.<br><br>Normally active low (address saved on rising edge), the polarity can be changed via the HBI_ale_polarity_strap. |

**TABLE 3-5: SPI/SQI PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | SPI/SQI Slave Chip Select | **SCS#** | VIS (PU) | This pin is the SPI/SQI slave chip select input. When low, the SPI/SQI slave is selected for SPI/SQI transfers. When high, the SPI/SQI serial data output(s) is(are) 3-stated. |
| 1 | SPI/SQI Slave Serial Clock | **SCK** | VIS (PU) | This pin is the SPI/SQI slave serial clock input. |
| 4 | SPI/SQI Slave Serial Data Input/Output | **SIO[3:0]** | VIS/VO8 (PU) | These pins are the SPI/SQI slave data input and output for multiple bit I/O. |
| | SPI Slave Serial Data Input | **SI** | VIS (PU) | This pin is the SPI slave serial data input. **SI** is shared with the **SIO0** pin. |
| | SPI Slave Serial Data Output | **SO** | VO8 (PU) Note 4 | This pin is the SPI slave serial data output. **SO** is shared with the **SIO1** pin. |

**Note 4:** Although this pin is an output for SPI instructions, it includes a pull-up since it is also SIO bit 1.

**TABLE 3-6: EEPROM PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | EEPROM $I^2C$ Serial Data Input/Output | **EESDA** | VIS/VOD8 | When the device is accessing an external EEPROM this pin is the $I^2C$ serial data input/open-drain output.<br>**Note:** This pin must be pulled-up by an external resistor at all times. |
| 1 | EEPROM $I^2C$ Serial Clock | **EESCL** | VIS/VOD8 | When the device is accessing an external EEPROM this pin is the $I^2C$ clock input/open-drain output.<br>**Note:** This pin must be pulled-up by an external resistor at all times. |

**TABLE 3-7: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | LED 2 | **LED2** | VO12/ VOD12/ VOS12 | This pin is configured to operate as an LED when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **E2PSIZE** strap value sampled at reset.<br>**Note:** Refer to Section 16.3, "LED Operation," on page 385 to additional information. |
| | General Purpose I/O 2 | **GPIO2** | VIS/VO12/ VOD12 (PU) | This pin is configured to operate as a GPIO when the LED 2 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). |
| | EEPROM Size Configuration Strap | **E2PSIZE** | VIS (PU) | This strap configures the value of the EEPROM size hard-strap. See Note 5.<br>A low selects 1K bits (128 x 8) through 16K bits (2K x 8).<br>A high selects 32K bits (4K x 8) through 512K bits (64K x 8). |
| 1 | LED 1 | **LED1** | VO12/ VOD12/ VOS12 | This pin is configured to operate as an LED when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **MNGT1** strap value sampled at reset.<br>**Note:** Refer to Section 16.3, "LED Operation," on page 385 to additional information. |
| | General Purpose I/O 1 | **GPIO1** | VIS/VO12/ VOD12 (PU) | This pin is configured to operate as a GPIO when the LED 1 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). |
| | Host Interface Configuration Strap 1 | **MNGT1** | VIS (PU) | This strap, along with **MNGT0**, **MNGT2**, and **MNGT3** configures the host interface mode. See Note 5.<br>See Table 7-3, "HBI Strap Mapping," on page 61 for the host interface strap settings. |

**TABLE 3-7: GPIO, LED & CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | LED 0 | **LED0** | VO12/ VOD12/ VOS12 | This pin is configured to operate as an LED when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is set. The buffer type depends on the setting of the LED Function 2-0 (LED_FUN[2:0]) field in the LED Configuration Register (LED_CFG) and is configured to be either a push-pull or open-drain/open-source output. When selected as an open-drain/open-source output, the polarity of this pin depends upon the **MNGT0** strap value sampled at reset.<br>**Note:** Refer to Section 16.3, "LED Operation," on page 385 to additional information. |
| | General Purpose I/O 0 | **GPIO0** | VIS/VO12/ VOD12 (PU) | This pin is configured to operate as a GPIO when the LED 0 Enable bit of the LED Configuration Register (LED_CFG) is clear. The pin is fully programmable as either a push-pull output, an open-drain output or a Schmitt-triggered input by writing the General Purpose I/O Configuration Register (GPIO_CFG) and the General Purpose I/O Data & Direction Register (GPIO_DATA_DIR). |
| | Host Interface Configuration Strap 0 | **MNGT0** | VIS (PU) | This strap, along with **MNGT1**, **MNGT2**, and **MNGT3** configures the host mode. See Note 5.<br>See Table 7-3, “HBI Strap Mapping,” on page 61 for the host interface strap settings. |
| 1 | Host Interface Configuration Strap 3 | **MNGT3** | VIS (PU) | This strap, along with **MNGT0**, **MNGT1**, and **MNGT2** configures the host mode. See Note 5.<br>See Table 7-3, “HBI Strap Mapping,” on page 61 for the host interface strap settings. |
| 1 | Host Interface Configuration Strap 2 | **MNGT2** | VIS (PU) | This strap, along with **MNGT0**, **MNGT1**, and **MNGT3** configures the host mode. See Note 5.<br>See Table 7-3, “HBI Strap Mapping,” on page 61 for the host interface strap settings. |

**Note 5:** Configuration strap pins are identified by an underlined symbol name. Configuration strap values are latched on power-on reset or **RST#** de-assertion. Refer to Section 7.0, "Configuration Straps," on page 54 for more information.

**TABLE 3-8: MISCELLANEOUS PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | Power Management Event Output | **PME** | VO8/VOD8 | When programmed accordingly this signal is asserted upon detection of a wakeup event. The polarity and buffer type of this signal is programmable via the PME Enable (PME_EN) bit of the Power Management Control Register (PMT_CTRL).<br><br>Refer to Section 6.0, "Clocks, Resets, and Power Management," on page 37 for additional information on the power management features. |
| 1 | Interrupt Output | **IRQ** | VO8/VOD8 | Interrupt request output. The polarity, source and buffer type of this signal is programmable via the Interrupt Configuration Register (IRQ_CFG). For more information, refer to Section 8.0, "System Interrupts," on page 62. |
| 1 | System Reset Input | **RST#** | VIS (PU) | As an input, this active low signal allows external hardware to reset the device. The device also contains an internal power-on reset circuit. Thus this signal may be left unconnected if an external hardware reset is not needed. When used this signal must adhere to the reset timing requirements as detailed in the Section 19.0, "Operational Characteristics," on page 399. |
| 1 | Regulator Enable | **REG_EN** | AI | When tied to 3.3 V, the internal 1.2 V regulators are enabled. |
| 1 | Test Mode | **TESTMODE** | VIS (PD) | This pin must be tied to **VSS** for proper operation. |
| 1 | Crystal Input | **OSCI** | ICLK | External 25 MHz crystal input. This signal can also be driven by a single-ended clock oscillator. When this method is used, **OSCO** should be left unconnected. |
| 1 | Crystal Output | **OSCO** | OCLK | External 25 MHz crystal output. |
| 1 | Crystal +1.2 V Power Supply | **OSCVDD12** | P | Supplied by the on-chip regulator unless configured for regulator off mode via **REG_EN**. |
| 1 | Crystal Ground | **OSCVSS** | P | Crystal ground. |
| 5 | Reserved | **RESERVED** | - | This pin is reserved and must be left unconnected for proper operation. |

**TABLE 3-9: JTAG PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | JTAG Test Mux Select | **TMS** | VIS | JTAG test mode select |
| 1 | JTAG Test Clock | **TCK** | VIS | JTAG test clock |
| 1 | JTAG Test Data Input | **TDI** | VIS | JTAG data input |
| 1 | JTAG Test Data Output | **TDO** | VO12 | JTAG data output |

**TABLE 3-10: CORE AND I/O POWER PIN DESCRIPTIONS**

| Num Pins | Name | Symbol | Buffer Type | Description |
|---|---|---|---|---|
| 1 | Regulator +3.3 V Power Supply | **VDD33** | P | +3.3 V power supply for internal regulators. See Note 6.<br>**Note:** +3.3 V must be supplied to this pin even if the internal regulators are disabled. |
| 5 | +1.8 V to +3.3 V Variable I/O Power | **VDDIO** | P | +1.8 V to +3.3 V variable I/O power. See Note 6. |
| 3 | +1.2 V Digital Core Power Supply | **VDDCR** | P | Supplied by the on-chip regulator unless configured for regulator off mode via REG_EN.<br><br>1 µF and 470 pF decoupling capacitors in parallel to ground should be used on pin 6. See Note 6. |
| 1 pad | Ground | **VSS** | P | Common ground. This exposed pad must be connected to the ground plane with a via array. |

**Note 6:** Refer to Section 4.0, "Power Connections," on page 26, the device reference schematic, and the device LANCheck schematic checklist for additional connection information.